# A Current-Mode Buck Converter With Reconfigurable On-Chip Compensation and Adaptive Voltage Positioning

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***Abstract*—Power management integrated circuits (PMICs) with on-chip compensation are widely used to power multiple loads in mobile devices with increased power density. However, there are two issues for on-chip compensated PMICs. First, on-chip compensation reconfigurability is required to obtain the appropriate response in various passive components. Second, a converter for a processor requires adaptive voltage positioning (AVP) to reduce the output capacitor size. In this paper, a novel reconfigurable on-chip compensated current-mode buck converter with AVP is proposed to solve the aforementioned issues without requiring high-speed and high-resolution analog-to-digital converter (ADC). A reconfigurable accurate load line control scheme and on-chip compensation are proposed to achieve an accurate load line and AVP in various load lines and passive components. The control scheme, small-signal model, and circuit implementation are illustrated in this paper. The proposed buck converter was implemented into an integrated circuit to verify the analysis.**

***Index Terms*—Adaptive voltage position (AVP), current-mode control, load line, on-chip compensation, power management integrated circuits (PMICs).**

## I. Introduction

MOBILE electronic devices, such as notebook and smart phones, require small size. Besides, there are multiple loads, such as processor, memory, and system power, in the device requiring power supplies with various voltage and current levels. If each load is powered by a power converter with its own controller and frequency compensation components, the converter circuits will occupy large board area and increase the cost.

Therefore, a power management integrated circuit (PMIC) with multiple outputs is widely used to power multiple loads in mobile electronic devices [1], [2]. A PMIC saves the board area by integrating various power converters, such as buck converters, and low-dropout regulators into a single chip. Besides, on-chip compensation is usually implemented in a PMIC. By integrating the frequency compensation components into a PMIC, it saves chip pin count and integrated circuit (IC) package cost. Besides, the power density of the power converters is increased.

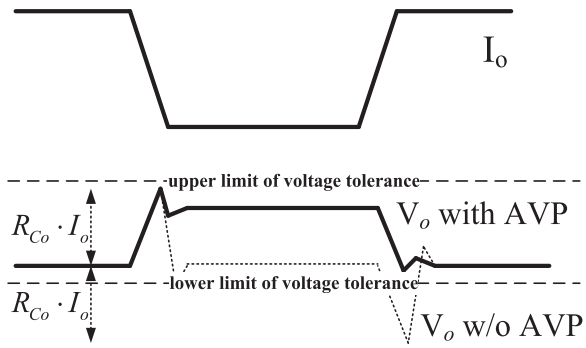


Fig. 1. Comparison of output voltage waveforms at step load changes for a converter with and without AVP.

However, there are two issues of the PMIC with on-chip compensation. First, programmability and independently parameters adjustability of on-chip compensation are required to have an appropriate response in various passive component values and loads [1]–[3]. Besides, the reduction of the circuit area of compensation in an IC is important for cost reduction.

Second, the converter in a PMIC for a processor requires adaptive voltage positioning to reduce output capacitor size [4]–[15]. The power requirements of a processor are more and more stringent due to the advancement of a processor in computing devices. The processor requires lower voltage and consumes large dynamic current, which is step load with fast slew rate. Therefore, the converter for a processor must provide small output voltage variation at fast load transient to ensure proper processor performance and user experience. Adaptive voltage position (AVP) function is often adopted to power a processor to reduce output voltage variation at load transient and to mitigate output capacitance requirement [5]–[15]. Fig. 1 shows that the comparison of output voltage waveforms at step load changes for a converter with and without AVP, where $R_{\mathrm{Co}}$ is the equivalent series resistance (ESR) of the output capacitor. It can be seen that the output voltage $V_o$ of the converter with

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TABLE I
COMPARISON OF PAPERS AND PRODUCTS FOR FAST TRANSIENT LOAD

| | 2015 [1] | 2015 [12], [15] | 2013 [18] | This paper |
|---|---|---|---|---|
| Control type | Hybrid | Digital | Hybrid | Hybrid |
| On-chip compensation | Yes | Yes | No | Yes |
| Programmable compensation | Yes | Yes | No | Yes |
| No need high-resolution ADC | Yes | No | Yes | Yes |
| AVP function | No | Yes | Yes | Yes |

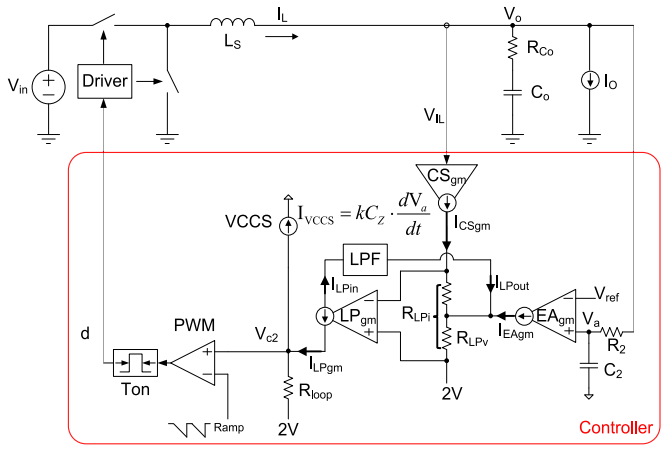



Fig. 2. Proposed reconfigurable on-chip compensated converter with accurate AVP.

the AVP control is not fixed. Instead, $V_o$ is higher at lower load current, $I_o$. Thus, the peak-to-peak output voltage deviation at load transient for the AVP control is reduced [6]. In Section II, this advantage of AVP control will be proved by simulation shown in Fig. 8.

Various papers and products were proposed to address the aforementioned issues for a PMIC partly. A PMIC product with analog control loop and reconfigurable on-chip compensation is proposed in [1]. The compensation is adjustable by $I^2C$ digital interface. Thus, it is defined as a hybrid control in the paper. However, the AVP function is lacking. References [12] and [15] adopted a digital control to provide on-chip frequency compensation, flexibility, and AVP for high-end server. However, high-speed and high-resolution analog-to-digital converter (ADC) is required to provide fast transient response and to avoid limit-cycle oscillation, resulting in higher cost and power loss [12], [15]–[17]. Therefore, the digital control is not suitable for low-cost and low-power PMIC application. To solve the aforementioned problems, in [18], a hybrid control is adopted to achieve fast transient response with analog control and flexibility by digital interface. However, the control scheme requires complex compensation to achieve AVP and occupies large chip area if integrated into an IC. Therefore, only the external compensation without programmability is implemented, which is not suitable for reconfigurable compensated PMIC. Table I summarizes the comparison of various papers and products for fast transient load. As will be explained in later sections, the proposed control achieves all the required features for a PMIC with fast transient loads, whereas other papers and products only achieve parts of the features.

In this paper, a novel on-chip compensated current-mode buck converter, shown in Fig. 2, is proposed to solve the aforementioned problems for a PMIC without requiring high-speed and high-resolution ADC. Reconfigurability and accurate AVP are achieved. Hybrid architecture with digital interface and analog reconfigurable control loop decouples the tradeoff between programmability and ADC requirements for fast transient response. Current-mode control reduces the complex compensation to achieve AVP and makes on-chip compensation possible. However, it causes output voltage offset problem [6], [9]. Therefore, a reconfigurable accurate load line (RALL) control scheme is proposed to achieve accurate load line and reduce output capacitor size for various processors and passive components. Besides, the proposed control scheme reduces the chip area of the on-chip compensation circuit. The advantages of flexibility, saving IC pin count, and saving engineering time of changing external components are also kept. The detail description and circuit operation, shown in Fig. 2, are explained in Section II.

In Section II, the proposed converter with the theoretical analysis on accurate load line control and on-chip frequency compensation is described, and a small-signal model is also proposed. In Section III, the circuit implementation of the proposed control scheme is illustrated. In Section IV, the design with simulation and experiment is validated. Finally, Section V concludes the results.

## II. PROPOSED RECONFIGURABLE CONVERTER AND A SMALL-SIGNAL MODEL

Fig. 2 shows the simplified control diagram of the proposed control scheme. It shows that no external compensation components are required for the control. A single-phase buck converter is used to illustrate the operation with simplicity, but the control can be easily extended to multiphase. In a multiphase converter, the controller senses the summation of per-phase inductor currents, and the generated on-time pulse is distributed to each phase [19], [20]. Therefore, the dc analysis for the single-phase converter is kept in the multi-phase converter. The buck converter is comprised of the power switches, the output inductor $L_S$, and the output capacitor $C_o$ with its ESR $R_{\rm Co}$. Current source $I_o$ represents the load. In the controller, voltage signals are transformed into current and flow into resistance for easier signal addition and subtraction in an IC. Therefore, transconductance amplifiers, such as $\rm EA_{gm}$, $\rm CS_{gm}$, and $\rm LP_{gm}$, are used to generate current for signal processing. Inductor current $I_L$ is sensed as the voltage signal $V_{\rm IL}$ and added to control by $\rm CS_{gm}$. A stable output voltage is achieved by connecting $V_o$ to the positive terminal of amplifier EAgm. If $V_o$ is larger than $V_{\rm ref}$, $I_{\rm EAGM}$ will increase and $I_{\rm LPGM}$ will decrease. Then, Vc2 will decrease, and

duty cycle will reduce. Finally, $V_o$ will be reduced, and a stable operation is achieved by this feedback loop. External ramp is implemented in a pulsewidth modulation (PWM) modulator for noise margin improvement.

Current-mode control with finite $\mathrm{EA_{gm}}$ dc gain is adopted to achieve AVP [6]. That is, finite dc gain compensation in the outer voltage loop is designed instead of the integrator-type compensation in the conventional control. However, the finite $\mathrm{EA_{gm}}$ dc gain introduces an offset problem when achieving AVP [9]. To achieve reconfigurable load line while avoiding the output voltage offset problem, an RALL control is proposed. A local positive feedback loop consists of $\mathrm{LP_{gm}}$, a low-pass filter (LPF), and $R_{\mathrm{LP}v}$ cancels the dc offset. The whole system stability is ensured by the outer voltage feedback loop. Besides, the load line adjustability is achieved by adjusting the resistance of $R_{\mathrm{LP}i}$. The detail derivation of the RALL control is illustrated in Section II-A.

To achieve appropriate AVP transient response as shown in Fig. 1, only one compensation pole and one compensation zero are required in the output-voltage feedback loop for the proposed control. Instead, the voltage-mode control with adaptive reference voltage adjusted by load current requires more complex type-III compensation to achieve AVP [6]. Thus, the proposed control scheme shows more advantage when on-chip compensation with independently adjustability is required. In Fig. 2, $V_o$ passes through the circuit composed of $R_2$ and $C_2$ to generate a compensation pole in the outer voltage loop. $V_{\mathrm{ref}}$ represents the reference voltage. $V_a$ is the output signal of compensation pole circuit. $\mathrm{EA_{gm}}$ is a transconductance amplifier that generates current proportional to the difference of $V_{\mathrm{ref}}$ and $V_a$. A high bandwidth error amplifier is not required. A voltage-controlled current source (VCCS) with its current proportional to the time derivative of compensation pole circuit output $V_a$ generates the compensation zero in the outer voltage loop. Detail derivation of compensation zero is illustrated in Section II-B. As can be seen, the proposed control scheme integrates the loop compensation circuits into the IC. Besides, compensation parameters can be changed independently to fit different operations without the need to change compensation components on the board. The details on how to adjust the compensations are explained in Section III.

The proposed control also adopts the constant on-time (COT) control to increase efficiency under light-load condition, which is very important in recent years [5], [8], [12], [21]–[24]. In Fig. 2, the summation of $V_o$ information and $I_L$ information determines the positive output of the PWM comparator. When the signals in positive output and negative output of the PWM comparator intersect, a predetermined on-time triggers. Under light-load condition, the operation of a converter can be set to change from continuous-conduction mode (CCM) to discontinuous-conduction mode (DCM). Thus, the switching frequency and its related switching loss reduce under light-load condition.

### A. RALL Control

The AVP control reduces output voltage variation at load transient. Unlike the conventional control, which regulates $V_o$ to a fixed level at any load current, the AVP control decreases output voltage linearly with the increase in output load. Thus, output capacitor requirement for the same output voltage deviation specification is reduced, which saves cost and board area.

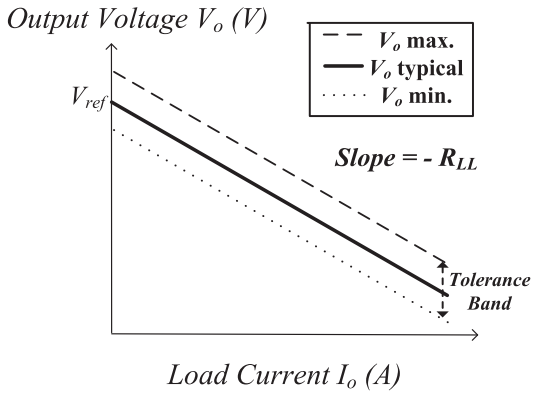



Fig. 3. Steady-state output load line for a converter with AVP function.

Fig. 3 shows the steady-state requirement of the output load line for the AVP control. Load line $R_{\mathrm{LL}}$ is defined as the slope of dc output voltage changes versus load current changes. Output voltage has to be within the tolerance band to ensure a proper processor operation [5], [8]. That is, load line and output voltage at no load shall both be accurate. The current-mode control with AVP function has an output voltage offset problem due to finite $\mathrm{EA_{gm}}$ dc gain. Besides, reconfigurable load line is required to power various processors, which may complicate the problem.

In this paper, the RALL control is proposed to achieve adjustable load line value and meet accurate output voltage requirement of AVP. To illustrate this, dc equations of transconductance amplifier outputs are derived from Fig. 2 as (1)–(3). In here, the dc transconductance of $\mathrm{EA_{gm}}$, $\mathrm{CS_{gm}}$, and $\mathrm{LP_{gm}}$ is defined as $\mathrm{gm_{EA}}$, $\mathrm{gm_{CS}}$, and $\mathrm{gm_{LP}}$, respectively. For simplicity, the sensing gain from $I_L$ to $V_{\mathrm{IL}}$ is set to one, whereas the sensing gain is lumped together with transconductance to form $\mathrm{gm_{CS}}$. It is noted that the variables in (1)–(3) are all dc values

$$I_{\mathrm{EAgm}} = \mathrm{gm_{EA}}\left(V_a - V_{\mathrm{ref}}\right) = \mathrm{gm_{EA}}\left(V_o - V_{\mathrm{ref}}\right) \tag{1}$$

$$I_{\mathrm{CSgm}} = \mathrm{gm_{CS}} \cdot V_{\mathrm{IL}} = \mathrm{gm_{CS}} \cdot I_L = \mathrm{gm_{CS}} \cdot I_O \tag{2}$$

$$\begin{aligned} I_{\mathrm{LPin}} &= I_{\mathrm{LPout}} \\ &= \mathrm{gm_{LP}} \cdot \left(I_{\mathrm{EAgm}} \cdot R_{\mathrm{LP}v} + I_{\mathrm{CSgm}} \cdot R_{\mathrm{LP}i} + I_{\mathrm{LPout}} \cdot R_{\mathrm{LP}v}\right). \end{aligned} \tag{3}$$

In order to cancel the $V_o$ dc offset, a local feedback loop is created. The output current of $\mathrm{LP_{gm}}$ is fed back into its input through an LPF and $R_{\mathrm{LP}v}$ to form a feedback loop, as shown in Fig. 2 and (3). It is very important to design $\mathrm{gm_{LP}}$ and $R_{\mathrm{LP}v}$ to meet (4), then $V_o$ dc offset is cancelled

$$\mathrm{gm_{LP}} \cdot R_{\mathrm{LP}v} = 1. \tag{4}$$

From (3) and (4), the following equation can be derived:

$$I_{\mathrm{EAgm}} \cdot R_{\mathrm{LP}v} + I_{\mathrm{CSgm}} \cdot R_{\mathrm{LP}i} = 0. \tag{5}$$

Substituting (5) into (1) and (2), the output voltage load line equation is derived as follows:

$$V_O = V_{\text{ref}} - I_O \cdot R_{\text{LL}} \tag{6}$$

where $R_{\text{LL}} = \text{gm}_{\text{CS}} \cdot R_{\text{LP}i}/\text{gm}_{\text{EA}} \cdot R_{\text{LP}v}$.

As can be seen from (6), the proposed RALL control achieves accurate AVP without offset if (4) is achieved. Load line $R_{\text{LL}}$ is determined by the value of $\text{gm}_{\text{EA}} \cdot R_{\text{LP}v}$, and it can be seen that infinite $\text{gm}_{\text{EA}}$ value makes the control loss AVP characteristics. The load line adjustability is easily achieved by adjusting the resistance ratio between $R_{\text{LP}i}$ and $R_{\text{LP}v}$, as shown in (6). Therefore, $R_{\text{LP}v}$ is kept fixed whereas $R_{\text{LP}i}$ is varied to achieve different load lines. Another insight from (5) and (6) is that VCCS shall be connected to the output port instead of the input port of $\text{LP}_{\text{gm}}$. Then, the nonideal offset current generated by VCCS will not affect the $V_o$ accuracy. It is also intuitively to see the $V_o$ dc offset issue from (5) if the LPF loop is not included. The dc value of $I_{\text{LPgm}}$ is not zero due to the ripple in modulation waveforms. If the LPF loop is removed, the left-hand portion of (5) is the dc value of $I_{\text{LPgm}}$ and will not be zero. So, the output voltage in (6) will have an extra term that refers to $V_o$ dc offset.

### *B. Proposed On-Chip Frequency Compensation and a Small-Signal Model*

To achieve AVP, as shown in Fig. 1, proper compensation to have a flat small-signal output impedance is necessary [6], [8]. Therefore, a small-signal model for the proposed control is required to design the loop gain. According to Yao *et al.* [6] and Chen *et al.* [8], the current-mode control achieves AVP with finite dc gain, one compensation pole, and one compensation zero in the outer loop gain $T_2$, where $T_2$ is the loop gain measured by breaking the $V_o$ feedback path. Chen *et al.* [8] uses an error amplifier with external compensation components, such as capacitors and resistors, to achieve the compensation.

Considering on-chip compensation, there are two main drawbacks to use the same compensation circuit in [8] with components integrated into an IC. First, the interdependence of compensation parameters is not preferred. The interdependence of parameters would make the range of compensation components value too large. Besides, it requires an iteration for setting compensation parameters. Second, the compensation circuit shall occupy small area in the IC to save the cost. Compensation capacitors with nanofarad capacitance in [8] are not acceptable.

In this paper, an on-chip compensation architecture with independently parameter adjustability and small circuit area is proposed. A compensation zero and a compensation pole in the outer voltage loop are derived from the control scheme. The compensation zero is generated by the feedforward path produced by the VCCS circuit. The VCCS circuit generates a current proportional to the time derivative of voltage $V_a$, which is the output of an LPF formed by $R_2$ and $C_2$. As will be explained in this section, this control architecture decouples the relationship between compensation zero and compensation pole. Thus, the independently parameter adjustability is achieved. To explain the derivation of the compensation zero, the converter shown in Fig. 2 is transformed to the equivalent control block

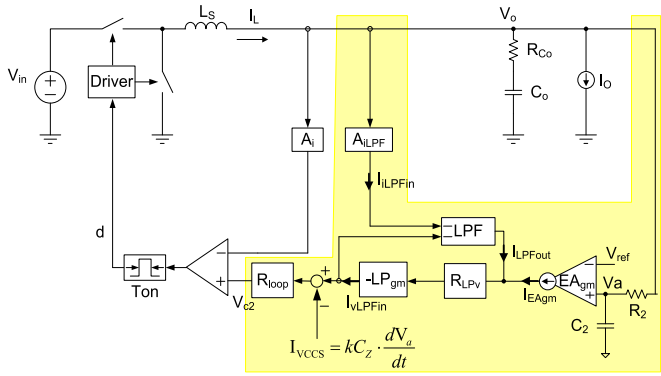



Fig. 4. Equivalent control block diagram of the proposed converter.

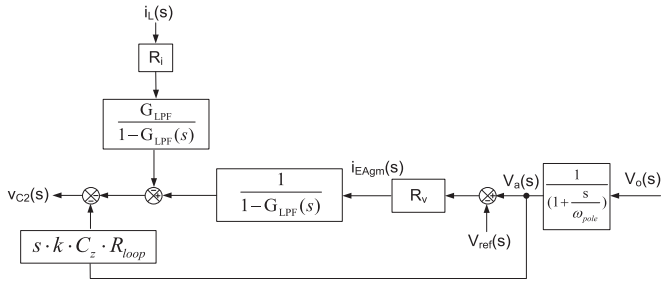



Fig. 5. Small-signal model of the circuit with yellow shade in Fig. 4.

diagram shown in Fig. 4. Fig. 4 separates the sensed inductor current paths to PWM input and LPF input. Then, the circuit outside the yellow shade can be identified as the current-mode buck converter with current sensing gain $A_i$ [see (7)], which is proportional to transconductance $\text{gm}_{\text{CS}}$. The gain from inductor current to LPF input is derived as (8). Since the small-signal model of the current-mode buck converter has been derived, this paper focus on the model derivation of the circuit with yellow shade

$$A_i = \text{gm}_{\text{CS}} \cdot R_{\text{loop}} \tag{7}$$

$$A_{i\text{LPF}} = \text{gm}_{\text{CS}} \cdot \frac{R_{\text{LP}i}}{R_{\text{LP}v}}. \tag{8}$$

The small-signal model of the circuit with yellow shade in Fig. 4 can be derived as Fig. 5, as shown below. Recalling from (4) that the multiplication of $\text{gm}_{\text{LP}}$ and $R_{\text{LP}v}$ is designed as one. Therefore, the feedback loop formed by LPF, $\text{LP}_{\text{gm}}$, and $R_{\text{LP}v}$ is simplified into two control blocks containing $G_{\text{LPF}}$, where $G_{\text{LPF}}$ is the transfer function of the LPF. Detail small-signal transfer function derivations with input as $I_{\text{EAgm}}$ and $I_{\text{LPFin}}$, respectively, are shown in (9)and (10) and (11) and (12) using superposition

$$I_{v\text{LPFin}}(s) = -I_{\text{EAgm}}(s) + G_{\text{LPF}}(s) \cdot I_{v\text{LPFin}}(s) \tag{9}$$

$$\frac{I_{v\text{LPFin}}(s)}{I_{\text{EAgm}}(s)} = -1 \cdot \frac{1}{1 - G_{\text{LPF}}(s)} \tag{10}$$

$$I_{v\text{LPFin}}(s) = G_{\text{LPF}}(s) \cdot I_{i\text{LPFin}}(s) + G_{\text{LPF}}(s) \cdot I_{v\text{LPFin}}(s) \tag{11}$$

$$\frac{I_{v\text{LPFin}}(s)}{I_{i\text{LPFin}}(s)} = \frac{G_{\text{LPF}}(s)}{1 - G_{\text{LPF}}(s)}. \tag{12}$$

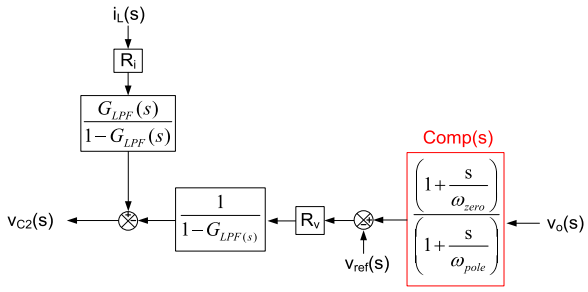



Fig. 6. Further simplified small-signal model from Fig. 5.

Besides, $R_V$ is defined in (13). $R_i$ is defined in (14). $\omega_{\text{pole}}$ is the pole generated by $R_2$ and $C_2$

$$R_V = \text{gm}_{\text{EA}} \cdot R_{\text{loop}} \tag{13}$$

$$R_i = \text{gm}_{\text{CS}} \cdot \frac{R_{\text{LP}i}}{R_{\text{LP}v}} \cdot R_{\text{loop}}. \tag{14}$$

The current of VCCS, $I_{\text{VCCS}}$, is express in (15), and its small-signal variable in the frequency domain is express in (16)

$$I_{\text{VCCS}} = k \cdot C_Z \cdot \frac{dV_a}{dt} \tag{15}$$

$$i_{\text{VCCS}}(s) = s \cdot k \cdot C_Z \cdot V_a(s). \tag{16}$$

On the basis of the derivation given below, the small-signal model shown in Fig. 5 can be further simplified as Fig. 6. The pole frequency of an LPF is designed to be much lower than $\omega_{\text{pole}}$ and $\omega_{\text{zero}}$ for dc offset cancellation, and transconductance of $\text{EA}_{\text{gm}}$ is designed as flat gain for frequency below $\omega_{\text{zero}}$. The transfer function from $V_a$ to $V_{C2}$ shown in Fig. 5 can be approximated as (17). As shown in (17), there exist a left half-plane zero from $V_a$ to $V_{C2}$

$$\frac{V_{C2}(s)}{V_a(s)} = \frac{-R_V}{1 - G_{\text{LPF}}(s)} \cdot \left(1 + \frac{1 - G_{\text{LPF}}(s)}{R_V} \cdot s \cdot k \cdot C_Z \cdot R_{\text{loop}}\right)$$
$$\approx \frac{-R_V}{1 - G_{\text{LPF}}(s)} \cdot \left(1 + \frac{s}{\omega_{\text{zero}}}\right) \tag{17}$$

where

$$\omega_{\text{zero}} = \frac{R_V}{s \cdot k \cdot C_Z \cdot R_{\text{loop}}} = \frac{\text{gm}_{\text{EA}}}{s \cdot k \cdot C_Z}.$$

An equivalent compensation transfer function, Comp(s), is obtained in Fig. 6. The transfer function has a compensation zero and a compensation pole. Its dc gain is equal to one. The compensation zero frequency, $\omega_{\text{zero}}$, is proportional to $\text{EA}_{\text{gm}}$ dc gain and inversely proportional to $C_z$, as shown in (17). Therefore, $\omega_{\text{zero}}$ can be adjusted independently by adjusting $C_z$. However, $\omega_{\text{pole}}$ can be adjusted independently by adjusting $R_2$ or $C_2$.

The small-signal model of the proposed converter is derived as shown in Fig. 7 by inserting the small-signal model shown in Fig. 6 into the current-mode control model [8]. It is noted that the transfer functions, such as $Z_o(s)$, $G_{vc}(s)$, $G_{ii}(s)$, and $G_{ic}(s)$, are derived with closed inner current loop with an external ramp and can be referred in [8] and [19]. In fact, ramp

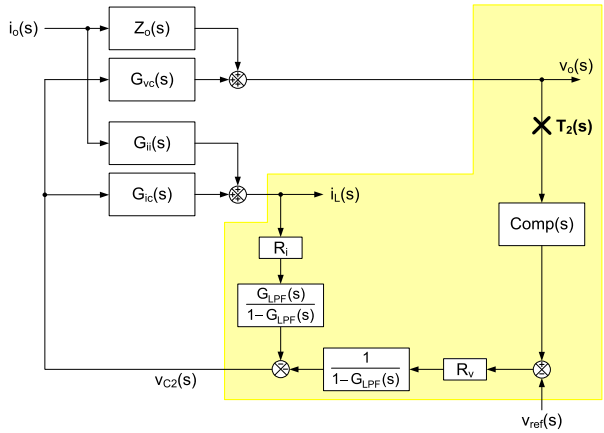



Fig. 7. Small-signal model of the proposed converter.

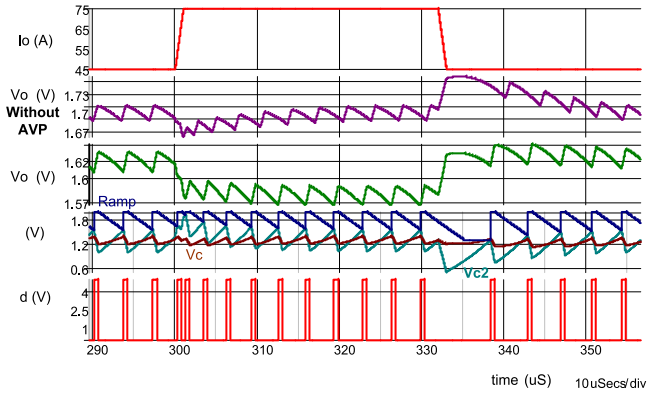



Fig. 8. Simulated load transient response of the proposed converter.

slope affects $G_{vc}(s)$ transfer function. This small-signal model can be extended to *n*-phase converter with below modification in the parameters of the single-phase converter [19]. First, the switching frequency is *n* times of original switching frequency. Second, the output voltage is *n* times of original $V_o$. The derivation of these transfer functions and the compensator design to achieve flat output impedance are not shown in this paper due to page limit. The current loop shown in Fig. 7 models the current loop passing through $A_{i\text{LPF}}$, instead.

The compensation transfer function, Comp(s), can be used to shape outer loop gain $T_2$ to achieve flat output impedance for proper AVP transient response, where $T_2$ is derived as (18) by breaking the point denoted as $T_2(s)$ in Fig. 7. To verify the stability of the system, one can use the loop gain equation (18) to check the phase margin

$$T_2(s) \approx \text{Comp}(s) \cdot \frac{R_V}{1 - G_{\text{LPF}}(s)} \cdot G_{vc}(s). \tag{18}$$

Fig. 8 shows the circuit simulation result of the load transient response of the proposed converter. A single-phase buck converter is used for simulation. Input voltage is 12 V. Inductor $L_o$ is 0.36 $\mu$H. Output capacitor parameters have a capacitance value of 2.24 mF with ESR as 1.75 m$\Omega$. $V_c$ signal is the $V_{c2}$ signal subtracted by VCCS-induced voltage. It can be seen that VCCS signal increases the magnitude of $V_{c2}$ to speed up $V_o$ transient response during load current step up, which shows

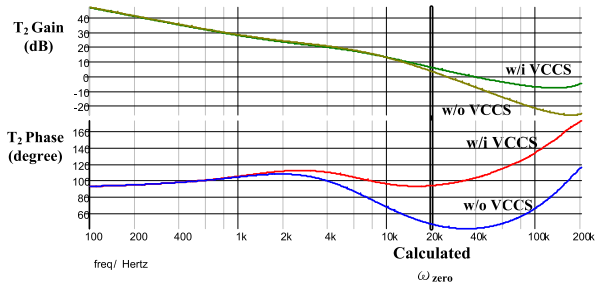



Fig. 9. Comparison of simulated loop gain $T_2$ of the proposed converter with and without VCCS circuit.

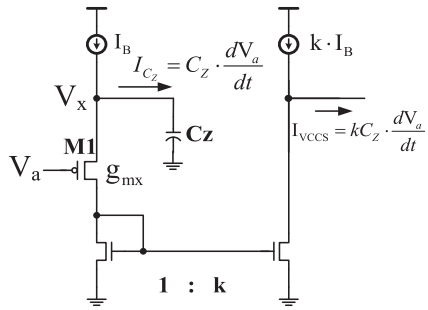



Fig. 10. Circuit diagram of the source follower circuit [25].

the compensation zero effect. To show the advantage of AVP control where $V_o$ peak-to-peak value is lower, $V_o$ without AVP control is simulated by setting $\mathrm{gm_{CS}}$ to zero. The comparison of simulation results show that $V_o$ peak-to-peak value is reduced from 100 to 75 mV when AVP function is enabled.

Fig. 9 shows the comparison of simulated loop gain $T_2$ of the proposed converter and its counterpart without VCCS circuit. $\omega_{\mathrm{zero}}$ is set to 20 kHz. It shows that an extra zero at $\omega_{\mathrm{zero}}$ frequency in $T_2$ is obtained for the proposed converter when comparing to its counterpart without VCCS circuit.

## III. Circuit Implementation of the Proposed Converter

### A. Proposed VCCS Circuit

A source follower circuit with its source terminal connected to capacitor, as shown in Fig. 10, can be used to generate the current of the VCCS circuit, which is proportional to the time derivative of voltage $V_a$ [25], [26]. The circuit occupied small chip area and has low power consumption compared to an error amplifier. MOSFET M1 is used as a source follower. The voltage variation in $V_a$ would appear in $V_x$ if resistance seen from $V_x$ could be neglected. This would produce a current $I_{Cz}$ flowing into the capacitor $C_z$. Using current mirrors with $k$-times of current ratio, $I_{\mathrm{VCCS}}$ is $k$-times of $I_{Cz}$. As can be seen in Fig. 10, the required $I_{\mathrm{VCCS}}$, as shown in (16), is achieved by the VCCS circuit.

However, VCCS circuit contains a main parasitic pole and may degrade the performance of the compensation zero. The parasitic pole can be derived by considering finite resistance seen from $V_x$ point. Equation (19) is derived based on the small-signal analysis from Fig. 10, where $g_{mx}$ is the small-signal transconductance of MOSFET M1. From (19), $I_{\mathrm{VCCS}}$ can be derived as

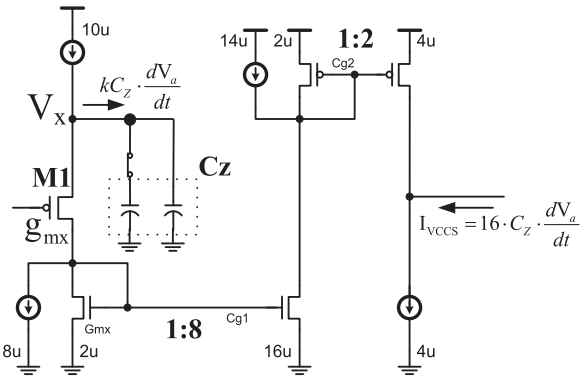



Fig. 11. Proposed VCCS circuit to mitigate parasitic pole issue.

(20). It can be seen that (20) is different from (16). If $I_{\mathrm{VCCS}}$ expression in Fig. 5 is replaced by (20), there would be a parasitic pole shown in (17) with its frequency equal to $\omega_p$. That is, the parasitic pole of the VCCS circuit introduces a parasitic pole at loop gain $T_2$. To retain the compensation zero effect on $T_2$, the parasitic pole frequency should be pushed beyond ten times of loop gain bandwidth. Thus, the parasitic pole will not affect the phase margin of $T_2$

$$\frac{V_x(s)}{V_a(s)} = \frac{\frac{1}{s \cdot C_Z}}{\frac{1}{g_{mx}} + \frac{1}{s \cdot C_Z}} \tag{19}$$

$$i_{\mathrm{VCCS}}(s) = \frac{s \cdot k \cdot C_Z}{\left(1 + \frac{s}{\omega_p}\right)} \cdot V_a(s) \tag{20}$$

where $\omega_p = g_{mx}/C_Z$.

To solve the parasitic pole issue, a modified VCCS circuit is proposed in Fig. 11 with low current consumption and small circuit area. The parasitic pole is pushed to higher frequency by increasing current passing MOSFET M1 to increase $g_{mx}$ in (20). By bypassing a 8-$\mu$A current, the parasitic pole is pushed to higher frequency without too much current consumption in later current mirrors. Thus, the advantage of low current consumption can be kept. In the design, $g_{mx}$ is around 30 $\mu$A/V. When $C_z$ is set to 12.5 pF, the parasitic pole frequency is around 3.5 MHz, which is much higher than $T_2$ loop gain bandwidth. A second stage of current mirror with gain ratio of two further increases the gain of $I_{\mathrm{VCCS}}$ with a relatively higher parasitic pole, and the requirement of $C_z$ is reduced according to (17). Therefore, the circuit area of capacitor $C_z$ is reduced. A 14-$\mu$A bypass current reduces the current consumption of the output current mirror to only 4 $\mu$A. It can also be seen that compensation zero frequency can be adjusted by connecting or disconnecting the capacitor cell $C_z$ by switches.

### B. Reconfigure Circuit Implementation

The digital interface receives the $I^2C$ command to adjust analog loop parameters. Compared to the conventional analog control where compensation and parameter define components are placed on-board, the proposed control adjusts the loop parameters without the need to desolder and solder on-board components. Therefore, design time can be reduced. Besides,

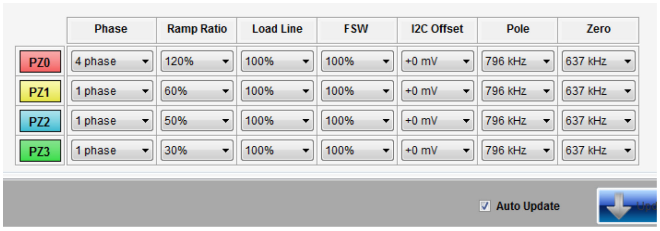



Fig. 12. GUI for loop parameters adjustment of the proposed converter.

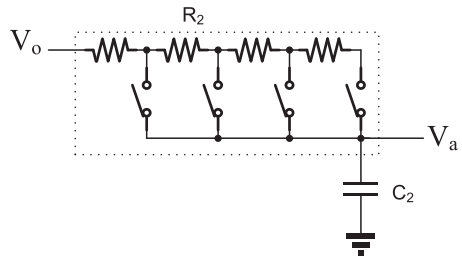



Fig. 13. Circuit diagram of the compensation pole generation with parameters adjustment.

the reconfigurability of the proposed control could serve as the foundation for future implementation of self-calibration function. Fig. 12 shows the graphical user interface (GUI) implemented in a personal computer to adjust loop parameters of the proposed converter. It shows that GUI can set various loop parameters, such as compensation pole frequency, zero frequency, load line, etc. In here, 100% refers that the setting value equals to the nominal value. For example, 100% means the setting load line equals to the nominal value, 1.5 m$\Omega$.

There are three parameters need to be set to achieve proper AVP transient response, that is, $R_{\rm LL}$, $\omega_{\rm zero}$, and $\omega_{\rm pole}$. First, Fig. 13 shows the circuit diagram of $R_2$ and $C_2$ to generate an adjustable compensation pole at $\omega_{\rm pole}$ in loop gain $T_2$. The compensation pole frequency adjustment is achieved by an array of switches. Thus, the equivalent resistance of $R_2$ can be adjusted to adjust the pole frequency shown in Fig. 12. Second, as can be seen in Fig. 11 and (17), $\omega_{\rm zero}$ can be adjusted by connecting or disconnecting the capacitor cell to vary the value of $C_z$.

Third, the load line slope $R_{\rm LL}$ can be adjusted by inserting the $\rm CS_{gm}$ current injection to different points of resistor array to adjust $R_{{\rm LP}i}$. Remember that (4) must be achieved to avoid the voltage offset problem. Therefore, $R_{{\rm LP}v}$ is kept fixed, whereas $R_{{\rm LP}i}$ is varied to achieve different load lines. As shown in (6), the accuracy of $R_{\rm LL}$ adjustment, which is a key requirement, can be achieved by proper layout matching between $R_{{\rm LP}v}$ and $R_{{\rm LP}i}$. One thing worth to mention is that the adjustment of the above-mentioned three parameters is independent from each other.

## IV. Experimental Results

A four-phase buck converter was implemented to validate the proposed control with on-chip compensation and parameters adjustability. The control scheme was implemented in a controller IC by TSMC 0.18 $\mu$m technology. Fig. 14 shows the chip layout with dimension 2200 $\mu$m $\times$ 1800 $\mu$m. The area of VCCS circuit

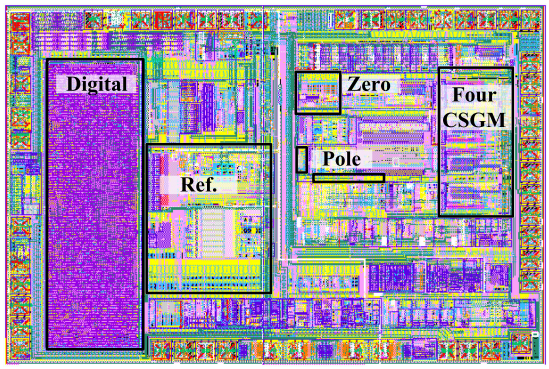



Fig. 14. Chip layout of the proposed control with on-chip frequency compensation.

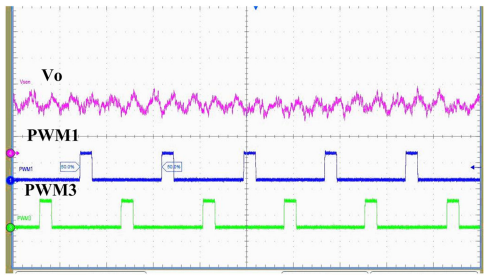



Fig. 15. Steady-state waveforms of the four-phase converter. (Vo voltage scale: 10 mV/div. Time scale: 2 $\mu$s/div.)

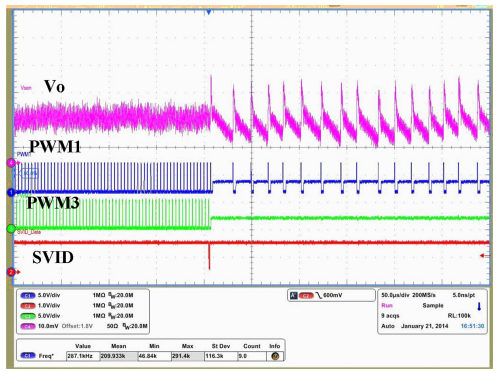



Fig. 16. Operation mode change from four-phase CCM to one-phase DCM after SVID command triggered.

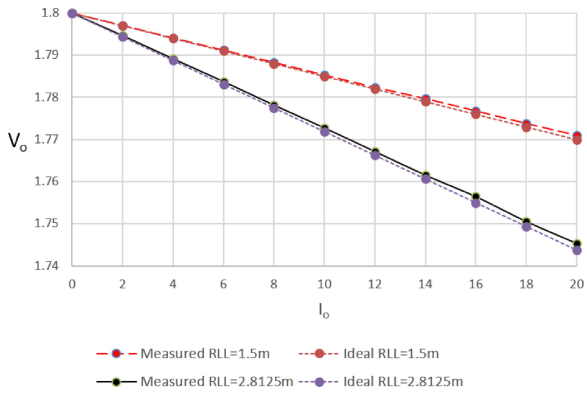



Fig. 17. Measured and ideal dc output voltage versus load current with two different settings of $R_{\rm LL}$.

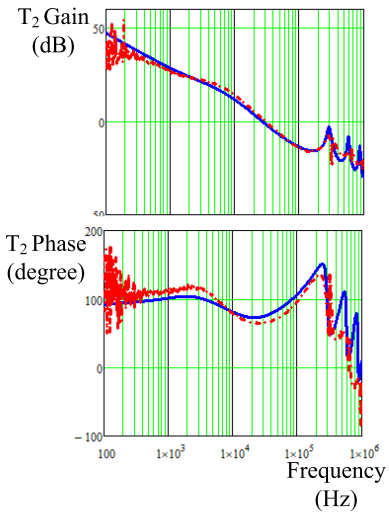



Fig. 18. Experimental model verification of loop gain $T_2$. (Dotted red line: measurement. Solid blue line: calculation.)

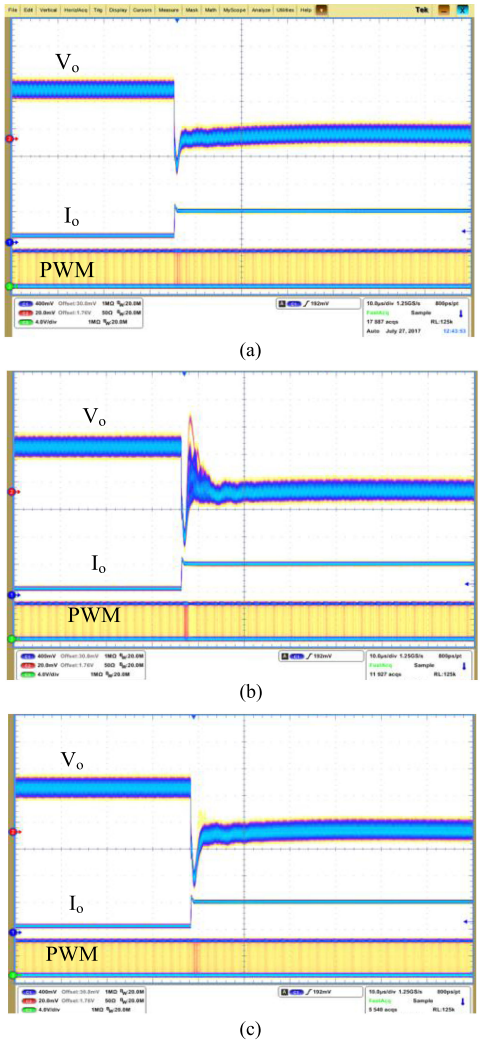



Fig. 19. Measured load transient response in various passive components with $I_o$ from 5 to 30 A. ($V_o$ voltage scale: 20 mV/div. Time scale: 10 $\mu$s/div.) (a) $\omega_{\text{pole}} = 114\,\text{kHz}$, $\omega_{\text{zero}} = 106\,\text{kHz}$; four bulk capacitors. (b) $\omega_{\text{pole}} = 114\,\text{kHz}$, $\omega_{\text{zero}} = 106\,\text{kHz}$; two bulk capacitors. (c) $\omega_{\text{pole}} = 114\,\text{kHz}$, $\omega_{\text{zero}} = 127\,\text{kHz}$; two bulk capacitors.

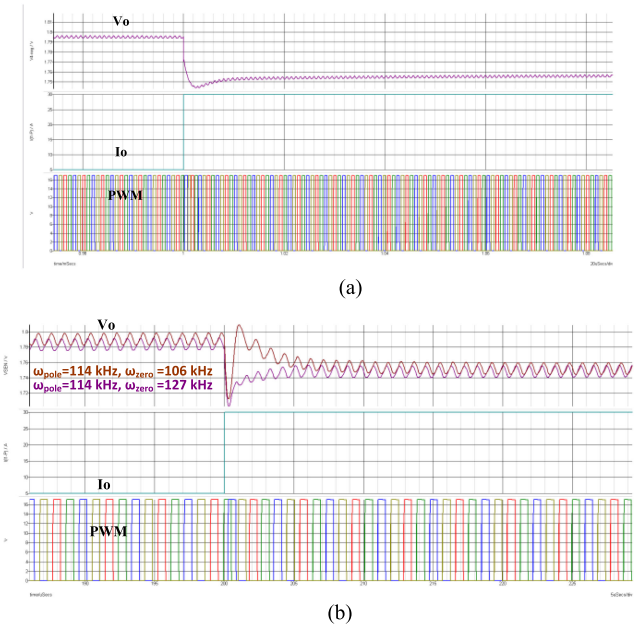


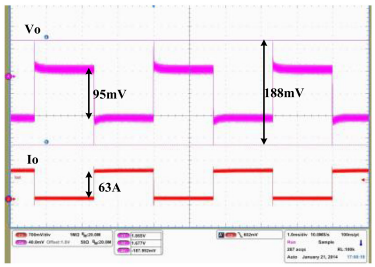

Fig. 20. Simulated load transient response in various passive components with $I_o$ from 5 to 30 A. (Time scale: 20 $\mu$s/div.) (a) $\omega_{\text{pole}} = 114\,\text{kHz}$, $\omega_{\text{zero}} = 106\,\text{kHz}$; four bulk capacitors. (b) $\omega_{\text{pole}} = 114\,\text{kHz}$, $\omega_{\text{zero}} = 106\,\text{kHz}$ versus $\omega_{\text{pole}} = 114\,\text{kHz}$, $\omega_{\text{zero}} = 127\,\text{kHz}$; two bulk capacitors.

is only 170 $\mu$m $\times$ 120 $\mu$m. No additional IC pins and external components are required for compensation.

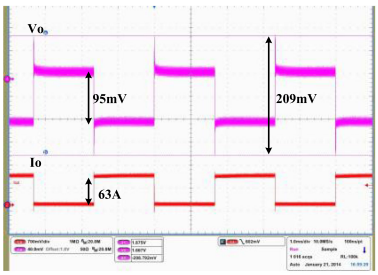
The experiment conditions and parameters are as follows. Input voltage is 12 V. Output voltage at no load condition is 1.8 V. Inductor $L_S$ is 0.36 $\mu$H. Four 560 $\mu$F/7 m$\Omega$ output capacitors and nineteen 22-$\mu$F multi-layer ceramic capacitor (MLCC) decoupling capacitors are used. Default load line $R_{\text{LL}}$ is set to 1.5 m$\Omega$. Steady-state switching frequency is around 280 kHz. Fig. 15 shows the steady-state output voltage waveforms for a four-phase converter, where only phase one and phase three PWM signals are shown. The output voltage waveform shows a stable operation. Fig. 16 shows the operation mode change from four-phase CCM to one-phase DCM after serial VID (SVID) command triggered. The converter in DCM operation reduces its switching frequency naturally due to COT control. Thus, the light-load efficiency is improved.

Fig. 17 shows the measured and ideal dc output voltage versus load current with two different settings of $R_{\text{LL}}$. The ideal value is derived from (6). Load line slope $R_{\text{LL}}$ is set to 1.5 and 2.8125 m$\Omega$, respectively, to verify the adjustability and accuracy of this parameter. It is shown that the measured $V_o$ is well matched with the ideal value. There is only 2-mV error between measured and ideal $V_o$ when $R_{\text{LL}}$ is set to 2.8125 m$\Omega$ and load current is 20 A. This error is well below the specification of Intel VR12.5. Therefore, the effectiveness of RALL control is proved.

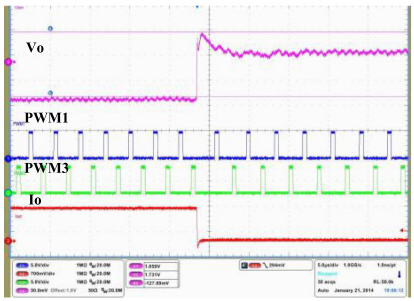
Fig. 18 shows the experimental model verification of loop gain $T_2$ described by (18). The experiment conditions is the same as mentioned above. Besides, the load is set to 20 A. It shows that measurement and calculation results match well for frequency below switching frequency. Thus, the proposed small-signal model and the effectiveness of on-chip compensation are verified.



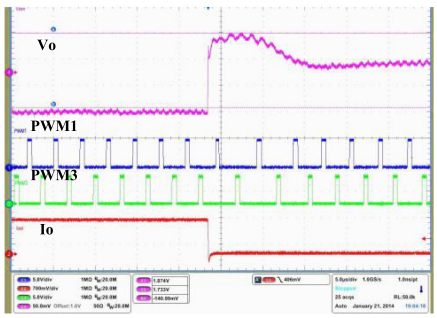

(a)




(b)




(c)




(d)

Fig. 21. Load transient for step load from 1 to 64 A with 300-Hz repetitive rate. (a) $\omega_{\text{pole}} = 40\,\text{kHz}, \omega_{\text{zero}} = 40\,\text{kHz}$. (b) $\omega_{\text{pole}} = 40\,\text{kHz}, \omega_{\text{zero}} = 160\,\text{kHz}$. (c) Zoomed plot: $\omega_{\text{pole}} = 40\,\text{kHz}$, $\omega_{\text{zero}} = 40\,\text{kHz}$. (d) Zoomed plot: $\omega_{\text{pole}} = 40\,\text{kHz}$, $\omega_{\text{zero}} = 160\,\text{kHz}$.

Fig. 19 verifies that the proposed converter achieves appropriate AVP response in various passive components. Fig. 19(a) shows load transient response when load current step is from 5 to 30 A. Four 560 $\mu$F/7 m$\Omega$ output bulk capacitors and nineteen 22-$\mu$F MLCC decoupling capacitors were used. The accumulation over time function of oscilloscope was enabled to catch the worst case response. Dedicated test facility called VTT tool was used as load to conduct the fast slewing test [27]. It is shown that the proper AVP response is achieved that $V_o$ is lower at higher $I_o$. Fig. 19(b) shows the load transient response when two output bulk capacitors were removed from the converter. The transient response shows large ring back. In Fig. 19(c), the compensation zero was adjusted from 106 to 127 kHz, and proper transient response is achieved again. Therefore, the proposed converter could adapt its compensation parameters to achieve proper response in various passive components. Fig. 20 shows the simulation results of load transient response corresponding to the conditions in Fig. 19. The simulation results match well with the measured results in Fig. 19.

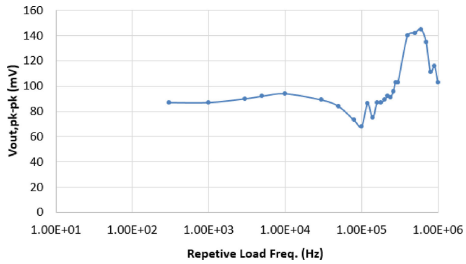



Fig. 22. Experimental output voltage peak-to-peak deviation at repetitive load transient.

Fig. 21 compares the load transient response for two different $\omega_{\text{zero}}$ settings, where step load is from 1 to 64 A with a 300-Hz repetitive rate. Both settings show accurate steady-state load line. During transient, the output voltage waveforms show that the output voltage peak-to-peak value reduces from 209 to 188 mV by changing $\omega_{\text{zero}}$ from 160 to 40 kHz. The zoomed plot can also see the faster transient response of output voltage after reducing $\omega_{\text{zero}}$.

Fig. 22 shows the measured output voltage peak-to-peak deviation at repetitive load transient with repetitive frequency sweeps from 300 Hz to 1 MHz. The compensation is set as $\omega_{\text{pole}} = 40\,\text{kHz}$, and $\omega_{\text{zero}} = 40\,\text{kHz}$. This test is required for microprocessor, and the measured result is within VR12.5 specification.

## V. Conclusion

This paper proposes a reconfigurable on-chip compensated current-mode buck converter to achieve reconfigurable compensation and AVP in various passive components and load lines. The proposed RALL control scheme cancels the $V_o$ offset under variable $R_{\text{LL}}$ conditions. The dc equations of the proposed control were derived, and the design constraint that the product of $\text{gm}_{\text{LP}}$ and $R_{\text{LP}v}$ must equal one to cancel the offset was recognized. A reconfigurable on-chip compensation control scheme and its small-signal model are proposed. A VCCS circuit is proposed to generate a compensation zero with less parasitic pole effect, low current consumption, and small circuit area. Finally, the experimental results validate the concept of the control scheme with reconfigurability and accurate $V_o$ in various passive components and load lines.

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