A Current-Fed Dual-Active-Bridge DC–DC Converter Using Extended Duty Cycle Control and Magnetic-Integrated Inductors With Optimized Voltage Mismatching Control

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***Abstract*—For a current-fed dual-active-bridge bidirectional dc–dc converter, an extended duty cycle control is proposed. The low-voltage-side (LVS) bottom switch duty cycle can operate lower than 50%. The conduction loss of switches can be reduced by using low-voltage-rating MOSFETs for the LVS. Meanwhile, a voltage mismatching control with adaptive clamp voltage regulation is proposed to achieve zero-voltage switching for all switches throughout full load range. Besides, for LVS dc inductors, a magnetic-integrated technique is used to reduce core loss, and power density can be improved by the use of only one core. The effectiveness of the proposed control is verified by the experimental results of a 1-kW laboratory prototype.**

***Index Terms*—Current fed, dual active bridge, magnetic integration, zero-voltage switching (ZVS).**

I. Introduction

BIDIRECTIONAL dc–dc converters are widely used in energy storage systems, electric vehicles, and solid-state transformers. Among them, a voltage-fed dual active bridge (VF-DAB) has been a preferred topology. Single-phase-shift modulation is very simple, but the circulating current is high. Meanwhile, when the voltages of the two ports are not matched, the peak current will be high and the zero-voltage switching (ZVS) range will be limited. To reduce the circulation loss, many modulation strategies have been proposed, including the extended-phase-shift [1], [2], dual-phase-shift [3], [4], and triple-phase-shift [5]–[7] modulations. The circulation loss can be reduced because of the greater degree of control freedom.

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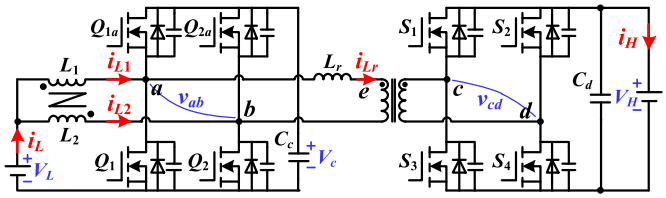

Fig. 1. Power circuit of the CF-DAB with magnetic-integrated inductors.

[26]–[29]. However, when the LVS voltage varying range is too wide, the maximum value for its bottom switch duty cycle is relatively high, causing too much circulation loss and high current ripple. Besides, the clamp voltage value is relatively high, meaning high-voltage-rating MOSFETs have to be used for the LVS. It is well known that high-voltage-rating MOSFETs have relatively higher ON-state resistance, and this causes higher conduction loss. Besides, the power density of the CF-DAB is relatively low compared with the VF-DAB due to the use of separated dc inductors for the LVS. The volume of the inductors can be reduced by using a smaller inductance value and magnetic-integration technology [30].

In this paper, an extended duty cycle control is proposed for the CF-DAB and the duty cycle for the LVS bottom switch can operate lower than 50%. The conduction loss of LVS MOSFETs can be reduced by using lower voltage rating ones, and the LVS current ripple can be minimized as well, since the duty cycle varies around 50%. ZVS for LVS switches can be achieved with lower dc inductance values when the duty cycle is less than 50%. Besides, since the voltage matching control cannot be used when the duty cycle is about 50% in view of ZVS achievement, a voltage mismatching control is proposed to generate the bias current to achieve ZVS for HVS switches. With the proposed adaptive clamp voltage regulation, the bias current can be controlled as small as possible as long as ZVS can be achieved. In addition, magnetic-integrated inductors are used to reduce core loss for dc inductors, and the power density can be improved. The converter can be used in bidirectional power applications such as battery energy storage [20]–[22], motor drive with braking absorption powered by a low-voltage battery [26], and solid-state transformers [31].

The rest of this paper is organized as follows. The operation principle of the proposed control is given in Section II. In Section III, the proposed extended duty cycle control, soft-switching condition, magnetic-integrated inductors, and adaptive clamp voltage control are discussed in detail. In Section IV, experiments are performed to verify the effectiveness of the proposed control. Section V provides the conclusions.

II. Operation Modes With the Proposed Control

A. Operation Principle of the CF-DAB With the Proposed Control

Fig. 1 illustrates the power circuit of the CF-DAB with magnetic-integrated inductors. In the LVS, two separated dc inductors are replaced by magnetic-integrated inductors just using one core. The clamp voltage V_c can be regulated by the duty cycle D for bottom switches Q_1 and Q_2. The ac inductor L_r represents the sum of the external inductor and the high-frequency transformer leakage inductor. In the HVS, MOSFETs S_1–S_4 constitute the full bridge. C_d is the HVS capacitive filter. The converter works in the boost mode as the power flows from the LVS to the HVS; otherwise, it works in the buck mode.

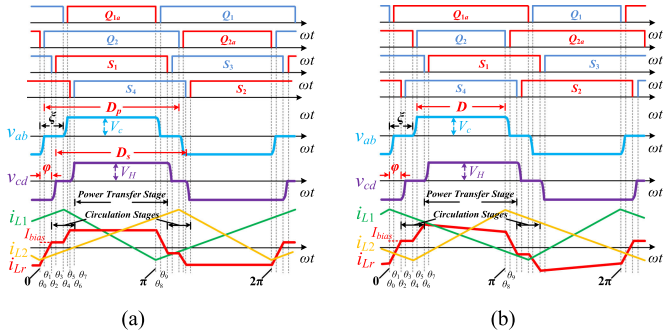

Fig. 2. Steady-state waveforms of the converter (a) of [28] when $D > 0.5$ and (b) with the proposed control when $D < 0.5$.

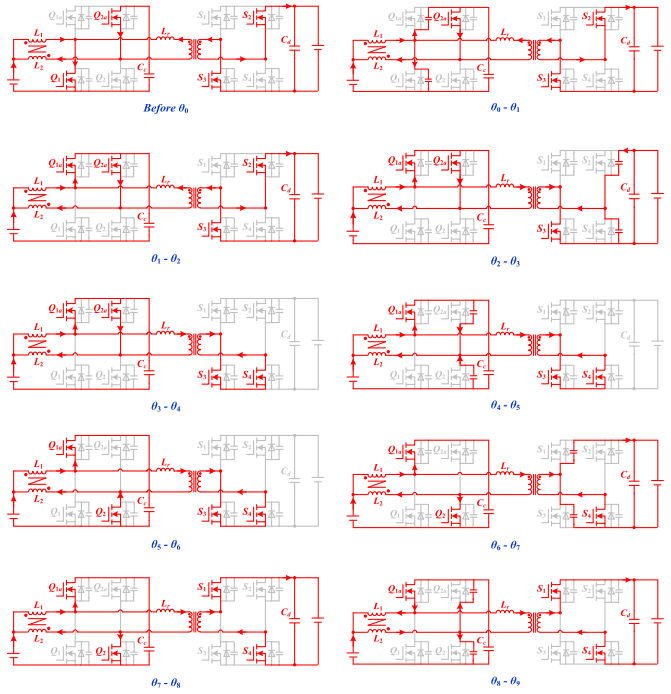

Fig. 3. Operation modes of the converter in the boost mode with $D < 0.5$.

The time diagram and steady-state waveforms of [28] when $D > 0.5$ and with the proposed control when $D < 0.5$ are shown in Fig. 2. v_{ab} and v_{cd} represent the high-frequency voltages across the transformer primary winding and secondary wingding, respectively. The phase-shift angle φ and duty cycle D are two control variables. The freewheeling interval ξ is defined as the stage when v_{ab} is zero. The power transfer stage is defined as the stage when v_{cd} is not zero, and the other stages are circulation stages. In Fig. 2(a), the effective duty cycles of the two sides D_p and D_s are unequal, and a bias current I_{bias} is generated to help achieve ZVS for HVS switches. However, this control method cannot be used when $D = 0.5$, so the duty cycle range is limited. In this paper, it is proposed that the duty cycle for the LVS bottom switch can operate lower than 50%, and ZVS can be achieved by using voltage mismatching con-

trol. As shown in Fig. 2(b), by employing proper phase shift between HVS two legs, the equivalent duty cycle of v_{ab} and v_{cd} can be same. With the proposed mismatching control strategy, the clamp voltage V_c is controlled to be a little bit lower than the primary-side-referred voltage V_s ($V_s = nV_H$). As a result, the slew rate of i_{Lr} during the main power transfer stage is negative, and a positive bias current I_{bias} is generated to help achieve ZVS for HVS switches. Fig. 3 illustrates the operation modes of the converter, and the detailed mode analysis is described as follows.

Stage 1 *(Before θ_0):* During this stage, Q_1, Q_{2a}, S_2, and S_3 conduct. v_{ab} is equal to $-V_c$, and v_{cd} is equal to $-V_H$. i_{Lr} increases slowly because of the mismatching control. Power flows from the LVS to the HVS.

Stage 2 *(θ_0–θ_1):* Q_1 turns OFF at θ_0. During the dead time, the sum of i_{L1} and $-i_{Lr}$ charges the junction capacitance of Q_1 and discharges the junction capacitance of Q_{1a} until the body diode of Q_{1a} conducts.

Stage 3 *(θ_1–θ_2):* Q_{1a} turns ON with ZVS at θ_1. v_{ab} is 0, and i_{Lr} increases linearly until S_2 turns OFF.

Stage 4 *(θ_2–θ_3):* Before S_2 turns OFF and stage 4 begins, i_{Lr} has increased to be positive. S_2 turns OFF at θ_2; i_{Lr} charges and discharges the junction capacitance of S_2 and S_4, respectively. After that, the body diode of S_4 begins to conduct.

Stage 5 *(θ_3–θ_4):* At θ_3, S_4 turns ON under ZVS. Both v_{ab} and v_{cd} are equal to 0 during this stage, and i_{Lr} remains at a small positive value I_{bias}.

Stage 6 *(θ_4–θ_5):* Q_{2a} turns OFF at θ_4. $-i_{L2}$ should be larger than i_{Lr} at this moment, and the difference between them charges and discharges junction capacitance of Q_{2a} and Q_2, respectively, until the body diode of Q_2 begins to conduct.

Stage 7 *(θ_5–θ_6):* At θ_5, Q_2 turns ON under ZVS. During this stage, i_{Lr} increases linearly to its peak value. And i_{L1} begins to decrease linearly.

Stage 8 *(θ_6–θ_7):* S_3 turns OFF at θ_6 when i_{Lr} reaches its peak value. This current charges and discharges the junction capacitance of S_3 and S_1, respectively. After that, the body diode of S_1 begins to conduct.

Stage 9 *(θ_7–θ_8):* At θ_7, S_1 turns ON under ZVS. Power flows from the LVS to the HVS.

Stage 10 *(θ_8–θ_9):* At θ_8, Q_2 turns OFF, and the sum of i_{L2} and i_{Lr} charges and discharges the junction capacitance of Q_2 and Q_{2a}, respectively. The operation modes in the second half period are similar to those of the first half period.

B. Switching Patterns and Power Expression

With the proposed control, the converter works in different switching patterns according to the transferred power value. All the possible switching patterns when the phase-shift angle φ is in the range of $[-\pi/2, \pi/2]$ are listed in Fig. 4. Taking the boost mode for example, when φ is less than the freewheeling interval ξ, the converter works in the switching patterns "light load," as shown in Fig. 4(a) and (b). When φ is larger, it operates at "heavy load," as shown in Fig. 4(c) and (d). The switching

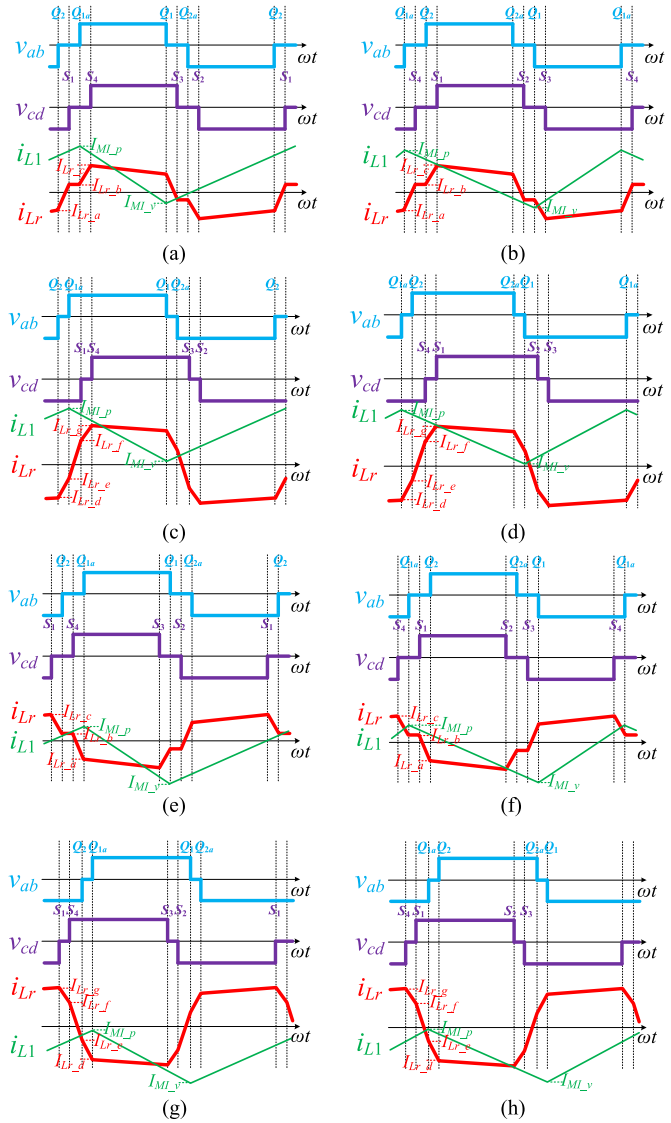

Fig. 4. Switching patterns with the proposed control. (a) Boost mode at light load $D > 0.5$. (b) Boost mode at light load $D < 0.5$. (c) Boost mode at heavy load $D > 0.5$. (d) Boost mode at heavy load $D < 0.5$. (e) Buck mode at light load $D > 0.5$. (f) Buck mode at light load $D < 0.5$. (g) Buck mode at heavy load $D > 0.5$. (h) Buck mode at heavy load $D < 0.5$.

patterns in the buck mode are similar to those in the boost mode and illustrated in Fig. 4(e)–(h). Based on Fig. 4, power expressions can be derived by

$$P = \frac{1}{T}\int_0^T v_{ab}(t) i_{Lr}(t) dt. \tag{1}$$

And the normalized power expressions can be obtained by normalizing the power expressions to the power base $P_{\text{base}} = V_c V_s T / L_r$. Power expressions of each switching patterns are listed in Table I (In Table I, $\Phi = \varphi/2\pi$ is the phase-shift ratio, $V_G = \min\{V_L, V_c - V_L\}$ is the smaller one of V_L and $V_c - V_L$).

The three-dimensional power curve has been plotted according to the normalized power expressions in Table I and has been illustrated in Fig. 5. The dashed lines are the boundaries between different switching patterns. As seen, the converter always works in these four switching patterns when $0.4 < D < 0.6$

TABLE I
POWER EXPRESSIONS IN EACH MODE

Mode	Power expression and normalized power expression
Boost Light load	$\begin{cases} P=\dfrac{V_sT}{2\pi L_r}\left(-\dfrac{V_c\lvert\varphi\rvert^2}{2\pi}+2V_G\lvert\varphi\rvert\right) \\ P^*=-\lvert\Phi\rvert^2+\dfrac{2V_G}{V_c}\lvert\Phi\rvert \end{cases}$
Buck Light load	$\begin{cases} P=-\dfrac{V_sT}{2\pi L_r}\left(-\dfrac{V_c\lvert\varphi\rvert^2}{2\pi}+2V_G\lvert\varphi\rvert\right) \\ P^*=\lvert\Phi\rvert^2-\dfrac{2V_G}{V_c}\lvert\Phi\rvert \end{cases}$
Boost Heavy load	$\begin{cases} P=\dfrac{V_sT}{2\pi L_r}\left(2\pi V_G-\dfrac{V_c\pi}{2}+V_c\lvert\varphi\rvert-\dfrac{2\pi V_G^{\,2}}{V_c}-\dfrac{V_c\lvert\varphi\rvert^2}{\pi}\right) \\ P^*=-2\lvert\Phi\rvert^2+\lvert\Phi\rvert-\dfrac{V_G^{\,2}}{V_c^{\,2}}+\dfrac{V_G}{V_c}-\dfrac{1}{4} \end{cases}$
Buck Heavy load	$\begin{cases} P=-\dfrac{V_sT}{2\pi L_r}\left(2\pi V_G-\dfrac{V_c\pi}{2}+V_c\lvert\varphi\rvert-\dfrac{2\pi V_G^{\,2}}{V_c}-\dfrac{V_c\lvert\varphi\rvert^2}{\pi}\right) \\ P^*=2\lvert\Phi\rvert^2-\lvert\Phi\rvert+\dfrac{V_G^{\,2}}{V_c^{\,2}}-\dfrac{V_G}{V_c}+\dfrac{1}{4} \end{cases}$

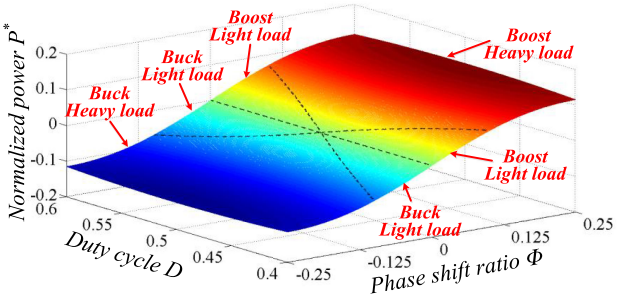

Fig. 5. Normalized power P^* curve versus D and Φ.

and $-0.25 < \Phi < 0.25$, and the working mode can be switched between different switching patterns automatically. The transferred power P increases with the increase of the phase-shift ratio Φ. The transferred power with $D < 0.5$ is symmetric with that of $D > 0.5$.

III. CONVERTER PERFORMANCE ANALYSIS

A. Proposed Extended Duty Cycle Control

For the converter, the relationship between the clamp voltages V_c and V_L is given by

$$V_c = \frac{V_L}{1-D}. \tag{2}$$

Generally, V_c cannot vary too much. If there is a significant mismatch between V_c and the HVS voltage V_H, the slew rate of i_{Lr} during the power transfer stage will be steep, causing high current spike and large circulation loss. Meanwhile, ZVS might be lost especially at light load.

Fig. 6 illustrates steady-state waveforms with different duty cycles in the boost mode. It can be seen that the circulation stage is minimum with 50% duty cycle. The lengths of circulation stages with 40% and 60% duty cycle are same. From Fig. 6(b)–(d), it can be seen that for the same output power, larger duty cycle results in longer circulation stage and high peak current. Hence, from the view of circulation loss and peak current reduction, it is better for the converter to operate with the duty cycle around 50% instead of the conventional control with duty cycle above 50% (e.g., 53–70% in [28] and 55–70% in [29]). In addition, for the same LVS voltage, lower duty cycle means a lower clamp voltage V_c. As a result, MOSFETs with low drain–source breakdown voltage can be chosen. The ON-state resistance values can be reduced, and the conduction loss can be reduced as well.

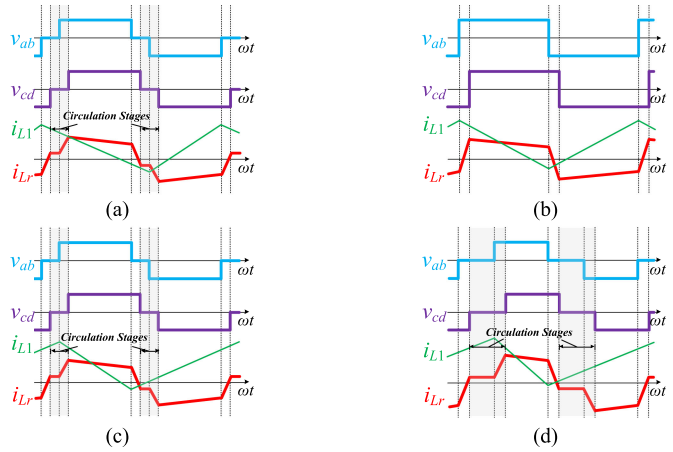

Fig. 6. Steady-state waveforms with different duty cycles in the boost mode. (a) $D = 0.4$. (b) $D = 0.5$. (c) $D = 0.6$. (d) $D = 0.7$.

TABLE II
SYSTEM SPECIFICATIONS OF THE PROPOSED D RANGE AND THE CONVENTIONAL D RANGE

	D range	V_c	N_1:N_2	MOSFETs (V_{DS})	$R_{DS\,(on)}$
Proposed	0.435~0.565	46V	0.128	IPT007N06N (60V)	0.75mΩ
Conventional	0.5~0.615	52V	0.144	IPT012N08N5 (80V)	1.2mΩ

A comparison has been made between the proposed control and the conventional control according to the system specifications in Table IV. In Table II, V_c is designed according to the duty cycle operating range. MOSFETs with different rated voltage are used as LVS power switches. The clamp voltage is 46 V with the proposed extended duty cycle, and Infineon OptiMOS IPT007N06N can be used since its rated voltage is 60 V. Since the clamp voltage is 52 V with the conventional control, IPT012N08N5 whose voltage rating is 80 V is chosen as the LVS MOSFETs for reliability.

The conduction loss comparison of LVS power switches is shown in Fig. 7. Although V_c is lower with the proposed duty cycle range, the RMS of LVS switch currents is almost the same as that with the conventional duty cycle range because of the shorter circulation stage. With the selected LVS MOSFETs shown in Table II, the drain–source ON-state resistance can be reduced significantly with the proposed control, so the conduction loss can be reduced in a wide range, as shown in Fig. 7.

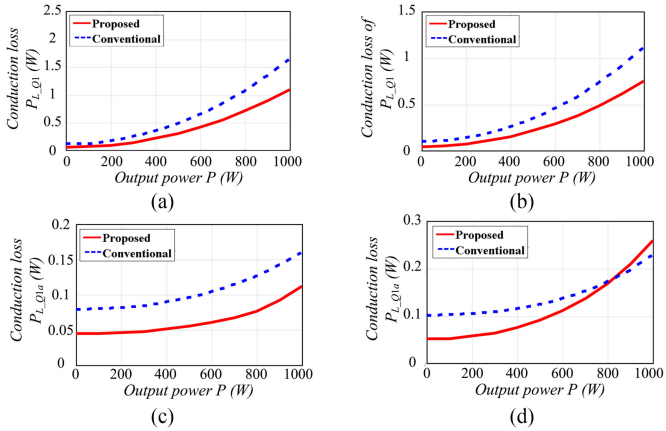

Fig. 7. Conduction loss comparison for LVS power switches. (a) Q_1 when $V_L = 20$ V. (b) Q_1 when $V_L = 26$ V. (c) Q_{1a} when $V_L = 20$ V. (d) Q_{1a} when $V_L = 26$ V.

B. Soft-Switching Conditions

If the junction capacitance of the switches is neglected, power switches can turn ON under ZVS when there is a current flowing from source to drain before the switch turns ON. From the mode analysis given in Section II, the secondary-side-referred i_{Lr} helps to achieve ZVS of HVS power switches, while the junction capacitance of LVS switches is charged and discharged by the difference between i_{Lr} and i_{L1} (or i_{L2}). Taking the operation in the boost mode at light load with $D < 0.5$ for example, from Fig. 4(b), the secondary-side-referred bias current I_b flows from source to drain before S_4 turns ON, while the secondary-side-referred peak current I_c flows from source to drain before S_1 turns ON. Then, the ZVS condition for S_4 and S_1 can be obtained as $I_b > 0$ and $I_c > 0$, respectively. For LVS switches, the current $I_{MI\_p} - I_a$ charges and discharges the junction capacitance before Q_{1a} turns ON. And the current $-I_{MI\_v} - I_b$ helps to achieve ZVS before Q_1 turns ON. Since the ZVS conditions for S_2, S_3, Q_{2a}, and Q_2 are same as S_4, S_1, Q_{1a}, and Q_1 respectively, the ZVS conditions for all switches in this switching pattern have been obtained. The ZVS conditions in other switching patterns can be obtained similarly and have been summarized in Table III.

Some of ZVS conditions in Table III can be met easily. For example, when the converter works in the boost mode at light load with $D < 0.5$, the peak current I_c is always larger than the bias current I_b. So once the ZVS conditions of S_2 and S_4 can be met, the ZVS of S_1 and S_3 can be achieved surely. In the LVS, it can be seen from Fig. 4 that all power switches can achieve ZVS easily when $D > 0.5$. However, when $D < 0.5$, half of the switches cannot achieve ZVS easily, and the magnetic-integrated inductance should be properly designed to meet the ZVS condition. The ZVS conditions that are difficult to be met are highlighted with asterisk in Table III.

In order to achieve ZVS for all the switches throughout the full-load range in spite of the LVS voltage, all the highlighted ZVS conditions in different switching patterns should be considered. According to the highlighted ZVS conditions in Table III, the ZVS current (the current that helps to achieve ZVS) for the HVS switches, which are difficult to achieve ZVS, is defined as

$$I_{\text{sc\_}H} = \begin{cases} nI_b, & \text{light load} \\ nI_f, & \text{heavy load} \end{cases} \tag{3}$$

where $n = N_1/N_2$ is the turn ratio of the transformer.

The ZVS current for LVS switches, which are difficult to achieve ZVS, is defined with $D < 0.5$ as

$$I_{\text{sc\_}L} = \begin{cases} -I_{\text{MI\_}v} - I_b, & \text{boost light load} \\ -I_{\text{MI\_}v} - I_e, & \text{boost heavy load} \\ I_{\text{MI\_}p} - I_b, & \text{buck light load} \\ I_{\text{MI\_}p} - I_e, & \text{buck heavy load.} \end{cases} \tag{4}$$

The ZVS currents I_{sc_H} and I_{sc_L} include all of the ZVS conditions with asterisk in Table III. Fig. 8 illustrates the ZVS current curves versus D and φ based on the parameters shown in Table IV, and these curves show that in which case it is the most difficult to achieve ZVS. The switches can turn ON under ZVS if there is a current large enough to charge and discharge the junction capacitors. As can be seen in Fig. 8(a), the ZVS current I_{sc_H} becomes minimum and varies very slightly at light load, and ZVS can be achieved easier for HVS switches at heavy load. Fig. 8(b) indicates that it is the most difficult for LVS switches to achieve ZVS at the critical load when the duty cycle is minimum. At the critical load, the converter works in the boundary conduction mode between light load and heavy load, as shown in Fig. 4. It must be pointed out that at the critical load, the leakage inductance current i_{Lr} becomes continuous

TABLE III
ZVS CONDITIONS FOR ALL SWITCHING PATTERNS

	S_1&S_3	S_2&S_4	Q_1&Q_2	Q_{1a}&Q_{2a}
Boost Light load D>0.5	***I_b>0**	I_c>0	-I_{MI_v}-I_a>0	I_{MI_p}-I_b>0
Boost Light load D<0.5	I_c>0	***I_b>0**	***-I_{MI_v}-I_b>0**	I_{MI_p}-I_a>0
Boost Heavy load D>0.5	***I_f>0**	I_g>0	-I_{MI_v}-I_d>0	I_{MI_p}-I_e>0
Boost Heavy load D<0.5	I_g>0	***I_f>0**	***-I_{MI_v}-I_e>0**	I_{MI_p}-I_d>0
Buck Light load D>0.5	I_c>0	***I_b>0**	-I_{MI_v}-I_b>0	I_{MI_p}-I_a>0
Buck Light load D<0.5	***I_b>0**	I_c>0	-I_{MI_v}-I_a>0	***I_{MI_p}-I_b>0**
Buck Heavy load D>0.5	I_g>0	***I_f>0**	-I_{MI_v}-I_e>0	I_{MI_p}-I_d>0
Buck Heavy load D<0.5	***I_f>0**	I_g>0	-I_{MI_v}-I_d>0	***I_{MI_p}-I_e>0**

TABLE IV
SYSTEM SPECIFICATIONS

P	1kW	f	50kHz
V_L	20~26V	V_H	400V
L	4.3μH	L_r	3.62μH
N_1:N_2	6:47	k_{vc}	1.2V/kW
$t_{dz.L}$	333ns	$t_{dz.H}$	467ns

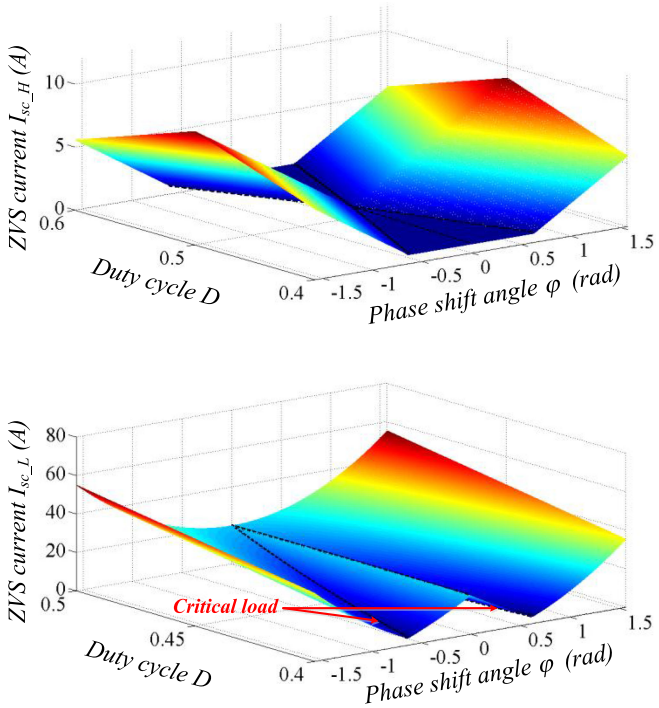

Fig. 8. ZVS current curves versus D and φ. (a) HVS current $I_{\text{sc\_}H}$. (b) LVS current $I_{\text{sc\_}L}$.

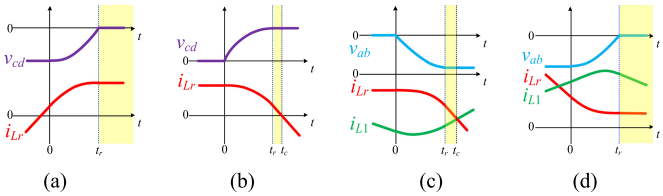

Fig. 9. Zoomed waveforms of the ZVS process. (a) S_1 in the boost mode at light load $D > 0.5$. (b) S_4 in the buck mode at light load $D > 0.5$. (c) Q_1 in the boost mode at light load $D < 0.5$. (d) Q_{1a} in the buck mode at light load $D < 0.5$.

and the slew rate does not change in the circulating stage. In other words, once the ZVS condition can be met in these cases, ZVS can be achieved for all switches throughout the full-load range in spite of V_L. As illustrated in Fig. 8, the parameters shown in Table IV are suitable for the ZVS achievement.

In order to design a proper dead time to achieve ZVS, the resonant process within the dead time period should be discussed in detail. Fig. 9(a) shows the ZVS process of S_1 in the boost mode at light load. The complementary switch S_3 turns OFF at $t = 0$; then, the junction capacitor of the switches resonates with the leakage inductor until the body diode of S_1 begins to conduct. The resonance ends at time t_r, and S_1 can turn ON under ZVS after t_r as shown in the shadowed area. However, in Fig. 9(b), when the converter works in the buck mode, a negative secondary-side-referred i_{Lr} will charge and discharge the junction capacitance reversely after time t_c if S_4 does not turn ON immediately. That means the HVS dead time $t_{dz.H}$ not only has to be larger than t_r, but also smaller than t_c. In Fig. 9(c) and (d), the LVS junction capacitors resonate with both the leakage inductor and the magnetic-integrated inductors

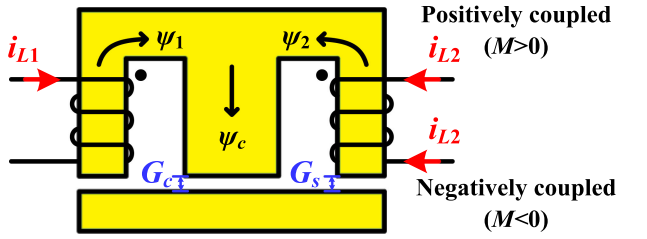

Fig. 10. Physical structure of the magnetic-integrated inductors using EI cores.

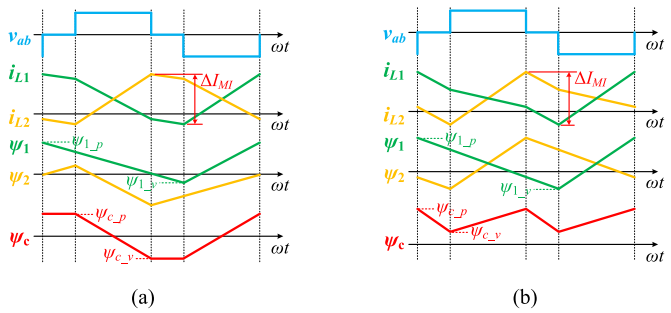

Fig. 11. Flux linkage waveforms of magnetic-integrated inductors with $D < 0.5$ in the boost mode. (a) Positively coupled. (b) Negatively coupled.

within the dead time. The inductance of magnetic-integrated inductors and the LVS dead time $t_{dz.L}$ also have to be designed properly.

According to (3) and Fig. 8(a), the ZVS range of the HVS switches can be wider by increasing the bias current I_{bias}, which can be implemented by decreasing the clamp voltage V_c. From (4) and Fig. 8(b), once I_{bias} is determined, a large current ripple on magnetic-integrated inductors ΔI_{MI} is helpful for the ZVS achievement of LVS switches. A large ΔI_{MI} can be obtained by a small inductance of magnetic-integrated inductors. The dead time range can be widened using large ZVS currents. However, a large ΔI_{MI} causes additional power loss on the magnetic-integrated inductors. As a result, the ZVS current should be designed as small as possible as long as ZVS can be obtained. It is better to achieve ZVS precisely during the dead time.

C. Analysis of the Magnetic-Integrated Inductors

In order to design optimized magnetic-integrated inductors L_1 and L_2, the flux linkage ripple and current ripple with different coupling coefficients with EI cores are discussed. The core physical structure is illustrated in Fig. 10.

When L_2 is connected with the dotted terminal, two inductors L_1 and L_2 are positively coupled, and the mutual inductance M is defined positive in this case. Otherwise, the inductors are negatively coupled and M is negative. ψ_1 and ψ_2 are the flux linkages in the two outer legs, respectively, and ψ_c is the flux linkage in the center leg. The current and flux waveforms with positively and negatively coupled inductors are illustrated in Fig. 11.

Negatively coupled inductors are widely used because of the reduction of core loss. As shown in Fig. 11, the magnitude of peak-to-peak flux linkage ripple in the center leg $\Delta\psi_c$ can be reduced by the negatively coupled inductors. According to

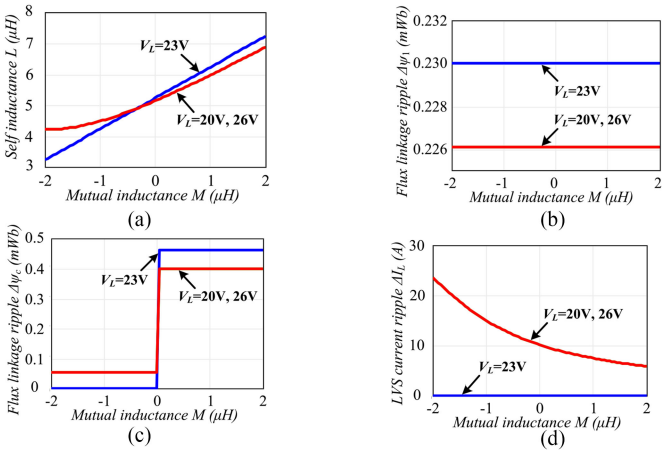

Fig. 12. Curves versus the mutual inductance M when $\Delta I_{MI} = 44$ A. (a) Self-inductance L. (b) Flux linkage ripple in the outer leg $\Delta\psi_1$. (c) Flux linkage ripple in the center leg $\Delta\psi_c$. (d) LVS current ripple ΔI_L.

Fig. 11, $\Delta\psi_1$ and $\Delta\psi_c$ in these two cases can be expressed by

$$\Delta\psi_1 = \Delta\psi_2 = V_L DT \tag{5}$$

$$\Delta\psi_c = \begin{cases} 2V_G\,|D-0.5|\,T, & M<0 \\ V_G T, & M>0. \end{cases} \tag{6}$$

The performance with different coupled coefficients of the coupled inductors is studied to choose the optimum value of the coupling coefficient. Since the ZVS condition of LVS switches is related to the current ripple on inductors ΔI_{MI}, L and M of the magnetic-integrated inductors should be designed to make ΔI_{MI} large enough in view of ZVS achievement. Fig. 12(a) shows the self-inductance L to make $\Delta I_{MI} = 44$ A with different M. ΔI_{MI} is constant when L and M follow this curve, meaning that ZVS conditions are same when L and M follow this curve. Based on this curve, the flux linkage ripple and LVS current ripple ΔI_L curve versus M are illustrated in Fig. 12(b)–(d). As can be seen in Fig. 12(b), $\Delta\psi_1$ has nothing to do with the coupled coefficient, and $\Delta\psi_c$ is also constant when $M < 0$, as shown in Fig. 12(c), meaning that the core loss does not change with the coupled coefficient when the inductors are negatively coupled. As shown in Fig. 12(d), the LVS current ripple ΔI_L decreases with the increase of M, and ΔI_L is minimum when M is close to 0 when the inductors are negatively coupled. As a result, the magnetic-integrated inductors should be negatively coupled, M should be close to 0, and L should be designed to make ΔI_{MI} large enough in view of the ZVS achievement. Thus, for the EI as shown in Fig. 10, the air gap distance of the two outer legs is larger than that of the center leg. The coupled coefficient is close to 0, and the current waveforms are similar to two separated inductors, but the core loss in the center leg is minimized due to the magnetic integration.

D. Analysis of the Adaptive Clamp Voltage

All the circuit elements are considered to be ideal in previous analysis. But, for an actual circuit, the parasitic resistance of components causes voltage drop. In this paper, ZVS is achieved

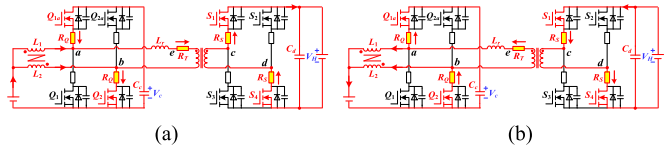

Fig. 13. Working modes of the main power transfer stage with different power flow directions when $D < 0.5$. (a) In the boost mode. (b) In the buck mode.

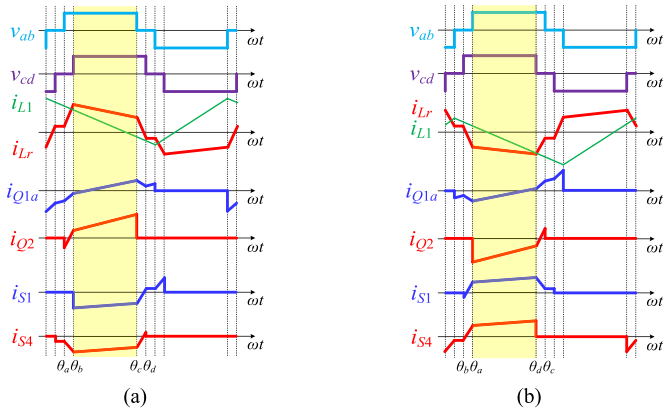

Fig. 14. Currents of power switches with different power flow directions when $D < 0.5$. (a) In the boost mode. (b) In the buck mode.

by the voltage mismatching control. The voltage drops will affect ZVS conditions especially under heavy-load conditions, and ZVS may be lost for LVS switches in the boost mode and for HVS switches in the buck mode. To deal with this issue, an adaptive clamp voltage is proposed, with which the clamp voltage can adapt to the transferred power value automatically. The ZVS conditions can be kept almost the same regardless of transferred power values.

Fig. 13 illustrates working modes of the main power transfer stage with different power flow directions. R_Q, R_S, and R_T represent the parasitic resistance of the LVS switches, HVS switches, and the transformer primary winding, respectively. In order to describe the voltage drops, V_P, V_S, and V_D represent the amplitude of v_{ab}, v_{eb}, and v_{cd}, respectively. If the parasitic resistors are neglected, it is easy to conclude that $V_P = V_c$ and $V_S = nV_D = nV_H$. As can be seen in Fig. 13, the current directions in these components are different in boost and buck modes. From Fig. 13(a), it can be obtained that $V_P < V_c$ and $V_S > nV_D > nV_H$. Since the difference between V_P and V_S is increased due to the voltage drops, it is easier to achieve ZVS for HVS switches but more difficult for LVS switches. However, opposite conclusion can be got once it works in the buck mode, as shown in Fig. 13(b). As a result, it is difficult to achieve ZVS throughout the full-load range with fixed-clamp-voltage regulation.

The current waveforms of power switches with different power flow directions are shown in Fig. 14. In Fig. 14, $\theta_a - \theta_c$ is defined as the stage when v_{ab} is positive, and $\theta_b - \theta_d$ is the stage when v_{cd} is positive. In order to calculate the voltage drops, the average currents in power switches during specific stages need to be known. For example, when the parasitic resistance is taken into account, v_{ab} is not constant during the stage $\theta_a - \theta_c$. Thus,

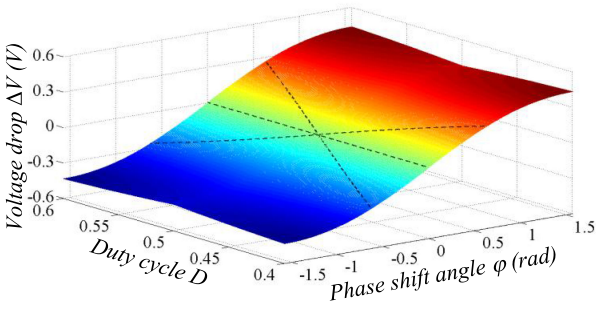

Fig. 15. Total voltage drop ΔV curve versus D and φ.

V_P can be considered as the average value of v_{ab} during $\theta_a - \theta_c$. So, the average currents of i_{Q1a} and i_{Q2} need to be known.

According to the waveforms shown in Fig. 4, the average value of i_{Lr} during the stage $\theta_a - \theta_c$ can be expressed by (7) shown at the bottom of this page.

The average value of i_{L1} and i_{L2} during the stage $\theta_a - \theta_c$ can be obtained as

$$i_{L1\text{avg\_ac}} = i_{L2\text{avg\_ac}} = \frac{P}{2V_L}. \tag{8}$$

And the average currents of i_{Q1a} and i_{Q2} during the stage $\theta_a - \theta_c$ can be obtained as

$$\begin{cases} i_{Q1a\text{avg\_ac}} = i_{Lr\text{avg\_ac}} - i_{L1\text{avg\_ac}} \\ i_{Q2\text{avg\_ac}} = i_{Lr\text{avg\_ac}} + i_{L2\text{avg\_ac}}. \end{cases} \tag{9}$$

The average currents of i_{S1} and i_{S4} during the stage $\theta_b - \theta_d$ can be expressed by

$$i_{S1\text{avg\_}bd} = i_{S4\text{avg\_}bd} = -ni_{Lr\text{avg\_}bd} = -n\frac{V_P}{V_S}i_{Lr\text{avg\_ac}}. \tag{10}$$

Then, the voltage drops on the LVS switches, transformer, and HVS switches can be written, respectively, by

$$\begin{cases} \Delta V_Q = V_c - V_p = \left(i_{Q1a\text{avg\_ac}} + i_{Q2\text{avg\_ac}}\right) R_Q \\ \qquad = 2i_{Lr\text{avg\_ac}} R_Q \\ \Delta V_T = V_s - nV_D = 2i_{Lr\text{avg\_}bd} R_T \\ \Delta V_S = V_D - V_H = -\left(i_{S1\text{avg\_}bd} + i_{S4\text{avg\_}bd}\right) R_S \\ \qquad = 2ni_{Lr\text{avg\_}bd} R_S. \end{cases} \tag{11}$$

And the total voltage drop is defined as

$$\Delta V = \Delta V_Q + \Delta V_T + n\Delta V_S. \tag{12}$$

Fig. 15 shows the total voltage drop ΔV curve versus D and φ when $R_Q = 0.75\,\text{m}\Omega$, $R_S = 80\,\text{m}\Omega$, and $R_T = 5\,\text{m}\Omega$. According to Fig. 15, the difference between V_P and V_S becomes maximum at heavy load in the boost mode, but is minimum at heavy load in the buck mode. The voltage drop is determined by the transferred power value, and the LVS voltage value has less effect on it. The voltage drop is nearly 0.3 V with 1-kW output power according to the given parameters.

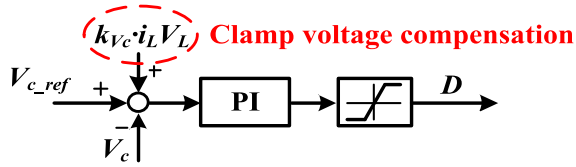

Fig. 16. Control strategy of the adaptive clamp voltage.

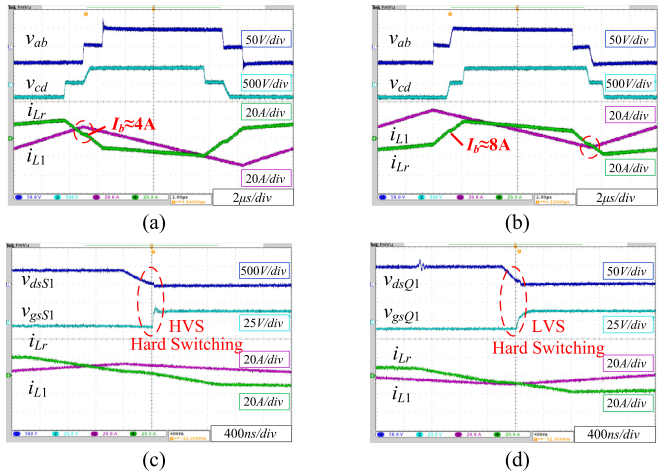

Fig. 17. Experimental results with constant clamp voltage under the critical load condition when $V_L = 26$ V. (a) Steady-state waveforms in the buck mode. (b) Steady-state waveforms in the boost mode. (c) ZVS loss of S_1 in the buck mode. (d) ZVS loss of Q_1 in the boost mode.

An adaptive clamp voltage control is proposed, as shown in Fig. 16. The clamp voltage reference varies in a narrow range according to the transferred power. k_{vc} is the adapt clamp voltage coefficient. Since $i_L V_L$ represents the transferred power value, the clamp voltage V_c increases as the transferred power increases. When the parasitic resistance is large, a large k_{vc} is necessary to keep the bias current under different load conditions; otherwise, a small k_{vc} is enough. So, k_{vc} should be set according to the specific prototype and the experimental test. The effectiveness of the proposed adaptive clamp voltage will be verified by the experimental results in the next section.

IV. Experimental Results

A 1-kW experimental prototype has been built in order to verify the effectiveness of the current-fed bidirectional dc–dc

$$i_{Lr\text{avg\_ac}} = \begin{cases} \frac{T}{8\pi^2 L_r V_G}\left(-|\varphi|^2 V_P V_S + 4\pi|\varphi| V_G V_S\right), & \text{boost light load} \\ -\frac{T}{8\pi^2 L_r V_G}\left(-|\varphi|^2 V_P V_S + 4\pi|\varphi| V_G V_S\right), & \text{buck light load} \\ \frac{TV_S}{8\pi^2 L_r V_G V_P}\left(-2|\varphi|^2 {V_P}^2 + 2\pi|\varphi| {V_P}^2 - \pi^2 {V_P}^2 + 4\pi^2 V_G V_P - 4\pi^2 {V_G}^2\right), & \text{boost heavy load} \\ -\frac{TV_S}{8\pi^2 L_r V_G V_P}\left(-2|\varphi|^2 {V_P}^2 + 2\pi|\varphi| {V_P}^2 - \pi^2 {V_P}^2 + 4\pi^2 V_G V_P - 4\pi^2 {V_G}^2\right), & \text{buck heavy load.} \end{cases} \tag{7}$$

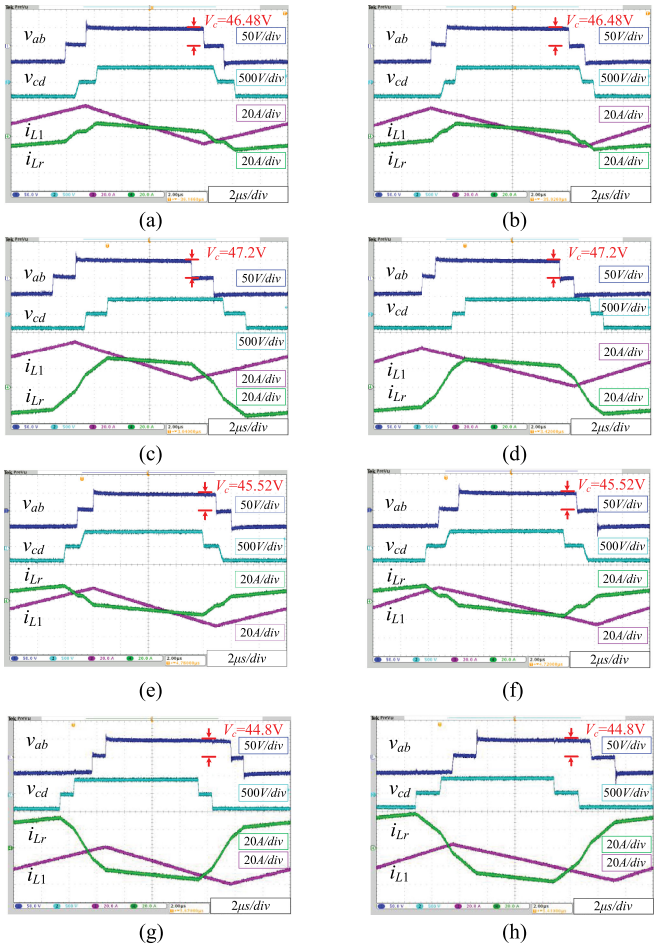

Fig. 18. Steady-state operating waveforms with the proposed control. (a) In boost mode when $P = 400$ W and $V_L = 20$ V. (b) In the boost mode when $P = 400$ W and $V_L = 26$ V. (c) In the boost mode when $P = 1$ kW and $V_L = 20$ V. (d) In the boost mode when $P = 1$ kW and $V_L = 26$ V. (e) In the buck mode when $P = 400$ W and $V_L = 20$ V. (f) In the buck mode when $P = 400$ W and $V_L = 26$ V. (g) In the buck mode when $P = 1$ kW and $V_L = 20$ V. (h) In the buck mode when $P = 1$ kW and $V_L = 26$ V.

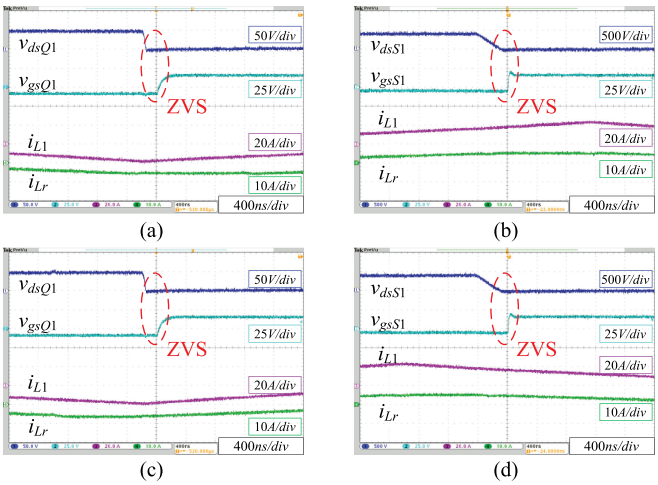

Fig. 19. ZVS waveforms of the converter with the proposed control with no load. (a) Q_1 when $V_L = 20$ V. (b) S_1 when $V_L = 20$ V. (c) Q_1 when $V_L = 26$ V. (d) S_1 when $V_L = 26$ V.

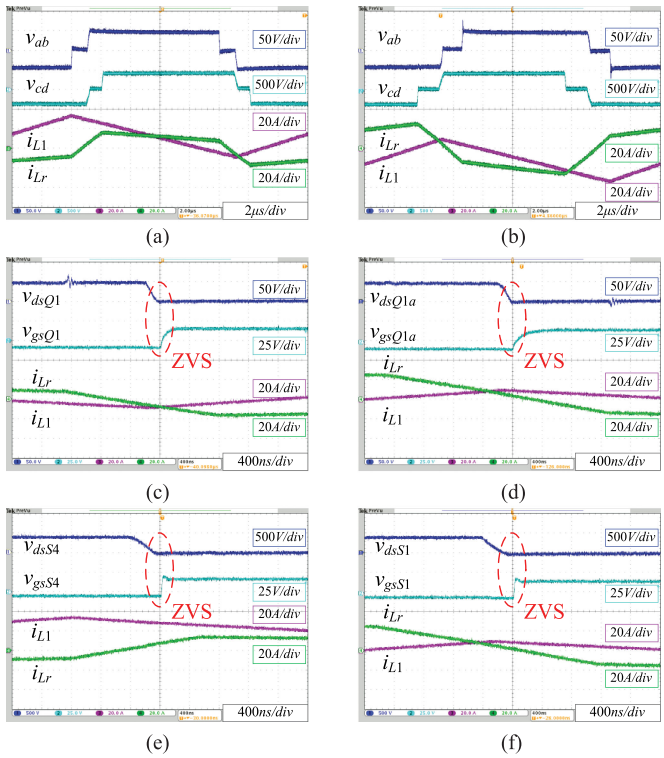

Fig. 20. Experimental results with the critical load when $V_L = 26$ V. (a) Steady-state waveforms in the boost mode. (b) ZVS waveforms of Q_1 in the boost mode. (c) ZVS waveforms of S_4 in the boost mode. (d) Steady-state waveforms in the buck mode. (e) ZVS waveforms of Q_{1a} in the buck mode. (f) ZVS waveforms of S_1 in the buck mode.

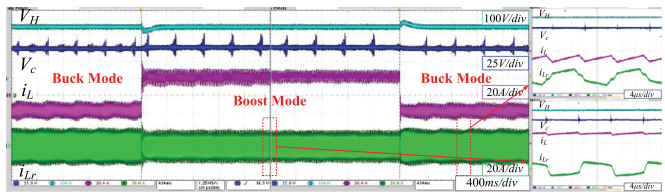

Fig. 21. Mode transition waveforms from –500 to 500 W and vice versa.

converter with the proposed control. The dc inductors are magnetic integrated, and the power loss can be reduced. The system specifications are illustrated in Table IV. The self-inductance L is 4.3 μH to make $\Delta I_{MI} = 44$ A for the ZVS achievement for LVS switches. The turn ratio is designed as 6:47 to ensure the voltage mismatching control. The dead times of LVS and HVS switches are 333 and 467 ns, respectively, to achieve ZVS precisely during the dead time. The adapt clamp voltage coefficient k_{vc} is selected as 1.2 V/kW according to the voltage drop of the actual prototype. Besides, the clamp voltage reference V_{c_ref} is 46 V. Infineon OptiMOS IPT007N06N with 60-V voltage rating are used as LVS switches. And HVS switches are CREE SiC MOSFET C2M0080120D. The entire control of the system has been implemented by TI DSP TM320F28335.

In this paper, adaptive clamp voltage control is used to keep the bias current fixed at different loads. As aforementioned, if the clamp voltage is fixed, the bias current may vary at different

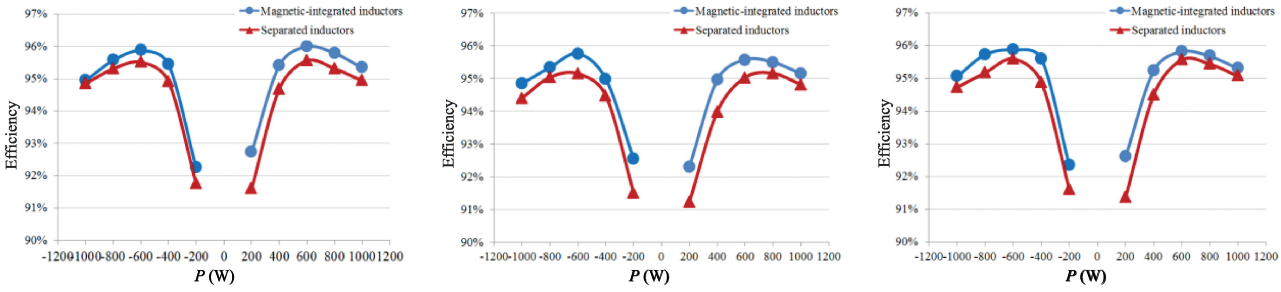

Fig. 22. Efficiency curve comparison with the proposed magnetic-integrated inductors and conventional separated inductors. (a) $V_L = 20$ V. (b) $V_L = 23$ V. (c) $V_L = 26$ V.

TABLE V
DETAILED INFORMATION OF THE MAGNETIC-INTEGRATED INDUCTORS AND SEPARATED INDUCTORS

	Core	l_e	A_e	V_e	N	ΔB_1	ΔB_c	l_g
Separated inductors	UF31D	78.9mm	133mm^2	10493.7mm^3	8	212mT	212mT	1.27mm
Magnetic-integrated inductors	EI42	67.5mm	119.5mm^2	16132.5mm^3	8	236mT	27mT	2.29mm

loads. Fig. 17(a) and (b) shows the experimental results with the voltage mismatching control and fixed clamp voltage under the critical-load condition when $V_L = 26$ V in buck and boost modes, respectively. Although the LVS voltage V_L, the HVS voltage V_H, and the clamp voltage V_c are same in these two cases, the bias currents are different due to the voltage drops on the components. As can be seen, the bias current in Fig. 17(a) is about 4 A, which is not large enough for HVS switches to achieve ZVS. Meanwhile, the bias current in Fig. 17(b) is about 8 A. Although ZVS can be achieved easily for HVS switches, the difference between i_{Lr} and i_{L1} when Q_1 turns ON is not large enough to achieve ZVS for LVS switches. Fig. 17(c) and (d) shows that ZVS is lost for S_1 in the buck mode and Q_1 in the boost mode. The benefits of the adaptive clamp voltage can be more useful in higher power applications.

Fig. 18 gives the steady-state waveforms of the converter with the proposed control working in different operating patterns. The experimental waveforms agree well with the theoretical waveforms shown in Fig. 4. Since the adaptive clamp voltage control is employed, the clamp voltage varies in a narrow range according to the transferred power and power flow direction. Fig. 18(a)–(d) shows the operating waveforms when the converter works in the boost mode. In Fig. 18(e)–(h), v_{ab} lags v_{cd} in phase implying that the power flow is reversed. The bias current is about 6 A under light-load conditions in spite of the power flow direction.

ZVS waveforms of the converter under no load are shown in Fig. 19. In this case, ZVS can be achieved for all switches by employing the proposed control. Fig. 20 illustrates the steady-state and ZVS waveforms at the critical load with the proposed adaptive clamp voltage control. Compared with ZVS loss by using fixed clamp control shown in Fig. 17, ZVS can be ensured, thanks to the adaptive clamp voltage control. The experimental results shown in Figs. 18– 20 indicate that ZVS can be achieved for all switches throughout full range of load by using the proposed control.

A mode transition experiment is conducted in order to show the dynamic response of the converter. In the experiment, a 25.5-V battery is connected with the converter in the LVS, while the HVS is connected with a three-phase inverter. Fig. 21 illustrates the mode transition waveforms from –500 to 500 W and vice versa, and the zoomed waveforms are shown on the right side. The battery voltage is about 25 V in the boost mode but 26 V in the buck mode because of the internal resistance. The experimental result shows that the working mode can be switched between boost and buck modes automatically.

The conversion efficiency including driving loss for the converter with the proposed control with different battery voltages is shown in Fig. 22. The overall conversion efficiency is high, and the highest efficiency of the converter reaches 96% under the 600-W-load condition. With the conventional duty cycle range control, the efficiency with low battery voltage is low especially under the heavy-load condition because of the large duty cycle [28]. However, the maximum duty cycle is reduced by the proposed extended duty cycle range, and the conversion efficiency is almost the same with different battery voltages.

In order to verify the effectiveness of the magnetic-integrated inductors, the efficiency with separated inductors is also measured. The detailed information of the magnetic-integrated inductors and separated inductors is given in Table V. Both the magnetic-integrated inductors and separated inductors are designed with self-inductance $L = 4.2\,\mu$H. The cores are UF31D and EI42 from DMEGC, respectively. From Table V, it can be seen that the effective areas A_e of the two cores are almost same, and the volume of the magnetic-integrated inductors (16 132.5 mm^3) is reduced compared with the conventional two separated inductors ($2 \times 10\,493.7$ mm^3). Both of the two designs are eight turns. As can be seen, the flux density in the

center leg ΔB_c can be reduced significantly by the magnetic integration. l_g is the theoretical air gap of the inductors to make $L = 4.2\,\mu$H. In the experiment, the air gap is slightly different with the theoretical value.

As shown in Fig. 22, magnetic-integrated inductors achieve higher efficiency than the separated inductors with the same magnetic material. Since the core loss makes up the majority of the total loss under the light-load condition, the power loss at light load can be reduced significantly by using magnetic-integrated inductors.

V. Conclusion

In this paper, an extended duty cycle range and optimized voltage mismatching control are proposed for the CF-DAB. With the extended duty cycle control, the LVS bottom switch duty cycle can operate lower than 50%. This makes low-voltage-rating MOSFETs be used for LVS, and the conduction loss can be reduced. The LVS current ripple can be reduced in many cases. The circulating duration length can be shortened when the LVS voltage is relatively high. The proposed voltage mismatching control with adaptive clamp voltage is very effective in obtaining ZVS for all of the switches throughout the full-load range in spite of the transferred power and power flow directions. Magnetic-integrated dc inductors help to improve the power conversion efficiency especially at light-load conditions. The design considerations have been demonstrated. Experimental results from a 1-kW prototype have verified the effectiveness of the theoretical analysis.

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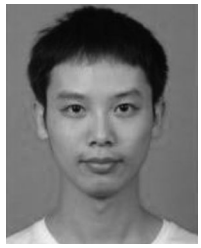

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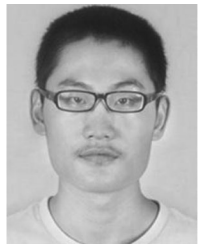

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