A Comprehensive Optimization Control of Dual-Active-Bridge DC–DC Converters Based on Unified-Phase-Shift and Power-Balancing Scheme

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***Abstract*—This paper presents a comprehensive optimization control scheme to improve efficiency and dynamic response of dual-active-bridge (DAB) dc–dc converters. Unified-phase-shift (UPS) control is widely used to increase the efficiency of DAB dc–dc converters by minimizing the peak current, but dynamic performance of the converters needs to be further enhanced. In this paper, to gain superior dynamic performance of DAB dc–dc converters, an equivalent power-balancing (PB) model is employed, which is capable of predicting dynamic behavior of converter output voltages due to input voltage fluctuation and load disturbance. And then, combining the UPS control and the PB control, a comprehensive UPS and PB (UPS-PB) scheme is proposed to improve the efficiency and dynamic performance simultaneously. This work also includes the detailed inductance parameter sensitivity of the proposed UPS-PB scheme and a zonal voltage control strategy to further improve dynamic responses of the output voltage under the start-up process or a large step change of the output voltage reference. Moreover, the variant of UPS-PB scheme for constant power load is analyzed in the experimental part. Finally, experimental results have verified the excellent performance of the proposed UPS-PB scheme and correctness of theoretical analysis in this work.**

***Index Terms*—Dynamic response, efficiency, peak current, power-balancing (PB) model, unified-phase-shift (UPS) control, zonal control.**

I. Introduction

A DUAL-ACTIVE-BRIDGE (DAB) dc–dc converter topology was first proposed in [1] at the beginning of 1990s, as shown in Fig. 1. It is a symmetric, isolated, and bidirectional dc–dc converter, which can easily realize zero-voltage switching and form cascading or paralleling configurations. Thus, this converter topology has been widely used in distributed generation systems [2]–[4], automotive applications [5]–[8], energy storage systems [9]–[10], and railway locomotive power electronic transformer applications [11], [12].

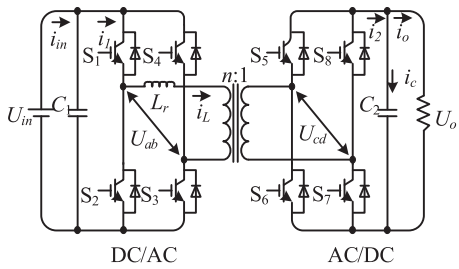

Fig. 1. Topology of a DAB dc–dc converter.

High efficiency is an essential requirement of DAB dc–dc converters in all the above-mentioned applications. As a result, in order to improve the converter efficiency, various switching strategies were reported to directly minimize power losses by establishing the power-loss model of DAB dc–dc converters [13], [14]. However, these control methods require offline computations according to various operating conditions, so it is difficult to realize continuous optimal control of the converter. In addition, the efficiency improvement can also be realized by reducing the peak current [15]–[18] or root-mean-square (rms) value [19], [20] of inductor current in DAB dc–dc converters. In order to improve converter efficiency and reduce complicated computation in the traditional current-stress-optimized (CSO) strategies [16], [17], a simple CSO scheme was proposed in [18] to realize the minimum-current-stress performance by using a unified-phase-shift (UPS) control. On this basis, a minimum rms current method was proposed in [19] to improve the efficiency of DAB dc–dc converters. Comparing with the switching strategy in [20], this minimum rms current strategy can reduce the calculation complexity.

However, the aforementioned optimization strategies [15]–[20] only focused on boosting the efficiency of DAB dc–dc converters, while dynamic performance has not been mentioned. In almost all DAB converter applications, superior dynamic performance of the converter is desired, particularly under input

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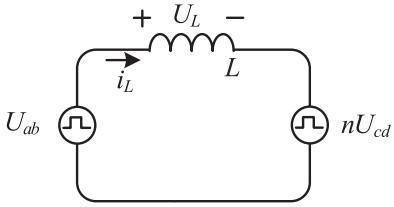


Fig. 2. Equivalent topology of DAB dc–dc converters.

voltage fluctuation and output load disturbance. For dynamic control of DAB converters, Zhao *et al.* [21]–[23] have utilized various advanced mathematic methods, such as the small-signal modeling and the discrete-time average modeling methods, to describe dynamic characteristics of DAB dc–dc converters. In addition, combining with the single-phase-shift (SPS) control, Segaran *et al.* [24] proposed a load current feed-forward compensation strategy to improve transient response of DAB dc–dc converters under the load disturbance condition. Similarly, in order to improve dynamic response to load changes, a model-based phase-shift control was proposed and analyzed with a feed-forward control theory in [25] and [26]. Moreover, a virtual direct power control scheme was developed [27] to achieve superior dynamic behaviors for DAB converters. However, none of these schemes can achieve efficiency improvement and excellent dynamic control of DAB converters simultaneously.

Due to the lack of a comprehensive optimization solution to improve both efficiency and dynamic response, a hybrid control scheme, named UPS and power-balancing (PB) (UPS-PB) scheme, is proposed in this paper. It employs the UPS control [18] to improve converter efficiency, and utilizes an equivalent PB model to improve dynamic performance of the output voltage, especially in the input voltage fluctuation and load disturbance conditions. Moreover, based on the energy storage characteristic of the capacitor, this paper adopts a zonal control of the output voltage to further enhance the dynamic responses when the actual output voltage is very far away from its desired value, such as during the start-up process and a large reference step change conditions.

The rest of the paper is organized as the following. In Section II, the UPS control idea is introduced. A PB model is presented in Section III. The hybrid control of UPS and PB scheme is proposed and discussed in Section IV. The zonal control of output voltage is given in Section IV. In Section V, an experimental hardware prototype of DAB dc–dc converter is developed to verify the accuracy of the adopted PB model, to test inductance parameter sensitiveness of UPS-PB scheme, and to compare the performance of the proposed UPS-PB scheme, UPS control, and SPS control. Finally, the work is concluded in Section VI.

II. Analysis of UPS Control

An equivalent and simplified topology of DAB dc–dc converters is shown in Fig. 2.

In Fig. 2, L represents the total inductance consisting of the transformer leakage inductor and auxiliary inductor; U_{ab} and U_{cd} represent the output pulse voltages of H_1-bridge and H_2-bridge, respectively; U_L and i_L represent the voltage and current of inductor L. n is the transformer turns ratio.

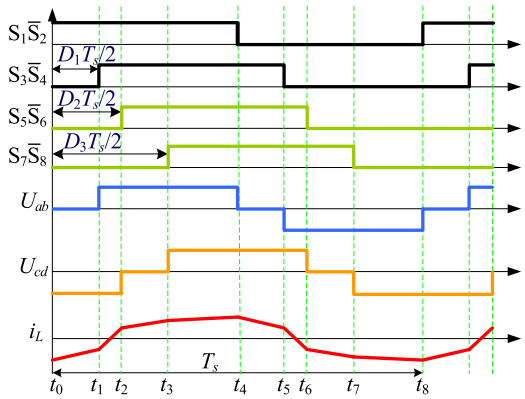


Fig. 3. Phase-shift curves of DAB dc–dc converters with UPS control.

Phase-shift curves of DAB dc–dc converters with UPS control are shown in Fig. 3 [22], where T_s represents a switching cycle, $D_1T_s/2$ represents the phase shift angle between S_1 and S_3, $D_2T_s/2$ represents the phase shift angle between S_1 and S_5, and $D_3T_s/2$ represents the phase shift angle between S_1 and S_7. Phase-shift angles are all referred to the same reference modulation signal S_1.

The transferred power P of DAB dc–dc converters with UPS control is described as

$$P = \begin{cases} \dfrac{nU_{\text{in}}U_o}{4f_sL}(-D_1+D_2+D_3-D_1^2 \\ \quad -D_2^2-D_3^2+D_1D_2+D_1D_3) & (D_1 \le D_2 \le D_3 \le 1) \\ \dfrac{nU_{\text{in}}U_o}{4f_sL}(-D_1+D_2+D_3 \\ \quad +D_1D_3-D_3^2-D_1D_2) & (D_2 \le D_1 \le D_3 \le 1) \\ \dfrac{nU_{\text{in}}U_o}{4f_sL}(-D_1+D_2+D_3 \\ \quad +D_1^2-D_1D_2-D_1D_3) & (D_2 \le D_3 \le D_1 \le 1) \end{cases} \tag{1}$$

where f_s is the switching frequency. Assuming $k = U_{\text{in}}/nU_o$ and $k \ge 1$ (the other condition $k < 1$ can be analyzed similarly), the peak current i_{PU} can be expressed as [18]

$$i_{\text{PU}} = \frac{nU_o}{4f_sL}[D_2+D_3-1+k(1-D_1)]. \tag{2}$$

According to (1) and (2), the unified transferred power p and the unified peak current i_{pu} with UPS control can be

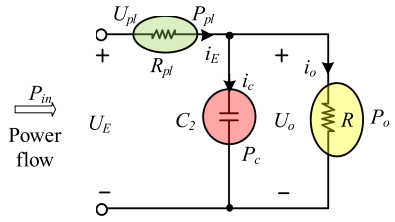


Fig. 4. Power flow model of the adopted DAB dc–dc converter.

rewritten as

$$\begin{cases} p=\dfrac{P}{P_N}= \\ \begin{cases} -D_1+D_2+D_3-D_1^2 \\ -D_2^2-D_3^2+D_1D_2+D_1D_3 \quad (D_1\le D_2\le D_3\le 1) \\ -D_1+D_2+D_3 \\ +D_1D_3-D_3^2-D_1D_2 \quad (D_2\le D_1\le D_3\le 1) \\ -D_1+D_2+D_3 \\ +D_1^2-D_1D_2-D_1D_3 \quad (D_2\le D_3\le D_1\le 1) \end{cases} \\ i_{pu}=\dfrac{i_{\mathrm{PU}}}{i_{PN}}=D_2+D_3-1+k(1-D_1) \end{cases} \tag{3}$$

where P_N and i_{PN} are defined as

$$\begin{cases} P_N=\dfrac{nU_{\mathrm{in}}U_o}{4f_sL} \\ i_N=\dfrac{nU_o}{4f_sL} \end{cases}. \tag{4}$$

Similarly, the unified transferred power p and unified peak current i_{ps} in SPS control [3] can be also expressed with respect to the phase-shift ratio D as

$$\begin{cases} p=2D(1-D) \\ i_{ps}=2D-1+k \end{cases}. \tag{5}$$

III. PB Model of DAB DC–DC Converter

It is well known that direct power control is an efficient strategy to boost the dynamic response of power converters when there exists the input voltage or the load fluctuation. So, if the relation between the input and output powers can be directly described, the dynamic response of DAB dc–dc converters can be significantly improved. The simplified power flow model of this converter seen from the load side can be shown as Fig. 4.

In Fig. 4, U_E is equal to the input voltage, i_E equals the input current, P_{in} is the input power, U_{pl} is the voltage across the equivalent loss resistance R_{pl}, P_{pl} is the power loss, P_c is the absorbing power of C_2, and P_o is the output power. Based on the Energy Conservation Law, the energy-balancing model during an interval t' of the DAB dc–dc converter can be expressed as

$$\begin{aligned} W_E&=\int_t^{t+t'}U_Ei_E\,dt=E_{pl}+E_o+\Delta E_c \\ &=\int_t^{t+t'}U_{pl}i_E\,dt+\int_t^{t+t'}U_oi_o\,dt+\int_t^{t+t'}U_oi_c\,dt \end{aligned} \tag{6}$$

where W_E is the equivalent input energy, E_{pl} is the loss energy, E_o is the consumed energy by load R, and ΔE_c is the stored energy of capacitor C_2. According to (6), the PB model of this converter during a switching cycle can be approximately expressed with respect to the average values of U_{pl}, U_o, i_o, and i_c as follows:

$$\begin{aligned} P_{\mathrm{in}}&=f_sW_E \\ &=f_s\int_t^{t+T_s}U_{pl}i_E\,dt+f_s\int_t^{t+T_s}U_oi_o\,dt+f_s\int_t^{t+T_s}U_oi_c\,dt \\ &=(\overline{U_{pl}}+\overline{U_o})\overline{i_o}+(\overline{U_{pl}}+\overline{U_o})\overline{i_c} \end{aligned} \tag{7}$$

where f_s is the switching frequency.

However, the input power in (7) of this converter is not easily obtained online by digital controllers, and this is because the average current value cannot be easily estimated due to current fluctuations. Fortunately, the transferred power of DAB dc–dc converters can be estimated through the relationships among the input and output powers. Assuming that power losses of this converter are equal to zero, the input power P_{in}, the transferred power P', and the output power P_o should be the same. Then, the relationships of these power values can be expressed as

$$P_{\mathrm{in}}=U_{\mathrm{in}}i_{\mathrm{in}}=P'=\frac{nU_{\mathrm{in}}U_o'}{4f_sL}p=P_o'=U_o'i_o'=\frac{U_o'^2}{R} \tag{8}$$

where U_o' and i_o' represent the output voltage and load current without power losses of DAB dc–dc converter. When the power losses are considered, the output power P_o can be expressed with respect to the input power P_{in} as

$$P_o=U_oi_o=\frac{U_o^2}{R}=\eta P_{\mathrm{in}}=\eta U_{\mathrm{in}}i_{\mathrm{in}} \tag{9}$$

where η is the efficiency of the DAB dc–dc converter. Combining (8) and (9), U_{o} can be approximatively expressed by U_o' as

$$U_o=\sqrt{\eta}U_o'. \tag{10}$$

Combining (8)–(10), the transferred power with power losses can be calculated as

$$P=\frac{nU_{in}U_o}{4f_sL}p=\frac{nU_{\mathrm{in}}\sqrt{\eta}U_o'}{4f_sL}p=\sqrt{\eta}P_{\mathrm{in}}. \tag{11}$$

Thus, when the converter operates in steady-state condition, the relationships among the input power, the transferred power, and the output power with considering power losses can be approximate expressed as

$$P_o=U_oi_o=\sqrt{\eta}P=\sqrt{\eta}\frac{nU_{\mathrm{in}}U_o}{4f_sL}p=\eta P_{\mathrm{in}}=\eta U_{\mathrm{in}}i_{\mathrm{in}}. \tag{12}$$

Based on (12), the transferred power can replace the actual input power; therefore, it saves a current sensor for measuring the input current. Then, according to (7), the PB model of the DAB dc–dc converter can be further demonstrated as

$$P=(\overline{U_{pl}'}+\overline{U_o})\overline{i_o}+(\overline{U_{pl}'}+\overline{U_o})\overline{i_c} \tag{13}$$

where $\overline{U_{pl}'}$ is the average voltage across the equivalent resistor introduced by the power losses between the transferred power

and the output power. During the short switching cycle, because the changes of i_c, i_o, and U_o are nearly linear, the average values of i_c, i_o, and U_o can be calculated as a half of the sum of their initial values and final values. Therefore, the average current $\overline{i_c}$ is expressed as

$$\begin{aligned}\overline{i_c} &= \frac{\frac{1}{2}f_s C_2[U_o^2(t+T_s)-U_o^2(t)]}{\frac{1}{2}[U_o(t+T_s)+U_o(t)]}\\ &= f_s C_2[U_o(t+T_s)-U_o(t)]. \end{aligned} \tag{14}$$

Combining (13) and (14), the transferred power can be expressed as

$$\begin{aligned}P &= \frac{n[U_{\rm in}(t+T_s)+U_{\rm in}(t)][U_o(t+T_s)+U_o(t)]}{16 f_s L}p\\ &= \frac{1}{4}[U_{pl}^{/}(t+T_s^{/})+U_{pl}(t)][i_o(t+T_s)+i_o(t)]\\ &\quad+\frac{1}{4}[U_o(t+T_s)+U_o(t)][i_o(t+T_s)+i_o(t)]\\ &\quad+\frac{1}{2}f_s C_2[U_o(t+T_s)+U_o(t)+U_{pl}^{/}(t+T_s)\\ &\quad+U_{pl}^{/}(t)][U_o(t+T_s)-U_o(t)]. \end{aligned} \tag{15}$$

Then, according to (12) and (13) by using the output power and the transmission power, $\overline{U_{pl}^{/}}$ can be approximatively expressed by $\overline{U_o}$ as

$$\overline{U_{pl}^{/}} = \frac{\overline{U_o}}{\sqrt{\eta}} - \overline{U_o}. \tag{16}$$

Combining (13) and (16), when the DAB dc–dc converter operates during the dynamic adjustment process, the output power should contain the absorbing power of capacitor C_2. Since only the power losses caused by $\overline{U_{pl}^{/}}$ are defined as power losses in the converter, and the equivalent loss resistance of DAB dc–dc converter will not change too much, the steady-state efficiency value could be used during the dynamic adjustment process.

In addition, combining (15) and (16), assuming the output voltage has reached its desired value, when the input voltage changes from $U_{\rm in}(t)$ to $\mu U_{\rm in}(t)$ at time *t*, during the next switching cycle, the PB can be expressed as follows:

$$\begin{aligned}\frac{n\mu U_{\rm in}(t)p}{16 f_s L} &= \frac{1}{2}f_s C_2\frac{[U_o(t+T_s)-U_o(t)]}{\sqrt{\eta}}\\ &\quad+\frac{[U_o(t+T_s)+U_o(t)]}{4\sqrt{\eta}R}. \end{aligned} \tag{17}$$

According to (17), the output voltage $U_o(t+T_s)$ at $t+T_s$, can be calculated as

$$\begin{aligned}U_o(t+T_s) &= U_o(t)-\frac{2}{1+2RC_2 f_s}U_o(t)\\ &\quad+\frac{R\sqrt{\eta}p}{2Lf_s(1+2RC_2 f_s)}\mu U_{\rm in}(t). \end{aligned} \tag{18}$$

Similarly, assuming the output voltage has reached its desired value, when the load resistance steps from $R(t)$ to $\mu R(t)$ at time *t*, the output voltage $U_o(t+T_s)$ at $t+T_s$, can be calculated by $U_o(t)$ as

$$\begin{aligned}U_o(t+T_s) &= U_o(t)-\frac{2}{1+2\mu R(t)C_2 f_s}U_o(t)\\ &\quad+\frac{\sqrt{\eta}p}{Lf_s(1+2\mu R(t)C_2 f_s)}\mu R(t)U_{\rm in}. \end{aligned} \tag{19}$$

Combining (18) and (19), $U_o(t+T_s)$ can be further rewritten as

$$\begin{aligned}U_o(t+T_s) &= U_o(t)-\frac{2}{1+2C_2 f_s\sqrt{\eta}R(t)}U_o(t)\\ &\quad+\frac{\sqrt{\eta}}{2Lf_s[1+2C_2 f_s\sqrt{\eta}R(t)]}pR(t)U_{\rm in}(t). \end{aligned} \tag{20}$$

From (20), dynamic behaviors of the output voltage with respect to the change of input voltage and the load resistance can be predicted and adopted to analyze dynamic characteristics of the DAB dc–dc converter.

IV. Proposed UPS With PB Scheme

A. Principle of the Proposed UPS-PB Scheme

In Section III, a PB model of the DAB dc–dc converter is established. In order to boost the dynamic performances, assuming the desired output voltage can be obtained during a switching cycle, and ignoring the power losses caused by i_c and $U_{pl}^{/}$, the desired transferred power P^* can be expressed as follows:

$$\begin{aligned}P^* &= \frac{1}{2}U_{pl}^{/}(i_o^*+i_o)+\frac{1}{4}(U_o^*+U_o)(i_o^*+i_o)\\ &\quad+\frac{1}{2}(U_o^*+U_o)f_s C_2(U_o^*-U_o). \end{aligned} \tag{21}$$

When the output voltage reaches its desired value, $(U_o^*+U_o)(i_o^*+i_o)/4$ can represent the steady-state output power of the DAB dc–dc converter, which represents the main component of the desired transferred power. Moreover, when the output voltage is far away from the desired value, $(U_o^*+U_o)f_s C_2(U_o^*-U_o)/2$ can meet the compensation power for the capacitor C_2 to force the output voltage to be equal to its desired value quickly. However, the adopted switching frequency of the DAB converter is higher than 10 kHz, thus the desired transferred power P^* is very sensitive to the output voltage error, which will lead to system instability. Thus, this paper sets a proportional limit value λ to avoid this case. Then, the required transmission power is rewritten as

$$\begin{aligned}P^* &= \frac{1}{2}U_{pl}^{/}(i_o^*+i_o)+\frac{1}{4}(U_o^*+U_o)(i_o^*+i_o)\\ &\quad+\frac{1}{2}\lambda f_s C_2(U_o^*+U_o)(U_o^*-U_o) \end{aligned} \tag{22}$$

where i_o^* can be acquired as

$$i_o^* = \frac{U_o^*}{U_o}i_o. \tag{23}$$

Combining (22) and (23), P^* can be substituted by the desired and unified transferred power p^*. Thus, the PB model can be

described as

$$p^* = \frac{2f_sL}{nU_{\text{in}}U_o}\left[\frac{1}{2}i_o(U_o^*+U_o)\left(\frac{U_o^*}{U_o}+1\right)+U_{pl}^{/}i_o\left(\frac{U_o^*}{U_o}+1\right)+\lambda f_sC_2\left(U_o^*-U_o\right)\left(U_o^*+U_o\right)\right]. \tag{24}$$

According to the existing current-stress-optimizing method [22], in order to reach minimum-current-stress and improve efficiency of the DAB dc–dc converters, the relationship of the phase-shift ratios in UPS control should satisfy as

$$\begin{cases} D_2 = \begin{cases} (k-1)(1-D_1) & \left(\frac{k-1}{k} < D_1 \le 1\right) \\ \frac{(2-k)(1-D_1)}{2(k-1)} + \frac{2k-3}{2(k-1)} & \left(0 < D_1 \le \frac{k-1}{k}\right) \end{cases} \\ D_3 = \begin{cases} D_1 & \left(\frac{k-1}{k} < D_1 \le 1\right) \\ \frac{(2-k)(1-D_1)}{2(k-1)} + \frac{2k-3}{2(k-1)} & \left(0 < D_1 \le \frac{k-1}{k}\right). \end{cases} \end{cases} \tag{25}$$

In addition, based on (3) and (25), phase-shift ratio D_1 can be expressed with the desired and unified transferred power as

$$D_1 = \begin{cases} 1-\sqrt{\frac{p^*}{k-1}} & \left(0 \le p < \frac{k-1}{k^2}\right) \\ (k-1)\sqrt{\frac{1-2p^*}{k^2-2k+2}} & \left(\frac{k-1}{k^2} \le p \le \frac{1}{2}\right). \end{cases} \tag{26}$$

Then, combining (3), (5), and (25), the unified peak current of the SPS and UPS control schemes can be expressed by the corresponding unified transferred power as follows:

$$\begin{cases} i_p = \begin{cases} 2\sqrt{(k-1)p^*} & \left(0 \le p < \frac{k-1}{k^2}\right) \\ k-\sqrt{(1-2p^*)(k^2-2k+2)} & \left(\frac{k-1}{k^2} \le p \le \frac{1}{2}\right) \end{cases} \\ i_{ps} = k-\sqrt{1-2p^*} \quad \left(0 \le p \le \frac{1}{2}\right). \end{cases} \tag{27}$$

According to (27), the ratio d of the unified peak current i_{ps} (SPS control) to i_p (UPS control) can be obtained as

$$d = \frac{i_{ps}}{i_p} = \begin{cases} \frac{k-\sqrt{1-2p_s^*}}{2\sqrt{(k-1)p^*}} & \left(0 \le p^* < \frac{k-1}{k^2}\right) \\ \frac{k-\sqrt{1-2p_s^*}}{k-\sqrt{(1-2p^*)(k^2-2k+2)}} & \left(\frac{k-1}{k^2} \le p^* \le \frac{1}{2}\right). \end{cases} \tag{28}$$

The curves of the specific value d with respect to p and k are shown in Fig. 5.

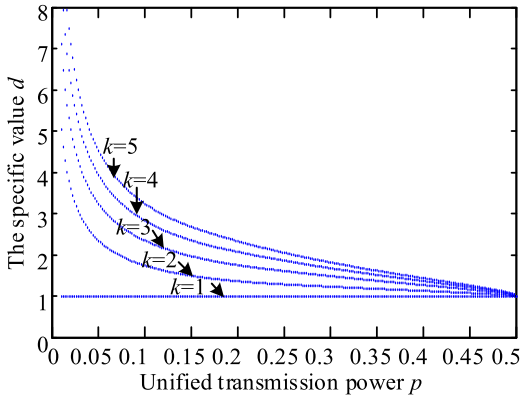


Fig. 5. Curves of the specific value d with respect to p and k.

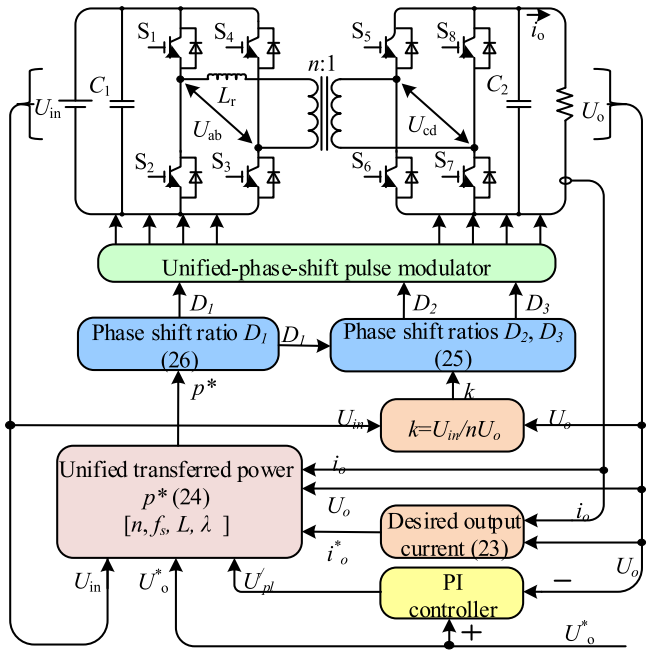


Fig. 6. Control block diagram of the proposed UPS-PB scheme.

Fig. 5 shows the curves of the ratio d of the unified peak current of SPS control to UPS control with respect to the unified transferred power p and the voltage conversion ratio k. It is clear that UPS control can significantly reduce peak current, especially when the unified transferred power p is far from 0.5 and the voltage conversion ratio k is much larger than 1. Moreover, when the voltage conversion ratio $k = 1$, the UPS control is equivalent to the SPS control, and can reach minimum peak current.

Combining (23)–(26), the UPS-PB scheme can be realized, and the control block diagram of the UPS-PB scheme is shown as Fig. 6. As the above analysis, various relationships among these phase-shift ratios D_1, D_2, and D_3 can result in different peak currents. Thus, according to (25), the peak current minimization for the DAB dc–dc converter can be achieved. On the other hand, when the desired unified transferred power can be directly gotten from (24), and the excellent dynamic performances of this converter can be realized, and which will not mainly depend on

the PI controller. Therefore, the UPS-PB scheme can improve both the efficiency and dynamic response.

According to Fig. 6, in order to implement the UPS-PB scheme, the input voltage U_{in}, output voltage U_{o}, and the load current i_o in each switching cycle should be acquired. According to (23), the desired load current i_o^* can be calculated with load current i_o and output voltage U_o, and then, the voltage ratio k can be expressed as $U_{\text{in}}/n/U_o$. The voltage $U_{pl}^{/}$ across the equivalent-loss resistor can be acquired from the PI controller to represent power loss. Then, based on (24), the unified transferred power p^* can be estimated by using input voltage U_{in}, output voltage U_{o}, the load current i_o, the desired load current i_o^*, and the voltage $U_{pl}^{/}$. According to the unified transferred power p^*, the phase-shift ratio D_1 is acquired from (26). Moreover, the phase-shift ratios D_2 and D_3 are expressed with phase-shift ratio D_1 and the voltage ratio k. Finally, the control signals are generated from the UPS pulse modulator.

B. Inductance Sensitivity Analysis of the Proposed UPS-PB Scheme

According to (24), inductance parameter is used to estimate the unified transferred power of the DAB dc–dc converter. Therefore, the inductance value mismatch may affect the performance of the UPS-PB scheme. The inductance parameter mismatch effect is analyzed in detail in this section. Based on the previous analysis, the relationships among D_1, D_2, and D_3 are still satisfied due to no inductance value in (25); there are no effect on the peak current minimization and the efficiency improvement of the DAB dc–dc converter. Thus, inductance mismatch only affects dynamic performance of this converter. According to (24), when the inductance is accurate and the desired output voltage is obtained, the desired unified transferred power p^* can be written as

$$p^* = \frac{4Lf_s(U_{pl}^{/} + U_o^*)}{nRU_{\text{in}}}. \tag{29}$$

According to (29), $U_{pl}^{/}$ can be expressed as

$$U_{pl}^{/} = \frac{nRU_{\text{in}}}{4f_sL}p^* - U_o^*. \tag{30}$$

The inductance mismatch ratio is defined as β, when the output voltage reaches its desired value, it is clear that p^* will be same as the unified transferred power with the accurate inductance. Thus, the new $U_{l\beta}^{/}$ can be written as

$$U_{l\beta}^{/} = \frac{nRU_{\text{in}}}{4\beta f_sL}p^* - U_o^*. \tag{31}$$

Combining (30) and (31), $U_{l\beta}^{/}$ can be expressed by $U_{pl}^{/}$ and U_o^* as

$$U_{l\beta}^{/} = \frac{U_{pl}^{/} + U_o^*}{\beta} - U_o^*. \tag{32}$$

According to (32), because $U_{l\beta}^{/}$ can compensate the inductance error, the desired output voltage can also be gained, which means a new PB model is established. Thus, when the input voltage or load resistance is changed, the desired phase-shift ratios D_1, D_2, and D_3 will be achieved quickly by using the new PB model, because of the linear relationships between p^* and U_{in} or R.

In addition, it is obvious that when the inductance value is accurate, $U_{pl}^{/}$ is close to 0. When the inductance value is not accurate, $U_{pl}^{/}$ is away from 0 for getting the desired output voltage, and the value $U_{pl}^{/}$ will be adjusted to compensate the error of phase-shift ratios, which will result in poor start-up performance of the DAB dc–dc converter. Similarly, when the desired output voltage steps up or down, there are two different conditions. According to (31), when β is larger than 1, $U_{pl}^{/}$ becomes negative to get the desired output voltage. Thus, the more negative compensation is required, the larger overshoot of the output voltage may appear, which will affect the dynamic performance of the converter. In contrary, when β is smaller than 1, $U_{pl}^{/}$ needs to be increased to obtain the desired output voltage. Thus, the more positive compensation is required, which will influence the dynamic performance of the DAB dc–dc converter.

Moreover, from (12), when the equivalent inductance of DAB dc–dc converters is not known, the accurate inductance can be estimated with the output power and the transferred power as

$$L = \frac{nU_{\text{in}}\sqrt{\eta}}{4i_of_s}p. \tag{33}$$

From (33), the accurate inductance can be easily estimated by measuring the input voltage, output voltage, input current, and the load current. In addition, from (12), the efficiency η can be shown as

$$\eta = \frac{U_oi_o}{U_{\text{in}}i_{\text{in}}}. \tag{34}$$

Combining (33) and (34), the inductance value can be estimated. Moreover, if the approximate efficiency of the DAB dc–dc converter is known, the inductance can also be obtained by using online estimation with the sampling input and output voltage and currents.

In conclusion, the inductance parameter mismatch has no effect on the performances of peak current optimal control and the dynamic performance when the input voltage or the load resistance is changed. Unfortunately, when the converter operates during start-up process, or the desired output voltage is changed, the dynamic performance will be affected. Because there is no effect on dynamic performance when the input voltage or the load resistance is changed, this paper takes no account of the inductance online estimation. Moreover, the next section will adopt a solution to improve the dynamic performance under start-up and the desired output voltage change conditions.

C. Zonal Control of the Output Voltage

In order to improve the dynamic performance under start-up and the desired output voltage fluctuation conditions, this paper adopts a zonal control of the output voltage by using the energy storage property of capacitor C_2 during the start-up process and the desired output voltage change. The boundary selection for each zone is described in this section.

When the output voltage is lower than the desired output voltage, the maximum transferred power can force the output voltage to reach the desired value quickly. According to (21) and ignoring $U_{pl}^{/}$, the maximum transferred power can be applied before capacitor C_2 voltage reaches the desired output voltage during a switching cycle as follows:

$$\frac{nU_{\text{in}}}{16f_sL}=\frac{U_o^*+U_{o\,\min}}{4R}+\frac{1}{2}f_sC_2(U_o^*-U_{o\,\min}). \tag{35}$$

According to (35), the lower limiting value of the output voltage can be obtained as

$$\begin{aligned}U_{o\,\min}&=\frac{8LRC_2f_s^2+4Lf_s}{8LRC_2f_s^2-4Lf_s}U_o^*-\frac{nR}{8LRC_2f_s^2-4Lf_s}U_{\text{in}}\\&\approx U_o^*-\frac{n}{8LC_2f_s^2}U_{\text{in}}.\end{aligned} \tag{36}$$

From (36), when the switching frequency is over 10 kHz, $U_{o\min}$ is always close to the desired output voltage U_o^*. Thus, in order to enlarge the control section of the UPS-PB scheme, $0.9\,U_o^*$ can be used as other lower limiting output voltage. Then, the lower limiting output voltage can be expressed as

$$U_{o\,\min}=\text{Min}\left[0.9U_o^*,U_o^*-\frac{n}{8LC_2f_s^2}U_{\text{in}}\right]. \tag{37}$$

Thus, when U_o is smaller than $U_{o\min}$, the maximum transferred power can be used to increase the output voltage quickly, where $D_1=D_3=1$ and $D_2=0$ under the UPS control.

When the output voltage is larger than the desired value, based on the energy storage characteristic of the supporting capacitor C_2, the energy storing in C_2 can be used as the only power source for the load, which forces the output voltage to reach the desired value quickly. Assuming the output voltage can reach the desired value within a switching cycle as follows:

$$\frac{1}{2}f_s\,C\left(U_{o\,\max}^2-U_o^{*^2}\right)=\frac{(U_{o\,\max}+U_o^*)^2}{4R}. \tag{38}$$

In (38), the upper limiting value of the output voltage can be obtained as

$$U_{o\,\max}=\frac{1+2CRf_s}{2CRf_s-1}U_o^*=U_o^*+\frac{2}{2CRf_s-1}U_o^*. \tag{39}$$

According to (39), when the switching frequency is over 10 kHz, $U_{o\max}$ is always close to the desired value U_o^*. In addition, when $2CRf_s$ is smaller than 1, $U_{o\max}$ will be meaningless. Thus, in order to enlarge the control section of the UPS-PB scheme, $1.1\,U_o^*$ can be used as the upper limiting voltage. Then, the upper limitation value is expressed as

$$U_{o\,\max}=\text{Max}[1.1U_o^*,U_o^*+\frac{2}{2CRf_s-1}U_o^*]. \tag{40}$$

From (40), when U_o is higher than $U_{o\max}$, the output power can be only offered by capacitor C_2, and the output voltage can drop fast, where $D_1=0$ and $D_2=D_3=0.5$ under the UPS control.

According to (37) and (40), the schematic diagram of zonal voltage control can be summarized in Fig. 7.

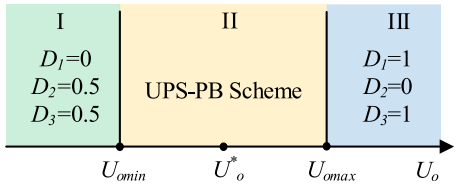


Fig. 7. Schematic diagram of the zonal voltage control.

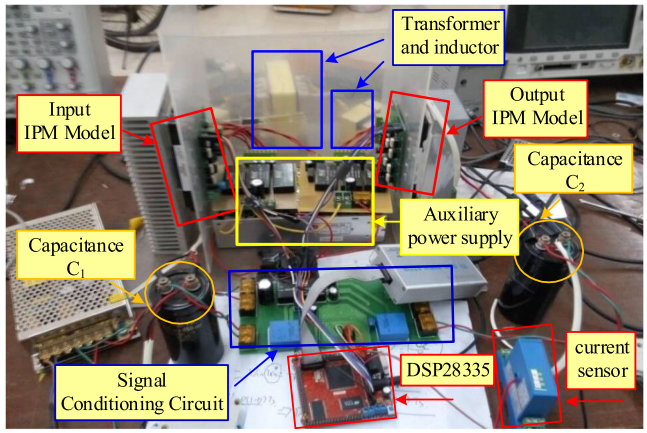


Fig. 8. Photo of the experimental hardware prototype.

TABLE I
ELECTRICAL PARAMETERS OF THE DAB DC–DC CONVERTER EXPERIMENTAL PROTOTYPE

Parameters	Values
The transformer turn ratio	$n=1$ (25:25)
The auxiliary inductor	$L_r=200.056\ \mu$H
The excitation inductance	$L_m=9.46274$ mH
The leakage inductance	$L_l=1.91075\ \mu$H
Switching frequency	$f_s=10$ kHz
The input-side capacitor	$C_1=2.2$ mF
The output-side capacitor	$C_2=2.2$ mF
The resistive load	$R=15, 20\ \Omega$
The switches devices	PM50B4LA060

V. EXPERIMENTAL ANALYSIS OF UPS-PB SCHEME

In order to verify the effectiveness of the proposed method in this paper, an experimental hardware prototype of DAB dc–dc converter is developed with TMS320F28335 DSP controller of Texas Instruments. The photo of experimental prototype is shown in Fig. 8. And electrical parameters of the adopted DAB dc–dc converter are listed in Table I.

A. Accuracy Verification of PB Model

Because SPS control and UPS control can achieve the same unified transmission power p, the SPS control can be used to verify the accuracy of the PB model. When the experimental parameters are set as $D=0.3$, $R=15\ \Omega$, and $U_{\text{in}}=70$ V, Fig. 9 shows the partial waveforms of U_{ab}, U_{cd}, and i_L, and the corresponding measured results of U_{in}, U_o, i_{in}, and i_o are shown in Table II.

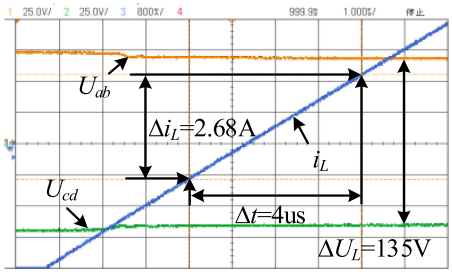


Fig. 9. Partial waveforms of U_{ab}, U_{cd}, and i_L.

TABLE II
MEASURED RESULTS OF U_{IN}, U_o, i_{IN}, AND i_o

Parameters	Values
U_{in}	70.8 V
U_o	54.3 V
i_{in}	2.971 A
i_o	3.479 A

TABLE III
MEASURED EFFICIENCY UNDER DIFFERENT CONDITIONS

Conditions	η
$D = 0.25, U_{\text{in}} = 60$ V, $R = 15\ \Omega$	0.879
$D = 0.25, U_{\text{in}} = 90$ V, $R = 15\ \Omega$	0.902
$D = 0.25, U_{\text{in}} = 60$ V, $R = 20\ \Omega$	0.890
$D = 0.30, U_{\text{in}} = 60$ V, $R = 15\ \Omega$	0.874
$D = 0.30, U_{\text{in}} = 90$ V, $R = 15\ \Omega$	0.900
$D = 0.30, U_{\text{in}} = 60$ V, $R = 20\ \Omega$	0.872
$D = 0.35, U_{\text{in}} = 60$ V, $R = 15\ \Omega$	0.871
$D = 0.35, U_{\text{in}} = 90$ V, $R = 15\ \Omega$	0.879
$D = 0.35, U_{\text{in}} = 60$ V, $R = 20\ \Omega$	0.878

According to Fig. 9, the equivalent inductance can be calculated as

$$L = \frac{\Delta t \Delta U_L}{\Delta i_L} = \frac{4\ \text{s} \times 10^{-6} \times 135\ \text{V}}{2.68\ \text{A}} = 201.5\ \mu\text{H}. \quad (41)$$

Combining (33) and Table II, the equivalent inductance can also be calculated as

$$L' = \frac{nU_{\text{in}}D(1-D)}{2i_o f_s}\sqrt{\frac{U_o i_o}{U_{\text{in}} i_{\text{in}}}} = 200.8\ \mu\text{H}. \quad (42)$$

Comparing (41) with (42), the inductor error between the measured inductance L and the estimated inductance L' can be shown as

$$L_{\text{error}} = \left|\frac{L'-L}{L}\right| = 3.5\%_0. \quad (43)$$

According to (43), the inductor error is very small, which can verify the high precision of the PB model. Moreover, when the experimental parameter is set as $D = 0.3$, Table III shows the measured efficiency η under various input voltages and load resistances.

Combining (20) and Table III, Fig. 10 shows experimental waveforms of the output voltages U_o, input voltage U_{in}, the predicted output voltage U_{o_p}, and load current i_o, with different

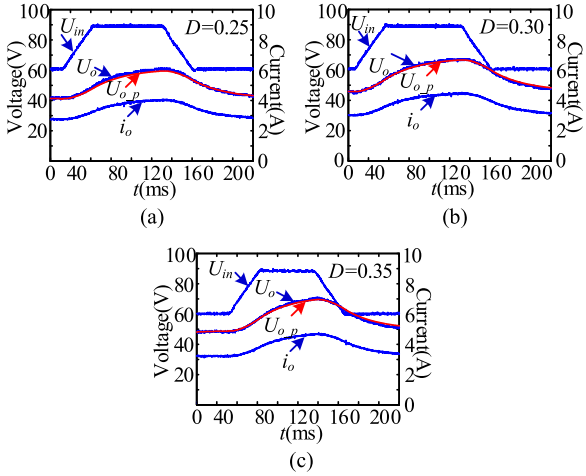


Fig. 10. Open-loop experimental results when the input voltage steps up and down. (a) $D = 0.25$. (b) $D = 0.30$. (c) $D = 0.35$.

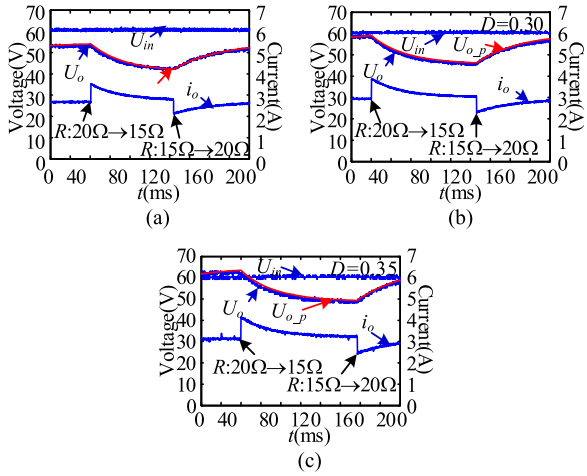


Fig. 11. Open-loop experimental results when the load resistance steps up and down. (a) $D = 0.25$. (b) $D = 0.30$. (c) $D = 0.35$.

phase-shift ratio D when the input voltage steps between 60 and 90 V, where U_o (blue line) is the measured value, and U_{o_p} (red line) is the iterative operation result by using (20). Similarly, Fig. 11 shows experimental waveforms under the step change of load resistance between 15 and 20 Ω with different phase-shift ratio D, where U_o (blue line) is the measured value and U_{o_p} (red line) has also matched the result from (20).

From Figs. 10 and 11, it is obvious that the actual output voltage under the step change of the input voltage and load resistance is very close to the estimated value by using the PB model, which can further verify the accuracy of the PB model. Thus, the proposed PB model in this paper is useful to analyze dynamic behaviors of the output voltage.

In addition, Fig. 12 shows experimental results when the initial value of the output voltage is mismatched that is used to test the iterative operation performance. From Fig. 12, it is obvious that the output voltage value U_{o_p1} has the indication of convergence even with the wrong initial output voltage. Thus, based on the PB model, the output voltage prediction by using (20) has a good astringency. Moreover, U_{o_p2} represents the

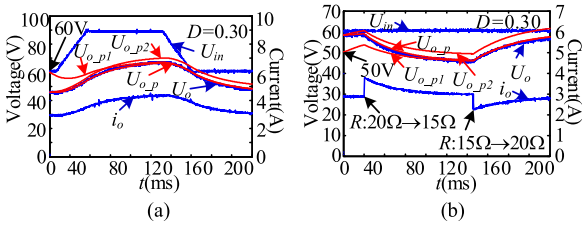


Fig. 12. Open-loop experimental results when the initial output voltage is mismatched or the power losses are ignored. (a) Input voltage steps between 60 and 90 V. (b) Load steps between 15 and 20 Ω.

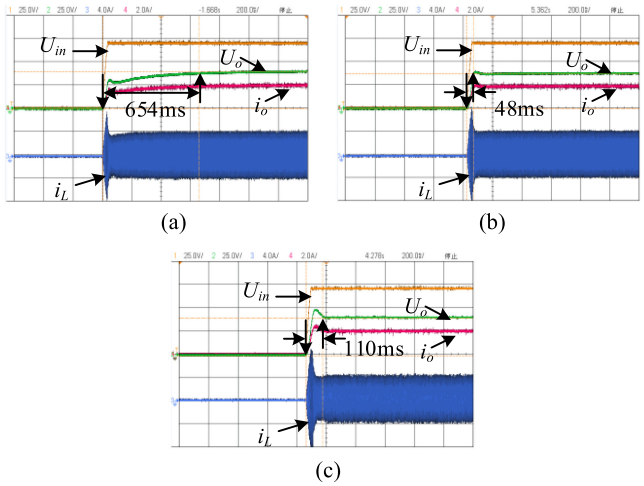


Fig. 13. Experimental results during the start-up process of the UPS-PB scheme. (a) $\beta = 0.5$. (b) $\beta = 1$. (c) $\beta = 1.5$. (U_{in} and U_o: 25 V/div; i_L: 4 A/div; i_o: 2 A/div; Time: 200 ms/div).

iterative result with ignoring power losses. Comparing U_{o_p} and U_{o_p2}, it is obvious that the iterative model containing the actual efficiency is more accurate. So, on the basis of the relationships among the input power, the transmission power, and the output power, the converter efficiency is relative to precision of the PB model, and this model is also simple.

B. Inductance Parameter Sensitivity Verifications of the UPS-PB Scheme

When the experimental parameters are set as $R = 20\,\Omega$, $U_{\text{in}} = 70$ V, and $U_o^* = 40$ V, Fig. 13 shows the transient experimental results of the DAB dc–dc converter during start-up process with different inductance mismatch ratio β. From Fig. 13(a)–(c), it is clear that the start-up times are 654 ($\beta = 0.5$), 48 ($\beta = 1$), and 110 ms ($\beta = 1.5$). During start-up process, it is obvious when $\beta = 1$, the converter can reach the better dynamic responses by using the UPS-PB scheme, and the inductance mismatch will affect dynamic performance during start-up process.

When the experimental parameters are set as $U_{\text{in}} = 70$ V and $U_o^* = 40$ V, Fig. 14 shows experimental results of the DAB dc–dc converter with step-change of the load resistance by using the UPS-PB scheme under different β, where the load resistance steps between 15 and 20 Ω. From Fig. 14, it is clear that the output voltage will be kept the same when the load resistance is changed no matter what β is adopted, which means that

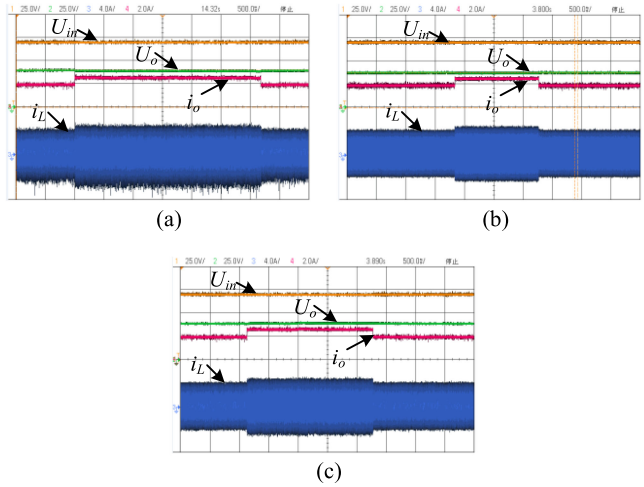


Fig. 14. Experimental results when the load steps between 15 and 20 Ω in the UPS-PB scheme. (a) $\beta = 0.5$. (b) $\beta = 1$. (c) $\beta = 1.5$ (U_{in} and U_o: 25 V/div; i_L: 4 A/div; i_o: 2 A/div; Time: 500 ms/div).

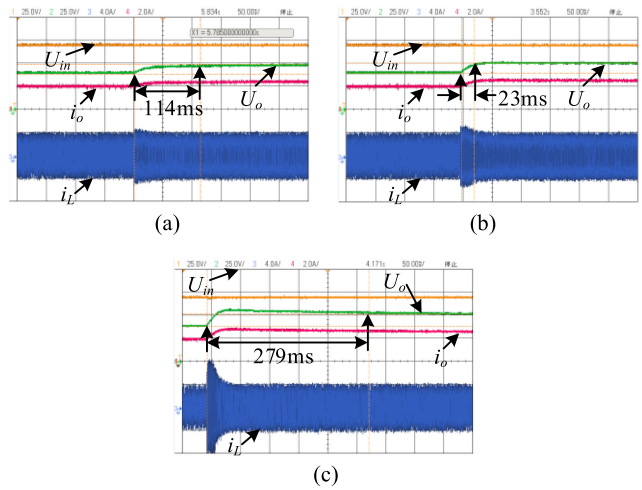


Fig. 15. Experimental results when the desired output voltage steps from 40 to 50 V. (a) $\beta = 0.5$. (b) $\beta = 1$. (c) $\beta = 1.5$ (U_{in} and U_o: 25 V/div; i_L: 4 A/div; i_o: 2 A/div; Time: 50 ms/div).

inductance mismatch has no effect on dynamic performance of the DAB dc–dc converter under the load power fluctuation.

When the experimental parameters are set as $R = 20\,\Omega$, $U_{\text{in}} = 70$ V, Fig. 15 shows the transient experimental results of the DAB dc–dc converter system under the desired output voltage step-change condition, where the desired output voltage U_o^* steps from 40 to 50 V. From Fig. 15(a)–(c), the settling times of the output voltage are 114, 23, and 279 ms when $\beta = 0.5$, 1, and 1.5, respectively. When the desired output voltage is changed, it is obvious when $\beta = 1$, the converter can achieve superior dynamic responses by using the UPS-PB scheme, and the inductance mismatch has effect on dynamic performance of this converter during step-change of the desired output voltage.

C. Experimental Comparison of Peak Current and Efficiency

When the experimental parameters are set as $R = 15\,\Omega$, and $U_o^* = 40$ V, Fig. 16(a) and (b) shows the experimental curves of

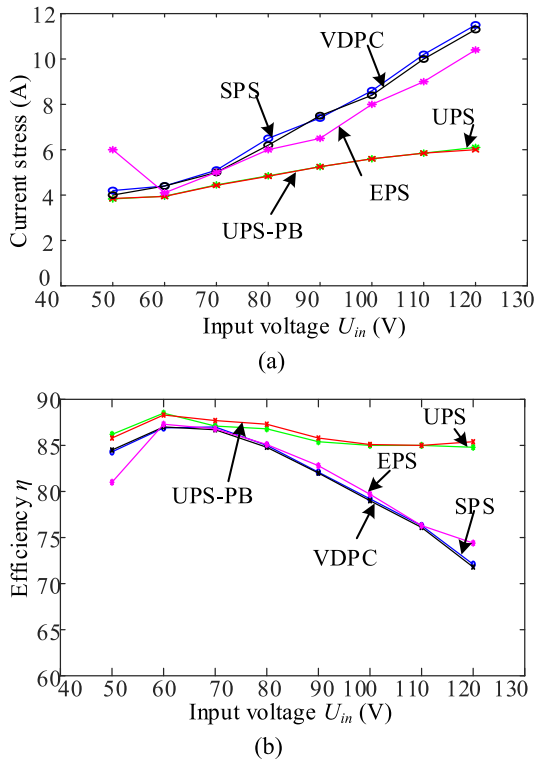


Fig. 16. Experimental curves of peak current and efficiency with respect to the input voltage U_{in} in five schemes. (a) Peak current. (b) Efficiency.

peak current and efficiency with respect to the input voltage U_{in} in five schemes, respectively. It can be noticed from Fig. 16(a) that UPS control and UPS-PB scheme have the similar results, which can gain lower peak current than SPS and EPS control. In addition, from Fig. 16(b), compared to SPS and EPS controls, UPS and UPS-PB schemes can also achieve higher efficiency, especially in high input voltage condition. The EPS control has a little better performance than the SPS control in high input voltage. But when the input voltage is very close to the output voltage, the EPS control has higher peak current and lower efficiency than SPS control. Thus, it can be summarized that the UPS control and the UPS-PB scheme can achieve the best peak current suppression and highest efficiency in high input voltage condition, compared with SPS and EPS control.

D. Experimental Comparison of Dynamic Response

In this part, in order to test the performance of the zonal control of output voltage, the UPS-PB scheme adds this zonal control to compare with SPS, virtual direct power control (VDPC), EPS, and UPS schemes. When the experimental parameters are set as $R = 15\,\Omega$, $U_{\text{in}} = 60$ V, and $U_o^* = 40$ V, Fig. 17(a)–(e) shows experimental results of the input voltage, the inductor current and the output voltages during start-up process for these five schemes. It is clear from Fig. 17 that the start-up time is 262, 150, 250, 241, and 54 ms in the SPS, VDPC, EPS, UPS, and UPS-PB schemes, respectively. Thus, the UPS-PB control has fastest dynamic response, and compared with other five methods, and VDPC scheme have better dynamic performance. Moreover, in the VDPC and UPS-PB scheme, there is no overshoot in the output voltage during start-up process.

When experimental parameters are set as $R = 20\,\Omega$ and $U_o^* = 40$ V, Fig. 18 shows the transient experimental results of the DAB dc–dc converter with the input voltage step-change, where the input voltage U_{in} steps down from 80 to 70 V. From Fig. 18, SPS [see Fig. 18(a)], EPS [see Fig. 18(c)], and UPS [see Fig. 18(d)] controls take a long settling time (over 100 ms) in the input voltage step-down condition for the output voltage to reach the desired value. Furthermore, under VDPC [see Fig. 18(b)] and UPS-PB [see Fig. 18(e)] schemes, the output voltage is almost unchanged during the input voltage step-change. Thus, VDPC and UPS-PB schemes can keep the output voltage constant, and achieve excellent dynamic behaviors when the input voltage is fluctuated.

When the experimental parameters are set as $U_{\text{in}} = 80$ V and $U_o^* = 40$ V, Fig. 19 shows the experimental results of the adopted DAB dc–dc converter with step-change of the load resistance. From Fig. 19, the transient responses under SPS, EPS, and UPS controls of the output voltage are very slow [see Fig. 19(a), (c), and (d)], with a long settling time (over 90 ms) in the load step-up condition, but EPS and UPS controls can achieve better dynamic performance. Moreover, the output voltage under VDPC [see Fig. 19(b)] and UPS-PB schemes [see Fig. 19(e)] can almost keep the same when the load steps up, which can significantly improve dynamic performances of the DAB dc–dc converter.

When the experimental parameters are set as $R = 15\,\Omega, U_{\text{in}} = 60$ V, Figs. 20 and 21 show the transient experimental results of the DAB dc–dc converter system under the desired output voltage step change condition, where the desired output voltage U_o^* steps from 50 to 40 V in Fig. 20, and conversely in Fig. 21. In the SPS control, when the desired output voltage U_o^* steps down or up, the transient response of the output voltage is slow [see Figs. 20(a) and 21(a)] with the settling time over 100 ms. In the VDPC scheme, when the desired output voltage U_o^* steps down or up, the transient response of the output voltage is fast [see Figs. 20(b) and 21(b)] with the settling time between 50 and 100 ms. In the EPS control, when the desired output voltage U_o^* steps down or up, the transient response of the output voltage is slow [see Figs. 20(c) and 21(c)] with the settling time over 100 ms. In the UPS control [see Figs. 20(b) and 21(b)], the settling times are close to 100 ms. Obviously, the UPS-PB scheme [see Figs. 20(c) and 21(c)] can achieve fast response while the setting time is 26 and 7 ms, respectively. Thus, even if the desired output voltage steps up or down, the proposed UPS-PB scheme can realize the shortest settling time, compared with the SPS, VDPC, and UPS methods, and VDPC scheme have better dynamic responses than other two controls.

According to Figs. 16–21, an experimental performance comparison of SPS control, VDPC, EPS control, UPS control, and UPS-PB scheme can be concluded in Table IV. From Table IV, it is easy to find that the proposed UPS-PB scheme with zonal control of the output voltage can achieve the best dynamic performance among these five schemes, and the proposed scheme can also reduce peak current and boost efficiency of DAB dc–dc converters.

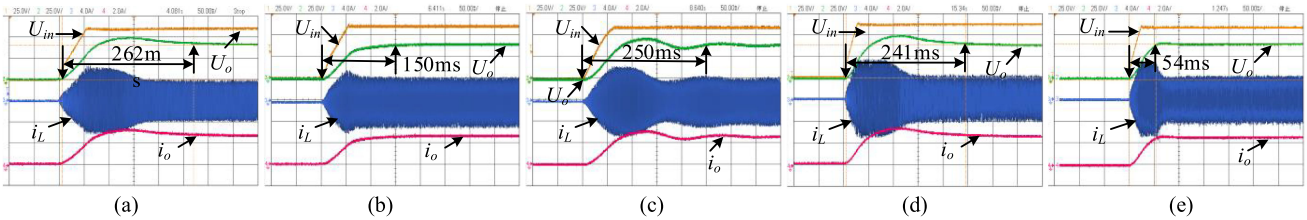


Fig. 17. Experimental results of voltages and currents during the start-up process. (a) SPS control. (b) VDPC scheme. (c) EPS control. (d) UPS control. (e) UPS-PB scheme. (U_{in} and U_o : 25 V/div; i_L : 4 A/div; i_o : 2 A/div; Time: 50 ms/div).

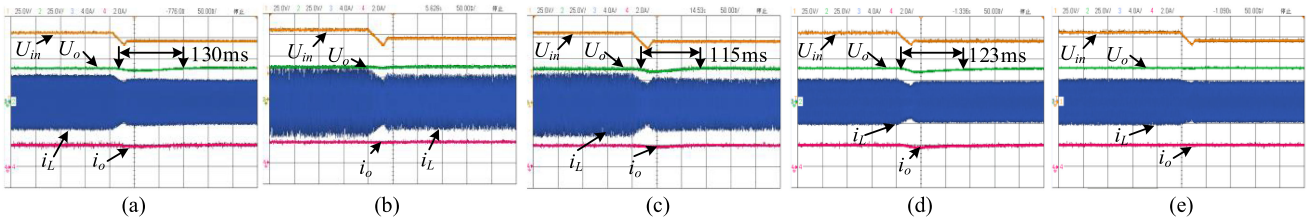


Fig. 18. Experimental results of voltages and currents when the input voltage steps down from 80 to 70 V. (a) SPS control. (b) VDPC scheme. (c) EPS control. (d) UPS control. (e) UPS-PB scheme. (U_{in} and U_o : 25 V/div; i_L : 4 A/div; i_o : 2 A/div; Time: 50 ms/div).

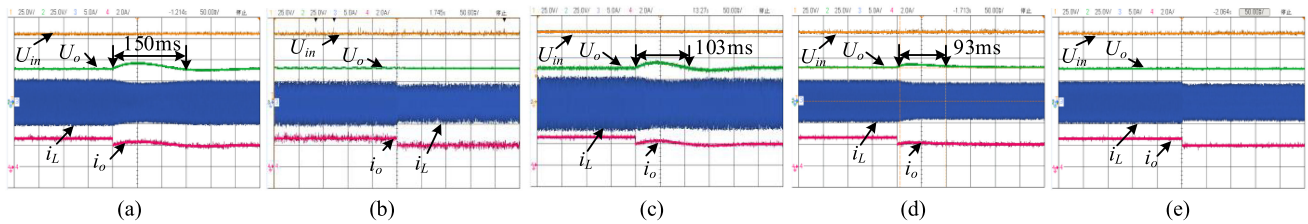


Fig. 19. Experimental results when load steps up from 15 to 20 Ω. (a) SPS control. (b) VDPC scheme. (c) EPS control. (d) UPS control. (e) UPS-PB scheme. (U_{in} and U_o : 25 V/div; i_L : 5 A/div; i_o : 2 A/div; Time: 50 ms/div).

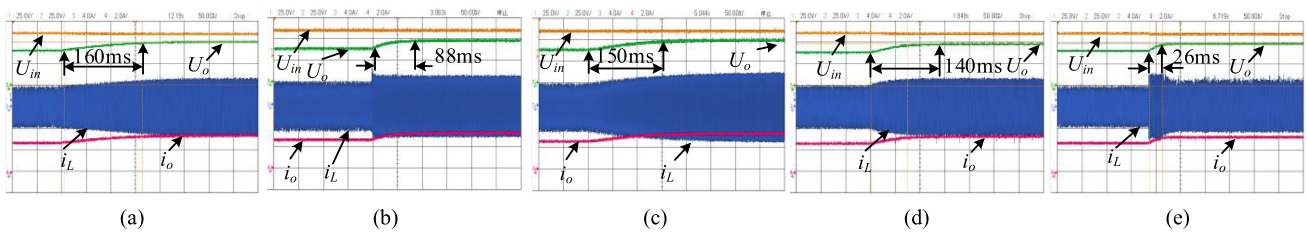


Fig. 20. Experimental results when the desired output voltage steps up from 40 to 50 V. (a) SPS control. (b) VDPC scheme. (c) EPS control. (d) UPS control. (e) UPS-PB scheme. (U_{in} and U_o : 25 V/div; i_L : 4 A/div; i_o : 2 A/div; Time: 50 ms/div).

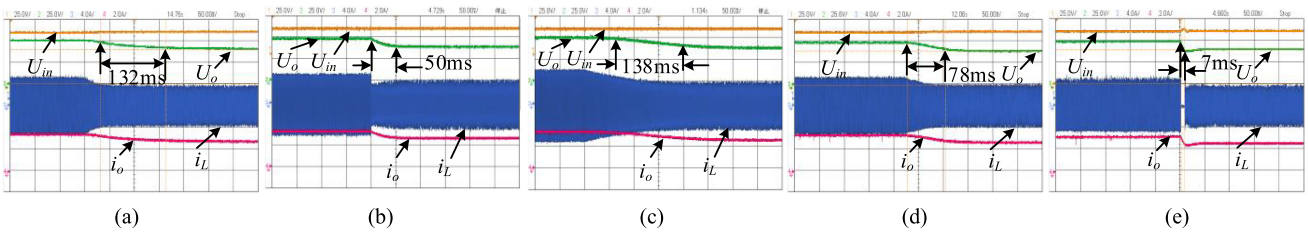
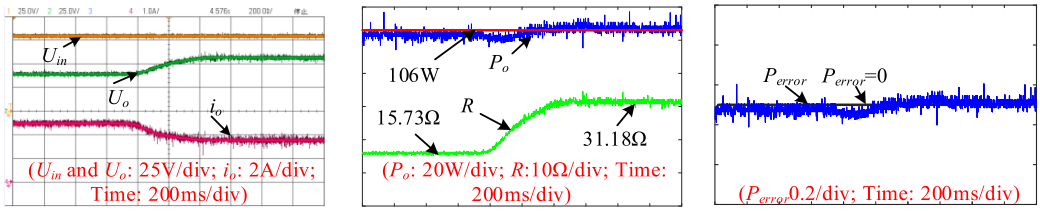


Fig. 21. Experimental results when the desired output voltage steps down from 50 to 40 V. (a) SPS control. (b) VDPC scheme. (c) EPS control. (d) UPS control. (e) UPS-PB scheme. (U_{in} and U_o : 25 V/div; i_L : 4 A/div; i_o : 2 A/div; Time: 50 ms/div).

TABLE IV
EXPERIMENTAL PERFORMANCE COMPARISON OF FIVE CONTROL SCHEMES

Control Schemes	Start-up	Input voltage variations	Load disturbance	Desired output voltage variations	Peak current	Efficiency
SPS control	Slow	slow	slow	slow	large	low
VDPC scheme	Faster	faster	faster	faster	large	low
EPS control ($D_1 = 0.1$)	Slow	slow	fast	slow	large	low
UPS control	Fast	slow	fast	fast	small	high
UPS-PB scheme	Fastest	faster	faster	fastest	small	high

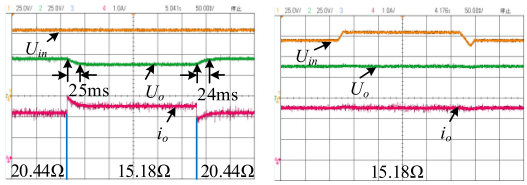


(a) (b) (c)

Fig. 22. Experimental results when the load resistor changes from 15.73 to 31.18 Ω. (a) Waveforms from oscilloscope. (b) Corresponding output power and load resistor. (c) Corresponding power error.

TABLE V
STEADY VALUES OF Uo, io, Po, AND P_{ERROR}

R (Ω)	U_o (V)	i_o (A)	P_o (W)	P_{error}
15.18	39.7	2.615	103.82	−0.021
15.73	40.7	2.587	105.29	−0.007
20.44	46.4	2.270	105.33	−0.006
31.18	58.0	1.860	107.88	0.018



(a) (b)

Fig. 23. Experimental results when the load resistor and the input voltage steps up or down. (a) Load resistor steps up and down. (b) Input voltage steps up and down.

E. Application of the Proposed Method for the Constant Power Load

The basic goal of the proposed UPS-PB method is to reach the desired output voltage, not the desired power transmission, and the DAB dc–dc converter can offer a stable dc voltage source for next converter stage. In order to study the performances for constant power load, the variation of control model should be expressed as

$$P^* = \frac{U_o^{*2}}{R}. \tag{44}$$

According to (44), the desired output voltage is expressed as

$$U_o^* = \sqrt{RP^*} = \sqrt{\frac{U_o P^*}{I_o}}. \tag{45}$$

According to (45), when the load is changed and the output power is stable, the constant power transmission control is equivalent to a changing desired output voltage control. In order to study the UPS-PB scheme for constant power load clearly, the power error between the desired output power P^* and the measured output power P_o can be expressed as

$$P_{\text{error}} = \frac{P_o - P^*}{P^*}. \tag{46}$$

When the desired output power is equivalent to 106 W, Table V presents the steady values of output voltage U_o and load current i_o measured by FLUKE 15B+ under different load resistors R and the corresponding output power and P_o and power error P_{error}.

According to Table V, under different load resistor from 15 to 31 Ω, the desired output power can be obtained, and the power error is less than 3%. Fig. 22 shows the experimental results when the load resistor changes from 15.73 to 31.18 Ω slowly. According to Fig. 22(b), the output power is close to the desired output power all the time, and according to Fig. 22(c), it is clear that the desired output power can be obtained when the load resistor is changed, and the power error is less than 10% (containing noises) during this changing process.

Moreover, Fig. 23 shows the experimental results when the load resistor or the input volateg steps up and down quickly. Accoding to Fig. 23(a), when the load resistor step changes, the desired output power can be obtained again suddenly, and the settling times are close to 25 ms. In addition, according to Fig. 23(b), the output power can be kept stable when the input voltage steps up or down. So, the variant of UPS-PB scheme can be used in constant power load applications, and the excellent dynamic performances can also be achieved.

VI. CONCLUSION

This paper proposes a hybrid UPS-PB control of DAB dc–dc converters for improvement of both the converter operation efficiency and dynamic response. Specifically, the UPS control can

significantly improve the efficiency of the adopted converters, and the PB control scheme based on the developed PB model can effectively enhance the output voltage control dynamics under input voltage fluctuations and load changes. With experimental verification and comparison of other four existing methods, the conducted studies in this work can lead to the following conclusions.

1) Based on the PB model, the accurate inductance value of the DAB dc–dc converter can be estimated and its error is less than 5% in the adopted test platform.
2) The PB model presents high accuracy to analyze the dynamic behaviors of the DAB dc–dc converter under the input voltage or the load variations. Moreover, the output voltage will converge even with the wrong initial values.
3) Under the UPS-PB scheme, the inductance parameter mismatch has only effect on dynamic performances during the start-up process and the large step-change of the desired output voltage.
4) Compared with SPS control, the UPS control and UPS-PB scheme can both improve efficiency of DAB dc–dc converters, especially it is obvious in high input voltage condition.
5) Under the input voltage fluctuation or load disturbance conditions, the proposed UPS-PB scheme can achieve excellent dynamic behavior.
6) In the start-up process or under a large step-change of the desired output voltage, the proposed UPS-PB scheme with zonal voltage control can significantly improve dynamic response, comparing with the SPS control and UPS control

In addition, the variant type of UPS-PB scheme can be used in constant power load applications, and the excellent dynamic performances can be still kept.

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