Surface-Potential-Based Silicon Carbide Power MOSFET Model for Circuit Simulation

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***Abstract*—Transistor models have been playing a key role in designing efficient power converters. As the operating frequency of the converters becomes higher, transistor models need to represent physical device behavior accurately. This paper proposes a comprehensive surface-potential-based model of silicon carbide (SiC) power MOSFETs that realizes accurate circuit simulations. Whereas conventional simulation models are based on empirical formulas, the proposed model is constructed in a surface-potential-based framework by considering the physical structure and behavior of vertical power SiC MOSFETs. The proposed model represents both *I–V* and *C–V* characteristics from weak inversion to the high-power region. In addition, the proposed model calculates the channel mobility degradation due to SiC/SiO_2 interface traps, which significantly affects the circuit performance. Through experiments using a commercial SiC power MOSFET, excellent agreements are obtained between measurement and simulation in *I–V* and *C–V* characteristics at various temperatures for wide power ranges up to 1 kW. The transient behavior of a double-pulse tester is also well reproduced within a timing error of 12.6 ns even under the high temperature.**

***Index Terms*—Compact modeling, device modeling, interface trap, SPICE simulation.**

I. Introduction

SILICON carbide (SiC) is one of the most promising materials to realize high-frequency switching power converters that operate very efficiently at high currents and voltages [1]. As the operating frequency of the power converters increases, the design optimization using circuit simulators becomes an increasingly important step. The simulation accuracy of power converters that utilize SiC power MOSFETs depends greatly on the accuracy of the simulation model of the power MOSFETs. Hence, a precise model that reflects the behavior of SiC power MOSFETs is important for accurate circuit simulations [2], [3].

In the analysis of power converters using SiC devices, Si-based empirical models have been applied [4], [5]. However, the fitting of those models to the characteristics of SiC power MOSFETs, such as dc currents and capacitances, is not always satisfactory. Moreover, the simulation models are difficult to consider physical phenomena, such as an interface trap, which is one of the critical issues in predicting the inconsistent circuit performance using SiC power MOSFETs [6]. Recently, surface-potential-based compact models, which can physically represent the device behavior, have been successfully applied for simulating lateral Si devices [7]–[11].

There are several surface-potential-based circuit simulation models of SiC MOSFETs proposed considering interface traps [12], [13]. However, in [12], the mobility degradation due to the trapped charges is not clearly described. It is, thus, difficult to accurately compute the drain current near the threshold voltage. Furthermore, the model description of the capacitance characteristics, more specifically the gate–drain capacitance, is not written in [13], whereas the gate–drain capacitance is one of the most important characteristics for reproducing the switching behaviors. Moreover, in the existing models, in addition to lacking the treatment of either mobility degradation or input capacitance, temperature dependence of the models is not thoroughly discussed, making simulation of power converters in various operational conditions inaccurate.

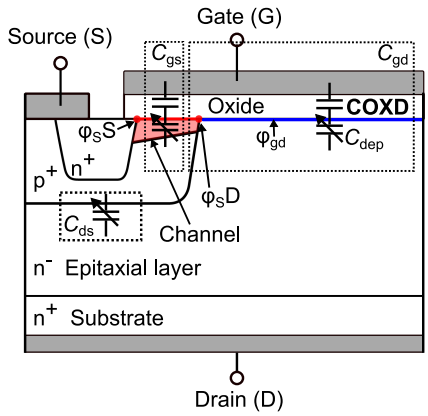

Fig. 1. Cross section of a SiC power MOSFET cell.

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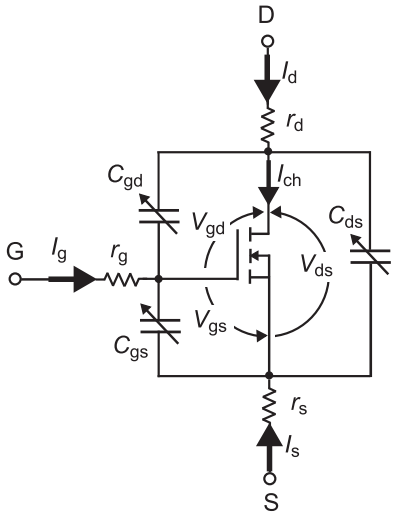

Fig. 2. Equivalent circuit of the SiC power MOSFET.

In this paper, we propose an accurate SiC power MOSFET model that is fully based on the surface potential calculation. Fig. 1 shows the vertical double-diffused MOSFET (VDMOSFET) structure, which is widely used in high-breakdown-voltage applications. In the proposed model, this structure is assumed to calculate *I–V* and *C–V* characteristics on the basis of the voltages at the surface of the MOSFET capacitor. The proposed SiC MOSFET model, for the first time, takes the influence of carrier trapping at the SiC/SiO_2 interface into account in the surface-potential-based framework. Through experiments using a commercial SiC device, the accuracy of the proposed model has been verified over a wide power range from milliwatts to kilowatts to comprehensively cover the typical operating regions of practical power converters.

The main contribution of this work is summarized as follows.

1) *An accurate SiC power MOSFET model based on surface potential considering the interface traps*: In the proposed model, from the surface potential at the MOS interface, the current and the capacitance characteristics are accurately computed while considering the structure of the VDMOSFET. In addition, assuming the trap density of state (DoS), the proposed model calculates the trapped electron charge due to the interface trap. The model then successfully captures the influence of the interface traps on the electron mobility from the trapped charge.
2) *I–V and C–V characteristics validation over a wide range of operating conditions*: Because the proposed model is a physical model, the *I–V* and *C–V* characteristics can be accurately simulated over a wide voltage and temperature range. Through the model validation using a commercial SiC power MOSFET, the fitting of the modeled *I–V* characteristics has been confirmed in the range of 0.02 W–1 kW measured by a dedicated short-pulse curve tracer, which involves a negligible self-heating effect [14].

The remainder of this paper is organized as follows. Section II describes the current and capacitance model equations on the basis of the surface potential considering the interface trap charges. In Section III, we present the validation of the proposed model with measured data on *I–V*, *C–V*, and transient characteristics using a commercial SiC power MOSFET. Finally, we will conclude this paper in Section IV.

TABLE I
LIST OF SYMBOLS FOR THE PROPOSED SiC POWER MOSFET MODEL

Symbol	Description
k	Boltzmann's constant [J/K]
q	Elementary charge [C]
T	Absolute temperature [K]
T_0	Reference temperature [K]
$\varepsilon_{\rm SiC}$	Permittivity of SiC [F/m]
$\varepsilon_{\rm ox}$	Permittivity of gate oxide [F/m]
L	Channel length [m]
W	Channel width [m]
M	Number of MOSFET cells [-]
$\mu_{\rm eff}$	Effective channel mobility [$\rm cm^2/Vs$]
$\phi_{\rm F}$	Fermi level [V]
$\phi_{\rm f}$	Quasi-Fermi level [V]
$\phi_{\rm t}$	Thermal voltage (kT/q) [V]
$\phi_{\rm s}$	Surface potential [V]
$\phi_{\rm sS}$	Surface potential at the source side [V]
$\phi_{\rm sD}$	Surface potential at the drain side [V]
$\phi_{\rm gd}$	Surface potential of the drain depletion layer under the gate [V]
$V_{\rm ox}$	Electric potential at the gate oxide [V]
$I_{\rm ch}$	Current through MOSFET channel [A]
$I_{\rm d}$	Drain current [A]
$I_{\rm g}$	Gate current [A]
$I_{\rm s}$	Source current [A]
$V_{\rm gs}$	Effective gate–source voltage [V]
$V_{\rm ds}$	Effective drain–source voltage [V]
$V_{\rm gd}$	Effective gate–drain voltage [V]
$C_{\rm ox}$	Oxide capacitance per unit area [$\rm F/cm^2$]
$C_{\rm gs}$	Gate–source capacitance [F]
$C_{\rm ds}$	Drain–source capacitance [F]
$C_{\rm gd}$	Gate–drain capacitance [F]
$C_{\rm dep}$	Gate–drain junction capacitance [F]
$Q_{\rm s}$	Total charge density at the MOS interface [$\rm C/cm^2$]
$Q_{\rm gs}$	Charge stored in $C_{\rm gs}$ [C]
$Q_{\rm ds}$	Charge stored in $C_{\rm ds}$ [C]
$Q_{\rm gd}$	Charge stored in $C_{\rm gd}$ [C]
E	Trapped energy [eV]
$E_{\rm F}$	Fermi energy [eV]
$E_{\rm C}$	Bottom of the conduction band [eV]
$N_{\rm S}$	Electron density per unit area at the surface [$\rm cm^{-3}$]
$N_{\rm T}$	Trapped electron density per unit area [$\rm cm^{-3}$]

II. SIMULATION MODEL OF A SiC POWER MOSFET

Fig. 2 shows an equivalent circuit of the proposed simulation model. The model is characterized by the device current through the MOSFET channel, which is denoted as $I_{\rm ch}$ and three terminal capacitances: the capacitance $C_{\rm gs}$ between the gate and the source, the capacitance $C_{\rm ds}$ between the drain and the source, and the capacitance $C_{\rm gd}$ between the gate and the drain. The mobile charge due to the capacitive coupling can be calculated by obtaining the surface potential at the channel, as shown in Fig. 1. The channel current $I_{\rm ch}$ and the MOS capacitance $C_{\rm gd}$ are then derived from the mobile charge. In actual devices, the flat-band voltage is affected by the interface trap. Hence, in the proposed model, the surface potential is computed by considering the shift in the flat-band voltage. In addition, we have

TABLE II
MODEL PARAMETERS (*I–V* CHARACTERISTICS)

Parameter	Description
TOX	Oxide thickness [m]
VFBC	Flat-band voltage of channel region [V]
NA	Acceptor concentration [cm^{-3}]
K	Current gain factor [cm^2/V]
MU	Electron mobility in the bulk semiconductor [cm^2/V]
RG	Parasitic resistance at the gate side [Ω]
RS	Parasitic resistance at the source side [Ω]
RD	Parasitic resistance at the drain side [Ω]
LAMBDA	Channel length modulation [1/V]
THETA	Channel mobility degradation [1/V]
DELTA	Smoothing parameter for gradual transition between linear and saturation regions [-]
DMID	Midgap interface trap DoSs [$\mathrm{cm}^2{\cdot}\mathrm{eV}^{-1}$]
DC	Band-edge interface trap DoSs [$\mathrm{cm}^2{\cdot}\mathrm{eV}^{-1}$]
SIGMA	Band-tail energy parameter [meV]
GAMMAC	Coefficient for Coulomb scattering [$\mathrm{eV}^{-1}\cdot\mathrm{cm}^{-2}$]
NC	Empirical parameter for μ_{C} [$\mathrm{Q/cm}^{-3}$]
ZETAC	Empirical parameter for μ_{C} [-]

TABLE III
MODEL PARAMETERS (*C–V* CHARACTERISTICS)

Parameter	Description
CGSO	Gate–source capacitance (constant) [F]
ADS	Drain–source overlap area [cm^2]
ND	Donor concentration [cm^{-3}]
VBI	Built-in potential of p-n junction [V]
COXD	Gate–drain oxide capacitance [F]
AGD	Gate–drain overlap area [cm^2]
VFBD	Gate–drain flat-band voltage [V]

implemented mobility degradation due to the trapping of the electron charges [15].

Tables I–III provide the nomenclature for the symbols and basic model parameters used in our proposed model. In this paper, the model parameters are typed in boldface, as shown in Tables II and III. In the proposed model, the constants $\mathbf{RG}$, $\mathbf{RD}$, and $\mathbf{RS}$ represent the gate, drain, and source parasitic resistances, respectively. In the rest of this paper, the drain and source voltages in the model calculation, V_{ds} and V_{gs}, are the effective voltages considering the voltage drop caused by the parasitic resistances shown in Fig. 2.

A. Surface Potential

In the proposed model, the surface potential of a channel formed in the semiconductor region is computed. As shown in Fig. 1, the VDMOSFET structurally has two types of MOS interfaces: one is the n-type MOS structure above the p^+ region, i.e., (metal)-(gate oxide)-(p^+ region), and the other is the p-type structure formed above the n^- epitaxial layer, i.e., (metal)-(gate oxide)-(n^- epitaxial layer). The surface potential of the MOS structures is calculated to derive I_{ch} and C_{gd} characteristics. In this subsection, we discuss the surface potential ϕ_{s} of the channel formed in the n-type MOS structure. Although not widely available yet, the surface potential equation of the p-type MOS structure is represented similarly by negating the polarities of the variables.

TABLE IV
PHYSICAL CONSTANTS

Parameter	Value
k [J/K]	1.38×10^{-23}
q [C]	1.60×10^{-19}
$\phi_{\mathrm{t}}(=kT/q)$ [mV]	0.026
$\varepsilon_{\mathrm{SiC}}$ [F/m]	$9.7\times8.85\times10^{-12}$
$\varepsilon_{\mathrm{ox}}$ [F/m]	$3.9\times8.85\times10^{-12}$

In [3], [8], [9], and [16], the total charge density at the MOS interface, Q_{s}, is derived by (1) shown at the bottom of this page. In addition, using Gauss' law, Q_{s} can also be expressed as the product of C_{ox} and V_{ox}:

$$Q_{\mathrm{s}} = C_{\mathrm{ox}}V_{\mathrm{ox}} = C_{\mathrm{ox}}(V_{\mathrm{gs}} - V'_{\mathrm{fbc}} - \phi_{\mathrm{s}}) \tag{2}$$

where $C_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/\mathbf{TOX}$. Eliminating Q_{s} from (1) and (2), a nonlinear equation for ϕ_{s} is derived as (3) shown at the bottom of the next page.

In order to accurately model the behavior of SiC power MOSFETs, it is crucial to consider the interface states found in $\mathrm{SiC/SiO_2}$. In our model, the surface potential is modified by considering the interface-trapped charge. We focus on an acceptor-like trap only because we treat nMOS transistors in this study.

The DoS of the acceptor-like trap is described as a function of the trap energy E [17]

$$D_{\mathrm{it}}(E) = \mathbf{DMID} + \mathbf{DC}\cdot\exp\left(\frac{E-E_{\mathrm{c}}}{\mathbf{SIGMA}}\right) \tag{4}$$

where E_{c} is the bottom of the conduction band. As described later in Section II-B, in the proposed model, the model parameters related to the interface trap, i.e., **DMID** and **DC**, are modeled using linear functions of the temperature. By integrating (4) with respect to E, the number of acceptor traps n_{it} is obtained as shown in (5) shown at the bottom of the next page [18]. Because the interface trap shifts the flat-band voltage, the flat-band voltage considering the interface trap V'_{bfc}

$$Q_{\mathrm{s}} = \sqrt{2q\varepsilon_{\mathrm{SiC}}\cdot\mathbf{NA}}\sqrt{\phi_{\mathrm{t}}e^{-\phi_{\mathrm{s}}/\phi_{\mathrm{t}}} + \phi_{\mathrm{s}} - \phi_{\mathrm{t}} + e^{-(2\phi_{\mathrm{F}}+\phi_{\mathrm{f}})/\phi_{\mathrm{t}}}(\phi_{\mathrm{t}}e^{\phi_{\mathrm{s}}/\phi_{\mathrm{t}}} - \phi_{\mathrm{s}} - \phi_{\mathrm{t}})} \tag{1}$$

$$C_{\mathrm{ox}}(V_{\mathrm{gs}} - V'_{\mathrm{fbc}} - \phi_{\mathrm{s}}) = \sqrt{2q\varepsilon_{\mathrm{SiC}}\cdot\mathbf{NA}}\sqrt{\phi_{\mathrm{t}}e^{-\phi_{\mathrm{s}}/\phi_{\mathrm{t}}} + \phi_{\mathrm{s}} - \phi_{\mathrm{t}} + e^{-(2\phi_{\mathrm{F}}+\phi_{\mathrm{f}})/\phi_{\mathrm{t}}}(\phi_{\mathrm{t}}e^{\phi_{\mathrm{s}}/\phi_{\mathrm{t}}} - \phi_{\mathrm{s}} - \phi_{\mathrm{t}})} \tag{3}$$

TABLE V
MODEL PARAMETERS FOR *I–V* CHARACTERISTICS EVALUATION ($T = 298$ K)

I–V model parameter	Value
TOX [m]	5.00×10^{-8}
VFBC [V]	0.32
NA [cm^{-3}]	4.16×10^{16}
K [-]	2879
MU [cm^2/V· s]	42.45
RG [Ω]	4.50
RD [Ω]	0.0427
RS [Ω]	3.21×10^{-3}
LAMBDA [1/V]	0.00233
THETA [1/V]	1.29×10^{-17}
DMID [$cm^2 \cdot eV^{-1}$]	4.217×10^{11}
DC [$cm^2 \cdot eV^{-1}$]	1.302×10^{12}
SIGMA [meV]	0.543
GAMMAC [$eV^{-1} \cdot cm^{-2}$]	1.451×10^{10}
NC [Q/cm^{-3}]	2.388×10^{18}
ZETAC [-]	0.235

TABLE VI
MODEL PARAMETERS FOR *C–V* CHARACTERISTICS EVALUATION ($T = 298$ K)

C–V model parameter	Value
CGSO [F]	6.78×10^{-10}
ADS [cm^2]	0.0129
ND [cm^{-3}]	1.15×10^{16}
VBI [V]	2.02
COXD [F]	4.36×10^{-10}
AGD [cm^2]	0.0063
VFBD [V]	-0.100

is written as

$$V'_{\rm bfc} = \mathbf{VFBC} - \frac{n_{\rm it}(E)}{C_{\rm ox}}. \tag{6}$$

The proposed device model considers the flat-band voltage as a variable.

Finally, the charge of the inversion layer is calculated from $\phi_{\rm s}$. By integrating the charge from the drain to the source of the channel, a channel current $I_{\rm ch}$ is derived. In addition, the derivative of the surface potential gives the capacitance at the channel of the MOSFET. In [8], [11], and [16], the surface potential $\phi_{\rm s}$ is derived by solving the nonlinear equation shown in (3).

B. I–V Characteristic

The inverted charge of the channel is described as a function of the surface potential. Hence, the channel current $I_{\rm ch}$ can be computed by $\phi_{\rm sS}$ (derived by solving (3) at $\phi_{\rm f} = 0$) and $\phi_{\rm sD}$ (derived by solving (3) at $\phi_{\rm f} = V_{\rm ds}$) [8], [11] as

$$I_{\rm ch} = \mathbf{K} \cdot \mu_{\rm eff} \cdot I_{\rm DD} \tag{7}$$

$$\begin{aligned} I_{\rm DD} =& C_{\rm ox}(V_{\rm gs} - V'_{\rm fbc} + \phi_{\rm t})(\phi_{\rm sD} - \phi_{\rm sS}) - \frac{1}{2} C_{\rm ox}(\phi^2_{\rm sD} - \phi^2_{\rm sS}) \\ & - \frac{2}{3}\phi_{\rm t}\sqrt{2\varepsilon_{\rm SiC} kT \cdot \mathbf{NA}} \left\{ \left(\frac{\phi_{\rm sD}}{\phi_{\rm t}} - 1\right)^{\frac{3}{2}} - \left(\frac{\phi_{\rm sS}}{\phi_{\rm t}} - 1\right)^{\frac{3}{2}} \right\} \\ & + \phi_{\rm t}\sqrt{2\varepsilon_{\rm SiC} kT \cdot \mathbf{NA}} \left\{ \left(\frac{\phi_{\rm sD}}{\phi_{\rm t}} - 1\right)^{\frac{1}{2}} - \left(\frac{\phi_{\rm sS}}{\phi_{\rm t}} - 1\right)^{\frac{1}{2}} \right\} \end{aligned} \tag{8}$$

where $\mathbf{K} = M \cdot (W/L)$ is the current gain factor.

By considering channel length modulation and mobility degradation, (7) is rewritten as

$$\begin{aligned} I_{\rm ch} =& \frac{1}{1 + \mathbf{THETA} \cdot V_{\rm gs}}(1 + \mathbf{LAMBDA} \cdot V_{\rm ds}) \\ & \cdot \mathbf{K} \cdot \mu_{\rm eff} \cdot I_{\rm DD}. \end{aligned} \tag{9}$$

$V_{\rm ds_{mod}}$ is defined to replace $V_{\rm ds}$ in (9) to represent a smooth transition between the linear and saturation regions:

$$V_{\rm ds_{mod}} = \frac{V_{\rm ds}}{\left[1 + \left(\frac{V_{\rm ds}}{V_{\rm gs}}\right)^{\mathbf{DELTA}}\right]^{1/\mathbf{DELTA}}} \tag{10}$$

where $\mathbf{DELTA}$ is a parameter to compensate for mismatches of pinch-off voltages between measurement and simulation due to the gradual channel approximation [8], [9].

Electron mobility in the inversion layer in the SiC power MOSFET is strictly limited due to the interface trap. The mobility is expressed using Matthiessen's rule as

$$\frac{1}{\mu_{\rm eff}} = \frac{1}{\mathbf{MU}} + \frac{1}{\mu_{\rm PH}} + \frac{1}{\mu_{\rm C}} + \frac{1}{\mu_{\rm SR}} \tag{11}$$

TABLE VII
MODEL PARAMETERS FOR TEMPERATURE CHARACTERISTIC EVALUATION

Temperature model parameter	Values
VFBCS [-]	-1.162×10^{-2}
THETAS [-]	1.774×10^{-19}
MUS [-]	4.281×10^{-1}
RDS [V]	2.678×10^{-3}
DMIDS [-]	-2.239×10^{9}
DCS [-]	6.327×10^{10}
SIGMAS [-]	-7.994×10^{-4}
GAMMACS [-]	-8.211×10^{7}
NCS [-]	2.076×10^{16}
ZETACS [-]	-1.784×10^{-3}

$$\begin{aligned} n_{\rm it}(E_{\rm s}) &= q\int_{E_{\rm F}}^{E_{\rm s}} D_{\rm it}(E)dE \\ &= q\left[\mathbf{DMID}E_{\rm s} + \mathbf{SIGMA} \cdot \mathbf{DC} \cdot \exp\left(\frac{E_{\rm F} - E_{\rm C}}{\mathbf{SIGMA}}\right)\left(\exp\left(\frac{E_{\rm S}}{\mathbf{SIGMA}}\right) - 1\right)\right] \end{aligned} \tag{5}$$

where $\mu_{\rm PH}$ is the mobility due to surface phonon scattering, $\mu_{\rm C}$ is the mobility due to Coulomb scattering, and $\mu_{\rm SR}$ is the mobility due to surface roughness scattering. Among them, Coulomb scattering is the dominant factor of the mobility degradation when the interface trap is considered [19]. In our model, Coulomb scattering is modeled by a physics model [15] as

$$\mu_{\rm C} = \frac{\mathbf{GAMMAC}}{N_{\rm S}} T \left(1 + \frac{N_{\rm T}}{\mathbf{NC}}\right)^{\mathbf{ZETAC}} \tag{12}$$

where $\mathbf{NC}$ is the sum of all surface charge densities, i.e., of the fixed oxide charge and the trapped interface charge. $n_{\rm S}$ denotes the total charge density at the interface, and it can be calculated by (2). In this model, we treat $\mathbf{GAMMAC}$, $\mathbf{NC}$, and $\mathbf{ZETAC}$ as empirical parameters.

From (7), the terminal currents $I_{\rm d}$, $I_{\rm s}$, and $I_{\rm g}$ in the MOSFET are obtained by

$$I_{\rm d} = I_{\rm ch} + \frac{dQ_{\rm ds}}{dt} - \frac{dQ_{\rm gd}}{dt} \tag{13}$$

$$I_{\rm g} = \frac{dQ_{\rm gs}}{dt} + \frac{dQ_{\rm gd}}{dt} \tag{14}$$

$$I_{\rm s} = -I_{\rm ch} - \frac{dQ_{\rm ds}}{dt} - \frac{dQ_{\rm gs}}{dt}. \tag{15}$$

Here, $Q_{\rm gs}$, $Q_{\rm ds}$, and $Q_{\rm gd}$ are the charges stored in each terminal capacitance, as explained in Section II-C.

In power electronics, modeling of temperature effects during MOSFET operation is also crucial because the circuit performance can be greatly affected by the heat generated by the power MOSFET itself. It is well known that the current characteristic of MOSFETs is temperature dependent [1], [16]. In the proposed model, except the parameters that are known to be temperature independent, such as $\mathbf{NA}$, $\mathbf{TOX}$, and $\mathbf{DELTA}$, the model parameters are represented to change linearly with temperature as follows:

$$\mathbf{VFBC} = \mathbf{VFBC0} + \mathbf{VFBCS} \cdot (T - T_0) \tag{16}$$

$$\mathbf{THETA} = \mathbf{THETA0} + \mathbf{THETAS} \cdot (T - T_0) \tag{17}$$

$$\mathbf{MU} = \mathbf{MU0} + \mathbf{MUS} \cdot (T - T_0) \tag{18}$$

$$\mathbf{RD} = \mathbf{RD0} + \mathbf{RDS} \cdot (T - T_0). \tag{19}$$

Here, $\mathbf{VFBC0}$, $\mathbf{THETA0}$, $\mathbf{MU0}$, and $\mathbf{RD0}$ are the parameters at the reference temperature T_0. $\mathbf{VFBCS}$, $\mathbf{THETAS}$, $\mathbf{MUS}$, and $\mathbf{RDS}$ are the temperature sensitivities of the parameters. $\mathbf{VFBC}$ is defined by the work function of the gate electrode [20] and, thus, is assumed to change linearly with temperature. When the carriers move in the bulk, $\mathbf{RD}$ is affected due to scattering by the lattice vibration [1]. $\mathbf{MU}$ and $\mathbf{THETA}$ are changed by the temperature [21]. In this model, $\mathbf{MU}$ and $\mathbf{THETA}$ are empirically modeled as (17) and (18). Although the other parameters related to the interface trap, such as $\mathbf{DMID}$, $\mathbf{DC}$, $\mathbf{NIT}$, $\mathbf{NC}$, and $\mathbf{ZETAC}$, are also known to have complex temperature dependencies [22], these parameters are also modeled linearly considering the temperature range in the device operation.

C. C–V Characteristic

As shown in Fig. 2, the simulation model of the power MOSFET consists of three terminal capacitances: $C_{\rm gs}$, $C_{\rm ds}$, and $C_{\rm gd}$. In particular, $C_{\rm ds}$ and $C_{\rm gd}$ are highly nonlinear and have considerably impact on the transient characteristic of the high-frequency switching process [4], [23]. In the proposed model, the three capacitances are modeled as

$$C_{\rm gs} = \mathbf{CGSO} \tag{20}$$

$$C_{\rm ds} = \mathbf{ADS} \cdot \sqrt{\frac{\varepsilon_{\rm SiC} \cdot q \cdot \mathbf{ND}}{2(\mathbf{VBI} + V_{\rm ds})}} \tag{21}$$

$$C_{\rm gd} = \mathbf{COXD} \parallel C_{\rm dep}. \tag{22}$$

The gate–source capacitance $C_{\rm gs}$ is the series capacitance of the nonlinear MOS capacitance formed at the channel surface and the constant gate oxide capacitance, as shown in Fig. 1. The change in the MOS capacitance depends on $\phi_{\rm s}$. However, in the proposed model, $C_{\rm gs}$ is approximated as a constant, as $\mathbf{CGS0}$ in (20), because the change of the gate–source capacitance can be considered to be insignificant compared to that in $C_{\rm ds}$ or $C_{\rm gd}$.

The drain–source capacitance $C_{\rm ds}$ is a bias-dependent junction capacitance, which varies with the depletion width at the $\rm p^+$ region and the $\rm n^-$ epitaxial layer in Fig. 1. Hence, $C_{\rm ds}$ is calculated on the basis of the capacitance model of the p-n junction as shown in (21). $C_{\rm gd}$ is calculated by a combination of the constant gate oxide capacitance and the bias-dependent MOS capacitance of the p-type semiconductor formed at the MOS surface in the JFET region.

The gate–drain capacitance $C_{\rm gd}$ is given by (22), which is the series capacitance of the gate oxide capacitance $\mathbf{COXD}$ and the MOS capacitance $C_{\rm dep}$. Considering the body effect [16], $C_{\rm dep}$ is a function of the surface potential $\phi_{\rm gd}$ of the hole channel formed on the drain region under the JFET region, as shown in Fig. 1. Here, $C_{\rm dep}$ is represented as shown in (23) bottom of this page. $\phi_{\rm gd}$ is computed in a similar way to the $\phi_{\rm s}$ calculation using (3) by replacing ($V_{\rm gs}$, $\phi_{\rm f}$, $\mathbf{NA}$, $V'_{\rm fbc}$) with ($V_{\rm gd}$, $V_{\rm ds}$, $\mathbf{ND}$, $\mathbf{VFBD}$), respectively.

$Q_{\rm gs}$, $Q_{\rm ds}$, and $Q_{\rm gd}$ in (13) and (14) are derived by integrating each voltage

$$Q_{\rm gs} = \int C_{\rm gs} dV_{\rm gs} \tag{24}$$

$$Q_{\rm ds} = \int C_{\rm ds} dV_{\rm ds} \tag{25}$$

$$Q_{\rm gd} = \int C_{\rm gd} dV_{\rm gd}. \tag{26}$$

$$C_{\rm dep} = \mathbf{AGD} \cdot \sqrt{2q\varepsilon_{\rm SiC} \cdot \mathbf{ND}} \frac{1 - e^{-\phi_{\rm gd}/\phi_{\rm t}} + e^{-(2\phi_{\rm F} + V_{\rm ds})/\phi_{\rm t}} (e^{\phi_{\rm gd}/\phi_{\rm t}} - 1)}{2\sqrt{\phi_{\rm t} e^{-\phi_{\rm gd}/\phi_{\rm t}} + \phi_{\rm gd} - \phi_{\rm t} + e^{-(2\phi_{\rm F} + V_{\rm ds})/\phi_{\rm t}} (\phi_{\rm t} e^{\phi_{\rm gd}/\phi_{\rm t}} - \phi_{\rm gd} - \phi_{\rm t})}} \tag{23}$$

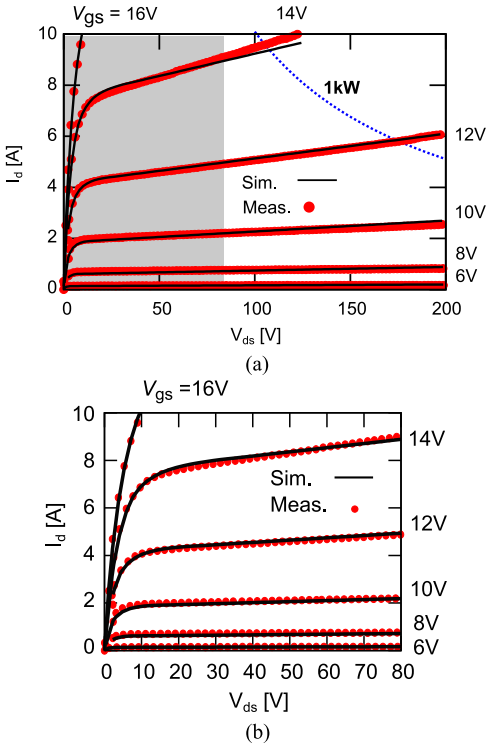

Fig. 3. Measured and simulated $I_{\rm d}$–$V_{\rm ds}$ characteristics. The shaded region in (a) is enlarged in (b). (a) 0 V $\leq V_{\rm ds} \leq$ 200 V. (b) 0 V $\leq V_{\rm ds} \leq$ 80 V.

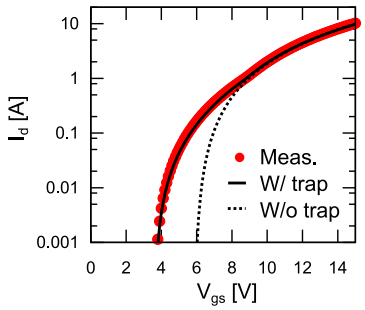

Fig. 4. Measured and simulated $I_{\rm d}$–$V_{\rm gs}$ characteristics.

III. Experiments and Model Validation

To evaluate the proposed model, the *I–V*, *C–V*, temperature, and transient characteristics are compared to the measurement results obtained by using a commercial SiC power MOSFET (ROHM Co., Ltd., SCT2450KE, 1200 V, 10 A [24]).

The *I–V* curves of the SiC power MOSFET are obtained by using a dedicated curve tracer that utilizes a very short pulse to avoid current change due to the self-heating effect [14]. The measured $C_{\rm gs}$ and $C_{\rm gd}$ curves are obtained from the switching trajectory measurement [25]. The $C_{\rm ds}$ curve is measured by a commercial curve tracer (Keysight Technologies, B1505A [26]) at 1 MHz.

The proposed surface-potential-based model is implemented using Verilog-A [27]. The *I–V*, *C–V*, and transient characteristics are calculated by a commercial SPICE simulator (SIMetrix Technologies, SIMetrix [28]). The physical constants are summarized in Table IV. Tables V–VII show the values of the model

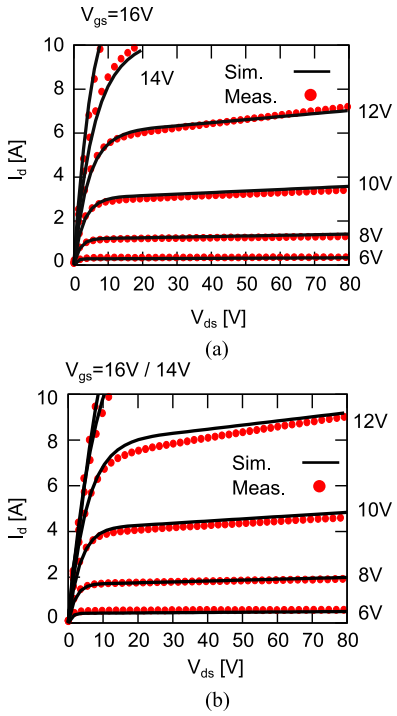

Fig. 5. Measured and simulated $I_{\rm d}$–$V_{\rm ds}$ characteristics at (a) 348 and (b) 398 K.

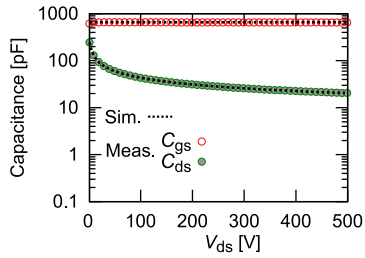

Fig. 6. Measured and simulated $C_{\rm gs}$ and $C_{\rm ds}$ characteristics.

parameters at room temperature (298 K). Using an impedance analyzer [29], **RG** is estimated by fitting the frequency characteristics to an equivalent series resistance of $C_{\rm gs}$. We assume **TOX** to be 50 μm. The remaining model parameters are determined by a simulated annealing method [30] with the extracted parameters as the initial values. In the evaluation of the temperature dependence, the reference temperature is set as $T_0 = 298$ K. Hence, the intercept of the parameters for the temperature, such as **VFBC0** and **RD0**, is equal to the values shown in Table V, and they are omitted in Table VII. The temperature-related parameters are calculated from the measured *I–V* curves at 298 and 398 K.

A. I–V and C–V Characteristics

The measured and simulated *I–V* and *C–V* characteristics are shown in Figs. 3–7. The proposed model accurately reproduces wide range of the *I–V* and *C–V* characteristics of the SiC MOSFET. In Fig. 3(a), the dashed lines express the contours of the power dissipation. It should be noted that our model could accurately simulate the *I–V* curve in the high-power region of

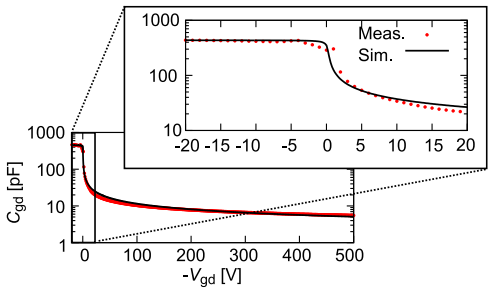

Fig. 7. Measured and simulated $C_{\rm gd}$ characteristics.

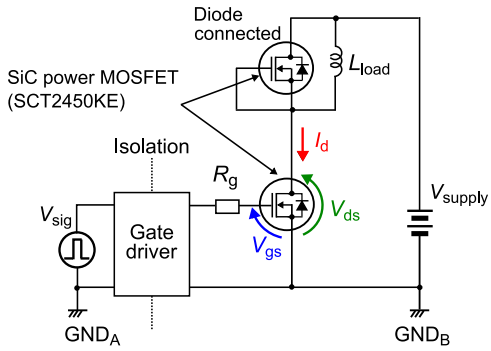

Fig. 8. Double-pulse tester circuit.

more than 1 kW, wherein practical high-power converters operate. Fig. 3(b) shows the *I–V* curves in the region, which is shaded in Fig. 3(a), again showing good agreement with the measured ON-resistance. In addition, Fig. 4 shows the measured and simulated $I_{\rm d}-V_{\rm gs}$ characteristics at $V_{\rm ds}=20$ V. The solid and dashed lines represent the simulated curves with and without the interface trap effect. When the interface trap is not considered, the model can never fit to the measurement, whereas the proposed model can accurately simulate the drain current modulated by the interface trap in the small gate voltage region. From Figs. 3 and 4, we conclude that the proposed model is applicable to the wide power region from 0.02 W to over 1 kW. Because the proposed model is physically accurate, it should be applicable beyond the power regions verified. Fig. 5 shows the measured and simulated *I–V* characteristics at 348 and 398 K. The agreements between the simulated and the measured characteristics are again excellent.

Fig. 6 shows the simulated and measured results of the $C_{\rm gs}$ and $C_{\rm ds}$ curves, and Fig. 7 shows the simulated and measured result of $C_{\rm gd}$. All the proposed capacitance models achieve good accuracy. In particular, the $C_{\rm gd}$ of the proposed model shows a smooth transition about that voltage through computation of the $V_{\rm gd}$ dependence of the surface potential.

B. Transient Characteristics

The evaluation of the transient analysis is conducted using the double-pulse tester shown in Fig. 8. Two SCT2450KE devices are used for both measurements and simulations. The upper transistor is used as a freewheeling diode and the lower one is the switching device. The diode characteristics are modeled by using the traditional p-n junction diode model [31]. The parasitic impedances of the packages and the passive components are measured with an impedance analyzer (Agilent Technologies, 4294A [32]) and are modeled as simple equivalent circuits comprised of a few circuit elements. In the double-pulse tester,

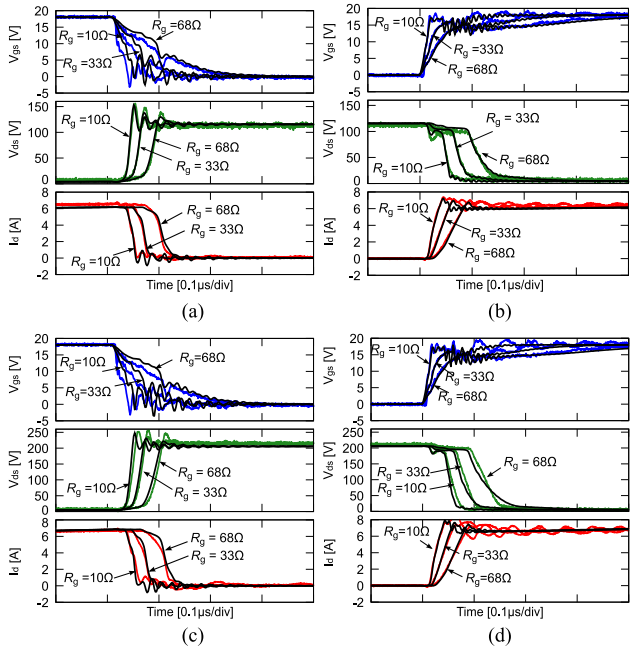

Fig. 9. Measured and simulated switching waveforms ($T=298$ K, colored: measured, black: simulated). (a) Turn-OFF ($V_{\rm supply}=100$ V). (b) Turn-ON ($V_{\rm supply}=100$ V). (c) Turn-OFF ($V_{\rm supply}=200$ V). (d) Turn-ON ($V_{\rm supply}=200$ V).

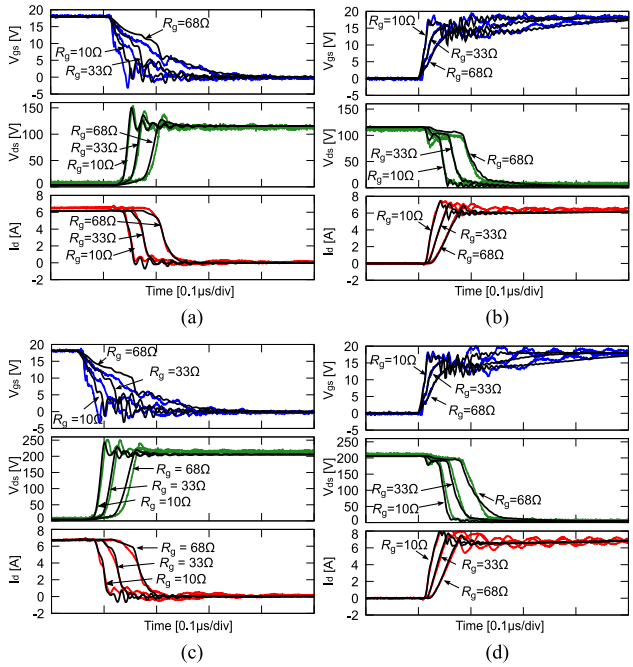

Fig. 10. Measured and simulated switching waveforms ($T=348$ K, colored: measured, black: simulated). (a) Turn-OFF ($V_{\rm supply}=100$ V). (b) Turn-ON ($V_{\rm supply}=100$ V). (c) Turn-OFF ($V_{\rm supply}=200$ V). (d) Turn-ON ($V_{\rm supply}=200$ V).

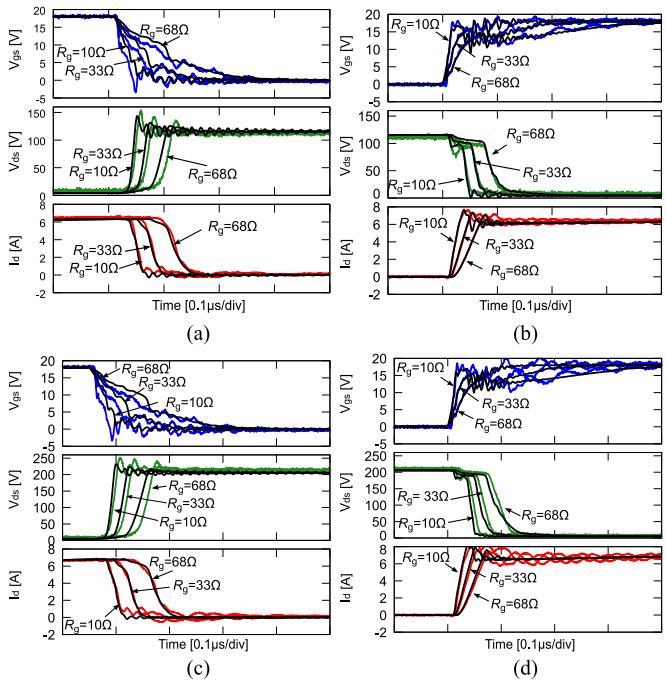

Fig. 11. Measured and simulated switching waveforms ($T = 398$ K, colored: measured, black: simulated). (a) Turn-OFF ($V_{\rm supply} = 100$ V). (b) Turn-ON ($V_{\rm supply} = 100$ V). (c) Turn-OFF ($V_{\rm supply} = 200$ V). (d) Turn-ON ($V_{\rm supply} = 200$ V).

TABLE VIII
TIMING ERRORS BETWEEN THE SIMULATED AND MEASURED SWITCHING WAVEFORMS ($T = 298$ K)

	10 Ω	33 Ω	68 Ω
Turn-ON (100 V/200 V)	0.8 ns/3.6 ns	0.6 ns/7.4 ns	−1.9 ns/6.4 ns
Turn-OFF (100 V/200 V)	0.2 ns/3.4 ns	−0.4 ns/2.0 ns	1.9 ns/4.6 ns

TABLE IX
TIMING ERRORS BETWEEN THE SIMULATED AND MEASURED SWITCHING WAVEFORMS ($T = 348$ K)

	10 Ω	33 Ω	68 Ω
Turn-ON (100 V/200 V)	0.2 ns/2.6 ns	−0.9 ns/5.2 ns	−5.2 ns/3.2 ns
Turn-OFF (100 V/200 V)	0.4 ns/1.2 ns	1.9 ns/3.6 ns	5.3 ns/7.8 ns

the load inductance $L_{\rm load}$ is 380 μH. The value of the external gate resistor $R_{\rm g}$ is either 10, 33, or 68 Ω, and the supply voltage $V_{\rm supply}$ is 100 or 200 V. In addition, the temperature of the MOSFET, T, is set to 298, 348, and 398 K.

In Figs. 9–11, the simulated and the measured waveforms of $I_{\rm d}$, the gate–source voltage $V_{\rm gs}$, and $V_{\rm ds}$ at the turn- ON and turn-OFF periods are compared. The device temperatures in Figs. 9–11 are at $T = 298$ K, 348 K, and 398 K, respectively. In the respective figures, (a) and (b) show the switching behavior at $V_{\rm supply} = 100$ V and (c) and (d) show those at $V_{\rm supply} = 200$ V.

TABLE X
TIMING ERRORS BETWEEN THE SIMULATED AND MEASURED SWITCHING WAVEFORMS ($T = 398$ K)

	10 Ω	33 Ω	68 Ω
Turn-ON (100 V/200 V)	1.0 ns/6.0 ns	1.4 ns/7.4 ns	− 0.2 ns/7.4 ns
Turn-OFF (100 V/200 V)	2.9 ns/2.6 ns	5.6 ns/7.4 ns	12.6 ns/12.2 ns

In all combinations of the temperatures and supply voltages, the proposed MOSFET model with a single set of model parameters is consistently used. The measurement waveforms change slightly as we changed the supply voltage; the simulation results tracked the changes very well. Tables VIII–X show the timing error between the simulated and measured switching waveforms at each temperature. The timing error is defined as the difference of the measurement and simulation at $V_{\rm ds} = 50$ V or 100 V, which is half of the supply voltage. In the tables, positive error means that the timing in the measurement is faster than that of the simulation. These results demonstrate that, for all $R_{\rm g}$ values, the proposed model can accurately simulate the transient characteristics of the double-pulse tester, achieving a maximum error of 12.6 ns in the transient. The proposed model successfully reproduces the switching behavior in various conditions, since the timing error is sufficiently small considering the typical operation frequencies of power converters of megahertz.

IV. CONCLUSION

In this paper, a surface-potential-based simulation model for SiC power MOSFETs is proposed that reproduces the device behavior with good accuracy for a very wide range of operating biases and temperatures. In the proposed model, the *I–V* and *C–V* characteristics are consistently represented by the surface potential equations that reflect the structure of the vertical power MOSFET. The proposed model also considers the influence of the interface trap on the basis of the physical behavior that impacts on the channel mobility degradation using the surface potential equation. Experimental results using a commercial SiC power MOSFET show that the proposed simulation model successfully reproduces the *I–V* and *C–V* characteristics in the power regions from 0.02 W to 1 kW. It is also demonstrated that the transient waveforms are accurately predicted within the timing error of 12.6 ns by the inductive-load double-pulse tester even under the high temperature.

Our future work includes an evaluation with a practical supply voltage, e.g., 600 V for an SiC MOSFET with a rated voltage of 1200 V, demonstrating the accuracy of the proposed model. Also, modeling of parasitic elements of the power converters is required to evaluate the proposed model under the faster operation frequency. In addition, the modeling of the interface trap in the proposed model is still limited, since the model parameters are treated as the linear function of the temperature. We intend to investigate the nonlinearity of the model parameters related to the interface trap, as presented in [22], to correctly capture the interface trap effect in circuit simulations.

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