Operation and Control Scheme of a Five-Level Hybrid Inverter for Medium-Voltage Motor Drives

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***Abstract*—This paper proposes a control method for a five-level hybrid flying-capacitor (5L-HFC) inverter, of which structure stems from the conventional five-level active neutral-point-clamped (5L-ANPC) topology by dividing the dc-link stage into three series-connected capacitors. In this inverter, the voltage stress on the power switches connected to the dc link is reduced by a half compared with that of the 5L-ANPC topology, thus the lower number of equally voltage-rated power devices can be employed. Also, the power losses in the 5L-HFC inverter are more evenly distributed than in the 5L-ANPC. In order to balance the dc-link capacitor voltages, a third-order harmonic offset injection is applied. When a diode rectifier is used to supply the dc bus voltage, the balancing method is not effective if the modulation index is higher than 0.64. Thus, an auxiliary circuit is needed to support the balancing of the dc-link capacitor voltages. However, the unbalancing problem can be overcome in a full-range operation without the auxiliary circuit if the back-to-back configuration is utilized. Finally, simulation and experiment results have verified the performance of the 5L-HFC inverter with the proposed control method.**

***Index Terms*—Active neutral-point-clamped inverters, capacitor voltage balancing, flying capacitor (FC), multilevel inverter, power loss distribution.**

I. Introduction

In MEDIUM-VOLTAGE (MV) motor drive applications, variable-speed drive (VSD) systems have been employed widely due to significant advantages such as energy-saving potential and enhanced performance. Due to the growing demand of MV VSD applications, numerous inverter topologies have been proposed and developed. Most of them are multilevel topologies, which can generate high-quality output voltages and currents with low total harmonic distortion (THD), low *dv/dt*, and low common-mode voltage. Thus, the inverter power loss and the stress on bearings and windings of the motor can be reduced if the multilevel inverters with a large number of voltage levels are utilized [1]–[3].

The conventional multilevel topologies are mainly classified into three types [4]: the neutral-point clamped (NPC), the flying capacitor (FC), and the cascaded H-Bridge (CHB). For three-level applications, the NPC, the active NPC (ANPC) [5], and the T-type NPC [6] topologies have been developed to a mature technology and have been used widely in industry. For a MV level like 6.6 kV [7], five-level inverters are a preferable solution due to the limitation of voltage rating of commercial semiconductor devices. Unfortunately, each type of the conventional five-level inverters has some major drawbacks that make them inappropriate for industrial applications. First, the five-level NPC (5L-NPC) inverter suffers from the voltage drift phenomenon of four series-connected dc-link capacitors [8] and requires a large number of clamping diodes. Second, the 5L-FC inverter requires a large number of FCs, where the FC voltage control is much complicated [4]. Third, although the 5L-CHB inverter can avoid the capacitor voltage unbalance problems, it requires isolated dc power sources [4].

To overcome the aforementioned drawbacks of the existing five-level topologies, many new topologies have been introduced in the literature [9]–[15]. One of the most promising topologies is the active neutral-point-clamped five-level inverter based on the hybrid FC, which is called the five-level active NPC (5L-ANPC) inverter [9], [16]–[19]. The structure of this topology is a combination of a three-level active NPC leg and a three-level FC cell. Compared with the conventional 5L-NPC and 5L-FC topologies, the cost and control complexity of the 5L-ANPC topology can be reduced since it requires only one FC per phase without any clamping diodes. Furthermore, the dc-link capacitor voltages can be self-balanced if passive front-end rectifiers are used. Due to these advantages of the 5L-ANPC inverter, it has been used in industrial applications.

This paper proposes a control scheme for a five-level hybrid inverter named as five-level hybrid flying-capacitor (5L-HFC) inverter (see Fig. 1). The 5L-HFC structure is derived from the 5L-ANPC topology, having one three-level FC unit connected with two two-level converter units. Compared with the 5L-ANPC topology, the dc-link stage of the proposed topology is divided by three capacitors without the middle-point connection. The three dc-link capacitors are charged and controlled at different voltages. The top and bottom capacitor voltages are a quarter of the dc-link voltage. Therefore, the voltage rating of semiconductor devices connected to the dc bus is decreased by a half compared with that of the 5L-ANPC inverter. As a result, the lower number of power devices with the identical voltage rating is employed. In addition, in the 5L-HFC, the loss distribution among the power switches is improved compared with that of the 5L-ANPC topology. However, by splitting the

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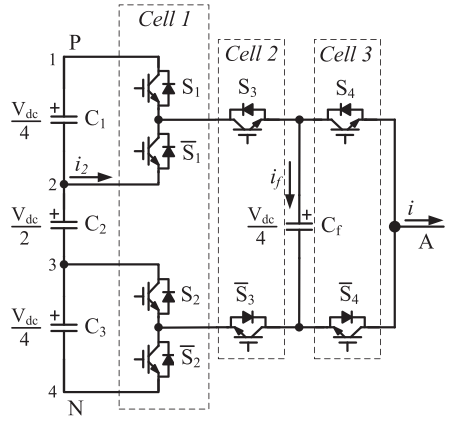

Fig. 1. Single-phase diagram of the proposed 5L-HFC inverter.

dc-link stage into three series-connected capacitors, the 5L-HFC inverter cannot avoid the voltage unbalance of the dc-link capacitors. This problem cannot be solved over a full operation range by a modulation technique when a diode front-end rectifier is used. Thus, an auxiliary circuit for balancing the dc-link capacitor voltages is needed. However, the unbalance problem can be solved by modifying the modulation technique in back-to-back configuration systems, where no additional hardware is required for controlling the capacitor voltages. Simulation has been performed for a 4.16 kV/1 MW 5L-HFC inverter system, which verifies the validity of the proposed scheme. Also, experiment results in the 5-kW down-scaled system has been presented, which shows the feasibility of the proposed 5L-HFC inverter. In addition, a comparison between the proposed 5L-HFC topology and existing ones is conducted in terms of power losses and component costs. For a 4.16 kV/1 MW back-to-back system, the analysis shows that the cost of the 5L-HFC rectifier/inverter is decreased by 11%, 14%, and 28% compared with the 5L-FC, 5L-ANPC, and 5L-NPC rectifiers/inverters, respectively.

II. Proposed 5L-Hybrid Inverter Topology and Operation

A. Structure of the Proposed 5L-HFC Topology

Fig. 1 shows a single-phase diagram of the proposed 5L-HFC inverter topology, where a phase leg consists of two two-level half-bridge units (Cell 1) and a three-level FC topology (Cell 2 and Cell 3). The main difference in comparison with the 5L-ANPC inverter is that the dc-link stage of the proposed topology is split into three capacitors and that there is no connection to the middle-point of the dc link. Due to this difference, the voltage rating of switching devices in Cell 1 can be decreased by a half compared with that of the 5L-ANPC inverter. However, the dc-link capacitor voltages cannot be balanced by a modulation technique. In this case, these voltages should be controlled by an auxiliary circuit or an active front-end converter resulting in a back-to-back configuration. The unbalance of dc-link capacitor voltages will be analyzed in detail in Section III.

To operate the 5L-HFC inverter, the voltage of each capacitor should be precharged and maintained at the reference values.

TABLE I
Switching States of the Proposed 5L-HFC With Effects on Voltages of C_f and C_2

S_1	S_2	S_3	S_4	V_{AN}	States	Effect on V_{C_f}		Effect on V_{C_2}	
						$i>0$	$i<0$	$i>0$	$i<0$
0	0	0	0	0	V_0	0	0	0	0
0	0	0	1	$V_{dc}/4$	V_1^*	−	+	0	0
0	1	0	0	$V_{dc}/4$	V_1	0	0	+	−
0	1	0	1	$V_{dc}/2$	V_2	−	+	+	−
0	1	1	0	$V_{dc}/2$	V_3	+	−	−	+
0	1	1	1	$3V_{dc}/4$	V_4	0	0	−	+
1	1	1	0	$3V_{dc}/4$	V_4^*	+	−	0	0
1	1	1	1	V_{dc}	V_5	0	0	0	0

For the dc-link stage consisting of three capacitors, the upper and lower capacitors, C_1 and C_3, are charged to $V_{dc}/4$ and the middle-capacitor C_2 is charged to $V_{dc}/2$, respectively. Each phase of the inverter has an FC, which is charged to $V_{dc}/4$.

It should be noted that the switching devices are not rated at the equal blocking voltage. In particular, the voltage stress in the devices of Cell 1 and Cell 3 is $V_{dc}/4$, but that of in the devices of Cell 2 is $V_{dc}/2$. Thus, the power switches in Cell 2 require double the voltage blocking capability compared with those in Cell 1 and Cell 3. If the inverter is designed with equally voltage-rated insulated-gate bipolar transistors (IGBTs), ten switches are needed for each phase leg, where two series-connected IGBTs are used for Cell 2.

Actually, the structure of the 5L-HFC topology is similar with those presented in [20] and [21], which are four-level and six-level inverter topologies, respectively. Although both topologies have a similar structure, the number of voltage levels is different, depending on the operating voltages of the dc-link and FCs. Both of these topologies aimed at applying to the MV applications, but depending on the voltage level and the voltage rating of available semiconductor devices, the appropriate topology should be chosen carefully to optimize the cost and efficiency of the system.

B. Operating Principle

Eight switching states of the 5L-HFC topology and their effects on the voltages of the FC and the middle dc-link capacitor are listed in Table I. The pairs of switches $(S_1, \overline{S_1})$, $(S_2, \overline{S_2})$, $(S_3, \overline{S_3})$, and $(S_4, \overline{S_4})$ are operated in a complementary way. So, for simplicity, only the states of four switches, S_1, S_2, S_3, and S_4, are listed in Table I, where the ON and OFF states of each switch are indicated by "1" and "0," respectively. The effects of charging and discharging on the FC voltages are in order represented by "+" and "−." In the case of no influence, it is indicated by "0."

It is noticed from Table I that there are three pairs of switching states which produce the equal output voltage level, that is, V_1^* & V_1, V_2 & V_3, and V_4 & V_4^*. Although the switching states, V_1^* and V_4^*, have no impact on the dc-link capacitor voltages, the use of these two states leads to the deviation of the FC voltages from their desired values, which causes the distortion of output voltages and currents. Therefore, only six switching

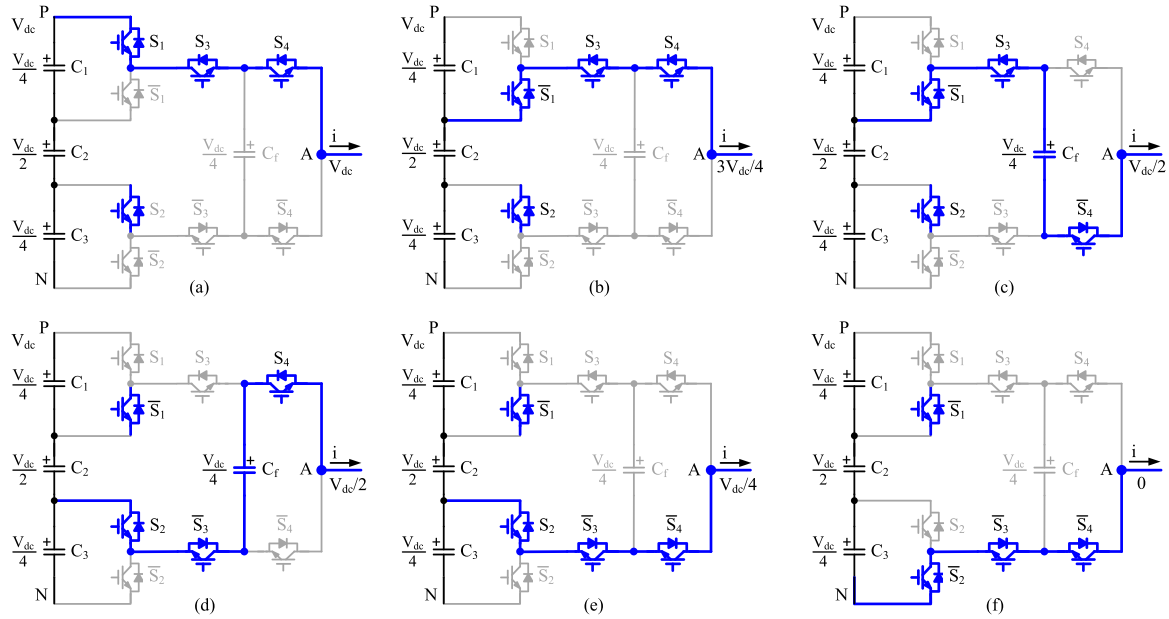

Fig. 2. Six switching states for the 5L-HFC inverter. (a) V_5. (b) V_4. (c) V_3. (d) V_2. (e) V_1. (f) V_0.

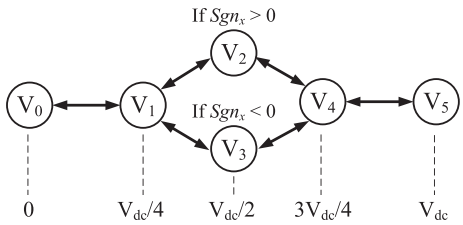

Fig. 3. Transitions for the proposed 5L-HFC.

states are utilized to generate the five output voltage levels. Fig. 2 illustrates six switching states used for the 5L-HFC inverter.

The voltages of the FCs can be maintained by two redundant states V_2 and V_3, which generate the pole voltage of $V_{\rm dc}/2$. The redundant states need to be selected appropriately according to the direction of the phase currents to charge or discharge the FCs. To make an appropriate selection of the redundant states, a simple sign function is used, defined as follows:

$$\mathrm{Sgn}_x = \mathrm{sgn}\left[\left(v_{fx} - V_{\rm dc}/4\right) i_x\right] \tag{1}$$

where v_{fx} and i_x are the FC voltage and the current of phase x, respectively. If Sgn_x is positive, then, the switching state V_2 should be chosen, whereas V_3 is selected if Sgn_x is negative.

Fig. 3 illustrates the transition sequence to generate five output voltage levels as well as to balance the FC voltages. The transition between every two adjacent switching states is made by switching only two devices, thus minimizing the switching power losses. It is worth noting that the direct commutation between V_2 and V_3 is not recommended since four devices need to be switched, which produces higher switching losses. Furthermore, during the dead time interval, the transition between V_2 and V_3 generates an undesirable output voltage level of $V_{\rm dc}/4$ or $3V_{\rm dc}/4$ when the output current is positive or negative, respectively.

III. Control of the DC-Link Capacitor Voltages

In the 5L-HFC topology, the voltage drift phenomenon of the dc-link capacitors is similar to that of the passive front-end 5L-NPC topology. Therefore, like the 5L-NPC topology, if the proposed 5L-HFC inverter is operated at a high modulation index (M), the middle-capacitor will gradually discharge, causing the deterioration of the output voltage waveform and consequently resulting in a failure or even damages to the inverter and motor [8]. Several methods employing additional hardware have been suggested to balance the dc-link capacitor voltages [22], [23]. These methods can solve the voltage drift problem for all operating conditions, but they require additional hardware, which increases the cost, weight, and complexity of the system, particularly in MV applications.

In this section, to keep the middle-capacitor voltage constant, a voltage modulation strategy that regulates the average currents through the switches $\overline{S_1}$ and S_2 is described.

A. Calculation of the Average Current Through $\overline{S_1}$

An in-phase disposition level-shifted multicarrier PWM method is adopted for the proposed 5L-HFC inverter. Since the system is symmetric, only one leg of the inverter is considered for simplicity. The reference voltage is expressed as follows:

$$v_{\rm ref} = 2M \sin\theta \tag{2}$$

where M is the modulation index and θ is the phase angle of the reference voltage.

To enhance the dc-link voltage utilization, a third-harmonic signal, which is defined as follows:

$$v_{3\rm rd} = -\frac{\max\left(v_{\rm aref}, v_{\rm bref}, v_{\rm cref}\right) + \min\left(v_{\rm aref}, v_{\rm bref}, v_{\rm cref}\right)}{2} \tag{3}$$

is injected to the sinusoidal reference signal [24].

The output current of the inverter is assumed to be in-phase with the reference voltage since only the active components of the currents have effect on the voltage balance [25]. Then

$$i_{\text{inv}} = I_{\text{pk}} \sin\theta \tag{4}$$

where I_{pk} is the peak value of the output current, which is given by the following:

$$I_{\text{pk}} = \sqrt{2}\frac{P}{3V_{\text{inv}}} = \frac{\sqrt{2}P}{3M\frac{V_{\text{dc}}}{2\sqrt{2}}} = \frac{4P}{3MV_{\text{dc}}} \tag{5}$$

where P is the output power of the inverter and V_{inv} is the rms value of phase voltages.

For a simple analysis, the normalized current is employed, where its base value is defined as follows:

$$I_{\text{base}} = 4P/3V_{\text{dc}}. \tag{6}$$

From (4) to (6), then, the per-unit value of the inverter output current is expressed as follows:

$$i'_{\text{inv}} = \frac{i_{\text{inv}}}{I_{\text{base}}} = \frac{1}{M}\sin\theta. \tag{7}$$

The middle-capacitor voltage is affected by four switching states, which are V_1, V_2, V_3, and V_4. However, the influences of V_2 and V_3 on V_{C2} are cancelled in one fundamental cycle as they are applied alternately to balance the FC voltages. On the other hand, V_1 affects the current through the switch S_2. As a result, it can be assumed that only V_4 has an effect on the average value of currents through the switch $\overline{S_1}$. Therefore, the duty cycle where the current flows through $\overline{S_1}$ is expressed as follows:

$$D_{i2} = \begin{cases} 2 - v_{\text{ref}}, & \text{if } 1 \le v_{\text{ref}} \le 2 \\ v_{\text{ref}} & \text{if } 0 \le v_{\text{ref}} \le 1 \end{cases}. \tag{8}$$

If the carrier frequency is higher than the fundamental one, then the average current flowing through $\overline{S_1}$ can be approximated as follows:

$$I'_{2\text{avg}} \approx \frac{1}{\pi}\int_0^{\pi} i'_{\text{inv}} D_{i2}\, d\theta = \frac{1}{\pi M}\int_0^{\pi} D_{i2}\sin\theta d\theta. \tag{9}$$

B. Control of the Average Currents Through $\overline{S_1}$ and S_2

An appropriate offset signal is injected to the reference signals in order to control the average currents in the branches connected to the middle dc-link nodes (see node 2 and 3 in Fig. 1) [26].

The frequency of the balancing offset signal is three times higher than the fundamental frequency so that it does not affect the fundamental components of the three-phase output voltages. The offset signal is chosen to affect the reference signal at $[\pi/3,\ 2\pi/3]$, since the duty cycle D_{i2} has stronger effects on the current $I'_{2\text{avg}}$ when the value of $\sin\theta$ is high, as can be seen from (9). Also from (9), the average current $I'_{2\text{avg}}$ increases when D_{i2} approaches to 1 and $I'_{2\text{avg}}$ decreases when D_{i2} is closer to 0. Therefore, to achieve the maximum average current $I'_{2\text{avg,max}}$, the offset signal must be chosen so that the new reference signal is equal to one at $[\pi/3,\ 2\pi/3]$. On the other hand, to minimize the average current, the new reference signal needs to be equal to two while θ is in $[\pi/3,\ 2\pi/3]$. The average current $I'_{2\text{avg}}$ can be controlled easily to a certain value between the maximum and minimum average currents ($I'_{2\text{avg,max}}$ and $I'_{2\text{avg,min}}$) by adjusting the pulsewidth d_{offset} of the balancing offset signal.

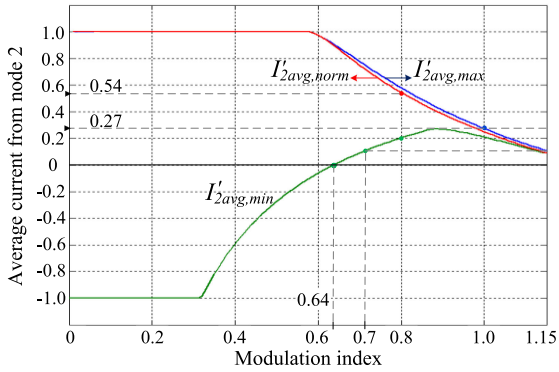

Fig. 4. Average current $I'_{2\text{avg}}$ versus modulation index.

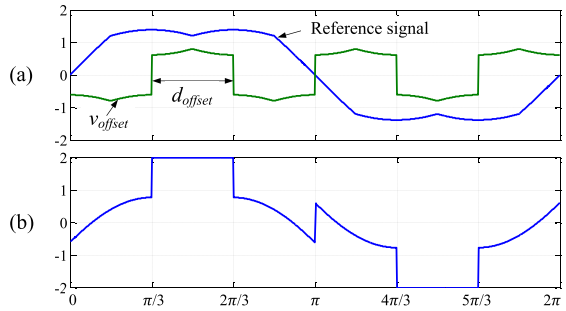

Fig. 5. Balancing offset signal with minimum average current. (a) Reference signal and offset signal. (b) Reference signal after adding offset signal.

The value of $I'_{2\text{avg,norm}}$ (no balancing offset signal added), $I'_{2\text{avg,min}}$, and $I'_{2\text{avg,max}}$ are calculated in (9) as the modulation index is changed from 0 to 1.15. These average values are illustrated in Fig. 4 as a function of modulation index.

Fig. 5 shows an example where the offset signal is chosen to get the minimum average currents. The modulation index of the reference signal in Fig. 5 is 0.8. From Fig. 4, at $M = 0.8$, without the balancing offset signal, the average current is 0.54, and when the offset signal is added, the average current is 0.2. The modified modulation technique also brings an additional advantage of reducing the switching losses, which will be analyzed in Section IV.

To balance the dc-link middle-capacitor voltages, the average current through $\overline{S_1}$ should be zero. As seen from Fig. 4, the value $I'_{2\text{avg,min}}$ is higher than zero if $M > 0.64$. Thus, the average current $I'_{2\text{avg}}$ cannot be controlled to be zero by the balancing offset signal if $M > 0.64$. Therefore, if the modulation index is higher than 0.64, an auxiliary circuit [21], as shown in Fig. 6, is required for balancing the middle-capacitor voltages. The control block diagram of the middle-capacitor voltage is illustrated in Fig. 7. Fig. 7(a) shows the control of V_{C2} using the offset signal where its pulsewidth d_{offset} is regulated by a PI controller. When the pulsewidth reaches the maximum value ($\pi/3$), a controller in Fig. 7(b) for the auxiliary circuit is activated to support the balancing of V_{C2}.

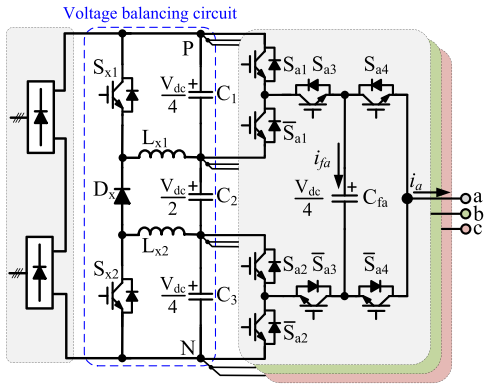

Fig. 6. Structure of the 5L-HFC with a dc-link voltage balancing circuit.

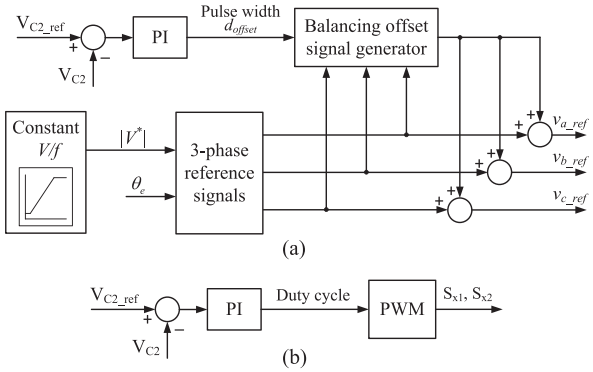

Fig. 7. Control block diagram for balancing the middle-capacitor voltage. (a) With balancing offset signal. (b) With the auxiliary circuit.

The unbalance problem of the dc-link capacitor voltages can be solved in a back-to-back rectifier/inverter configuration without any additional hardware [25], [26]. The basic idea is to coordinate the operations of the active rectifier and the inverter to balance the charging and discharging of the dc-link capacitors.

From the analysis results in Fig. 4, the maximum value of $I'_{2\mathrm{avg,min}}$ is 0.27 p.u. If the average currents of the inverter and the rectifier are controlled at 0.27 p.u., the middle-capacitor voltage can be kept constant. However, if the modulation index is higher than 1.0, $I'_{2\mathrm{avg}}$ cannot be controlled at 0.27 p.u. as seen from Fig. 4. Therefore, to ensure the dc-link voltage balancing with this method, the modulation index should be limited to 1.0. If the modulation index of the rectifier is kept below 0.7, the inverter can operate with a full range of modulation index.

IV. Power Loss Analysis

In this section, the power losses of the proposed 5L-HFC inverter are analyzed based on the thermal module in PSIM software, of which result is compared with that of the 5L-ANPC inverter. For the analysis, two 4.16 kV/1 MW inverter systems are designed with the parameters listed in Table II. The same IGBT module, FF200R33KF2C (3300 V/200 A), from Infineon Co. is adopted for the two inverter systems. The detailed selection of devices is listed is Table III. Both the inverters are controlled by a carrier-based (in phase-disposition level-shifted) PWM technique with a carrier frequency of 3 kHz. In this analysis, only the power losses of power semiconductor devices are considered, whereas those of passive components, i.e., capacitors and inductors, have been neglected.

TABLE II
Parameters for Simulation Model and Experimental Prototype

Description	Simulation	Experiment
Inverter parameters		
DC-link voltage	6200 V	312 V
DC-link capacitors C_1, C_2, C_3	2 mF, 1 mF, 2 mF	2 mF, 1 mF, 2 mF
Flying capacitors	1 mF	1 mF
Carrier frequency	3000 Hz	3000 Hz
Motor parameters		
Output power	1000 kW	3 kW
Rated voltage	4160 V	230 V
Rated current	165 A	10.9 A
Fundamental frequency	60 Hz	50 Hz
Rated speed	1789 r/min	1430 r/min
Rated torque	5338 N·m	20 N·m
Pole number	4	4
Rotor inertia	24.6 kg·m^2	0.01 kg·m^2

A. Comparison of Conduction and Switching Losses

Fig. 8 shows the comparison of the conduction and switching losses between two inverters at various speeds, where the subscripts "con," "sw," and "dc" denote the conduction and switching losses, and the losses of the auxiliary circuit, respectively. As seen from Fig. 8, the difference of the conduction losses between these inverters is insignificant. In contrast, due to the effect of the balancing offset signal, the switching losses of the 5L-HFC inverter are lower than that of the 5L-ANPC inverter as the modulation index is increased. During the period when the balancing offset signal is applied, only two out of the three phases are commutated, whereas the other phase is clamped to a particular voltage. As a result, the switching losses of the 5L-HFC is decreased considerably. When the speed is increased from 0.1 to 0.5 p.u., the switching loss is reduced gradually since the pulsewidth d_{offset} of the balancing offset signal is increased. If the speed is higher than 0.5 p.u., the switching losses is decreased by about 33% as the pulsewidth of the offset signal reaches its maximum value of $\pi/3$. When the modulation index is higher than 0.64, the total power losses of the 5L-HFC inverter becomes higher since the auxiliary circuit is activated.

B. Power Loss Distribution

In this section, the distribution of power losses is analyzed since it is an issue that limits the rated output power of the inverter when power losses in semiconductor devices are uneven. In the 5L-ANPC inverter, as the devices in Cell 1 are turned ON/OFF at a fundamental frequency, the switching losses are mostly generated in the devices of Cell 2 and 3. On the contrary, in the proposed 5L-HFC topology, the switching losses are more evenly distributed among the three cells. With the placement of IGBT modules (IM) shown in Fig. 9, the power loss distribution among IGBT modules in one phase leg of the 5L-ANPC and

TABLE III
COST COMPARISON OF DIFFERENT FIVE-LEVEL INVERTERS (IN US $)

Devices	Part Name	Rated value	5L-HFC		5L-ANPC		5L-NPC		5L-FC	
			no.	Price	no.	Price	no.	Price	no.	Price
Dual switch	FF200R33KF2C	3300 V / 200 A	15	9000	18	10 800	12	7200	12	7200
Clamped diode	DD200S33K2C	3300 V / 200 A					18	8640		
DC-link capacitor	C44UOGT7200G5SK	900 V / 2 mF	16	2080	16	2080	16	2080	16	2080
Flying capacitor	C44UOGT7200G5SK	900 V / 2 mF	6	780	6	780			36	4680
Gate driver	2SC0535T	3300 V	15	2250	18	2700	12	1800	12	1800
Summation				14 110		16 360		19 720		15 760

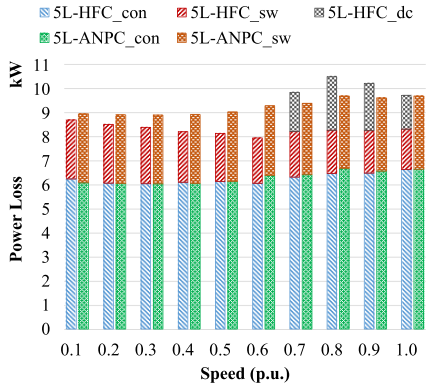

Fig. 8. Power loss comparison at various speeds between 5L-HFC and 5L-ANPC inverters under a full-load condition.

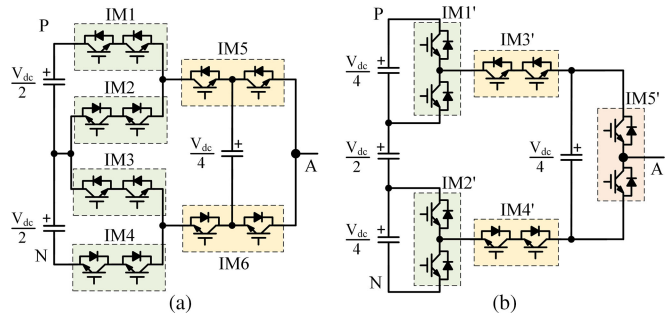

Fig. 9. IGBT modules for one phase of (a) 5L-ANPC inverter and (b) 5L-HFC inverter.

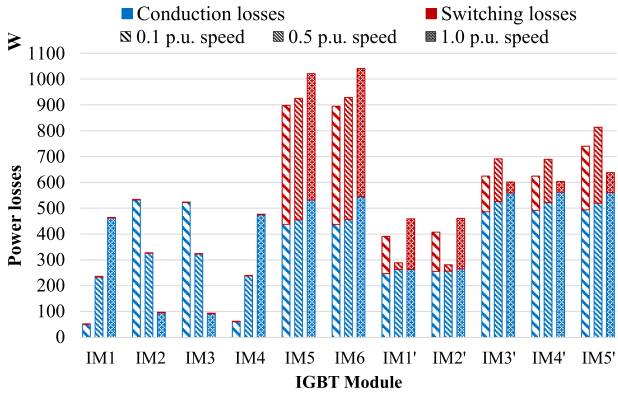

Fig. 10. Power loss distribution among IGBT modules in one phase of the 5L-ANPC inverter and 5L-HFC inverter.

TABLE IV
COST ESTIMATION OF THE BALANCING AUXILIARY CIRCUIT (IN US $)

Devices	Part Name	Rated value	5L-HFC	
			no.	Price
Inductor	CH-100	100 A / 0.5 mH	4	880
Dual switch	FF200R33KF2C	3300 V / 200 A	2	1200
Clamped diode	DD200S33K2C	3300 V / 200 A	2	960
Gate driver	2SC0535T	3300 V	2	300
Summation				3340

5L-HFC inverters is illustrated in Fig. 10. In the analysis, the motor operating speeds of 0.1, 0.5, and 1.0 p.u. are considered under a full-load torque condition. In IM1' of the 5L-HFC inverter, the power losses on the top device (IM1'_top) is higher than those of on the bottom device. However, the highest value of power losses on IM1'_top is not higher than that of other devices in IM3', IM4', and IM5'.

V. COST EVALUATION

In this section, a 4.16 kV/1 MW three-phase inverter system is designed and investigated for cost comparison between the 5L-HFC topology and the existing topologies (5L-ANPC, 5L-NPC, and 5L-FC). The system parameters are listed in Table II. Table III lists the part names and rated values of the chosen devices. The voltage rating of all switches is selected equally as 3300 V, which is about a double of $V_{dc}/4$, to offer a safety margin of about 100% which can lower the risk of failure due to overvoltage surges [27].

For the evaluation, only the costs of IGBT devices, gating drivers, diodes, and capacitors are taken into account. In a back-to-back system, where the auxiliary circuit is not required for balancing of dc-link capacitor voltages, the cost of the 5L-HFC inverter is reduced by 11%, 14%, and 28% compared with that of the 5L-FC, 5L-ANPC, and 5L-NPC inverters, respectively, as listed in Table III. If the 5L-HFC inverter is used with a front-end diode rectifier, the cost of the auxiliary circuit should be included, which is listed in Table IV.

VI. SIMULATION RESULTS

In this section, the performance of the proposed 5L-HFC inverter is verified and evaluated by simulation with PSIM software. The simulation studies are carried out for a 5L-HFC inverter system to drive a 4.16-kV/1-MW induction motor. The

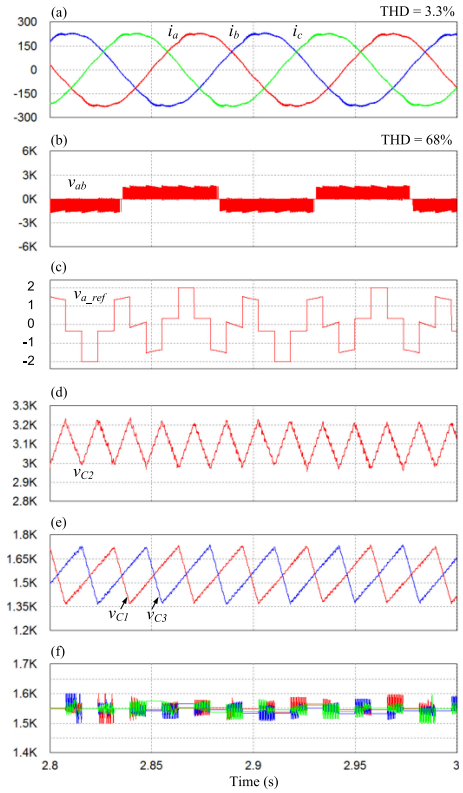

Fig. 11. Performance of the inverter at low speed (300 r/min) and full-load conditions. (a) Three-phase output current (A). (b) Line-to-Line output voltage (V). (c) Reference signal for phase A. (d) Middle dc-link capacitor voltage (V). (e) Top and bottom dc-link capacitor voltage (V). (f) Flying capacitor voltage (V).

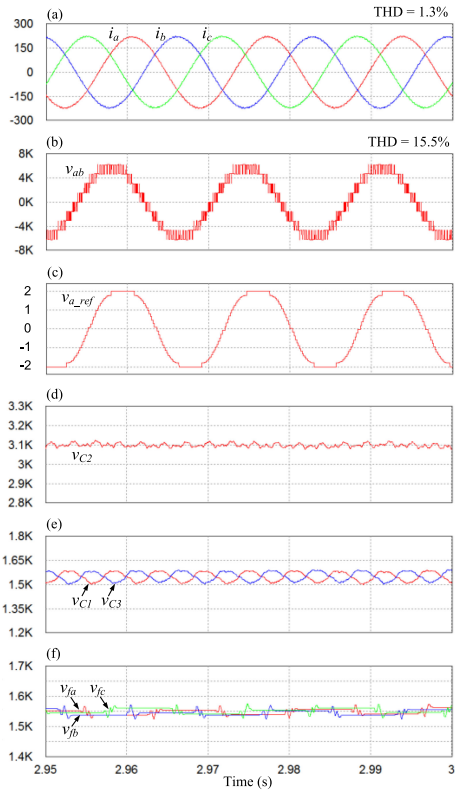

Fig. 12. Performance of the inverter at rated speed and full-load conditions. (a) Three phase output current (A). (b) Line-to-Line output voltage (V). (c) Reference signal for phase A. (d) Middle dc-link capacitor voltage (V). (e) Top and bottom dc-link capacitor voltage (V). (f) Flying capacitor voltage (V).

inverter parameters including capacitor values [21], [28] and the motor parameters are given in Table II.

The carrier frequency is selected to be 3 kHz. An offset signal is added to maintain the voltage of the middle-capacitor in all operation ranges. The upper and lower dc-link capacitor voltages are self-balanced at $V_{\rm dc}/4$ if the middle-capacitor voltage is controlled at $V_{\rm dc}/2$. However, the voltages in C_1 and C_3 have ripples, which depend on the magnitude of the output currents.

Fig. 11 shows the performance of the inverter when the motor is operated at 300 r/min and full-load conditions. The middle-capacitor voltage is kept at its reference of 3100 V. In this case, the auxiliary circuit is not activated. The voltage ripple in C_2 is about 3% (100 V). The voltages in C_1 and C_2 are balanced at 1550 V with a ripple of about 13% ($\pm$200 V). The FC voltages are well balanced with low ripples of about 2% ($\pm$30 V). Due to the large fluctuations of the top and bottom dc-link capacitor voltages, the THD of output currents is high (3.3%).

Fig. 12 shows the same performance as that of in Fig. 11 except that the motor speed is changed to its rated value. Since the modulation index is higher than 0.64, the auxiliary circuit is activated to supply a current for balancing the dc-link middle-capacitor voltage. The balancing offset signal is still added to the reference signals to decrease the switching losses. The dc-link capacitor voltages are well balanced with low ripples. The THD values of the line-to-line voltage and output currents are 15.5% and 1.3%, respectively.

Fig. 13 shows the simulation results under transient conditions when the load is changed from 0.1 to 1.0 p.u. and back to 0.1 p.u., while the motor speed is kept constant at 1000 r/min. Although the top and bottom capacitor voltages are self-balanced at their reference values, their voltage ripples are increased from 1.5% ($\pm$20 V) to 8% ($\pm$120 V) as shown in Fig. 13(c) due to the increase of load currents. The FC voltages are well regulated with ripples of about 5% ($\pm$70 V) under the full-load torque condition.

Fig. 14 shows the transient performance of the inverter when the motor speed is increased from 300 to 1800 r/min, at a full-load condition. Since the modulation index is increased as the motor speed is increased, the pulsewidth of the offset signal is also increased until it reaches the maximum value (π/3), corresponding to about 1000 r/min. From then on, the auxiliary circuit is activated to support the balancing control of the middle-capacitor voltages. The ripples of the dc-link capacitor voltages are decreased at high-speed operation.

VII. Experiment Results

A reduced-scale three-phase inverter prototype has been built to validate the performance of the 5L-HFC topology with the proposed control method. A photo of the experimental setup is shown in Fig. 15, where a 3 kW/230 V induction motor is coupled with a PMSG for applying the load. The parameters of the inverter and the motor are listed in Table II. The speed

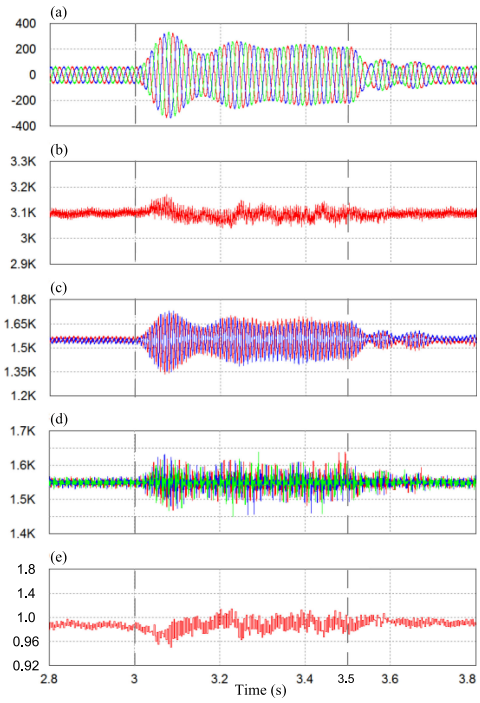

Fig. 13. Performance of the inverter when the load is changed from 0.1 to 1.0 p.u. and back to 0.1 p.u. (a) Three-phase output current (A). (b) Middle dc-link capacitor voltage (V). (c) Top and bottom dc-link capacitor voltage (V). (d) Flying capacitor voltage (V). (e) Pulsewidth of offset singal (radian).

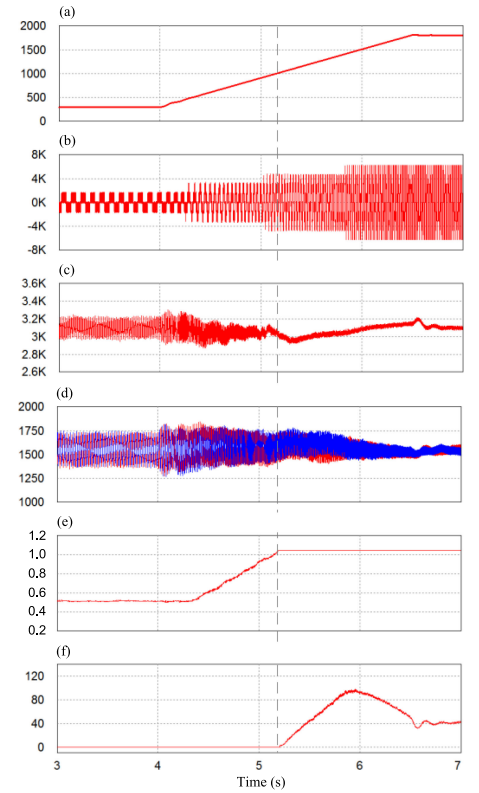

Fig. 14. Performance of the inverter when the motor is accelerated from 300 to 1800 r/min. (a) Rotor speed (rpm). (b) Line-to-Line output voltage (V). (c) Middle dc-link capacitor voltage (V). (d) Top and bottom dc-link capacitor voltage (V). (e) Pulsewidth of offset singal (radian). (f) Auxiliary inductor average current (A).

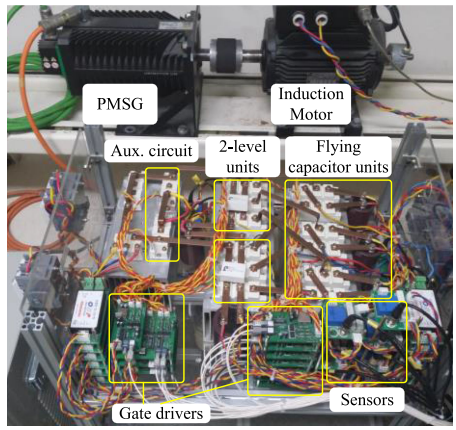

Fig. 15. Experiment setup of the 5L-HFC inverter.

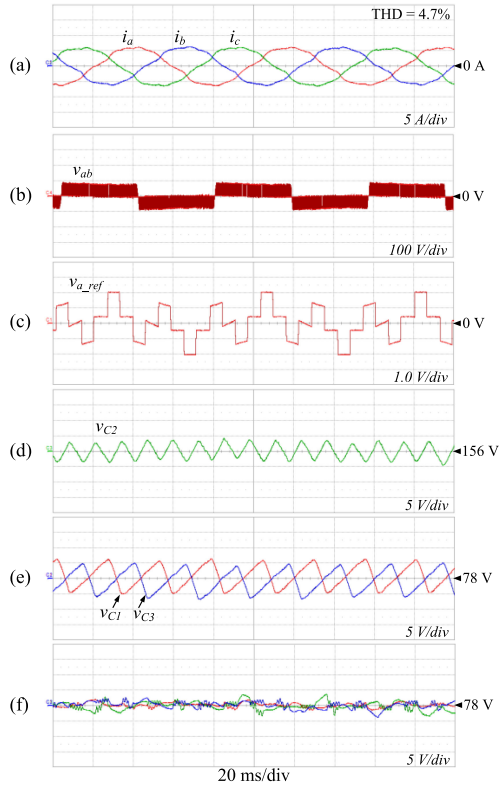

Fig. 16. Inverter control performance when the motor speed is 300 r/min and load torque is 3 N·m. (a) Three-phase output current (A). (b) Line-to-Line output voltage (V). (c) Reference signal for phase A. (d) Middle dc-link capacitor voltage (V). (e) Top and bottom dc-link capacitor voltages (V). (f) Flying capacitor voltages (V).

of the motor is controlled by the constant *V/f* method with a closed-loop feedback.

Fig. 16 shows the steady-state performance of the inverter at 300 r/min. The middle-capacitor voltage, V_{C2}, is controlled by adding the balancing offset signal to the modulation reference signals. The voltage V_{C2} is maintained around 156 V as a half of dc-link voltage, with a ripple of 2.5% ($\pm$4 V). The top and bottom capacitor voltages, V_{C1} and V_{C3}, are self-balanced at 76 V as a quarter of the dc-link voltage. The ripples of these voltages are about 8% ($\pm$6 V). The FC voltages are controlled

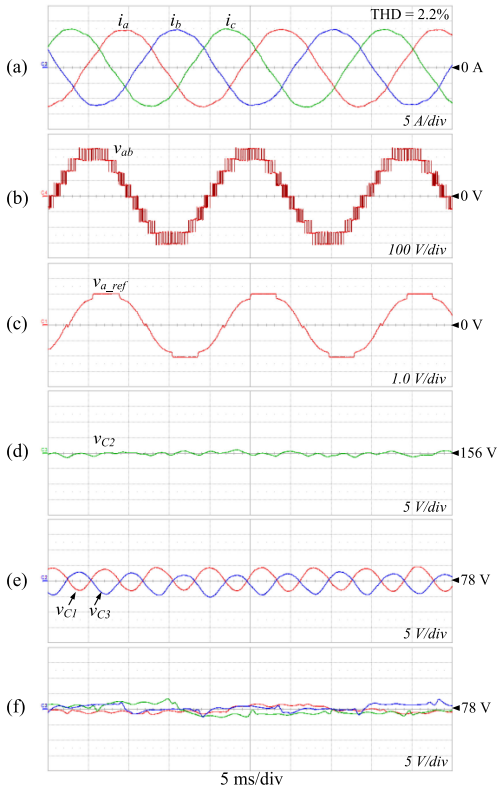

Fig. 17. Inverter control performance when the motor speed is 1500 r/min and load torque is 15 N·m. (a) Three-phase output current (A). (b) Line-to-Line output voltage (V). (c) Reference signal for phase A. (d) Middle dc-link capacitor voltage (V). (e) Top and bottom dc-link capacitor voltages (V). (f) Flying capacitor voltages (V).

independently with the dc-link capacitor voltages around 76 V with low ripples. The THD value of the output currents is 4.7%.

Fig. 17 shows the experimental results at 1500 r/min. At this speed, the voltage-balancing circuit is activated. All the capacitor voltages are well maintained at their reference values. As seen in Fig. 17(b), the output line-to-line voltage waveform has nine voltage levels, where each voltage step is 78 V. The output currents are sinusoidal and balanced, of which THD value is only 2.2%.

Fig. 18 shows the transient responses of the system in the case of load variations at 700 r/min, where the output power is changed from no load to 1 kW and back to no load condition. The dc-link capacitor voltages are well maintained around their reference values. However, higher voltage ripples appear at a high load condition, which are 2.5% ($\pm$4 V) for the middle-capacitor voltage and 10% ($\pm$8 V) for the top and bottom capacitor voltages.

Fig. 19 shows the transient responses of the inverter when the motor speed is increased from 700 to 1100 r/min. Since the balancing control of V_{C2} is only updated every $\pi/3$ in electrical angle, the response of V_{C2} is relatively slow. Thus, there is a decrease in V_{C2} by 6.4% (about 10 V). When the pulsewidth reaches the maximum value of $\pi/3$ at 900 r/min, the auxiliary circuit is activated for balancing control of V_{C2}.

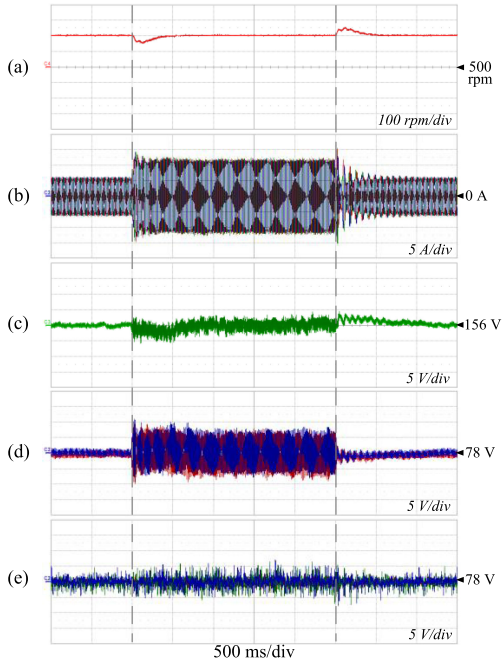

Fig. 18. Experimental results at load change conditions, while the motor speed is operating at 700 r/min. (a) Rootr speed (rpm). (b) Three-phase output currents (A). (c) Middle dc-link capacitor voltage (V). (d) Top and bottom dc-link capacitor voltages (V). (e) Flying capacitor voltages (V).

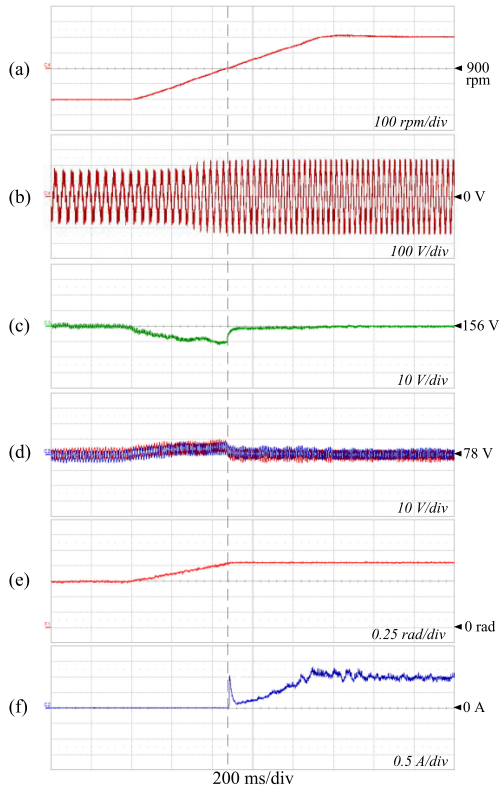

Fig. 19. Experiment results when motor speed is increased from 700 to 1100 r/min. (a) Rootr speed (rpm). (b) Three-phase output currents (A). (c) Middle dc-link capacitor voltage (V). (d) Top and bottom dc-link capacitor voltages (V). (e) Pulsewidth of offset signal (rad). (f) Auxiliary inductor average current (A).

VIII. Conclusion

In this paper, a novel five-level hybrid flying-capacitor inverter for MV motor drives has been proposed and its operating scheme has been developed. To balance the dc-link capacitor voltages, a modulation technique injecting the third-order offset voltage has been utilized, which can also reduce the switching power losses by 33%. However, in the inverter system with a front-end diode rectifier, an auxiliary circuit for balancing the dc-link capacitor voltages is required, which is activated when the modulation index is higher than 0.64. It has been proved that the power loss is distributed more evenly among power switches in the 5L-HFC topology than in the 5L-ANPC topology. The cost evaluation of back-to-back systems have shown that the 5L-HFC inverter system is cheaper by 11%, 14%, and 28% than the 5L-FC, 5L-ANPC, and 5L-NPC inverters, respectively. When considering both advantages and disadvantages of the 5L-HFC topology, the most feasible application is a back-to-back configured system, where no additional hardware is required for balancing the dc-link capacitor voltages.

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