Multirate Digital Signal Processing and Noise Suppression for Dual Active Bridge DC–DC Converters in a Power Electronic Traction Transformer

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***Abstract*—Power electronic traction transformer (PETT) is a single-phase ac–dc conversional system, which is made up of a cascaded H-bridge converter and output-parallel dc–dc converters, such as dual active bridge dc–dc (DAB) converters. As the voltage fluctuation of the dc output voltage of DAB converters is very small and the gain cross-over frequency of the open-loop transfer function of DAB converters is generally high, the DAB closed-loop control system is very sensitive to the influence of noises. The typical noises include the equivalent noise due to the conflict of controller interrupts, the noise due to the mismatch of sampling frequency and switching frequency (which is denoted as switching noise), the noise due to the second-order voltage ripple in the dc input side, the noise due to the quantization process of the analog-to-digital converter (which is denoted as quantization noise), and the noise due to the measuring error of transducers and conditioning circuits (which is denoted as measurement noise). The generation mechanism of these noises and their impacts on the DAB converters are analyzed. On the basis, the corresponding noise suppression schemes are presented, especially for the switching noise, quantization noise, and measurement noise. Besides, the mathematical models toward the sampling and the phase-shift modulation under multirate circumstance are derived, and the multirate digital control strategy of the PETT is proposed. Finally, based on a five-cell PETT laboratory prototype with a rated power of 30 kW, further research is carried out and the experiment results all verify the effectiveness of the proposed algorithms.**

***Index Terms*—Digital control, dual active bridge dc–dc (DAB) converter, multirate digital signal processing, noise attenuation coefficient (NAC), noise suppression, power electronic traction transformer (PETT).**

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I. Introduction

POWER electronic traction transformer (PETT) is aimed to replace the line-frequency traction transformer and the four-quadrant traction converter is now available in high-speed trains [1]–[4]. PETT is made up of a single-phase cascaded H-bridge (CHB) converter in the front end [5], [6] and several output-parallel dc–dc converters in the backward stage. The dc–dc converter is generally an *LLC* resonant converter (*LLC* RC) or a dual active bridge dc–dc (DAB) converter [7]–[12]. In order to further improve the modularization of the PETT equipment (for the convenience of manufacture, maintenance, and expansion), the PETT digital control system should be organized as a distributed control structure. The control structure can be separated into two layers. Among them, the top layer is the main-controller layer for the execution of PETT control algorithms, and the bottom layer is the slave-controller layer, in which each PETT cell has a slave controller, for the generation of driver signals and the collection of components' operation status. The information interaction between the main controller and each slave controller is realized through optical fibers [13]–[17]. In order to avoid the conflict of interrupts and the crowd with channels, there should be only one interrupt in the main controller [or more specifically, in the digital signal processor (DSP) or microcontrol unit of the main controller] to execute the control algorithms of the CHB and dc–dc converters [15]. In other words, the control frequency of the CHB is the same as the one of the dc–dc converters. It is different with [18]. In [18], the control frequencies of ac–dc converter and dc–dc converters are not the same, and there are two interrupts in the main controller to process the control algorithms of ac–dc converter and dc–dc converters. It may bring serious bad effect on the control performance, especially for DAB converters. For a single-core DSP, if there are several interrupts for control purpose in a DSP, the conflicts in time sequence between those interrupts cannot be avoided, which will disorder the control periods, make the sample abnormal, and postpone the effective time of control variables. In this case, in order to make the converters operate normally, it needs to significantly reduce the parameters of a closed-loop controller (for DABs, the authors find that the parameters used in the experiment are generally smaller than 1/30 of the ones

based on modeling and controller design). It will seriously influence the converters' dynamic control performance. What is worse, even when the controller parameters are reduced significantly, there is still small-amplitude low-frequency oscillation in the inductor current at some time. Therefore, in order to settle this problem completely, the control frequencies of the CHB and DAB converters should be the same.

For a DAB closed-loop control system, the influence of the conflict of interrupts and the crowd with channels can be regarded as some noise or random disturbance taking effect on the closed control loop equivalently. Noise is a key factor to restrict the development of the control performance of power electronic converters. And the DAB closed-loop control system is much more sensitive to the influence of noises. The essential reason is that the voltage fluctuation of the dc output voltage of the DAB converter is very small, and the gain cross-over frequency of the open-loop transfer function of the DAB converter is generally high. The detailed influence mechanism will be introduced in Section III. Several kinds of noises exist in the DAB closed-loop control system. According to the source of those noises, they can be divided into four categories:

1) Switching noise. There are some high-frequency components in the dc output voltage of DAB converters. If the sampling frequency of the dc output voltage is set to the same value as the control frequency, the mismatch between the sampling control frequency and the switching frequency may exist, and the high-frequency components (that is, switching noise) will be brought into the DAB closed-loop control system. With the impact of the switching noise, low-frequency oscillation will generate in the output control variable and the inductor current of DAB converters. Under this circumstance, on the one hand, large current peak may exist in the DAB inductor current, which will reduce the reliability of semiconductor power devices; on the other hand, the low-frequency oscillation may saturate medium-/high-frequency transformers, or produce some low-frequency vibration and noise of iron core.
2) Second-order voltage ripple in the dc input side of the DAB. As the CHB of a PETT is a single-phase ac–dc converter, there is a ripple on the dc output voltage in each CHB cell, which is also the dc input voltage of each DAB converter, at twice the line frequency [2]. Based on the research results in Section III, the second-order voltage ripple has a slight influence on DAB converters.
3) Quantization noise, including the noise generated from the quantization of sampled values in the analog-to-digital (A/D) converter, and the noise generated from the quantization of carrier waves and modulating waves in the digital pulse width modulation (DPWM) [19]–[22]. Strictly speaking, there are three categories of modulation techniques, including the pulse width modulation, the phase-shift modulation, and the variable switching-frequency modulation [33]. For the sake of denoting, they are all called as PWM in this paper. Sometimes, the quantization noise may result in the limit cycle oscillation (LCO) phenomenon. Its generation mechanism is introduced in [22], while its frequency and amplitude can be calculated based on the describing function method [20]. In order to eliminate the LCO, it is recommended to reduce the integral coefficient of the proportion-integral controller in [19], [20], and [22]. However, detailed analyses about the quantitative calculation of the integral coefficient and the influence of the proportion coefficient on the LCO are not presented in [19], [20], and [22]. What is worse, the dc–dc converters may suffer serious influence if the integral coefficient is greatly reduced. As for the quantization of DPWM, if the switching frequency is not so high and the DSP is configured properly, relatively high resolution of DPWM can be obtained and the DPWM quantization effect is quite slight [23], [31]. Besides, in [19], [20], and [22], it is believed that the LCO phenomenon generates from the synergistic effect of the A/D quantization process and the DPWM quantization process. However, as indicated in Section III, once the A/D quantization noise exists, even when the resolution of DPWM is infinitely high, the LCO still occurs.
4) Measurement noise generated from the transducers and conditioning circuits. As the measurement precision of transducers is not infinite [24] and the analog components of conditioning circuits are very sensitive to suffer influence of external temperature and humidity, there is an error between the real value and the sampled value; in other words, the noise or random disturbance exists. According to the generation mechanism and the statistical characteristic of this category of noises (in any two samples, they are uncorrelated, and any sequence has the same mean value), it can be described by the model of white wide-sense stationary (WSS) random signal [21]. If the variance of the measurement noise is very large, the control performance of power electronic converters may suffer the serious impact.

Besides, there are some other kinds of noises that are not presented in this paper, but sometime have serious impact on the control performance, such as the transient noise caused by an unsuitable modulating wave updating method [34] and the arithmetic noise caused by the finite word length [21], [22]. The recognition of noises is significant in practice, as some strange disorder or oscillation phenomena may occur under the noise effect, and they may be mistaken as some kind of instability problem caused by the inaccurate modeling or unsuitable designed controllers.

This paper is organized as follows. In Section II, the generation mechanism of the DAB switching noise is introduced, with the corresponding solution. On the basis of this switching noise suppression scheme, the sources of second-order voltage ripple, quantization noise, and measurement noise are analyzed, and the mechanism for those noises to deteriorate the control performance of DAB converters is presented in Section III. Before the above-mentioned elaboration, based on the corresponding physical significance, the mathematical models toward the sampling and the phase-shift modulation are derived, and the DAB small-signal model toward the output-voltage feedback control [25] is modified and simplified. In order to quantitatively mea-

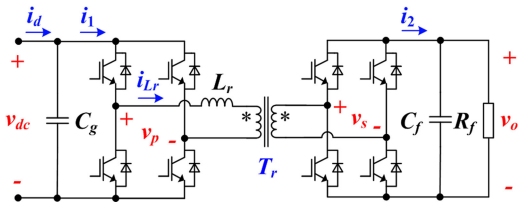

Fig. 1. Topology of a DAB converter.

sure the impact of noises on the DAB converters, a new variable is defined and named as noise attenuation coefficient (NAC) in this section. For the sake of understanding, the five-cell PETT laboratory prototype is taken as an instance, which will not restrict the application of the presented theoretical analysis. With the use of NAC, it is found that among those noises mentioned above, the impact of the measurement noise is the most serious, following the quantization noise and the second-order voltage ripple. Therefore, in the remaining part of Section III, the measurement noise is taken as an example to study the corresponding noise suppression scheme. It can be proved that the proposed noise suppression scheme is also suitable for the quantization noise, and the impact of the second-order voltage ripple can be neglected for DAB converters. In this section, the statistical model of the measurement noise and the method to obtain the model's parameters are presented as well. In Section IV, combining with the balance control strategy of the PETT [25], the multirate digital signal processing of the CHB (this part is introduced in detail in another paper), and the research results in the above-mentioned two sections, the PETT multirate control strategy is finally proposed. In this paper, the multirate concept means that the sampling frequency, control frequency, and modulating wave updating frequency can be separated from the switching frequency, and can be chosen as different values according to the practical requirements. In Section V, further research works are carried out based on a five-cell PETT laboratory prototype with a rated power of 30 kW. Conclusion and outlook are provided in Section VI.

II. Switching Noise and Corresponding Solution

A. Generation Mechanism of the Switching Noise

The topology of a DAB converter is shown in Fig. 1. C_g is the dc input capacitor, C_f is the dc output capacitor, L_r is the DAB storage inductor, T_r is the medium-/high-frequency transformer, and R_f is the equivalent load resistance. i_d is the dc input current of the DAB converter, i_1 is the input current of the DAB input H-bridge, i_{Lr} is the DAB inductor current, and i_2 is the output current of the DAB output H-bridge. $v_{\rm dc}$ is the dc input voltage, v_o is the dc output voltage, v_p is the midpoint voltage of the DAB input H-bridge, and v_s is the midpoint voltage of the DAB output H-bridge. Without the loss of generality, the turns ratio of T_r is set as $1:1$ in the following paper.

In this paper, a single-phase-shift modulation technique is adopted by DAB converters. The switching ripple contained in the dc output voltage v_o is bound up with the dc output current i_2

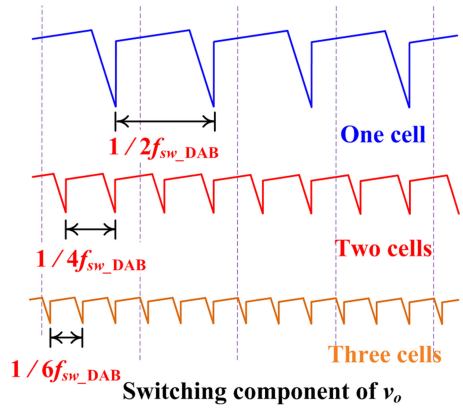

Fig. 2. DC output voltage waveforms of output-parallel DAB converters with the use of a carrier phase-shifting technique (or an interleaving technique).

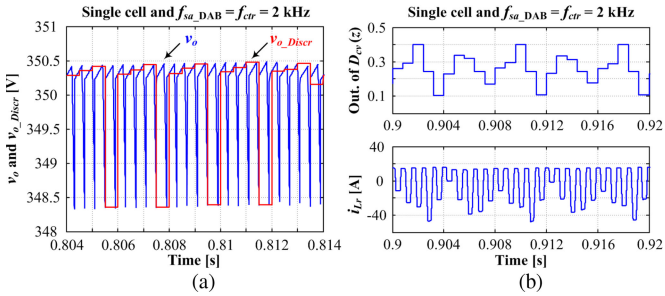

Fig. 3. Simulation waveforms of a single DAB converter, where the switching frequency is $f_{\rm sw\_DAB} = 1.25$ kHz, the sampling frequency is $f_{\rm sa\_DAB} = 2$ kHz, the control frequency is $f_{\rm ctr} = 2$ kHz, the PWM modulating wave updating frequency is $f_{\rm ud\_DAB} = 1.25$ kHz, and there are no measurement noise, A/D quantization noise, and second-order voltage ripple contained in the dc input voltage. (a) DC output voltage v_o and its sampled value $v_{o\_\rm Discr}$. (b) Output variable of the DAB's output-voltage controller $D_{\rm cv}(z)$ (top) and the DAB inductor current i_{Lr} (bottom).

[25], and its waveforms under different cell number are shown in Fig. 2.

Denote the switching frequency of the DAB as $f_{\rm sw\_DAB}$. As shown in Fig. 2, for a single DAB converter, the equivalent switching frequency of v_o is $2f_{\rm sw\_DAB}$; similarly, for N DAB converters whose dc output sides are in parallel, if the carrier phase-shifting technique (or an interleaving technique, where the carrier of *cell* $(j+1)$ is lagging behind the carrier of *cell* j by $\Delta t = T_{\rm sw\_DAB}/2N$. $T_{\rm sw\_DAB} = 1/f_{\rm sw\_DAB}$ and $j = 1, 2, \ldots, N-1$) is adopted, the equivalent switching frequency of v_o is $2Nf_{\rm sw\_DAB}$. Taking a single DAB converter as an instance, the influence of the mismatch between the sampling frequency and the switching frequency on the control system is analyzed as follows. The simulation waveforms of the real value and the sampled value of v_o are exhibited in Fig. 3(a). In the simulation, the switching frequency is $f_{\rm sw\_DAB} = 1.25$ kHz, the sampling frequency of v_o $(f_{\rm sa\_DAB})$ and the control frequency $(f_{\rm ctr})$ are all equal to 2 kHz, the PWM modulating wave updating frequency (also the frequency of PWM registers loading their new values) is $f_{\rm ud\_DAB} = 1.25$ kHz. Besides, there are no measurement noise, A/D quantization noise and second-order voltage ripple contained in the dc input voltage. As shown in Fig. 3(a), the sampled value of v_o, which is denoted as $v_{o\_\rm Discr}$, is

variable in different sampling times. In essence, this is a kind of aliasing phenomenon, where v_{o_Discr} contains the dc component and the distorted switching ripple [21], [22].

Through the sampling process, switching noise is brought into the DAB closed-loop control system and results in the cyclical oscillation in the output variable of the output-voltage controller $D_{\mathrm{cv}}(z)$ and the DAB inductor current i_{L_r}, as shown in Fig. 3(b). In this paper, a single voltage control loop is adopted and the parameters of $D_{\mathrm{cv}}(z)$ are the same expect particular explanation, no matter for the single DAB converter or for the output-parallel DAB converters. The control structure is shown in Figs. 7 and 16. And the output-voltage controller is

$$D_{\mathrm{cv}}(z) = K_{\mathrm{vp}}\left(1 + \frac{\omega_v}{2f_{\mathrm{ctr}}} \cdot \frac{1+z^{-1}}{1-z^{-1}}\right)$$

where $K_{\mathrm{vp}} = 0.0832$ and $\omega_v = 31.4159$.

B. Switching Noise Suppression

In order to deal with the switching noise problem, the corresponding solution is proposed as follows.

For N output-parallel DAB converters, the sampling frequency of v_o ($f_{\mathrm{sa\_DAB}}$) can be set as

$$f_{\mathrm{sa\_DAB}} = P_1 \times f_{\mathrm{sw\_DAB}} \text{ or } f_{\mathrm{sa\_DAB}} = P_2 \times 2N f_{\mathrm{sw\_DAB}} \quad (1)$$

where P_1 is the common divisor of $2N$ ($P_1 = 1, 2, \ldots, 2N$), and $P_2 = 2, 3, \ldots$. For example, when $N = 5$, $P_1 = 1, 2, 5, 10$, and $P_2 = 2, 3, 4, 5 \ldots$.

For the latter one of (1), where $f_{\mathrm{sa\_DAB}} > 2N f_{\mathrm{sw\_DAB}}$, the sampling value should be passed through a filter whose stopband edge frequency f_{s_DAB} is less than $2N f_{\mathrm{sw\_DAB}}$ (the physical meaning of stopband edge frequency f_{s_DAB} can be referenced in [21]) so that the switching ripple can be filtered. Besides, for the former one of (1), where $f_{\mathrm{sa\_DAB}} < 2N f_{\mathrm{sw\_DAB}}$, there is no need to filter the switching ripple. Although there is an error between the real dc component and the sampled one, it will not deteriorate the steady-state performance of DAB converters as the error is generally small.

When $f_{\mathrm{sa\_DAB}} > 2N f_{\mathrm{sw\_DAB}}$, if the sampling frequency and the control frequency are not the same, that is, $f_{\mathrm{sa\_DAB}} \neq f_{\mathrm{ctr}}$, frequency conversion after sampling is needed. In this case, only one filter is needed to filter the switching ripple and to convert the frequency at the same time. The stopband edge frequency f_{s_DAB} of that filter can be chosen as

$$f_{s\_\mathrm{DAB}} = \min\left(2N f_{\mathrm{sw\_DAB}}, 0.5 f_{\mathrm{ctr}}\right). \quad (2)$$

In another aspect, when $f_{\mathrm{sa\_DAB}} < 2N f_{\mathrm{sw\_DAB}}$, as the influence of aliasing in the sampling control frequency converting process is very small, an extra frequency conversion filter is unnecessary. In other words, it can directly convert the frequency after the sampling process. Detailed explanation will be exhibited in Section III.

Based on the above-mentioned switching noise suppression scheme, the simulation waveforms of a single DAB are shown in Fig. 4(a), while the simulation waveforms of five output-parallel DAB converters are shown in Fig. 4(b). In the simulation, the switching frequency is $f_{\mathrm{sw\_DAB}} = 1.25\,\mathrm{kHz}$, the sampling frequency is $f_{\mathrm{sa\_DAB}} = 2.5\,\mathrm{kHz}$, the control frequency is $f_{\mathrm{ctr}} = 2\,\mathrm{kHz}$, and the PWM modulating wave updating frequency is $f_{\mathrm{ud\_DAB}} = 1.25\,\mathrm{kHz}$. There is no filter in the sampling control frequency conversion, and there is no filter between the controller $D_{\mathrm{cv}}(z)$ and the PWM. Besides, there are no measurement noise, A/D quantization noise, and second-order voltage ripple. As shown in Fig. 4, no matter for the single DAB converter or for the five output-parallel DAB converters, the low-frequency oscillation of the output variable of $D_{\mathrm{cv}}(z)$ and the DAB inductor current i_{Lr} (or i_{Lrj}, $j = 1, 2, \ldots, 5$) is not obvious. Thus, based on the solution proposed above, it can effectively settle the DAB switching noise problem and improve the control performance of DAB converters.

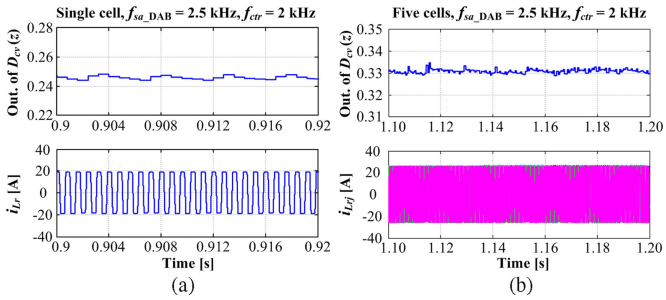

Fig. 4. Switching frequency is $f_{\mathrm{sw\_DAB}} = 1.25\,\mathrm{kHz}$, the sampling frequency is $f_{\mathrm{sa\_DAB}} = 2.5\,\mathrm{kHz}$, the control frequency is $f_{\mathrm{ctr}} = 2\,\mathrm{kHz}$, the PWM modulating wave updating frequency is $f_{\mathrm{ud\_DAB}} = 1.25\,\mathrm{kHz}$, and there are no measurement noise, A/D quantization noise, and second-order voltage ripple. (a) Simulation waveforms of a single DAB converter, the output variable of the DAB's voltage controller $D_{\mathrm{cv}}(z)$ (top) and the DAB inductor current i_{Lr} (bottom). (b) Simulation waveforms of the five output-parallel DAB converters, the output variable of the DAB's output-voltage controller $D_{\mathrm{cv}}(z)$ (top), and the DAB inductor current $i_{Lrj}, j = 1, 2, \ldots, 5$ (bottom).

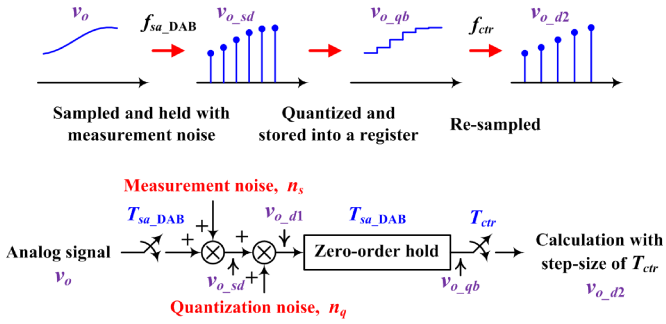

Fig. 5. Sampling process of the dc output voltage v_o (top) and its corresponding model (bottom).

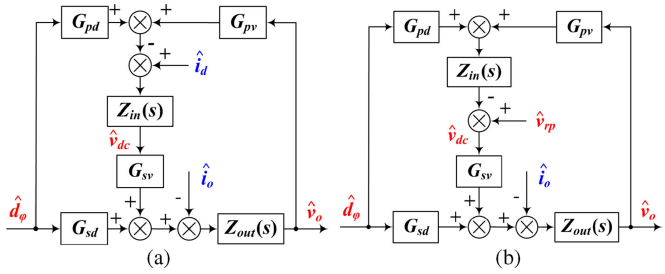

Fig. 6. Block diagram of the small-signal model of the DAB converter. (a) Original version in [25]. (b) Modified version in this paper.

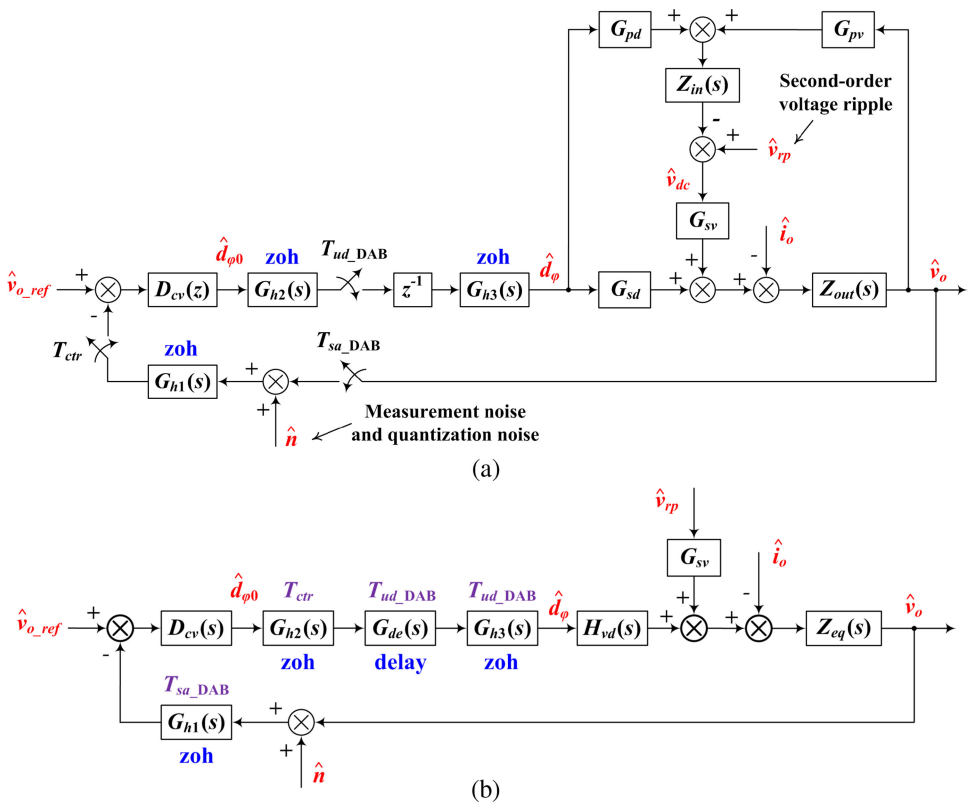

Fig. 7. Block diagram of the whole DAB output-voltage control loop without adopting frequency conversion filters. (a) Original version. (b) Simplified version.

III. Second-Order Voltage Ripple, Quantization Noise, and Measurement Noise

A. Overview

Similarly, the second-order voltage ripple in the dc input side, the noise due to the quantization process in the A/D converter (that is, quantization noise), and the noise due to the measuring error of transducers and conditioning circuits (that is, measurement noise) may result in the oscillation in the output variable of $D_{\rm cv}(z)$ and the DAB inductor current i_{Lrj}.

As the PETT is a single-phase ac–dc conversion equipment, there is a second-order voltage ripple in the intermediate dc-voltage side (that is, the dc input side of each DAB as well). It can be seen from the following analysis that although there is a certain impact of the second-order voltage ripple, it will not restrict the further improvement of DAB's control performance. In this point, the DAB is different with the *LLC* RC. The research result related to the *LLC* RC about similar problem is left to the future elaboration.

There is an interesting phenomenon. For the A/D converter, its resolution and conversion rate are approximately in an inverse proportional relationship [26]. In other words, if the resolution is high, the conversion rate is low, while if the conversion rate is high, the resolution is low. For example, for the integrated A/D module of DSP TMS320F28335 [23], the resolution is 12 bits and the conversion time is 80 ns; for some discrete A/D chips like ADS8364 [32], the resolution is 16 bits and the conversion time is 4 μs. In practical application, it is much more convenient to use the integrated A/D module because it can simplify the design of sampling circuits and the configuration of timing sequences. In this case, the effect of A/D quantization should be taken into consideration.

The measurement noise generated from the transducers and the conditioning circuits is similar to the quantization noise introduced below, because from the point of statistical characteristic, all of them can be described by the model of a zero-mean WSS random signal (that is, the white noise as well). The characteristic of the white noise is that in any two samples, they are uncorrelated; and any sequence has the same mean value (zero mean) and variance value. However, even though they can be modeled by the white noise, there is still an essential difference between them. The probability density function of the quantization noise is the uniform density function, and the variance of the A/D quantization noise can be calculated according to the measurement range of sampling circuits and the resolution of A/D converters [21]. Nevertheless, for the measurement noise, it is hard to choose a suitable probability density function and estimate its variance only by means of the technical parameters of transducers and conditioning circuits. According to [27] and [28], the measurement noise can be modeled like that: a white noise with the Gaussian density function passes through a digital filter and finally generates the measurement noise, where the variance of the white noise and the parameters of the digital filter can be calculated with the related data acquired in the experiment.

B. Mechanism to Deteriorate the Control Performance

The sampling process of the dc output voltage v_o and its corresponding model are exhibited in Fig. 5. The sampling frequency of v_o is $f_{\mathrm{sa\_DAB}}$, the control frequency of the DAB is f_{ctr}, and the switching frequency is $f_{\mathrm{sw\_DAB}}$. Here, the situation where $2Nf_{\mathrm{sw\_DAB}} > f_{\mathrm{sa\_DAB}} > f_{\mathrm{ctr}}$ is taken as an instance. N is the cell number of the PETT. It is provided that the sample-and-hold (S/H) circuit is ideal, that is, the period of S/H is infinitely small. After sampled and held with some measurement noise, the analog signal v_o is converted into the sampled data signal v_{o_sd} with continuous-amplitude and discrete-time characteristic. Then v_{o_sd} is quantized in amplitude and becomes the digital signal v_{o_d1} with discrete-amplitude and discrete-time characteristic. v_{o_d1} is first stored into a register and latter read for the use of control algorithms with a frequency of f_{ctr}. Then another digital signal v_{o_d2} is generated. As $f_{\mathrm{ctr}} \neq f_{\mathrm{sa\_DAB}}$, there is a zero-order-hold (ZOH) and resampling process from v_{o_d1} to v_{o_d2}. In other words, v_{o_d1} becomes the quantized boxcar signal v_{o_qb} with discrete-amplitude and continuous-time characteristic first, and then v_{o_qb} is resampled and becomes the digital signal v_{o_d2}. From the point of math, it can be considered that v_{o_qb} is generated from v_{o_d1} through ZOH [21]. In Fig. 5, n_s is the measurement noise, n_q is the quantization noise, $T_{\mathrm{sa\_DAB}} = 1/f_{\mathrm{sa\_DAB}}$, and $T_{\mathrm{ctr}} = 1/f_{\mathrm{ctr}}$.

According to [25], from the point of the output-voltage feedback control system, the output-parallel DAB converters can be equivalent to a single DAB converter. The small-signal models of them are the same and the corresponding block diagram is shown in Fig. 6(a). $\hat{v}_o$ is the small signal of the dc output voltage, $\hat{i}_o$ is the small signal of the load current, $\hat{d}_\varphi$ is the small signal of the phase-shift control variable, $\hat{i}_d$ is the small signal of the dc input current, $\hat{v}_{\mathrm{dc}}$ is the small signal of the dc input voltage, and $G_{\mathrm{pd}}, G_{\mathrm{pv}}, G_{\mathrm{sd}}, G_{\mathrm{sv}}, Z_{\mathrm{in}}(s), Z_{\mathrm{out}}(s)$ are the transfer functions. In order to analyze the influence of DAB's input-voltage disturbance on the closed-loop control system, the above-mentioned structure is modified and exhibited in Fig. 6(b), where $\hat{v}_{\mathrm{rp}}$ represents the input-voltage disturbance and $\hat{v}_{\mathrm{rp}} = Z_{\mathrm{in}}(s) \times \hat{i}_d$.

Synthesizing the above-mentioned analysis, the block diagram of the whole DAB output-voltage control loop can be obtained, as shown in Fig. 7(a). As the PWM modulating wave updating frequency is not equal to the control frequency, that is, $f_{\mathrm{ud\_DAB}} \neq f_{\mathrm{ctr}}$, similarly, there is still a ZOH and resampling process when updating the PWM modulating wave. More details about the selection of $f_{\mathrm{ud\_DAB}}$ will be presented in Section IV. Here, the effect of the ZOH is represented by $G_{h2}(s)$ whose dominant frequency is f_{ctr} (as shown below). As the double-register mode is adopted by the PWM modulating wave, the digital modulating wave after being resampled is stored into a shadow register, and then the stored value is loaded into the compare register with the frequency of $f_{\mathrm{ud\_DAB}}$. Therefore, from the digital modulating wave after being resampled to the digital signal once stored into the compare register, there is a delay of $T_{\mathrm{ud\_DAB}} = 1/f_{\mathrm{ud\_DAB}}$, which represents the quantization of the computation delay of control algorithms and the data transmission delay between the main controller and the slave controller, from the point of DAB converters. The signal in the compare register participates in the phase-shift modulation, which is a continuous-time signal. Therefore, the compare register represents another kind of ZOH effect, which is denoted by $G_{h3}(s)$ with the dominant frequency of $f_{\mathrm{ud\_DAB}}$. As shown in Fig. 7(a), the ZOH effect in the sampling process is represented by $G_{h1}(s)$ whose dominant frequency is $f_{\mathrm{sa\_DAB}}$, $\hat{n} = \hat{n}_s + \hat{n}_q$ represents the sum of the quantization noise and the measurement noise, $\hat{v}_{o\_\mathrm{ref}}$ is the small signal of the voltage reference, and $D_{\mathrm{cv}}(z)$ is the DAB voltage-closed-loop controller.

As there are multiple frequencies in the control loop and the ratio of each two of them is not an integer, it is not so convenient to carry out the research directly in the z-transform. Hence, at first, all the transfer functions in the z-transform are replaced with their corresponding ones in the s-transform, as shown in Fig. 7(b). Latter, for estimating the impact of $\hat{n}$, the control system will be represented in the z-transform again. In Fig. 7(b)

$$G_{\mathrm{de}}(s) = e^{-sT_{\mathrm{ud\_DAB}}},\ G_{h1}(s) = \frac{1 - e^{-sT_{\mathrm{sa\_DAB}}}}{sT_{\mathrm{sa\_DAB}}}$$

$$G_{h2}(s) = \frac{1 - e^{-sT_{\mathrm{ctr}}}}{sT_{\mathrm{ctr}}}, G_{h3}(s) = \frac{1 - e^{-sT_{\mathrm{ud\_DAB}}}}{sT_{\mathrm{ud\_DAB}}}.$$

Technically speaking, the ZOH shown in Fig. 7(a) and (b) is not the same, and there is some difference in the amplitude between them. Here, for the convenience of representation, the same symbols are used in the following paper without causing confusion. Besides

$$Z_{\mathrm{eq}}(s) = \frac{Z_{\mathrm{out}}(s)}{1 + G_{\mathrm{sv}}G_{\mathrm{pv}}Z_{\mathrm{in}}(s)Z_{\mathrm{out}}(s)}$$

$$H_{\mathrm{vd}}(s) = G_{\mathrm{sd}} - G_{\mathrm{sv}}G_{\mathrm{pd}}Z_{\mathrm{in}}(s).$$

Denote the open-loop transfer function as

$$L_{\mathrm{vdab}}(s) = G_{h1}(s)D_{\mathrm{cv}}(s)G_{h2}(s)G_{\mathrm{de}}(s)G_{h3}(s)H_{\mathrm{vd}}(s)Z_{\mathrm{eq}}(s). \tag{3}$$

From Fig. 7(b), the transfer function from $\hat{n}$ to $\hat{d}_{\varphi 0}$ and the transfer function from $\hat{v}_{\mathrm{rp}}$ to $\hat{d}_{\varphi 0}$ can be derived as

$$\left.\frac{\hat{d}_{\varphi 0}}{\hat{n}}\right|_{\hat{v}_{o,\mathrm{ref}}=0,\ \hat{i}_o=0,\hat{v}_{\mathrm{rp}}=0} = \frac{G_{h1}(s)D_{\mathrm{cv}}(s)}{1 + L_{\mathrm{vdab}}(s)} \triangleq H_{D\varphi\_\mathrm{Noise}}(s) \tag{4}$$

$$\left.\frac{\hat{d}_{\varphi 0}}{\hat{v}_{\mathrm{rp}}}\right|_{\hat{v}_{o,\mathrm{ref}}=0,\ \hat{i}_o=0,\hat{n}=0} = \frac{G_{\mathrm{sv}}(s)Z_{\mathrm{eq}}(s)G_{h1}(s)D_{\mathrm{cv}}(s)}{1 + L_{\mathrm{vdab}}(s)} \triangleq H_{D\varphi\_V\mathrm{rp}}(s). \tag{5}$$

The DAB voltage-closed-loop controller is $D_{\mathrm{cv}}(s) = K_{\mathrm{vp}}(1 + \omega_v/s)$, where $K_{\mathrm{vp}} = 0.0832$ and $\omega_v = 31.4159$. The frequency response of $L_{\mathrm{vdab}}(s)$ is shown in Fig. 8. Its gain cross-over frequency is $f_{\mathrm{cv}} = 52.1$ Hz, its phase margin is $\mathrm{PM}_v = 56.1°$, and its gain margin is $\mathrm{GM}_v = 9.5$ dB. The DAB voltage-closed-loop control system is stable.

The frequency response of $H_{D\varphi\_V\mathrm{rp}}(s)$ is shown in Fig. 9(a). The amplitude of $H_{D\varphi\_V\mathrm{rp}}(s)$ in 100 Hz is -56.1 dB. Taking the

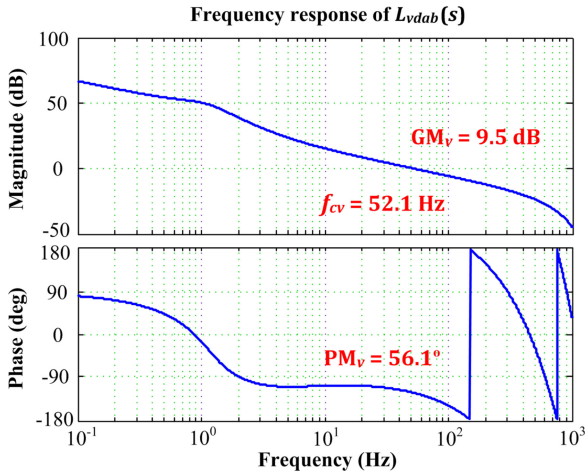

Fig. 8. Frequency response of $L_{\mathrm{vdab}}(s)$.

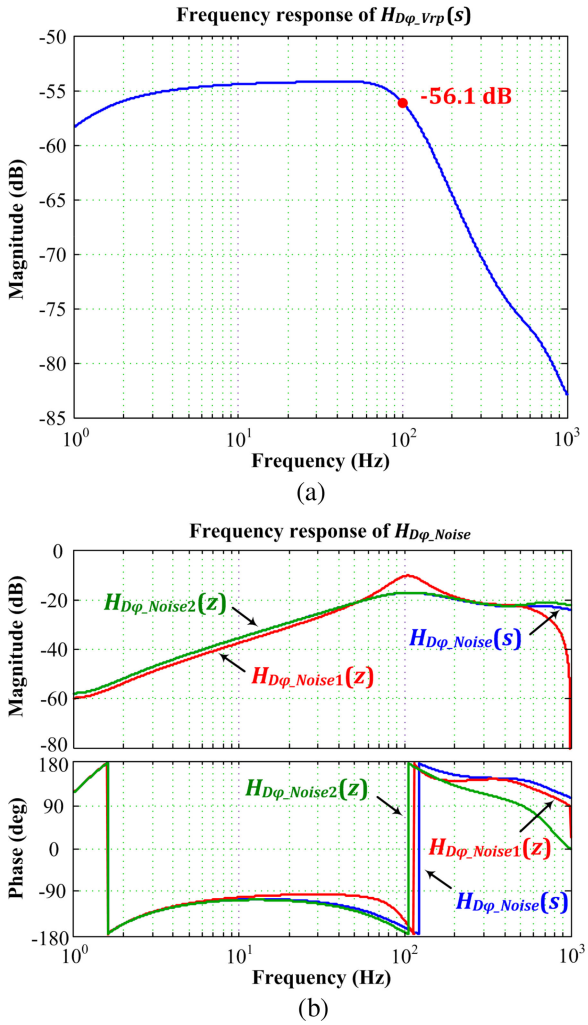

Fig. 9. Parameters of $D_{\mathrm{cv}}(z)$ are chosen as $K_{\mathrm{vp}} = 0.0832$ and $\omega_v = 31.4159$: (a) the frequency response of $H_{D\varphi\_V\mathrm{rp}}(s)$ and (b) the frequency response of $H_{D\varphi\_\mathrm{Noise}}(s)$, $H_{D\varphi\_\mathrm{Noise1}}(z)$, and $H_{D\varphi\_\mathrm{Noise2}}(z)$.

five-cell PETT laboratory prototype as an instance, the amplitude of the second-order voltage component in the intermediate-dc-voltage side is [29]

$$V_{\mathrm{dc\_2nd\_max}} = \frac{P^*_{\mathrm{cell}}}{2\omega_g C^*_g V^*_{\mathrm{dc}}} = 4.0123\,\mathrm{V}$$

where P^*_{cell} is the rated power of each PETT cell, $\omega_g = 2\pi \times 50$ rad/s, C^*_g is the rated value of the intermediate dc capacitance of each PETT cell, and V^*_{dc} is the rated value of the intermediate dc voltage of each PETT cell. In this example

$$P^*_{\mathrm{cell}} = 6\,\mathrm{kW},\ C^*_g = 6.8\,\mathrm{mF},\ V^*_{\mathrm{dc}} = 350\,\mathrm{V}$$

and $(V_{\mathrm{dc\_2nd\_max}}/V^*_{\mathrm{dc}})\% = 1.146\%$.

Therefore, the amplitude of the second-order component of $d_{\varphi 0}$, which is the output variable of $D_{\mathrm{cv}}(s)$, is

$$4.0123 \times 10^{-56.1/20} = 6.3591 \times 10^{-3}.$$

Then the variance of the second-order ripple of $d_{\varphi 0}$ can be derived as [28]

$$\sigma^2_{D\varphi\_\mathrm{rp}} = \frac{\left(6.3591 \times 10^{-3}\right)^2}{2} = 2.0219 \times 10^{-5}.$$

The frequency response of $H_{D\varphi\_\mathrm{Noise}}(s)$ is shown in Fig. 9(b). In order to quantitatively analyze the influence of the quantization noise and the measurement noise on $d_{\varphi 0}$, it is needed to discretize $H_{D\varphi\_\mathrm{Noise}}(s)$. Through the Tustin transform (which is also known as the trapezoidal integration based z-transform [22]), $H_{D\varphi\_\mathrm{Noise}}(s)$ is discretized to $H_{D\varphi\_\mathrm{Noise1}}(z)$. The frequency response of $H_{D\varphi\_\mathrm{Noise1}}(z)$ is shown in Fig. 9(b). It can be found that there is large distinction between $H_{D\varphi\_\mathrm{Noise1}}(z)$ and $H_{D\varphi\_\mathrm{Noise}}(s)$. Therefore, it is inappropriate to discretize $H_{D\varphi\_\mathrm{Noise}}(s)$ directly through the Tustin transform. Considering the location of sampling switches in Fig. 7(a), there is

$$\begin{aligned} &L_{\mathrm{vdab}}(s) \\ &= D_{\mathrm{cv}}(s)\, G_{h2}(s)\, G_{h1}(s)\, G_{\mathrm{de}}(s)\, G_{h3}(s)\, H_{\mathrm{vd}}(s)\, Z_{\mathrm{eq}}(s) \\ &\approx D_{\mathrm{cv}}(s) G_{h2}(s)\left[e^{-s(0.5T_{\mathrm{sa\_DAB}}+1.5T_{\mathrm{ud\_DAB}})} H_{\mathrm{vd}}(s)\, Z_{\mathrm{eq}}(s)\right]. \end{aligned} \tag{6}$$

Denote

$$P_{\mathrm{vdab}}(s) = e^{-s(0.5T_{\mathrm{sa\_DAB}}+1.5T_{\mathrm{ud\_DAB}})} \times H_{\mathrm{vd}}(s)\, Z_{\mathrm{eq}}(s). \tag{7}$$

Considering the ZOH effect of $G_{h2}(s)$, it can be obtained as

$$P_{\mathrm{vdab}}(z) = \left(1 - z^{-1}\right) \cdot \mathrm{Z}\left\{\mathrm{L}^{-1}\left(\frac{1}{\mathrm{s}} \cdot \mathrm{P}_{\mathrm{vdab}}(\mathrm{s})\right)\right\} \tag{8}$$

where the dominant frequency is f_{ctr}, that is, $z = e^{sT_{\mathrm{ctr}}}$.

$D_{\mathrm{cv}}(z)$ is obtained by discretizing $D_{\mathrm{cv}}(s)$ through the Tustin transform. Then

$$L_{\mathrm{vdab}}(z) = D_{\mathrm{cv}}(z) \times P_{\mathrm{vdab}}(z). \tag{9}$$

Hence, the discretization form of $H_{D\varphi\_\mathrm{Noise}}(s)$ is shown as

$$H_{D\varphi\_\mathrm{Noise2}}(z) = \frac{z^{-1} D_{\mathrm{cv}}(z)}{1 + L_{\mathrm{vdab}}(z)}. \tag{10}$$

In order to make the amplitude–frequency characteristic of $H_{D\varphi\_\mathrm{Noise2}}(z)$ nearly the same as the one of $H_{D\varphi\_\mathrm{Noise}}(s)$, $G_{h1}(s)$ is replaced by z^{-1}, as indicated in (10). For Fig. 9(b), in the low-frequency section, the amplitude–frequency characteristic of $H_{D\varphi\_\mathrm{Noise2}}(z)$ and $H_{D\varphi\_\mathrm{Noise}}(s)$ is almost the same, while in the high-frequency section, the amplitude of $H_{D\varphi\_\mathrm{Noise2}}(z)$ is a little larger than the one of $H_{D\varphi\_\mathrm{Noise}}(s)$. From the following analysis, we will find that it will make the calculated NAC a little larger than the real one. Besides, as in the following analysis, the information about the phase-frequency characteristic is not necessary, there is nothing bad effect for the phase mismatch in the high-frequency section.

Denote the variance of the measurement noise and the quantization noise in the sampling process as σ_{Ns}^2 and σ_{Nq}^2, respectively. Denote the variance of the ripple contained in $d_{\varphi 0}$ due to the measurement noise as $\sigma_{D\varphi\_Ns}^2$, and denote the variance of the ripple contained in $d_{\varphi 0}$ due to the quantization noise as $\sigma_{D\varphi\_Nq}^2$. According to [21]

$$\frac{\sigma_{D\varphi_{Ns}}^2}{\sigma_{Ns}^2} = \frac{\sigma_{D\varphi_{Nq}}^2}{\sigma_{Nq}^2} = \frac{2}{f_{\mathrm{ctr}}}\int_0^{f_{\mathrm{ctr}}/2} \left|H_{D\varphi\_\mathrm{Noise2}}\left(e^{jf}\right)\right|^2 df \triangleq \mathrm{NAC} \quad (11)$$

where NAC is the noise attenuation coefficient. By means of MATLAB, it can be calculated that $\mathrm{NAC} = 0.007959$. For the example of this paper, the dc-output-voltage sampling range of the signal conditioning circuits is -468.57 to $+468.57$ V and the resolution of the A/D converters is 12 bits. Then

$$\sigma_{Nq}^2 = \frac{1}{12} \times \left(\frac{2 \times 468.57}{2^{12}-1}\right)^2 = 4.3644 \times 10^{-3}.$$

Therefore

$$\sigma_{D\varphi\_Nq}^2 = \sigma_{Nq}^2 \times \mathrm{NAC} = 3.4736 \times 10^{-5}.$$

Based on the data acquired from the experiment shown in Section III-D, it can be estimated that the variance of the measurement noise is $\sigma_{Ns}^2 = 0.2614$. Then

$$\sigma_{D\varphi\_Ns}^2 = \sigma_{Ns}^2 \times \mathrm{NAC} = 2.080 \times 10^{-3}.$$

It can be observed that

$$\sigma_{D\varphi\_Ns}^2 \gg \sigma_{D\varphi\_Nq}^2 > \sigma_{D\varphi\_\mathrm{rp}}^2.$$

In other words, the influence of the measurement noise on DAB converters is the strongest, followed by the quantization noise and the second-order voltage ripple. It should be noticed that the impact strength of the second-order voltage ripple is essentially up to the value of $(V_{\mathrm{dc\_2nd\_max}}/V_{\mathrm{dc}}^*)\%$. However, even when a very large value of $(V_{\mathrm{dc\_2nd\_max}}/V_{\mathrm{dc}}^*)\%$ is selected, such as 10%, the impact of the second-order voltage ripple on DAB converters is still finite. Because the second-order voltage ripple is different with the quantization noise and the measurement noise. For the former one, the waveform is smooth without any sharp points (or singularities) and the energy is concentrated on the frequency of 100 Hz, so that the variation range of the second-order component of $d_{\varphi 0}$ is not so large.

In order to more intuitively observe the influence of noises on DAB converters, three different groups of simulation based on the five-cell PETT laboratory prototype are provided, as shown in Fig. 10. In the simulation, $f_{\mathrm{ctr}} = 2$ kHz, $f_{\mathrm{sa\_DAB}} = 2.5$ kHz, and $f_{\mathrm{ud\_DAB}} = 1.25$ kHz. There is no filter in the sampling control frequency conversion, and there is no filter between the controller $D_{\mathrm{cv}}(z)$ and the PWM. The parameters of $D_{\mathrm{cv}}(z)$ are $K_{\mathrm{vp}} = 0.0832$ and $\omega_v = 31.4159$. In the first group, there are A/D quantization noise and second-order voltage ripple in the dc input side, and there is no measurement noise. The simulation waveforms of $d_{\varphi 0}$ (the output variable of $D_{\mathrm{cv}}(z)$) and i_{Lrj} $(j = 1, 2, \ldots, 5)$ are shown in Fig. 10(a). It can be found that the low-frequency oscillation or LCO phenomenon exists in $d_{\varphi 0}$ and i_{Lrj} [19], [20], [22], and the maximum absolute value of i_{Lrj} is 28.93 A. As $\sigma_{D\varphi\_Nq}^2 > \sigma_{D\varphi\_\mathrm{rp}}^2$, the quantization noise may play the leading role, and therefore, the second-order ripple of $d_{\varphi 0}$ is not obvious in Fig. 10(a). In the second group, there is a second-order voltage ripple in the dc input side, and there is no A/D quantization noise and measurement noise. The simulation waveforms of $d_{\varphi 0}$ and i_{Lrj} are shown in Fig. 10(b). It can be found that the second-order ripple exists in $d_{\varphi 0}$ and i_{Lrj}, and the maximum absolute value of i_{Lrj} is 26.74 A. In the third group, there are measurement noise and second-order voltage ripple in the dc input side, and there is no A/D quantization noise. The simulation waveforms of $d_{\varphi 0}$ and i_{Lrj} are shown in Fig. 10(c). The statistical model of the measurement noise, which is adopted in the third group of simulation, is based on the autoregressive (AR) model and by use of the experimental data. Related presentation will be shown in the following part. As shown in Fig. 10(c), the oscillation in $d_{\varphi 0}$ and i_{Lrj} is quite strong and emerges without periodicity. The maximum absolute value of i_{Lrj} is 45.22 A. It is indicated from the above-mentioned simulation results that the influence of the measurement noise on DAB converters is the strongest and the most obvious, which is consistent with the above-mentioned theoretical analysis. As the impact of the measurement noise is much stronger than that of the A/D quantization noise and the second-order voltage ripple, for the sake of simplifying analyses, the measurement noise is taken as an instance to present the noise suppression scheme in the following paper.

C. Noise Suppression

In order to deal with the issue of measurement noise, two different kinds of solutions are proposed in this paper:

First, it is recommended to choose a higher sampling frequency of v_o ($f_{\mathrm{sa\_DAB}}$) to obtain high-frequency sampling data, and the high-frequency signal is filtered, decimated, and downsampled to the final generating signal with the frequency of f_{ctr} (the control frequency). Here, the filter plays two roles. On the one hand, it filters the measurement noise in the high-frequency section and lowers down the variance of the measurement noise [21]; on the other hand, it acts as a frequency conversion filter and avoids the aliasing after decimation. When $f_{\mathrm{sa\_DAB}} > 2N f_{\mathrm{sw\_DAB}}$, the filter also has the function to filter the switching noise of v_o.

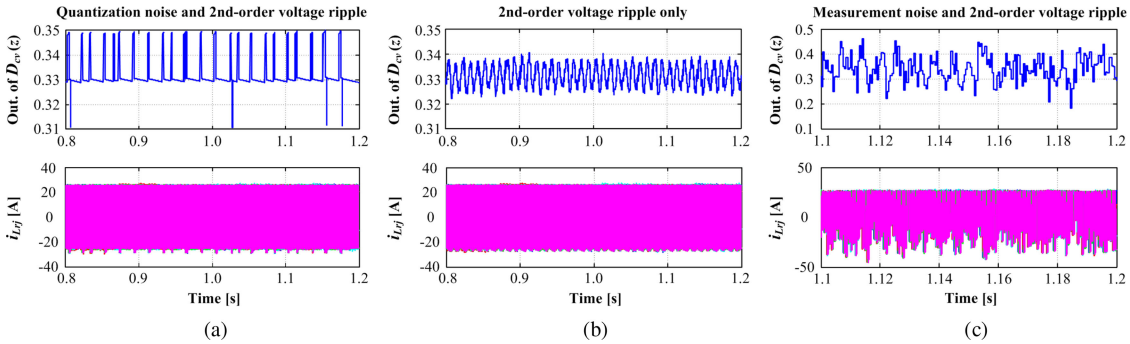

Fig. 10. Simulation waveforms of the five output-parallel DAB converters, the output variable of the (top) DAB's output-voltage controller $D_{\rm cv}(z)$ (top), and (bottom) the DAB inductor current $i_{Lrj}, j = 1, 2, \ldots, 5$ (bottom). (a) A/D quantization noise and the second-order voltage ripple exist, but the measurement noise does not exist. (b) Second-order voltage ripple exists, but the A/D quantization noise and the measurement noise do not exist. (c) Measurement noise and the second-order voltage ripple exist, but the A/D quantization noise does not exist.

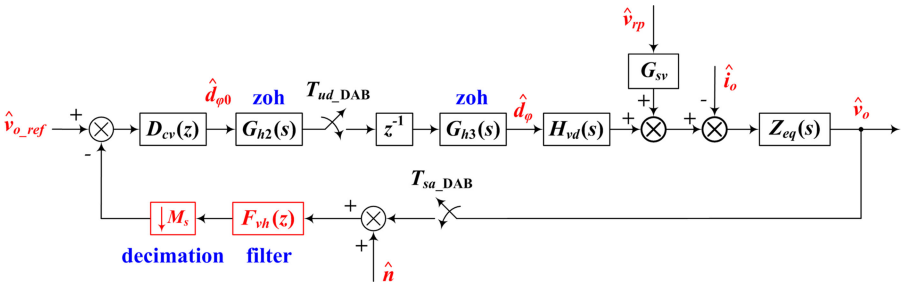

Fig. 11. Block diagram of the whole DAB output-voltage control loop with adopting the frequency conversion filter.

Second, it can adjust the parameters of $D_{\rm cv}(z)$ (the output-voltage closed-loop controller) to reduce the impact of the measurement noise.

The above-mentioned two solutions will be presented in the following paper.

1) Improving the Sampling Frequency: In this scheme, the attenuation of measurement noise is rated to the value of sampling frequency $f_{\rm sa\_DAB}$. In order to acquire the selection basis of $f_{\rm sa\_DAB}$, the quantitative relationship between NAC and $f_{\rm sa\_DAB}$ is derived. The block diagram of the DAB multirate closed-loop control system including the frequency conversion filter $F_{\rm vh}(z)$ is shown in Fig. 11. $f_{\rm sa\_DAB} = M_s f_{\rm ctr}$. The transfer functions of the frequency conversion filter in the dominant frequencies of $f_{\rm sa\_DAB}$ and $f_{\rm ctr}$ are $F_{\rm vh}(z)$ and $F_{\rm vl}(z)$, respectively.

$F_{\rm vh}(z)$ is an equiripple minimum-phase finite-impulse-response (FIR) filter (its design procedure is introduced in detail in another paper). The frequency response of $F_{\rm vh}(z)$ is shown in Fig. 12(a). It can be seen that the phase lag of $F_{\rm vh}(z)$ in the frequency section of $0 - 100$ Hz is very small. It is indicated that the influence of $F_{\rm vh}(z)$ on the dynamic response and the system stability is very small. That is why the minimum-phase filter is adopted for this application. In order to calculate the value of NAC, it is needed to derive the expression of $F_{\rm vl}(z)$. Denote $F_{\rm vh}(z) = a_0 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_n z^{-n}$, where the dominant frequency is $f_{\rm sa\_DAB}$ (that is, $z = e^{sT_{\rm sa\_DAB}}$). By means of the polyphase decomposition technique [21], (12) is acquired at the bottom of this page, where

$$\begin{aligned} E_{\rm vh0}\left(z^{-1}\right) &= a_0 + a_{M_s} z^{-1} + a_{2M_s} z^{-2} + \cdots \\ E_{\rm vh1}\left(z^{-1}\right) &= a_1 + a_{M_s+1} z^{-1} + a_{2M_s+1} z^{-2} + \cdots \\ &\vdots \\ E_{{\rm vh}(M_s-1)}\left(z^{-1}\right) &= a_{M_s-1} + a_{2M_s-1} z^{-1} + a_{3M_s-1} z^{-2} + \cdots \end{aligned}$$

$$\begin{aligned} F_{\rm vh}(z) &= \left(a_0 + a_{M_s} z^{-M_s} + a_{2M_s} z^{-2M_s} + \cdots\right) + \left(a_1 z^{-1} + a_{M_s+1} z^{-(M_s+1)} + a_{2M_s+1} z^{-(2M_s+1)} + \cdots\right) + \cdots \\ &\quad + \left(a_{M_s-1} z^{-(M_s-1)} + a_{2M_s-1} z^{-(2M_s-1)} + a_{3M_s-1} z^{-(3M_s-1)} + \cdots\right) \\ &= \left(a_0 + a_{M_s} z^{-M_s} + a_{2M_s} z^{-2M_s} + \cdots\right) + z^{-1}\left(a_1 + a_{M_s+1} z^{-M_s} + a_{2M_s+1} z^{-2M_s} + \cdots\right) + \cdots \\ &\quad + z^{-(M_s-1)}\left(a_{M_s-1} + a_{2M_s-1} z^{-M_s} + a_{3M_s-1} z^{-2M_s} + \cdots\right) \\ &\triangleq E_{\rm vh0}\left(z^{-M_s}\right) + z^{-1} E_{\rm vh1}\left(z^{-M_s}\right) + \cdots + z^{-(M_s-1)} E_{{\rm vh}(M_s-1)}\left(z^{-M_s}\right) \end{aligned} \tag{12}$$

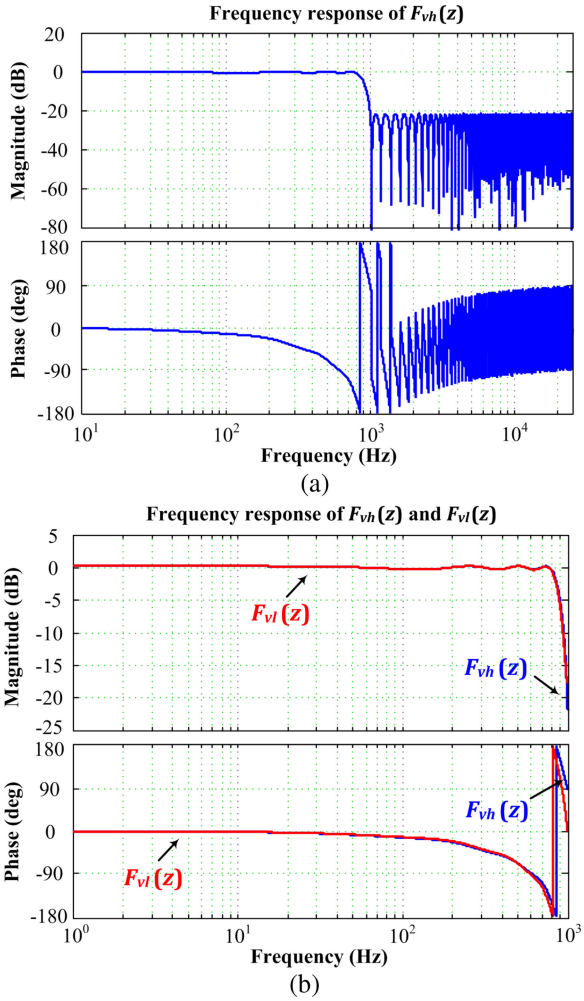

Fig. 12. Frequency response of the frequency conversion filter: (a) $F_{\mathrm{vh}}(z)$ in the frequency section below $0.5f_{\mathrm{sa\_DAB}}$ and (b) $F_{\mathrm{vh}}(z)$ and $F_{\mathrm{vh}}(z)$ in the frequency section below $0.5f_{\mathrm{ctr}}$.

Then

$$F_{\mathrm{vh}}\left(z^{\frac{1}{M_s}}\right) = E_{\mathrm{vh0}}\left(z^{-1}\right) + z^{-\frac{1}{M_s}} E_{\mathrm{vh1}}\left(z^{-1}\right) + \cdots + z^{-\frac{(M_s-1)}{M_s}} E_{\mathrm{vh}(M_s-1)}\left(z^{-1}\right). \tag{13}$$

In this paper, the first-order all-pass filter is used to replace z^{-k/M_s}, $k = 1, 2, \ldots, (M_s - 1)$. The reason of using the first-order all-pass filter is that its gain is identically equal to 1 and there is only one parameter needed to adjust to change its phase-frequency characteristic. For the control system with $f_{\mathrm{ctr}} = 2 - 3$ kHz, the gain cross-over frequency of the DAB open-loop transfer function is generally less than 200 Hz. Hence, before and after replacing, the phase-frequency characteristic in the frequency section below 200 Hz should be almost the same.

Denote

$$F_{\mathrm{vl}}(z) = E_{\mathrm{vh0}}\left(z^{-1}\right) + \mathcal{A}_1^1\left(z^{-1}\right) E_{\mathrm{vh1}}\left(z^{-1}\right) + \cdots + \mathcal{A}_1^k\left(z^{-1}\right) E_{\mathrm{vh}k}\left(z^{-1}\right) + \cdots + \mathcal{A}_1^{(M_s-1)}\left(z^{-1}\right) E_{\mathrm{vh}(M_s-1)}\left(z^{-1}\right) \tag{14}$$

where

$$\mathcal{A}_1^k\left(z^{-1}\right) = \frac{d_k + z^{-1}}{1 + d_k z^{-1}} \tag{15}$$

is the all-pass filter whose dominant frequency is f_{ctr}. The dominant frequency $F_{\mathrm{vl}}(z)$ is f_{ctr} as well, where $z = e^{sT_{\mathrm{ctr}}}$. Then

$$\mathcal{A}_1^k\left(e^{j\theta}\right) = \frac{d_k + \cos\theta - j\sin\theta}{1 + d_k\cos\theta - jd_k\sin\theta}$$

$$\angle\mathcal{A}_1^k\left(e^{j\theta}\right) = \tan^{-1}\frac{\left(d_k^2 - 1\right)\times\sin\theta}{2d_k + \left(1 + d_k^2\right)\times\cos\theta}.$$

Denote

$$\angle\mathcal{A}_1^k\left(e^{j\theta}\right) = -\frac{k}{M}\theta$$

and combining the above-mentioned equations, a quadratic equation with one unknown value of d_1 can be derived as

$$\left(\tan\left(\frac{k}{M}\theta\right)\cos\theta + \sin\theta\right) d_1^2 + 2\tan\left(\frac{k}{M}\theta\right) d_1 + \left(\tan\left(\frac{k}{M}\theta\right)\cos\theta - \sin\theta\right) = 0. \tag{16}$$

Denote

$$\theta = 2\pi\frac{(80 - 90)\,\mathrm{Hz}}{f_{\mathrm{ctr}}}.$$

Thus, the value of d_1 can be calculated and then $\mathcal{A}_1^k(z^{-1})$ and $F_{\mathrm{vl}}(z)$ can be obtained. The frequency response of $F_{\mathrm{vl}}(z)$ and $F_{\mathrm{vh}}(z)$ is shown in Fig. 12(b). It is indicated that the proposed method is effective and the phase difference between $F_{\mathrm{vl}}(z)$ and $F_{\mathrm{vh}}(z)$ is very small, especially in the frequency section below 200 Hz.

For the sake of analysis and calculation, the effect of $F_{\mathrm{vh}}(z)$ on the measurement noise is separated into two parts, including the part in the frequency of $0.5f_{\mathrm{ctr}} - 0.5f_{\mathrm{sa\_DAB}}$ and the part in the frequency of $0 - 0.5f_{\mathrm{ctr}}$. For the former one, as the impact of the DAB voltage-closed-loop control system is not beyond $0.5f_{\mathrm{ctr}}$, $F_{\mathrm{vh}}(z)$ attenuates the measurement noise with an open-loop control structure. However, for the latter one, the effect of the DAB voltage-closed-loop control system on the measurement noise should be taken into consideration, where the frequency conversion filter is $F_{\mathrm{vl}}(z)$. Then, similar to the above-mentioned derivation

$$H_{D\varphi\_\mathrm{Noise}}(z) = \frac{F_{\mathrm{vl}}(z)\,D_{\mathrm{cv}}(z)}{1 + L'_{\mathrm{vdab}}(z)} \tag{17}$$

where

$$L'_{\mathrm{vdab}}(z) = F_{\mathrm{vl}}(z) \times D_{\mathrm{cv}}(z) \times P'_{\mathrm{vdab}}(z)$$

$$P'_{\mathrm{vdab}}(z) = \left(1 - z^{-1}\right)\cdot \mathrm{Z}\left\{\mathrm{L}^{-1}\left(\frac{1}{\mathrm{s}}\cdot \mathrm{P}'_{\mathrm{vdab}}(\mathrm{s})\right)\right\}$$

$$P'_{\mathrm{vdab}}(s) = e^{-s\cdot 1.5T_{\mathrm{ud\_DAB}}} \times H_{\mathrm{vd}}(s)\,Z_{\mathrm{eq}}(s).$$

Then, the NAC can be calculated as

$$\mathrm{NAC} = \frac{\sigma^2_{D\varphi_{Ns}}}{\sigma^2_{Ns}} = \left[\frac{2}{f_{\mathrm{ctr}}}\int_0^{f_{\mathrm{ctr}}/2}\left|H_{D\varphi_{\mathrm{Noise}}}\left(e^{jf}\right)\right|^2 df\right] \times \left[\frac{2}{f_{\mathrm{sa\_DAB}} - f_{\mathrm{ctr}}}\int_{f_{\mathrm{ctr}}/2}^{f_{\mathrm{sa\_DAB}}/2}\left|F_{\mathrm{vh}}\left(e^{jf}\right)\right|^2 df\right]. \tag{18}$$

In the practical use, it is needed to estimate the variance of the measurement noise (σ^2_{Ns}) according to the experimental data. And then through the simulation or experiment, the maximum allowed value of $\sigma^2_{D\varphi\_Ns}$ is estimated as well, which can maintain the normal operation of the closed-loop control system. Hence, the maximum upper limit value of NAC, which is denoted as NAC_Max, can be calculated. Then, choose a suitable value of $f_{\mathrm{sa\_DAB}}$ to make NAC less than NAC_Max. For the example shown in this paper, the authors find that when $\sigma^2_{D\varphi\_Ns} < 1\times10^{-4}$, the oscillation of i_{Lrj} (the DAB inductor currents) is relatively small and there is no large current-peak value of i_{Lrj} in the steady state. Therefore, $\mathrm{NAC\_Max} = 3.826\times10^{-4}$. Then, $M_s = 25$ and $f_{\mathrm{sa\_DAB}} = 50$ kHz are chosen. In this case, $\mathrm{NAC} = 3.482\times10^{-4}$.

2) Adjusting the Parameters of the Output-Voltage Closed-Loop Controller: In this scheme, very high value of sampling frequency with the corresponding frequency conversion filter is not necessary. The related control structure diagram is shown in Fig. 7. The relationship between NAC and $D_{\mathrm{cv}}(z)$ has been derived and presented above. In the practical use, it can operate like that: at the beginning, in spite of the noise issue, the controller $D_{\mathrm{cv}}(z)$ is designed and its parameters (such as K_{vp} and ω_v) are selected just according to the indexes like gain cross-over frequency, phase margin, and gain margin; and then based on the designed controller, the value of NAC is calculated; if NAC > NAC_Max, the values of K_{vp} and ω_v should be reduced until NAC < NAC_Max. For the sake of comparison, three experiment groups (EG) are set up as follows.

EG-1st: the frequency conversion filter is adopted and $f_{\mathrm{sa\_DAB}} = 50$ kHz, $K_{\mathrm{vp}} = 0.0832$, and $\omega_v = 31.4159$.

EG-2nd: the frequency conversion filter is not adopted and $f_{\mathrm{sa\_DAB}} = 2.5$ kHz, $K_{\mathrm{vp}} = 0.03589$, and $\omega_v = 18.84956$.

EG-3rd: the frequency conversion filter is not adopted and $f_{\mathrm{sa\_DAB}} = 2.5$ kHz, $K_{\mathrm{vp}} = 0.0182$, and $\omega_v = 6.2832$.

The frequency response of $H_{D\varphi\_\mathrm{Noise}}(z)$ (or $H_{D\varphi\_\mathrm{Noise2}}(z)$) of these three EGs is shown in Fig. 13. As shown in Fig. 13, for the gain of $H_{D\varphi\_\mathrm{Noise}}(z)$, in the frequency of 1 Hz to 1 kHz, EG-3rd < EG-2nd < EG-1st. For EG-1st, the value of NAC is reduced mainly due to the large attenuation of the frequency conversion filter in the high-frequency section (>1 kHz) and the contribution of $H_{D\varphi\_\mathrm{Noise}}(z)$ is finite. For EG-2nd and EG-3rd, the value of NAC is closely bound up with the attenuation of $H_{D\varphi\_\mathrm{Noise2}}(z)$.

The NAC value, the variance $\sigma^2_{D\varphi\_Ns}$, the gain cross-over frequency f_{cv}, and the phase margin PM_v of these three EGs are exhibited in Table I. For the sake of comparison, a control group (CG) is set up without adopting any frequency conversion filters and with the parameters of $f_{\mathrm{sa\_DAB}} = 2.5$ kHz, $K_{\mathrm{vp}} = 0.0832$, and $\omega_v = 31.4159$. The values of related variables of CG are exhibited in Table I as well. From Table I, for EG-1st and EG-3rd, their NAC values are all smaller than NAC_Max, which means that the DAB converter can operate normally and steadily.

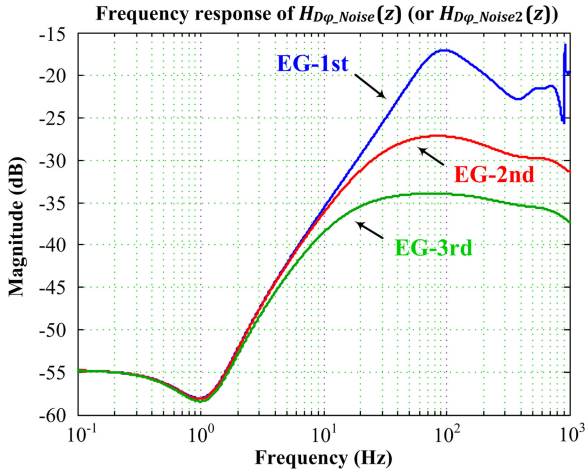

Fig. 13. Frequency response of $H_{D\varphi\_\mathrm{Noise}}(s)$ (or $H_{D\varphi\_\mathrm{Noise2}}(z)$) of EG-1st, EG-2nd, and EG-3rd in the frequency of 1 Hz to 1 kHz.

TABLE I
VALUES OF RELATED VARIABLES OF THREE EXPERIMENT GROUPS AND THE CONTROL GROUP

	CG	EG-1st	EG-2nd	EG-3rd
NAC	7.959×10^{-3}	3.482×10^{-4}	1.347×10^{-3}	3.371×10^{-4}
$\sigma^2_{D\varphi\_Ns}$	2.080×10^{-3}	9.102×10^{-5}	3.521×10^{-4}	8.812×10^{-5}
f_{cv}	52.1 Hz	52.7 Hz	22.7 Hz	11.5 Hz
PM_v	56.1°	52°	74.8°	89.6°

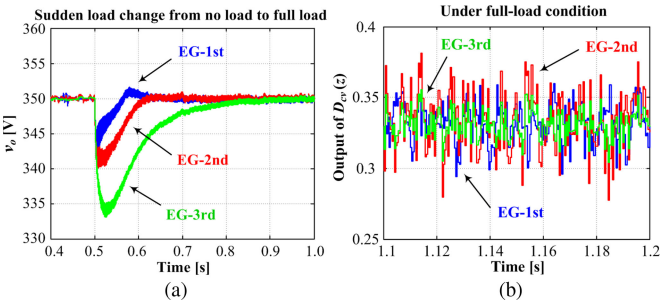

Fig. 14. Simulation waveforms based on the five-cell PETT laboratory prototype. There is measurement noise and no quantization noise in the sampling process of the dc output voltage v_o. (a) Simulation waveforms of v_o when there is sudden load change from no load to full load. (b) Simulation waveforms of v_o when the PETT is under full-load condition and in the steady state.

The simulation waveforms of these three EGs are shown in Fig. 14.

In the simulation models, there is measurement noise and no quantization noise in the sampling process of the dc output voltage v_o. The simulation model of the measurement noise is set up on the basis of experimental data. When there is sudden load change from no load to full load, the simulation waveforms of v_o is shown in Fig. 14(a). From the point of the decreasing amplitude of v_o, EG-1st < EG-2nd < EG-3rd; and from the point of

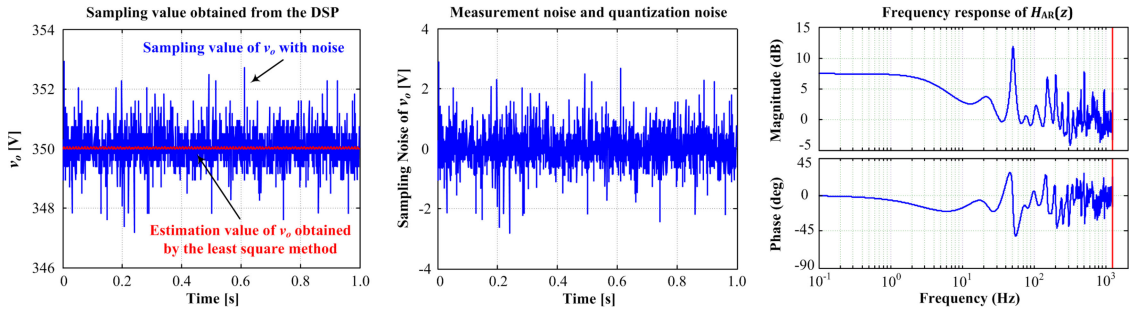

Fig. 15. Based on the five-cell PETT laboratory prototype. (a) Sampling values of v_o stored in the main controller, and the estimation values of v_o by means of the least square method. (b) Measurement noise and the A/D quantization noise contained in the sampling values of v_o. (c) Frequency response of $H_{\mathrm{AR}}(z)$, which is the denominator polynomial of the measurement noise model.

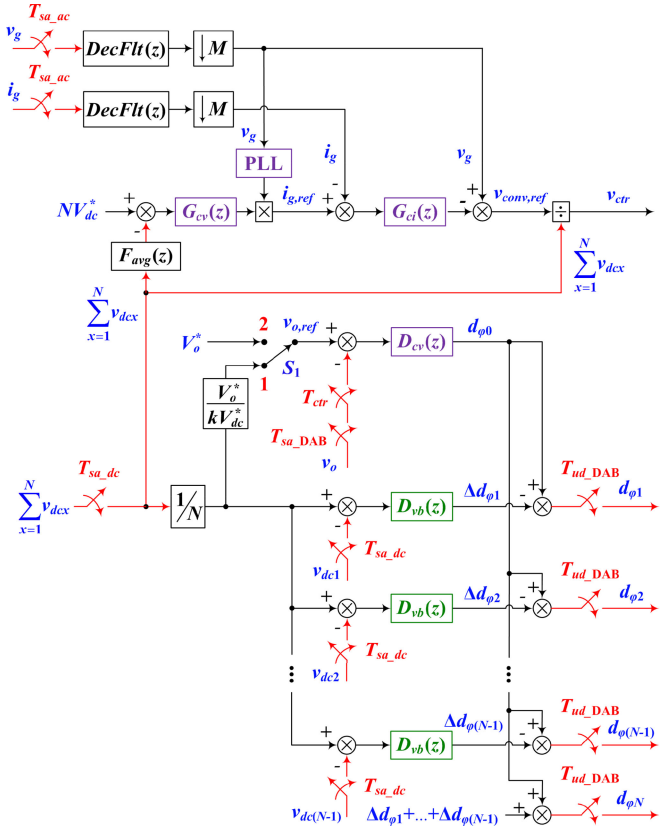

Fig. 16. Block diagram of the multirate digital control strategy of the PETT.

the recovery time of v_o, EG-1st < EG-2nd < EG-3rd. The results are consistent with the data about f_{cv} in Table I. When the PETT is under full-load condition and in the steady state, the simulation waveforms of $d_{\varphi 0}$, the output variable of $D_{\mathrm{cv}}(z)$, are shown in Fig. 14(b). From the point of the oscillation amplitude of $d_{\varphi 0}$, EG-3rd < EG-1st < EG-2nd, which is consistent with the values of $\sigma^2_{D\varphi\_Ns}$ in Table I. Synthetically, the above-mentioned theoretical analysis and simulation results indicate that the noise suppression scheme with improving the sampling frequency can largely attenuate the noises and maintain the superior dynamic performance as well, while the noise suppression scheme with adjusting the controller parameters attenuates the noises with the price of sacrificing the dynamic response. However, unfortunately, none of them are perfect and there is a weakness for the former scheme, which will inevitably occupy more memory space and calculation resource of the digital chips.

D. Statistical Model of the Measurement Noise

In the PETT laboratory prototype, the sampling of v_o is accomplished by the main controller. The parameters of $D_{\mathrm{cv}}(z)$ are chosen as $K_{\mathrm{vp}} = 0.0182$ and $\omega_v = 6.2832$. When the PETT is under full-load condition and in the steady state, the data of the sampling values of v_o stored in the DSP are exported. The sampling values of v_o are shown in Fig. 15(a). The sampling frequency of v_o is 2.5 kHz. It can be proved that in this situation, the sensitivity function $S_{\mathrm{vdab}}(z) \triangleq 1/(1 + L_{\mathrm{vdab}}(z))$ has quite small effect to amplify the noises in the sampling data, that is to say, the noises in the sampling data are nearly the same as the real ones.

As shown in Fig. 15(a), the variation range of v_o is very large, which is from 347 to 353 V. As is well-known, when the PETT is in the steady state, in the spectrum of v_o, the proportion of the dc component is the largest; although the amplitude of the second-order component is much smaller than that of the dc component, there is still a certain proportion for the second-order component; the proportion of other components is quite small and they can be neglected. Therefore, suppose the expression of v_o before being sampled as

$$v_o(t) = V_o + V_{o\_2\mathrm{nd}} \cdot \sin(2\omega_g t + \phi)$$

where V_o and $V_{o\_2\mathrm{nd}}$ are the amplitude of the dc component and the second-order component, respectively, ϕ is the initial phase of the second-order component, and $\omega_g = 2\pi \times 50\ \mathrm{rad/s}$. Based on the least square method, the values of V_o, $V_{o\_2\mathrm{nd}}$, and ϕ can be obtained. Then the curve of v_o before being sampled (also the estimation values of v_o) can be acquired and shown in Fig. 15(a). The noises in the sampling process, including the measurement noise and the A/D quantization noise, can be derived by subtracting the estimation values of v_o from the sampling values of v_o, as shown in Fig. 15(b). For the convenience to express, the measurement noise is denoted as $u_s(n)$, the A/D quantization noise is denoted as $u_q(n)$, the sum of the measurement noise and the A/D quantization noise is denoted as $u(n) = u_s(n) + u_q(n)$, and the length of the noise sample (or

the noise sequence) is denoted as $N_{\rm sa}$. Denote the autocorrelation functions of $u_s(n)$, $u_q(n)$, and $u(n)$ as $r_s(k)$, $r_q(k)$, and $r(k)$, respectively, taking $u(n)$ as an instance, its autocorrelation function is

$$r(k) = r(n, n-k) = E[u(n) \cdot u^*(n - k)] = \lim_{N_{\rm sa}\to\infty} \frac{1}{N_{\rm sa}} \sum_{n=0}^{N_{\rm sa}-1} u(n) \cdot u^*(n - k) \quad (19)$$

where $k = 0, \pm 1, \pm 2, \ldots$, and $r(-k) = r^*(k)$. $r^*(k)$ is the conjugate complex number of $r(k)$, while $u^*(n)$ is the conjugate complex number of $u(n)$.

According to [21], [27], and [28], when the sample length $N_{\rm sa}$ is finite but very large, an estimation value of $r(k)$, which is very close to the real one, can be acquired. In order to make full use of the sample data, the modulo operation or the circular time-reversal operation [21] is adopted, and

$$r(k) = E[u(n) \cdot u^*(n - k)] \approx \frac{1}{N_{\rm sa}} \sum_{n=0}^{N_{\rm sa}-1} u(n) \cdot u^*(n - k_{N_{\rm sa}}). \quad (20)$$

The meaning of (21) is like that: when $k = 0$

$$r(k) \approx \frac{1}{N_{\rm sa}} \sum_{n=0}^{N_{\rm sa}-1} u(n) \cdot u^*(n - k) \quad (21)$$

and when $k = 1, 2, \ldots$

$$r(k) \approx \frac{1}{N_{\rm sa}} \sum_{n=0}^{k-1} u(n) \cdot u^*(N_{\rm sa} + n - k) + \frac{1}{N_{\rm sa}} \sum_{n=k}^{N_{\rm sa}-1} u(n) \cdot u^*(n - k). \quad (22)$$

In this example, it is chosen that $N_{\rm sa} = 2500$. As there is no correlativity between $u_s(n)$ and $u_q(n)$

$$u(n)\, u^*(n - k) = u_s(n)\, u_s^*(n - k) + u_q(n)\, u_q^*(n - k). \quad (23)$$

Then

$$r(k) = r_s(k) + r_q(k) = \begin{cases} r_s(0) + r_q(0), & k = 0 \\ r_s(k), & k \neq 0 \end{cases}. \quad (24)$$

The statistical characteristic of the measurement noise $u_s(n)$ can be described by the AR model, where $u_s(n)$ is generated from a white noise $v(n)$ with Gaussian density function after passing through a digital filter. The filter is defined as

$$\frac{U_s(z)}{V(z)} \triangleq \frac{1}{H_{\rm AR}(z)} = \frac{1}{1 + b_1 z^{-1} + b_2 z^{-2} + \cdots + b_{M_r} z^{-M_r}} \quad (25)$$

where M_r is the order of $H_{\rm AR}(z)$, and $b_k (k = 1, 2, \ldots, M)$ is the real number. In this example, it is chosen as $M_r = 100$. Then, according to [21], [27], and [28], the value of b_k can be calculated by the following equation:

$$\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_M \end{bmatrix} = - \begin{bmatrix} r_s(0) & r_s(1) & \cdots & r_s(M_r - 1) \\ r_s(1) & r_s(0) & \cdots & r_s(M_r - 2) \\ \vdots & \vdots & \ddots & \vdots \\ r_s(M_r - 1) & r_s(M_r - 2) & \cdots & r_s(0) \end{bmatrix}^{-1} \times \begin{bmatrix} r_s(1) \\ r_s(2) \\ \vdots \\ r_s(M_r) \end{bmatrix}. \quad (26)$$

And the variance of the white noise $v(n)$ is

$$\sigma_v^2 = r_s(0) + b_1 r_s(1) + b_2 r_s(2) + \cdots + b_{M_r} r_s(M_r). \quad (27)$$

In this example, it is calculated that $\sigma_v^2 = 0.2115$, and the frequency response of $H_{\rm AR}(z)$ is shown in Fig. 15(c). In all of the simulation mentioned above, the model of the measurement noise is based on the AR noise model presented in this section. It should be noted that as the derivation process of the AR parameters does not refer to the corresponding sampling frequency, the variation of the sampling frequency will not change the variance of $v(n)$, the order M_r, and the parameters b_k of $H_{\rm AR}(z)$.

IV. Multirate Digital Control Strategy of the PETT

Although the noise suppression scheme with improving the sampling frequency can largely attenuate the noises and never deteriorate the dynamic performance of DAB converters, this scheme is still not adopted in the PETT multirate digital control strategy presented in the following paper due to the high requirement on the digital chips. Detailed explanation is given below.

Star-connected distributed control structure is adopted by the PETT digital control system, including a main controller and several slave controllers. The ac input voltage v_g, the ac input current i_g, and the dc output voltage v_o are sampled by the main controller [15]. The sampling frequency of v_g and i_g is $f_{\rm sa\_ac}$, and the sampling frequency of v_o is $f_{\rm sa\_DAB}$. In order to synchronize the sampling time, another frequency for synchronization control of time sequences should be set, which is denoted as $f_{\rm syn}$. $f_{\rm syn}$ is the least common multiple of $f_{\rm sa\_ac}$ and $f_{\rm sa\_DAB}$. If the frequency conversion filter (also the minimum-phase FIR filter) exists in the sampling of v_o, the order of that filter is related to the value of $f_{\rm syn}$. With the increase in the value of $f_{\rm syn}$, the order will become higher and the computation cost will become larger. According to the analysis in another paper related to the multirate digital signal processing for the CHB, it is concluded that $f_{\rm sa,ac} = 4N f_{\rm sw}$, where $f_{\rm sw}$ is the switching frequency of the CHB. For the example of this paper, $N = 5$, $f_{\rm sw} = 500$ Hz, and $f_{\rm sa,ac} = 10$ kHz.

In this paper, the switching frequency of DAB converters is $f_{\rm sw\_DAB} = 1.25$ kHz. Based on the elaboration in Section II, $f_{\rm sa\_DAB} = P_1 \times f_{\rm sw\_DAB}$ or $f_{\rm sa\_DAB} = P_2 \times 2N f_{\rm sw\_DAB}$, where P_1 is the common divisor of $2N$ ($P_1 = 1, 2, \ldots, 2N$) and $P_2 = 2, 3, \ldots$. It can be found that when the value of $f_{\rm sa\_DAB}$ is chosen as 12.5 or 25 or 50 kHz, $f_{\rm syn}$ is

identically equal to 50 kHz. Besides, when $f_{\mathrm{sa\_DAB}} = 12.5$ or 25 kHz, the process of interpolation and up-sampling is needed, which will result in a much higher order of the frequency conversion filter [21]. Combining the noise suppression effect elaborated in Section III, the value of $f_{\mathrm{sa\_DAB}}$ should be chosen as 50 kHz or the integral multiple of 50 kHz. However, in the experiment, it is found that when $f_{\mathrm{sa\_DAB}} = f_{\mathrm{syn}} = 50$ kHz, the space occupation of the digital chip has reached to its limitation. This result is related to the selection of digital chips, including the DSP and the field programmable gate array (FPGA) [30], the selection of digital-filter algorithms, and the cooperation of hardware and software resource. In order to adapt to the existing PETT control system, the noise suppression scheme with improving the sampling frequency is not adopted in the PETT multirate digital control strategy presented below. The application and optimization of this scheme are left for future research, which will include the optimization design of the control-system hardware and the digital-filter algorithms.

In the PETT multirate digital control strategy, the noise suppression scheme with adjusting the controller parameters is adopted. The parameters of $D_{\mathrm{cv}}(z)$ are selected as $K_{\mathrm{vp}} = 0.0182$ and $\omega_v = 6.2832$. The sampling frequency of v_o is $f_{\mathrm{sa\_DAB}} = 2.5$ kHz, the frequency for synchronization control of time sequences is $f_{\mathrm{syn}} = 10$ kHz. As for the PWM modulating wave updating frequency of DAB converters ($f_{\mathrm{ud\_DAB}}$), in order to avoid the disorder of the DAB phase-shift modulation, it can be chosen as

$$f_{\mathrm{ud\_DAB}} \le f_{\mathrm{ctr}} \text{ and } f_{\mathrm{ud\_DAB}} = \frac{f_{\mathrm{sw\_DAB}}}{P_3} \tag{28}$$

where $P_3 = 1, 2, 3, \ldots$. Generally, there is only dc component contained in the DAB normalized phase-shift variable d_φ. Hence, the frequency conversion filter is not necessary between the controller $D_{\mathrm{cv}}(z)$ and the phase-shift modulation. It can convert the frequency directly. Furthermore, unsuitable modulating wave updating method may cause transient noise or transient dc bias in i_{Lrj}, which may result in serious overcurrent in the transient state [34]. However, as the emphasis in this paper is placed on the noise issue in the steady state, the improvement presented in [34] has not been adopted in the experiment below.

Synthesizing the voltage balance control strategy of the PETT [25] and the multirate digital signal processing of the CHB converter and the DAB converters, the block diagram of the PETT multirate digital control strategy is shown in Fig. 16.

As shown in Fig. 16, the DAB converters process the intermediate-dc-voltage balance control to maintain the voltage balance and current sharing among different PETT cells. $G_{\mathrm{cv}}(z)$ and $G_{\mathrm{ci}}(z)$ are the voltage-outer-loop controller and the current-inner-loop controller of the CHB, respectively. $F_{\mathrm{avg}}(z)$ is the moving-average filter to avoid the second-order component of the intermediate dc voltages being introduced into the control system, to attenuate the intensity of interaction between different voltage balance control loops [25], and to suppress the measurement noise caused by the sampling process of $v_{\mathrm{dc}j}$ (the mechanism can be derived similarly as the above-mentioned paper). PLL is a phase-locked loop. $\mathrm{DecFlt}(z)$ is the frequency conversion filter after sampling v_g and i_g, and $T_{\mathrm{sa\_ac}} = 1/f_{\mathrm{sa\_ac}}, T_{\mathrm{sa\_ac}} = 1/f_{\mathrm{sa\_ac}}$. $v_{\mathrm{dc}j}$ is the intermediate dc voltage of *cell* j, where $j = 1, 2, \ldots, N$. $v_{\mathrm{conv,ref}}$ is the intermediate variable of the CHB control loop. v_{ctr} is the modulating wave of the CHB and each CHB cell has the same modulating wave. $D_{\mathrm{cv}}(z)$ is the output-voltage controller, while $D_{\mathrm{vb}}(z)$ is the DAB voltage-balance controller. The sampling frequency of $v_{\mathrm{dc}j}$ is $f_{\mathrm{sa\_dc}} = f_{\mathrm{ctr}}$ and $T_{\mathrm{sa\_dc}} = 1/f_{\mathrm{sa\_dc}}$. V_o^* and V_{dc}^* are the rated values, respectively, of v_o and $v_{\mathrm{dc}j}$. $k:1$ is the turns-ratio of the medium/high-frequency transformers. S_1 is the switch used in the PETT starting process. $v_{o,\mathrm{ref}}$ is the reference of v_o, $d_{\varphi 0}$ is the output variable of $D_{\mathrm{cv}}(z)$, $\Delta d_{\varphi j}$ is the output variable of $D_{\mathrm{vb}}(z)$ in *cell* j, and $d_{\varphi j}$ is the normalized phase-shift variable of the jth DAB converter.

TABLE II
SYSTEM PARAMETERS OF DAB CONVERTERS IN THE EXPERIMENT

Symbol	Quantity	Value
$v_{\mathrm{dc}j}$	DC input voltages of each DAB	350 V
v_o	DC output voltage of DABs	350 V
C_{gj}	DC input capacitors of each DAB	6.8 mF $\pm$ 20%
L_{rj}	DAB storage inductor of each DAB	1.8 mH $\pm$ 15%
C_{fj}	DC output capacitors of each DAB	6.8 mF $\pm$ 20%
$f_{\mathrm{sw\_DAB}}$	Switching frequency of DABs	1.25 kHz
$f_{\mathrm{sa\_DAB}}$	Sampling frequency of v_o	2.5 kHz
f_{ctr}	Control frequency	2 kHz
$f_{\mathrm{ud\_DAB}}$	Modulating wave updating frequency	1.25 kHz

V. EXPERIMENT RESULTS

The experiment results provided below are based on the five-cell PETT laboratory prototype. The rated power of the laboratory prototype is 30 kW. In the experiment, the output load of the PETT is the resistive load. The system parameters of DAB converters are exhibited in Table II.

The main circuit diagram of the laboratory prototype is shown in Fig. 17. For clarity, the CHB is not exhibited in Fig. 17. C_{gj} is the dc input capacitor, C_{fj} is the dc output capacitor, L_{rj} is the DAB storage inductor, and T_{rj} is the medium-frequency transformer with turns ratio of 1:1. $v_{\mathrm{dc}j}$ is the dc input voltage,v_{pj} is the midpoint voltage of each DAB input H-bridge,v_{sj} is the midpoint voltage of each DAB output H-bridge, and i_{Lrj} is the DAB inductor current ($j = 1, 2, \ldots, 5$). v_o is the dc output voltage.

In the following paper, three groups of experiment results are given. In these three groups of experiment, the parameters of the DAB voltage-closed-loop controller $D_{\mathrm{cv}}(z)$ are different. The experiment waveforms are shown in Figs. 18–20.

When the parameters of $D_{\mathrm{cv}}(z)$ are chosen as $K_{\mathrm{vp}} = 0.0832$ and $\omega_v = 31.4159$, the data obtained from the DSP including the sampling value of v_o and the output variable of $D_{\mathrm{cv}}(z)$ are shown in Fig. 18(a); the experiment waveforms of i_{Lr5}, v_{p5}, and v_{s5} are shown in Fig. 18(b); the experiment waveforms of $i_{Lr1} - i_{Lr4}$ are shown in Fig. 18(c); and the experiment waveforms of v_o, $v_{\mathrm{dc1}} - v_{\mathrm{dc2}}$, and i_{Lr5} are shown in Fig. 18(d). The PETT is under no-load condition. As shown in Fig. 18(c) and (d), even under no-load condition, there is a very large current-peak value of the DAB inductor currents i_{Lrj} and the variation range of i_{Lrj}

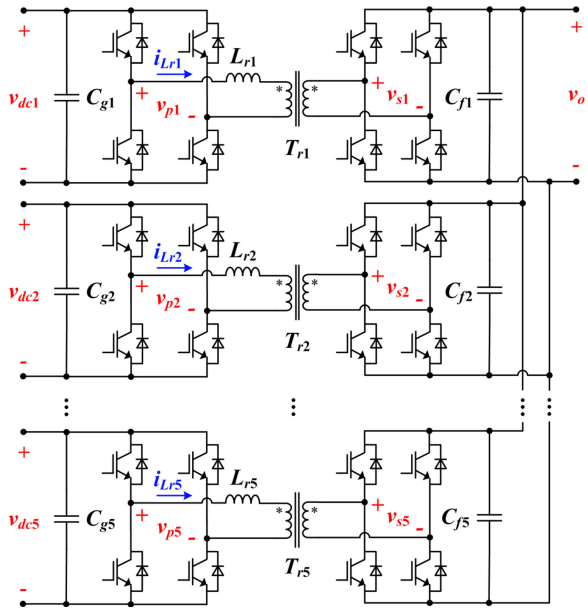

Fig. 17. Main circuit diagram of the five-cell output-parallel DAB converters.

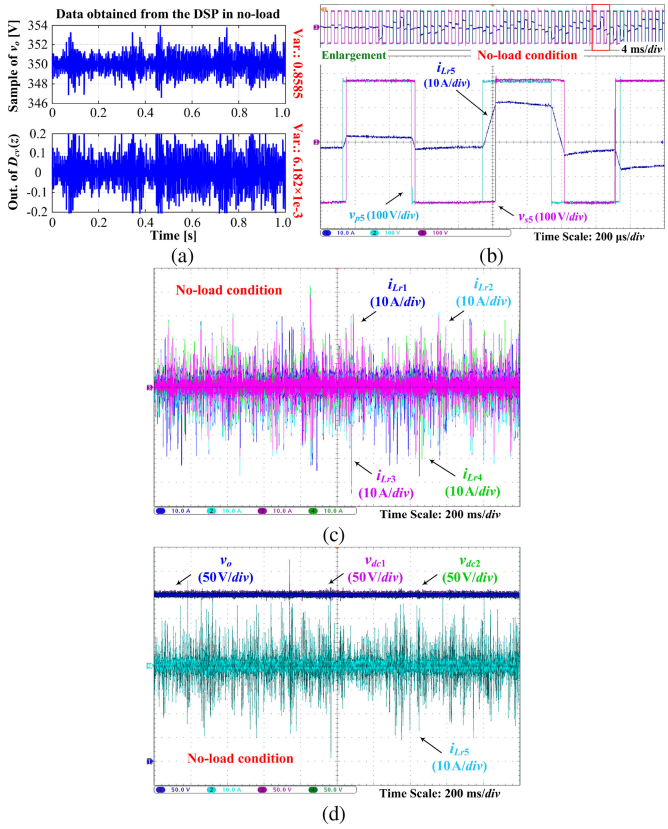

Fig. 18. Experiment waveforms based on the five-cell PETT laboratory prototype. The parameters of $D_{\rm cv}(z)$ are chosen as $K_{\rm vp} = 0.0832$ and $\omega_v = 31.4159$. The PETT is under no-load condition. (a) Data obtained from the DSP, including the sampling value of v_o (top) and the output variable of $D_{\rm cv}(z)$ (bottom). (b) Experiment waveforms of i_{Lr5}, v_{p5}, and v_{s5}. (c) Experiment waveforms of DAB inductor currents in *cells* 1–4 ($i_{Lr1} - i_{Lr4}$). (d) Experiment waveforms of the dc output voltage (v_o), intermediate dc voltages in *cells* 1 and 2 ($v_{\rm dc1} - v_{\rm dc2}$), and DAB inductor current in *cell* 5 (i_{Lr5}).

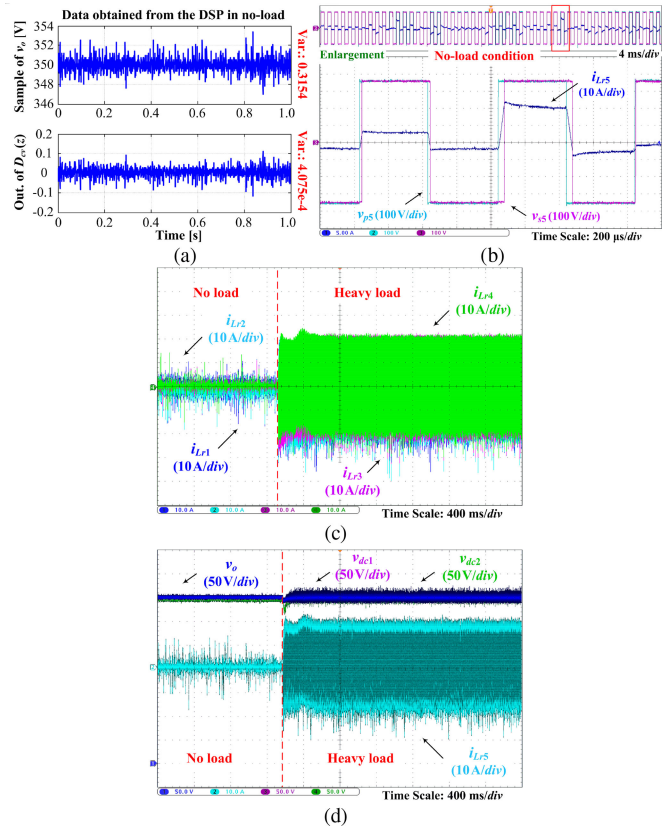

Fig. 19. Experiment waveforms based on the five-cell PETT laboratory prototype. The parameters of $D_{\rm cv}(z)$ are chosen as $K_{\rm vp} = 0.03589$ and $\omega_v = 18.84956$. The PETT has a sudden load change from no load to heavy load. (a) Data obtained from the DSP, including the sampling value of v_o (top) and the output variable of $D_{\rm cv}(z)$ (bottom). (b) Experiment waveforms of i_{Lr5}, v_{p5}, and v_{s5}. (c) Experiment waveforms of DAB inductor currents in *cells* 1–4 ($i_{Lr1} - i_{Lr4}$). (d) Experiment waveforms of the dc output voltage (v_o), intermediate dc voltages in *cells* 1 and 2 ($v_{\rm dc1} - v_{\rm dc2}$), and DAB inductor current in *cell* 5 (i_{Lr5}).

is about -45 to 45 A. It means that the measurement noise has very large impact on the DAB converters.

When the parameters of $D_{\rm cv}(z)$ are chosen as $K_{\rm vp} = 0.03589$ and $\omega_v = 18.84956$, the data obtained from the DSP including the sampling value of v_o and the output variable of $D_{\rm cv}(z)$ are shown in Fig. 19(a); the experiment waveforms of i_{Lr5}, v_{p5}, and v_{s5} are shown in Fig. 19(b); the experiment waveforms of $i_{Lr1} - i_{Lr4}$ are shown in Fig. 19(c); and the experiment waveforms of v_o, $v_{\rm dc1} - v_{\rm dc2}$, and i_{Lr5} are shown in Fig. 19(d). The PETT has a sudden load change from no load to heavy load. As shown in Fig. 19(c) and (d), the current-peak value of i_{Lrj} under no-load condition is close to 20 A, while the current-peak value of i_{Lrj} under heavy-load condition is close to 50 A. It is indicated that in this case, there is a certain impact of the measurement noise on DAB converters. Besides, after the sudden load change, the decreasing amplitude of v_o is very small, and the recovery speed of v_o is very fast.

When the parameters of $D_{\rm cv}(z)$ are chosen as $K_{\rm vp} = 0.0182$ and $\omega_v = 6.2832$, the data obtained from the DSP including the sampling value of v_o and the output variable of $D_{\rm cv}(z)$ are shown in Fig. 20(a); the experiment waveforms of i_{Lr5}, v_{p5},

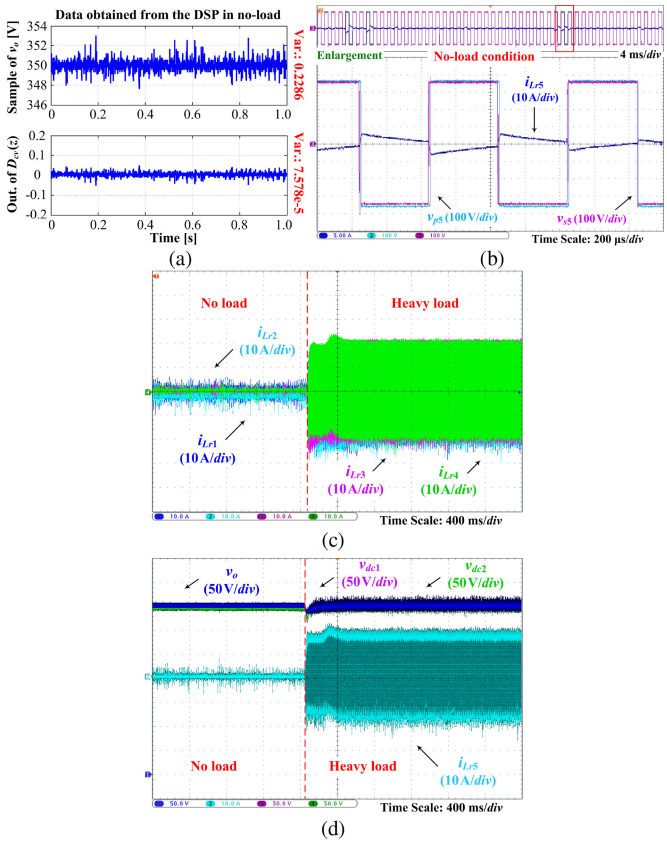

Fig. 20. Experiment waveforms based on the five-cell PETT laboratory prototype. The parameters of $D_{\rm cv}(z)$ are chosen as $K_{\rm vp} = 0.0182$ and $\omega_v = 6.2832$. The PETT has a sudden load change from no load to heavy load. (a) Data obtained from the DSP, including the sampling value of v_o (top) and the output variable of $D_{\rm cv}(z)$ (bottom). (b) Experiment waveforms of i_{Lr5}, v_{p5}, and v_{s5}. (c) Experiment waveforms of DAB inductor currents in *cells* 1–4 ($i_{Lr1} - i_{Lr4}$). (d) Experiment waveforms of the dc output voltage (v_o), intermediate dc voltages in *cells* 1 and 2 ($v_{\rm dc1} - v_{\rm dc2}$), and DAB inductor current in *cell* 5 (i_{Lr5}).

and v_{s5} are shown in Fig. 20(b); the experiment waveforms of $i_{Lr1} - i_{Lr4}$ are shown in Fig. 20(c); and the experiment waveforms of v_o, $v_{\rm dc1} - v_{\rm dc2}$, and i_{Lr5} are shown in Fig. 20(d). The PETT has a sudden load change from no load to heavy load. As shown in Fig. 20(c) and (d), no matter under no-load condition or under heavy-load condition, the DAB converters run quite steadily and there is no large current-peak value of i_{Lrj}. Under no-load condition, the variation range of i_{Lrj} is about -10 to 10 A, which is much smaller than the ones mentioned above. As for the decreasing amplitude of v_o and the recovery time of v_o after the sudden load change, the values in this group are all a little larger than the ones mentioned above. However, in this group, after the sudden load change, the decreasing amplitude of v_o is still not larger than 15 V, and v_o recovers to the normal steady state (2% of the rated value) within 120 ms. In this paper, it is recommended to choose the parameters of $D_{\rm cv}(z)$ as $K_{\rm vp} = 0.0182$ and $\omega_v = 6.2832$. From the experiment waveforms shown in Fig. 20, it means that based on the selected parameters, the DAB converters can achieve relatively good control performance.

TABLE III
VALUES OF RELATED VARIABLES OF THREE GROUPS OF EXPERIMENT

	$K_{\rm vp} = 0.0832$ $\omega_v = 31.4159$	$K_{\rm vp} = 0.03589$ $\omega_v = 18.84956$	$K_{\rm vp} = 0.0182$ $\omega_v = 6.2832$
σ^2_{Vo}	0.8585	0.3154	0.2286
$\sigma^2_{D\varphi}$	6.182×10^{-3}	4.075×10^{-4}	7.578×10^{-5}
Practical NAC	7.201×10^{-3}	1.292×10^{-3}	3.315×10^{-4}
Theoretical NAC	7.959×10^{-3}	1.347×10^{-3}	3.371×10^{-4}

As shown in Figs. 18(b), 19(b), and 20(b), it can be seen that the current peak of i_{Lrj} with quite large value is essentially caused by the frequent variation of the phase-shift variable, which is the output of $D_{\rm cv}(z)$. This discovery is consistent with the data exhibited in Figs. 18(a), 19(a), and 20(a). The mismatch between $v_{{\rm dc}j}$ and v_o plays a relative weak role in the above-mentioned phenomena. The variance values of the sampling data of v_o and the output of $D_{\rm cv}(z)$, which are calculated on the basis of the data obtained in the above-mentioned three groups of experiment, are collectively exhibited in Table III. The variance of the sampling data of v_o is denoted as σ^2_{Vo}, while the variance of the output of $D_{\rm cv}(z)$ is denoted as $\sigma^2_{D\varphi}$. As is analyzed above, the measurement noise is dominant in this laboratory prototype. Then, the NAC value can be approximately calculated as NAC $\approx \sigma^2_{D\varphi}/\sigma^2_{Vo}$. The values of the practical NAC and the theoretical NAC are also exhibited in Table III.

As shown in Table III, the practical NAC is nearly the same as the theoretical NAC. It is indicated that the theoretical deviation of NAC is correct. However, it should be noticed as well that the practical one is a little smaller than the theoretical one, which is consistent with the analysis related to Fig. 9(b) and (11). This is the limitation of the method proposed in this paper to estimate NAC. Further improvement of estimating precision is left for future research works.

VI. CONCLUSION AND OUTLOOK

The noise has great influence on the power electronic converters, which is a key factor to restrict the development of their control performance. In this paper, the emphases are placed on four typical noises, including the switching noise, the second-order voltage ripple, the A/D quantization noise, and the measurement noise. Their generation mechanism and their impact on the DAB control performance are analyzed. On the basis, the corresponding noise suppression schemes are presented. For the example of this paper, the influence of the switching noise and the measurement noise on DAB converters is the strongest, followed by the quantization noise and the second-order voltage ripple. By means of the NAC variable proposed in this paper, the impact of the measurement noise and the quantization noise on the DAB converters can be quantitatively evaluated, and the main parameters of the proposed noise suppression schemes, such as the sampling frequency and the controller parameters, can be calculated and selected.

In order to cooperate the converters in the front end and in the backward stage, the control algorithms of the CHB and the DABs are placed in the same interrupt with the same values of

control frequency. The control frequency, also the frequency to call and execute the interrupt in digital chips, is selected on the basis of the control delay (the execution time of the control algorithms) and the transmission delay (the data transmission time between the main controller and the slave controller). In order to mitigate the influence of the switching noise, the quantization noise, and the measurement noise, the DAB sampling frequency may need to be chosen as a different value with the control frequency. Besides, in order to avoid the disorder of the DAB phase-shift modulation, the PWM modulating wave updating frequency should be matched with the switching frequency, and also may have a different value with the control frequency. Thus, combining the multirate digital signal processing of the CHB and balance control strategy of the PETT, the PETT multirate digital control strategy is finally proposed in this paper.

Based on the proposed control strategy, the preferable steady-state performance can be achieved. In this case, further improvement of the PETT dynamic control performance is up to the control frequency. If the control frequency is much higher, the dynamic response will become much faster, especially when the DAB sampling frequency is much higher than the DAB switching frequency and the DAB switching frequency is higher than the control frequency. In another aspect, the increase of the control frequency is restricted by the control delay and the transmission delay. The smaller the control delay and the transmission delay, the higher the value of the control frequency can be selected. From this point of view, based on the same control algorithms, it is beneficial to reduce the control delay and the transmission delay by using the DSPs with higher dominant frequency and the optical fibers with a faster transmission rate, and thereby, to further increase the control frequency, following with the dynamic performance further improved. What is more, it can use some control and/or filter algorithms with computationally efficient structure and some digital chips (such as FPGAs) with very strong parallel processing ability, so that the control performance of the PETT can be further improved.

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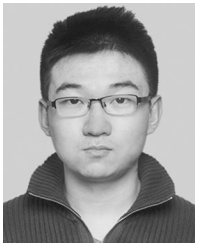

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