Multimode Operation of Resonant and Hybrid Switched-Capacitor Topologies

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***Abstract*—This paper presents an overview of resonant and hybrid switched-capacitor converters with a particular focus on multimode operation. The multimode approach is discussed as a tool to affect high efficiency and power density across a wide load range, provide variable regulation, and, as a general framework, to conceptualize the advantages and opportunities of the approach compared to more traditional dc–dc converters. A general analysis is provided to quantify the advantage of hybrid and resonant converters that factors in the tradeoffs between size and loss in the magnetic component and voltage stress on the active devices. A broader set of operating modes is presented that spans continuous and discontinuous conduction and includes resonant, quasi-resonant, and more traditional buck- or boost-like operation. A prototype flying-capacitor multilevel converter is presented to demonstrate the variety of operating modes and motivate important considerations such as voltage balance on the flying capacitors.**

***Index Terms*—DC–DC converter, flying-capacitor multilevel (FCML), hybrid switched capacitor, resonant switched capacitor (ReSC), soft-charging, voltage balancing.**

I. Introduction

IN MODERN dc–dc converters, magnetic components have become a limiting factor in shrinking size and improving efficiency. Highly integrated and high-frequency designs especially struggle with the size of magnetic components and the lack of efficient magnetic materials at high switching frequencies [1], [2]. In the absence of significant advances on magnetics, improvement in power density and efficiency will have to be driven by new converter topologies and operating modes that can reduce the inductor volt-second (V·s) rating and operate efficiently with reduced inductance requirements.

Switched-capacitor (SC) dc–dc converters hold the promise to completely eliminate magnetic components in dc–dc converters, and the authors of [3] and [4] showed that they can even outperform conventional magnetic-based topologies over a wide range of power and voltage levels. Due to the cascaded structure of SC converters, low-voltage devices can be stacked efficiently to interface with higher voltages and implement large conversion ratios with better device utilization than conventional inductive converters [4]–[6]. Low-voltage devices are capable of efficient operation at high switching frequencies, which reduces the required energy storage in passive elements.

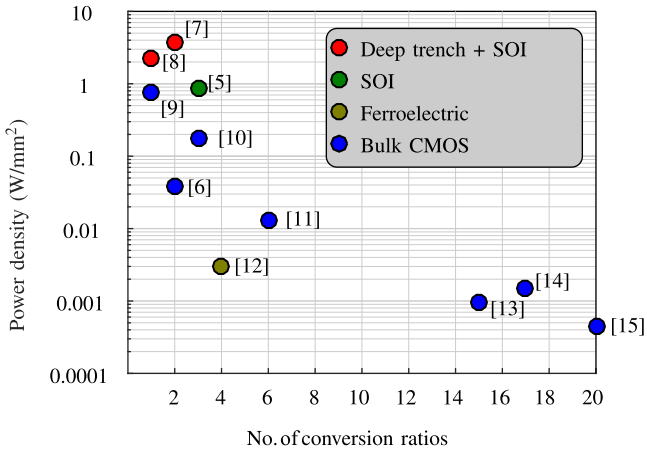

Fig. 1. Overview of previously published SC designs on a power density versus number of conversion ratios plot. Power density drops by more than an order of magnitude for designs with more than three conversion ratios.

Despite the many attractive features of SC converters, especially for on-chip power conversion, there exist a number of challenges that limit their application space. One of the main challenges is the poor utilization of the capacitive energy density due to charge-sharing losses, which inflates the amount of capacitance required for efficient operation. Second, regulation in SC converters can only be achieved through an increase in the output impedance, similar to a linear regulator, which hurts efficiency and power density. An increased number of discrete conversion ratios also cannot address this issue, as illustrated in Fig. 1. While designs with a moderate number of conversion ratios (i.e., 1–3) can achieve power densities on the order of 1 W/mm^2, designs with more than ten conversion ratios report power densities that are three orders of magnitude lower [5]–[15].

The challenges of SC power conversion identified above, therefore, revolve around *efficiently accessing the energy density of the flying capacitors* and providing output voltage regulation while maintaining high power density and efficiency. A converter class that offers the potential to achieve both better capacitor utilization and efficient regulation has recently attracted

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TABLE I
OVERVIEW OF PREVIOUS WORK

	[21]	[17]	[22]	[16]	[23]	[18]	[24]
Topology	FCML	FCML	Dickson	SP	FCML	ReSC	recursive
Conversion ratio	2:1	2:1	8:1	3:1	3:1	2:1	4:1
Input voltage	3.6 V	2.4 V	150 V	5 V	50 V	6 V	1.8 V
Flying capacitance	5.1 nF	18 nH	$7 \times 2.2\,\mu$F	$2 \times 22\,\mu$F	$2 \times 4.7\,\mu$F	24 nF	3 nF
Inductance	26 nH	1 nH	$3.3\,\mu$H	28 nH	$3.3\,\mu$H	1.1 nH	5.5 nH
Switching frequency	37 MHz	200 MHz	250 kHz	10 MHz	250 kHz	50 MHz	20 MHz
Output power	0.1 mW	1 W	18 W	0.8 W	42 W	7.7 W	110 mW
Efficiency	68.5%	77%	96%	82%	94.8%	85%	69%

attention [16]–[18]. Soft-charging, hybrid, or resonant topologies leverage a small inductor to prevent charge-sharing losses and thus allow a larger portion of the flying-capacitor energy to be transferred without the penalty of additional charge-sharing losses incurred otherwise in SC converters. The concept can be applied in a variety of ways and to a wide range of SC topologies and has been shown to provide performance benefits compared to pure SC designs [19], [20]. The hybrid approach also provides the opportunity for efficient regulation modes, which do not require reconfigurable topologies or linear-type regulation. While the need for an inductor can be considered a disadvantage, the inductance required is many times smaller than what is required for inductive converters, which opens up new possibilities for miniaturization [20].

In this paper, an overview of previous work on the hybrid, soft-charging, and resonant converter class is provided. A general analysis quantifies the potential advantage compared to pure SC converters. Compared to previous work, in this paper, a range of possible operating modes are discussed, and it is shown that a single converter can transition between them seamlessly based on the operating conditions (multimode operation). Moreover, a general model for multimode operation is presented, which builds on the SC modeling framework. Finally, a three- and four-level flying-capacitor multilevel (FCML) converter prototype is presented and used to demonstrate multimode operation with high efficiency across a wide range of output voltages and load currents.

II. BACKGROUND

Different terminologies have been used to describe a converter that combines elements of an SC and an inductive converter. Recently, soft-charging [16], [19], resonant [19], [20], [24], [25], and hybrid [26] have been used to describe this class of converters (see Table I). For simplicity, the term hybrid SC converter will be used as a broader term to describe the entire class of converters, whereas resonant switched-capacitor (ReSC) will be used to describe converters operating in a resonant mode.

ReSC converters have so far been presented as an extension of pure SC converters. However, ReSC can also be considered as part of a broader range of converter topologies with different operating modes. Possible operating modes extend beyond pure resonance and present a continuum between resonant and more conventional-buck-like-operation. Moreover, while much work has focused on operation at the boundary of the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM), both the DCM and the CCM can also be used with hybrid SC converters and can be beneficial under different operating conditions. Thus, this work will present a broader consideration of the resonant, hybrid, and soft-charging SC converter class across a range of operating modes.

A. Overview of Past Work

Even though hybrid SC converters have only recently received increased attention, FCML or Meynard converters have been used for some time [17], [21], [27] and can be considered a part of the same converter class. In [17] and [27], the converter is treated similarly to a regular buck converter with the capacitor voltage considered approximately constant. In contrast, Villar and Alarcón [21] report quasi-resonant behavior that hints at the possibility of resonant operation, which was demonstrated in [28]. Other implementations include a merged two-stage converter [16] that combines a series-parallel SC stage with a conventional buck converter. Conceptually, the buck converter is meant to serve as a constant current source, which "soft-charges" the SC front-end in order to eliminate charge-sharing losses. While the SC front-end provides a constant 3:1 conversion, the buck converter regulates the output voltage.

An 8:1 "dickson" topology is used in [22] with an output inductor in a resonant CCM operating regime. Even though the "dickson" topology does not readily lend itself to resonant or soft-charging operation because capacitors are internally connected in parallel, Lei *et al.* [22] introduce extra circuit states (split-phase) to eliminate the charge-sharing losses that would otherwise occur. If the timing of these circuit states is chosen correctly, the capacitor can be charged to the correct voltages and do, therefore, not cause losses when connected in parallel. A different technique is used in [24] with a recursive topology. In order to achieve partial soft-charging of cascaded stages, the switching frequency of the recursive stages is scaled by a gear ratio to avoid circuit states that would incur charge-sharing losses.

B. $R_{\rm eff}$-Based Comparison With an SC

Many hybrid SC topologies can be operated in a resonant mode, and the behavior in this mode of operation is in many ways similar to SC converters. Thus, resonant operation provides a useful index for converter performance compared to a pure SC converter. This index can be extended to describe performance across a broader range of operation, as will be shown

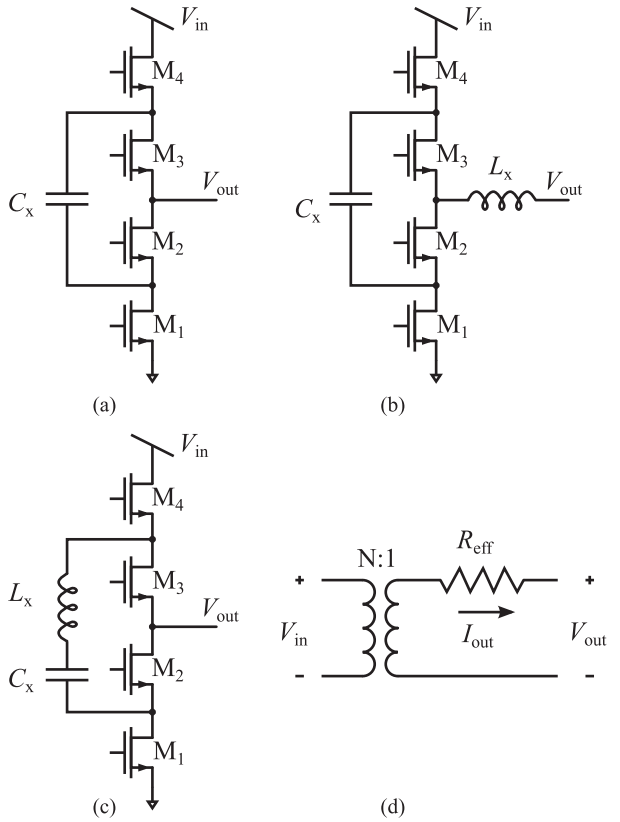


Fig. 2. (a) SC. (b) Direct resonant SC. (c) Indirect resonant SC topologies with 2:1 conversion ratio. (d) The behavioral converter model.

in Section III. *Therefore, developing loss models, optimization frameworks, and comparisons in the pure resonant mode can provide great insight into the achievable converter performance.*

Previous work shows that ReSC converters provide an advantage over pure SCs by preventing charge-sharing losses, but a framework to quantify the benefits is lacking. In [3], a simple model for SC converters was used to compare different SC topologies based on their output impedance, $R_{\rm eff}$. The generic circuit model is shown in Fig. 2. A comparison in terms of the converter output impedance $R_{\rm eff}$, that was used to analyze SC converters, can also provide some insight into the benefit of the ReSC. Consider the $R_{\rm eff}$ of a 2:1 SC and ReSC converter:

$$R_{\rm eff,SC} = \frac{1}{4C_{\rm x} f_{\rm sw}} \tag{1}$$

$$R_{\rm eff,ReSC} = \frac{\pi^2}{8} R_{\rm esr} \tag{2}$$

where $f_{\rm sw}$ is the switching frequency and $C_{\rm x}$ is the flying capacitance. For a fair comparison, we assume that both converters operate at the same switching frequency equal to the resonant frequency f_0. Only the slow-switching limit (SSL) impedance of the SC converters is considered, which favors the SC converter at higher switching frequencies. The terms SSL and fast-switching limit (FSL) are based on the SC framework in [3]. In the SSL region, the effective resistance $R_{\rm eff}$ is independent of the equivalent series resistance $R_{\rm esr}$ and is inversely proportional to switching frequency and flying capacitance, while in the FSL region $R_{\rm eff}$ is equal to $R_{\rm esr}$ (for more details, also see [29]). A comparison between SC and ReSC then yields

$$\frac{R_{\rm eff,SC}}{R_{\rm eff,ReSC}} = \frac{4}{\pi R_{\rm esr}} \sqrt{\frac{L_{\rm x}}{C_{\rm x}}} = \frac{4}{\pi} Q \tag{3}$$

where Q is the quality factor of the resonant circuit, $Q = \frac{1}{R_{\rm esr}} \sqrt{\frac{L_{\rm x}}{C_{\rm x}}}$. This result can be interpreted in two ways; compared to an equivalent SC design with equal flying capacitance, an ReSC design can operate with the following:

1) Q times lower $R_{\rm eff}$ at the same frequency;
2) Q times lower frequency with the same $R_{\rm eff}$.

Another interpretation of (3) is that resonant operation effectively boosts the voltage swing on the flying capacitor by approximately Q without incurring charge-sharing losses. This enables higher utilization of the available energy density of the flying capacitor and, ultimately, lower conduction loss for a given load current. While this can be perceived as a significant benefit, it does not factor in the additional losses that are incurred in the inductor or the added size and volume of the magnetic component. Therefore, a more detailed analysis is needed to consider these factors and will be presented in the following subsection.

C. Design Study

An optimization procedure for ReSC converters was developed to allow a comparison between ReSC and SC converters over a wide range of conditions. Details about the optimization procedure can be found in Appendix A. Based on this optimization procedure, a more practical comparison of ReSC and SC can be performed. Fig. 3 shows the minimum achievable power loss for the ReSC case, based on (14), and also a more detailed analysis that factors in the losses in several air-core inductor models with fixed form factor. Optimization for the SC case follows from [25], where optimal switch width is derived at a given switching frequency. The switching frequency is then swept across a reasonable range to find the minimum power loss numerically. The ReSC curves were generated by holding the inductor size constant, while inductance is scaled to match the resonant frequency to the switching frequency at each point. Using a simple scaling model for air-core solenoid inductors [1], both dc and ac resistances are scaled appropriately based on inductance and switching frequency. The inductor models are based on Coilcraft air-core inductors with the sizes listed in Fig. 3. All design constraints for the comparison are listed in Table II.

Importantly, each curve in Fig. 3 can be interpreted to represent the minimum achievable power loss at a given switching frequency. It can be seen that the SC trend follows the trends found in [5] and [30], where minimum power loss occurs close to the SSL/FSL boundary. With an ideal (lossless) inductor, the trend follows (14) and implies that power loss decreases in proportion to $\sqrt{f_{\rm sw}}$. The corresponding implication is that power loss decreases for arbitrarily large inductance, as there is no loss penalty for higher inductance in the ideal case. In a more practical comparison, when the inductor footprint or volume is fixed, power loss increases at low frequency as the number of turns must increase. As in [1], a higher number of turns with fixed

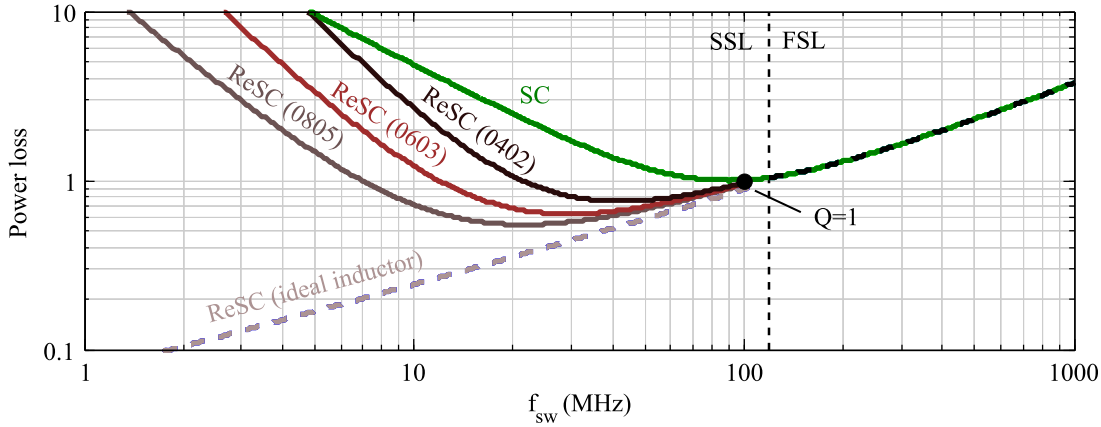


Fig. 3. Comparison of an SC and an ReSC with different inductor sizes (0402, 0603, and 0805) plotted versus frequency. Inductors are scaled to match the resonant frequency to the switching frequency, i.e., the inductance is adjusted to match the resonant frequency and inductor resistance is scaled accordingly. Thus, the quality factor Q is a function of the inductance, inductor resistance, and switch resistance.

TABLE II
DESIGN COMPARISON PARAMETERS

Parameter	Value
Topology	2:1
Process technology	180 nm
Output voltage	3 V
Output current	1 A
Flying capacitance	10 nF
Bottom plate ratio	0.01
Specific switch resistance	1.3 kΩ · μm
Specific gate capacitance	3 fF/μm

volume results in higher resistance and, therefore, higher power loss. At higher frequency, the needed inductance decreases, and resistance is scaled down. In the limit, the fixed footprint curves approach the ideal case, where loss is dominated by the expression in (14). Another observation is that as inductance scales down, the effective quality factor is reduced. For $Q < 1$, it can be seen that the ReSC curves approach the performance of the SC curve, which forms a limiting asymptote in the FSL.

D. Voltage Stress Constraints

Apart from the inductor volumetric constraints, voltage stress presents another limit to designing with very large Q. The charge transfer per cycle is effectively boosted by a factor of Q, which allows ReSC to operate at lower frequency than SC. This inevitably leads to a larger voltage swing on the flying capacitor, which must be rated to support the extra voltage swing. In addition to the higher voltage rating of the capacitor, in many topologies, the semiconductor switches must also be rated to support this extra voltage swing. Consider, for example, the 2:1 topologies in Fig. 2, for which the flying-capacitor voltage swing can be written as

$$\Delta V_{\mathrm{Cx}} = \pi I_{\mathrm{out}} \sqrt{\frac{L_{\mathrm{x}}}{C_{\mathrm{x}}}} \tag{4}$$

$$\Delta V_{\mathrm{Cx}} = \frac{8}{\pi} Q V_{\mathrm{droop}} \tag{5}$$

where ΔV_{Cx} is the peak-to-peak voltage swing on the flying capacitor and V_{droop} can be considered the voltage drop resulting from the loadline of the converter (or voltage drop across R_{eff} in the behavioral model in Fig. 2).

Consider now the two different forms of the ReSC converter shown in Fig. 2. In [28], the topology shown in Fig. 2(b) was termed the "direct" ReSC converter, and Fig. 2(c) was termed the "indirect" ReSC converter. While it may be appreciated that Fig. 2(b) is architecturally identical to the three-level buck converter, the above distinction was made to simplify discussion of the two topologies in pure resonant operation, where they are behaviorally identical except in the form of the inductor current waveform, which is unidirectional (full-wave rectified sine wave) in the direct topology and is bidirectional (sinusoidal) in the indirect topology.

Another important difference between these two topologies relates to voltage stress on the switching devices. The switch voltage stress for the indirect topology in Fig. 2(c) is limited to V_{out} and $V_{\mathrm{in}} - V_{\mathrm{out}}$ (in the 2:1 example, a maximum of $V_{\mathrm{in}}/2 + V_{\mathrm{droop}}$). However, in the direct (three-level) topology in Fig. 2(b), the capacitor voltage swing described by (5) adds to the switch voltage stress (a maximum of $V_{\mathrm{in}}/2 + \Delta V_{\mathrm{Cx}}/2$) and has to be considered when switch blocking voltages are chosen. For high-Q designs, this may be a significant effect and may require a higher blocking voltage for the switching devices. It should be noted that while this conclusion has been based on the nominal 2:1 architectures (see Fig. 2), the same concept extends to many other topologies, and the key point is that the placement of the inductor may have major implications on the voltage stresses in the active devices.

Importantly, (4) shows that the additional voltage stress is dependent on the load current. Therefore, the switch voltage rating can affect the maximum power rating for the design. This highlights a possible advantage of the "indirect" approach to operate with higher power levels for a given voltage rating of the switches even with high-Q designs. However, as discussed in [23], the "direct" topology is more favorable when considering power loss in the inductor due to the substantial dc component of the inductor current waveform. In the rest of this paper, we

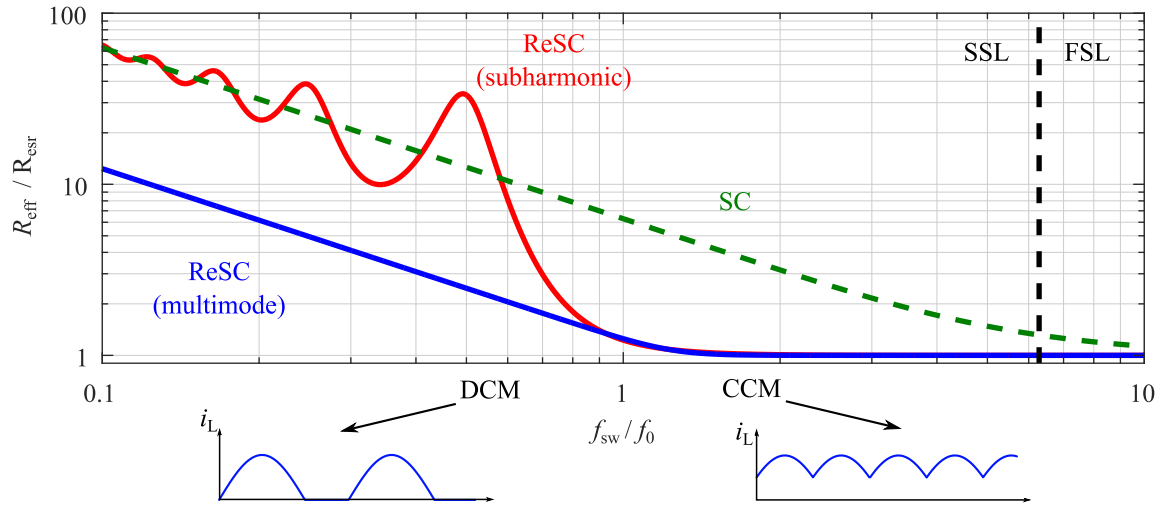


Fig. 4. Comparison of effective output resistance $R_{\rm eff}$ versus frequency of the ReSC converter in multimode operation and the SC converter.

TABLE III
EFFECTIVE RESISTANCE EXPRESSIONS FOR RESC

	DCM	Resonant	CCM	Subharmonic
$\mathbf{R}_{\rm eff}$	$\frac{\pi^2}{8}\frac{f_0}{f_{\rm sw}}R_{\rm esr}$	$\frac{\pi^2}{8}R_{\rm esr}$	$\frac{\pi\left(\frac{f_{\rm sw}}{f_0}\sin\left(\pi\frac{f_0}{f_{\rm sw}}\right)+\pi\right)}{4\left(\frac{f_{\rm sw}}{f_0}\right)^2\left(1-\cos\left(\pi\frac{f_{\rm sw}}{f_0}\right)\right)}R_{\rm esr}$	$\frac{1}{4f_{\rm sw}C_{\rm x}}\left(\frac{\sinh\left(\frac{R_{\rm esr}}{4f_{\rm sw}L_{\rm x}}\right)+\frac{R_{\rm esr}}{4\pi f_{\rm sw}L_{\rm x}}\sin\left(\pi\frac{f_0}{f_{\rm sw}}\right)}{\cosh\left(\frac{R_{\rm esr}}{4f_{\rm sw}L_{\rm x}}\right)-\cos\left(\pi\frac{f_0}{f_{\rm sw}}\right)}\right)$

will primarily focus on "direct" topologies and the potential for these topologies to leverage multimode operation.

III. MULTIMODE OPERATION

A. Resonant Operation in the DCM and the CCM

Thus far, the discussion of ReSC converters was limited to operation at the resonant frequency. In SC converters, the switching frequency is often used to modulate the output impedance and achieve output voltage regulation similar to a linear regulator. While this technique can reduce efficiency depending on the desired output voltage, it inherently offers good light-load efficiency, as the switching frequency scales in proportion to the load current. In [23], it was shown that a similar technique can be applied to ReSC by inserting a dead time between resonant half-cycles and thus achieve regulation by modulating this off time (dynamic off-time modulation). While the same scaling of switching frequency versus output impedance can be achieved with this method, the pulsewidth of the resonant states still needs to be tuned to achieve zero-current switching similar to DCM in inductive converters (e.g., buck).

Analogously to inductive converters, ReSC converters can also be operated in a CCM. In the CCM, the converter switches faster than the resonant frequency, and hence, the inductor current never reaches zero; [22] can be considered an example of this mode of operation. The benefit of operating in the CCM is the lower rms to dc current ratio, which can lead to higher efficiency at high load currents [23]. Thus, resonant operation can be considered a special case at the DCM/CCM boundary. Fig. 4 illustrates the output impedance of an ReSC converter across all operating modes alongside an SC converter with equal flying capacitance. Both $R_{\rm eff}$ curves have very similar shape and approach the same behavior in the limits at low and high frequencies (SSL and FSL). However, the ReSC curve is shifted to the left by roughly a factor of Q (in this case $Q = 4$), which again underlines the potential benefits of ReSC. Exact equations for the output impedance in the three regions of operation are given in Table III. In contrast to SC, the equations are exact in their respective regions of operation and give the same result at the resonant frequency. However, similar to SC, a continuous model over the entire frequency range is desirable to simplify analysis and optimization. A similar approach to the square root law used for SC [5] yields

$$R_{\rm eff,ReSC} = \sqrt[\alpha]{1+\left(\frac{\pi^2}{8}\frac{f_0}{f_{\rm sw}}\right)^{\alpha}}R_{\rm esr} \tag{6}$$

where f_0 is the nominal resonant frequency, $f_{\rm sw}$ is the switching frequency, and α is a behavioral parameter that can be found through regression analysis. A value of $\alpha = 9.2$ was found to be optimal in a least-squared sense and leads to a worst-case error below 2%.

Importantly, the expression in (6) and the multimode curve in Fig. 4 show that the behavior of the hybrid SC converter is quite similar to the behavior of the related SC circuit family. However, the inflection point in the $R_{\rm eff}$ versus frequency curve (similar to the SSL–FSL boundary in SC converters) is shifted to a frequency that is approximately Q times lower. Therefore, the hybrid converter class has the potential, as discussed in

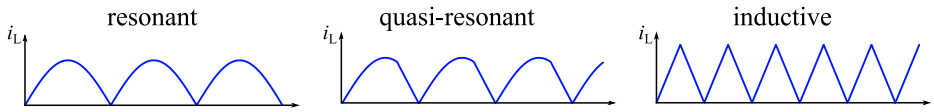


Fig. 5. Conceptual inductor current waveforms in resonant, quasi-resonant, and inductive operating regimes for a hybrid SC converter.

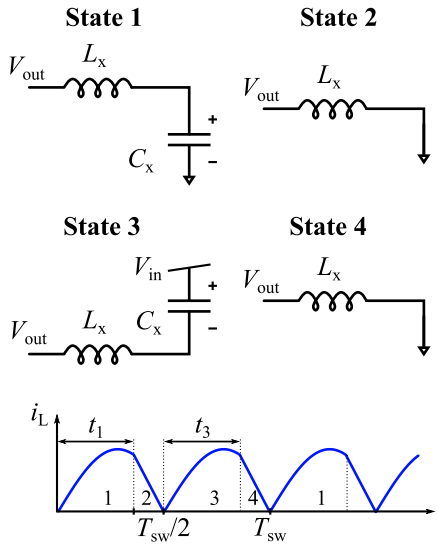


Fig. 6. Circuit states and inductor current waveform for the three-level FCML prototype.

Section II, to maintain favorable tradeoffs between switching and conduction loss compared to pure SC converters.

There is one important caveat to the effective resistance model for hybrid SC converters. While the equivalent series resistance in SC converters can be assumed to be constant across frequency, the inductor resistance in hybrid converters can add a frequency-dependent component. This effect was discussed in [23], and it was concluded that generally the contribution of inductor ac loss is reduced as frequency is increased due to lower ac amplitude of the inductor current. Since the inductor loss is highly nonlinear, this effect has to be evaluated for each design individually.

B. Quasi-Resonant and Inductive Operation

All operating modes described above assume operation at the nominal conversion ratio. In contrast to SC, hybrid SC converters also offer the possibility to introduce extra circuit states, as shown in Fig. 6. The conversion ratio can then be controlled through duty-cycled operation as in a conventional buck converters. Here, the duty cycle is defined as follows:

$$d = \frac{t_1 + t_3}{T_{\rm sw}} \tag{7}$$

where t_1 and t_3 are the time durations of states 1 and 3, respectively, and $T_{\rm sw}$ is the switching period. In normal operation, the inductor current waveform is periodic with $T_{\rm sw}/2$. Therefore, the duty cycle can also be considered the duration of state 1 (or state 3) divided by $T_{\rm sw}/2$. Resonant operation can, hence, be considered a special case with a duty cycle of 1. An example topology that can operate in resonance is the FCML converter. While most of the previous publications do not treat FCML converters in resonant operation, Villar and Alarcón [21] report quasi-resonant behavior in a three-level FCML. Here, quasi-resonant refers to operating conditions, which sill exhibit partially sinusoidal inductor current waveforms but in duty-cycled operation.

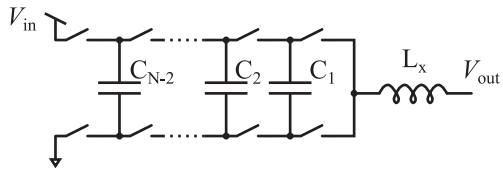


Fig. 7. Circuit schematic of an N-level FCML converter with $N-2$ flying capacitor and $2(N-1)$ switch elements.

Upon closer inspection, it becomes clear that FCML converters can continuously transition between resonant, quasi-resonant, and inductive behavior depending on the applied duty cycle and switching frequency. Fig. 5 shows inductor current waveforms for the different operating regimes. The three-level FCML converter can be shown to operate in all three regimes. Its circuit states are shown in Fig. 6. In resonant operation, only states 1 and 3 are used (duty cycle of 1). When states 2 and 4 are introduced after states 1 and 3, the converter enters a quasi-resonant or inductive mode depending on the applied duty cycle, load current, and switching frequency. It should be noted that, here, only the lowest nominal conversion ratio mode of FCML converters is discussed. However, an N-level FCML converter can operate with $N-1$ conversion ratios, as described in [26] and [31].

IV. FCML Converters

FCML converters are not limited to the three-level converter shown in Fig. 2 but can be extended to an arbitrary number of levels N, where N is the number of possible voltage levels that can be generated at the switching node, which can be written as

$$v_{\rm x} = V_{\rm in}\frac{i}{N-1}, \quad i = 0, \ldots, N-1. \tag{8}$$

The nominal conversion ratio of an N-level FCML is, therefore, $\frac{i}{N-1}$. Since high conversion ratios are the most likely scenario for FCML converters, only the case with $i = 1$ will be treated here. An N level buck converter requires $2(N-1)$ switches, which require a blocking voltage of $\frac{1}{N-1}V_{\rm in}$ (low-side switches can also be replaced by diodes). Additionally, $N-2$ flying capacitors are required, which are exposed to a voltage $V_{C,i} = \frac{i}{N-1}$, where i indicates the placement of the capacitor, as illustrated in Fig. 7. The inherent differences in the capacitor voltages can be important because they affect charge balance and resonant frequency if the capacitor technology has a non-negligible voltage coefficient. These effects will be discussed further with the experimental results.

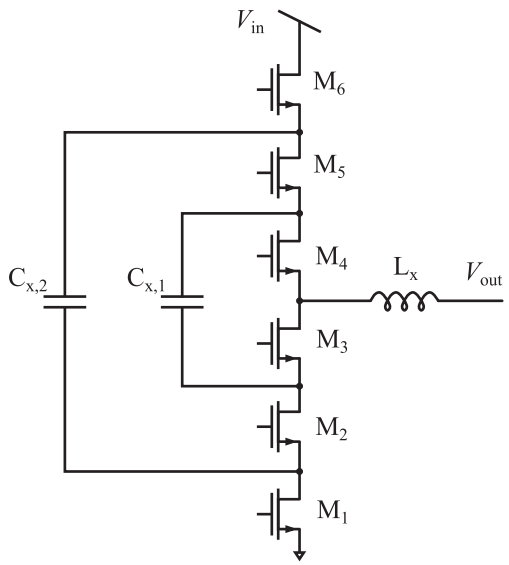


Fig. 8. Circuit schematic of a four-level FCML converter.

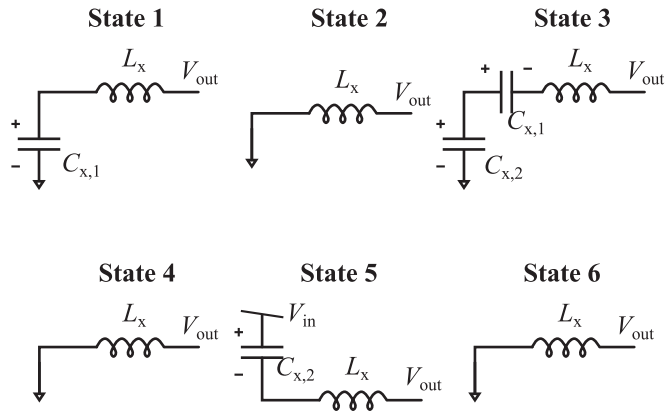


Fig. 9. Circuit states for the four-level FCML prototype

In contrast to the common two-state SC circuits, FCML topologies operate in $N-1$ states. An N-level FCML converter has one state, in which C_1 is connected from ground to the switching node and a state during which C_{N-1} is connected from $V_{\rm in}$ to the switching node. All other states involve two neighboring capacitors connected in series, where the negative terminal of capacitor i is connected to ground and the negative terminal of capacitor $i-1$ is connected to the switching node. As an example, the schematic switch signals and circuit states are shown in Fig. 8 and 9. The voltage at the switching node is thus always approximately $\frac{V_{\rm in}}{N-1}$. Analogously to a buck converter, the switching node can also be connected to ground after each state, which makes the FCML operate similar to a buck converter with an input voltage of $\frac{V_{\rm in}}{N-1}$. However, each switch is only switched once, while the converter goes through all states. Hence, during one switching period, the switching node transitions $N-1$ times between ground and $\frac{V_{\rm in}}{N-1}$, which means the inductor current ripple frequency is effectively multiplied by $N-1$. Consequently, to achieve the same current and output voltage ripple as a buck converter, the passive values can be scaled as follows [23]:

$$L_{\rm FCML} = \frac{1}{(N-1)^2} L_{\rm buck} \tag{9}$$

$$C_{\rm FCML} = \frac{1}{N-1} C_{\rm out} \tag{10}$$

where $L_{\rm FCML}$ and $C_{\rm FCML}$ are the inductance and output capacitance values, respectively, that lead to the same current and voltage ripple in an N-level FCML as $L_{\rm buck}$ and $C_{\rm out}$ in a buck converter. The potential for significantly reducing the required passive component values and the use of lower voltage devices makes the FCML attractive for high-conversion-ratio applications. Moreover, the use of resonant or quasi-resonant modes of operation can offer further advantages as will be demonstrated in the following section.

V. Flying-Capacitor Voltage Balance

So far, the discussion of resonant, hybrid, and soft-charging SC converters has assumed that the flying capacitors operate at fixed dc voltages. In all SC topologies, the flying-capacitor voltages are fractions of the input voltage that are set by the capacitor configuration. In hybrid topologies, the addition of an inductor decouples the flying-capacitor voltages from the output, which adds an additional degree of freedom and thus allows the flying-capacitor voltages to deviate from their nominal values [23], [32]–[34]. There are multiple reasons why this is undesirable. Inductor current ripple increases, and most importantly, both the switch and capacitor voltages stress can increase significantly. The problem becomes intuitively clear when the flying capacitor in a three-level converter is considered. For a simplified case that does not consider current ripple, the voltage change over one switching period can be expressed as follows:

$$V_{\rm drift} = \frac{1}{C_{\rm x}} \left(t_1 I_{\rm L} - t_2 I_{\rm L} \right) \tag{11}$$

where $V_{\rm drift}$ is the drift of the flying-capacitor voltage over one cycle, and t_1 and t_2 are the time periods spent in states 1 and 2, respectively. Even a small offset between t_1 and t_2 can cause the flying-capacitor voltage to deviate far from their nominal values. Consequently, an active feedback control algorithm is often required to maintain the flying-capacitor charge balance.

Many algorithms have been proposed for a related converter class, the modular multilevel converter, which require measurement of all individual flying-capacitor voltages and considerable computing power [35]. However, in lower-power applications, the cost of additional control complexity may hinder the adoption of hybrid SC converters such as the FCML.

For example, a simple method was presented in [23] that involved sampling of the switching nod to detect capacitor imbalance and then correct for this by adjusting the duty cycles of different states in the switching sequence. A potentially more robust and scalable method was hypothesized in [36] and [37]. These works proposed regulating the valley (or minimum) inductor current in each switching state to the same level and demonstrated (experimentally) that this would automatically enforce flying-capacitor voltage balance. A more rigorous math-

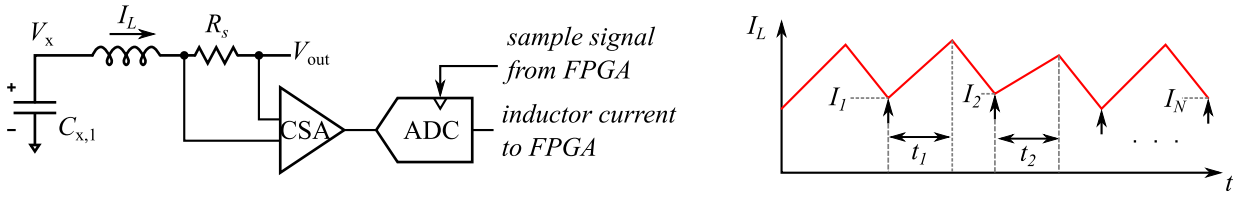


Fig. 10. Schematic of valley current instrumentation that was used for active balancing control.

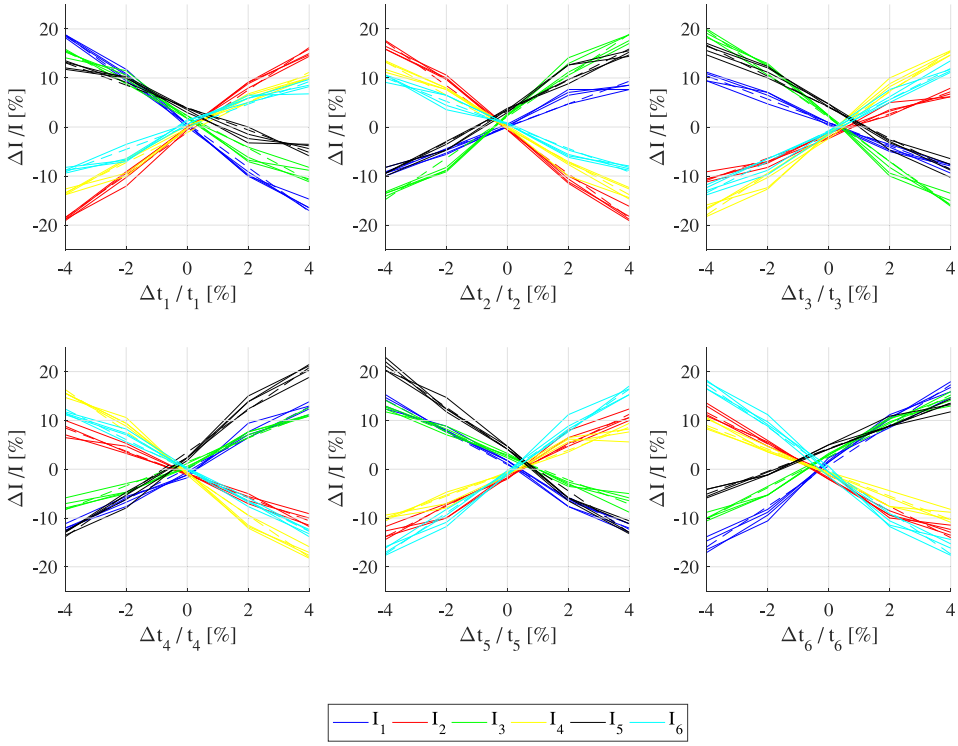


Fig. 11. Measured effect of changing state durations on valley currents.

ematical treatment and experimental validation for the valley current regulation method was provided in [34] and [38]. It was shown that if both valley and peak currents are regulated, then the median voltage of flying capacitors would converge to the correct value.

A similar method was adopted here. Using the instrumentation scheme shown in Fig. 10, the valley currents were sampled and digitized in each switching cycle. Note that Fig. 10 shows an exemplary method to measure and sample the inductor current. In applications where a sense resistor is impractical, a range of other alternatives are possible [39]. A feedback algorithm was used to adjust the time durations (duty cycles) of the different states in order to regulate all valley currents to the same level. In an N-level converter that regulates between the $V_{\text{in}}/(N-1)$ level and ground, there will be $N-1$ valley currents (I_1–I_N), and $N-1$ switching intervals (T_1–T_N), where charge is flowing in the flying capacitors. Changing one time duration affects all valley currents in some way. Fig. 11 shows an example of how changing the time duration of the different states affects the valley currents for a seven-level prototype, e.g., [34]. The seven-level converter has six independent valley currents and, therefore, six time intervals that can be adjusted to affect regulation. By approximating the *t–I* relation as a linear function, the relative gain values can be extracted. Table V shows these values. It can be seen that every time duration most strongly affects the valley current immediately after its corresponding state. The next valley current experiences a similarly strong, but oppositely directed change, with the significance of the change consecutively decreasing for the successive currents. The same principle is also true for the prototypes explored in this work.

Using the linearized gain matrix, a relatively simple control loop can be developed to balance the valley currents and, subsequently, the capacitor voltages. At every iteration, the valley current I_n with the biggest deviation from the average, $\Delta I_n = I_n - \overline{I}$, where $\overline{I}$ is the average of all valley current measurements, is determined. As one can see in Table V, each valley current I_n is most strongly affected by the two control variables T_n and T_{n-1}. For example, if the control algorithm's goal was to increase the value of I_3, it could either decrease T_3 or increase

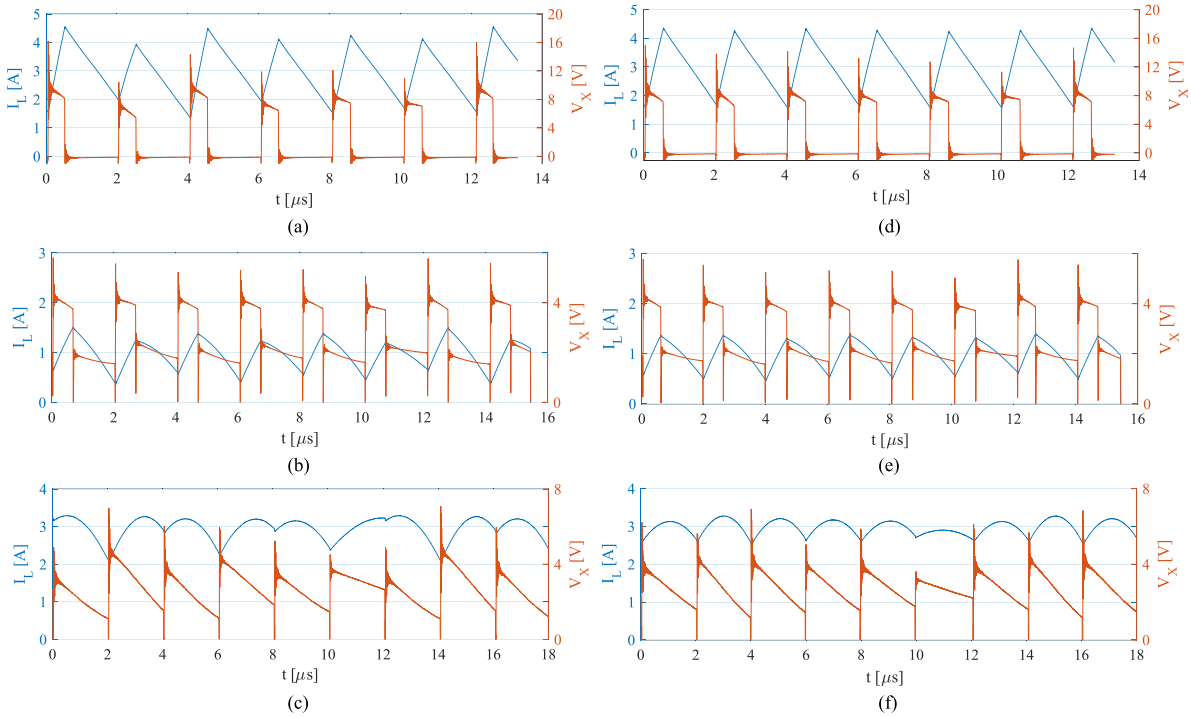


Fig. 12. Measurement results (a)–(c) without and (d)–(f) with balancing in inductive, quasi-resonant, and resonant operation.

T_2. Table V also shows that changing one of these variable will also have a similarly strong inverse effect on either the preceding current value I_{n-1} if T_{n-1} is chosen or the succeeding current I_{n+1} if T_n is chosen as the control variable. Since both control variables affect one of the neighboring currents inversely, the optimal control variable can, therefore, be chosen based on which of the two neighboring currents is the farthest removed from the selected valley current I_n. This will bring both of these values closer together and, therefore, reduce the average absolute deviation of all valley currents, which will eventually lead to a balanced current waveform.

As an example, Fig. 12 shows measurements to highlight the effectiveness of valley current regulation in balancing the flying-capacitor voltage levels. In the unregulated scenario [see Fig. 12(a)–(c)], the flying-capacitor voltages drift, leading to irregularity in the switching node and inductor current waveforms. In the scenario with the valley current regulation active [see Fig. 12(d)–(f)], the valley currents are forced equal, and the switching node becomes symmetric, indicating voltage balance of the flying-capacitor elements. Importantly, as mathematically shown in [34], the result is true in resonant, quasi-resonant, and inductive (buck-like) operation.

VI. Experimental Results

In order to demonstrate the full suite of multimode operating capabilities of the FCML topology, a four-level topology was used. Fig. 14 and 15 show the printed circuit board design and laboratory test setup; Table VI shows the design specifications. Circuit states for four-level operation are summarized in Fig. 9, and the corresponding switching state sequence in Table IV .

In resonant operation, only states 1, 3, and 5 are used. Fig. 13 shows a collection of measured inductor current waveforms across operating modes and duty cycles in four-level operation with an output voltage of 4 V. It can be seen that the converter transitions between resonant, quasi-resonant, and inductive behavior based on the conversion ratio or duty cycle. Moreover, the DCM and the CCM can be applied in all operating regimes. The measurement results emphasize that hybrid SC converters represent a class of converters that has many similarities with SC converters when operated at nominal conversion ratio but can also be operated similar to an inductive converter.

In resonant operation, the inductor current consists of three half periods of sine waves as the converter switches between states 1, 3, and 5. As shown in Fig. 9, in state 3, two flying capacitors are connected in series. The effective capacitance is, therefore, lower than in the two other states, which reduces the resonant frequency in that state. Since the charge transferred in every cycle needs to be equal to maintain the charge balance, the current waveform experiences a higher peak during those states. Beyond that, even though both flying capacitors were nominally identical, since they hold different voltages, the voltage derating of ceramic capacitors additionally affects the effective capacitance in each state. Expect for these asymmetries, the waveforms match very well with the ideal waveforms in Fig. 5.

Fig. 16(a) shows efficiency versus load current for different output voltages with an input voltage of 36 V. Operation with a nominal conversion ratio of 3:1 (resonant) results in a peak efficiency of 95% at 4 A, which drops to 89% for the output voltage of 5 V at 5 A and 84% at 3.3 V, 7 A. At the output current of 7 A and the output voltage of 12 V, the design achieves a power

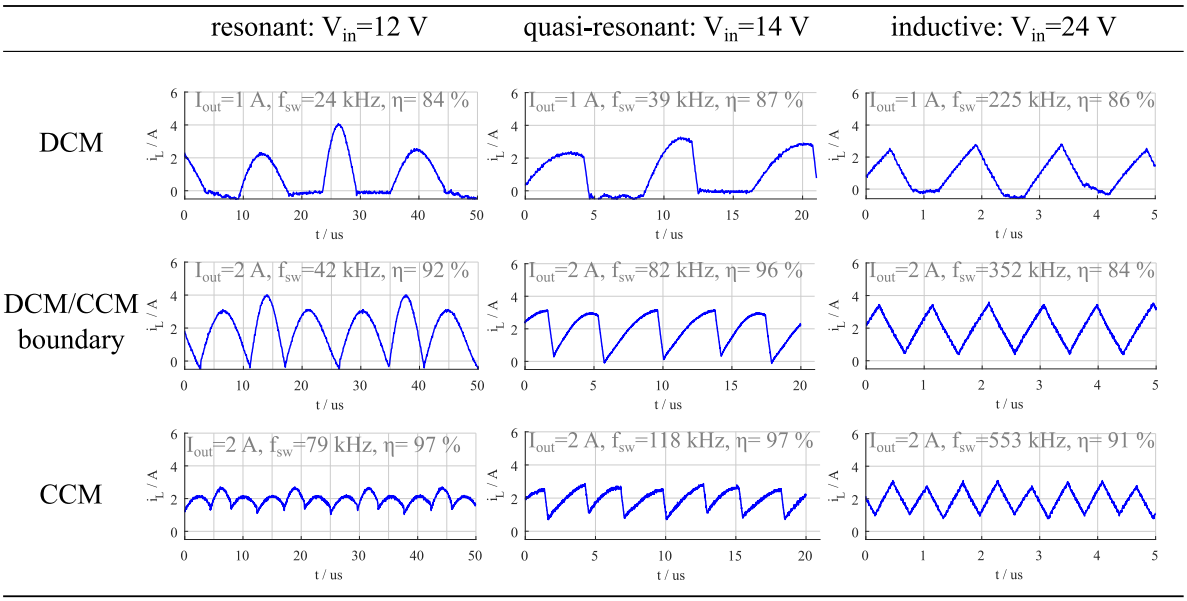


Fig. 13. Measured inductor current waveforms for a four-level converter operating in different regimes with an output voltage of 4 V.

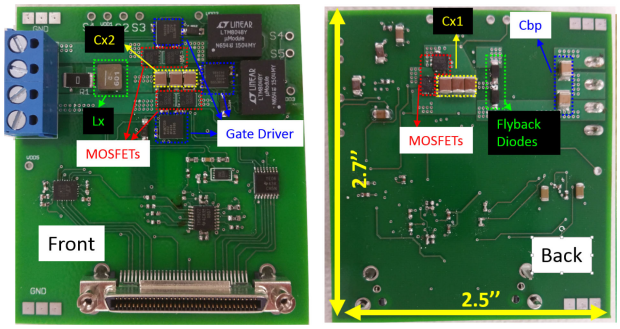
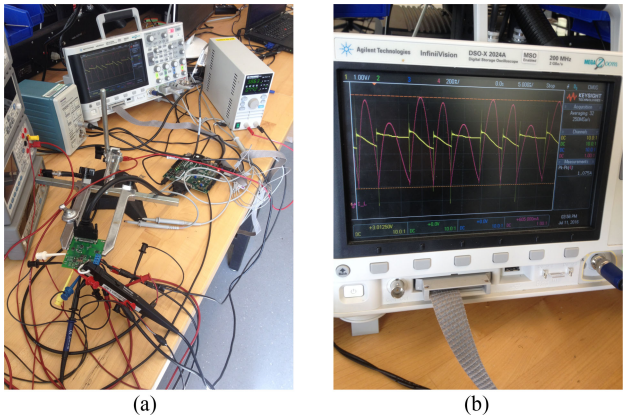


Fig. 14. Annotated photograph of the prototype printed circuit board, showing all main prototype elements.



(a) (b)

Fig. 15. Measurement setup with the hardware prototype. (a) Prototype PCB with an FPGA board and measurement equipment. (b) Oscilloscope waveforms for resonant operation showing inductor current (red) and switching node voltage (yellow).

TABLE IV
SWITCH STATES IN FOUR-LEVEL OPERATION

	State 1	State 2	State 3	State 4	State 5	State 6
$\mathbf{M_1}$	ON	ON	ON	ON	OFF	ON
$\mathbf{M_2}$	ON	ON	OFF	ON	ON	ON
$\mathbf{M_3}$	OFF	ON	ON	ON	ON	ON
$\mathbf{M_4}$	ON	OFF	OFF	OFF	OFF	OFF
$\mathbf{M_5}$	OFF	OFF	ON	OFF	OFF	OFF
$\mathbf{M_6}$	OFF	OFF	OFF	OFF	ON	OFF

TABLE V
RELATIVE EFFECT ON DIFFERENT VALLEY CURRENTS (IN %) OF CHANGING DIFFERENT TIME DURATIONS BY 1%

	I_1	I_2	I_3	I_4	I_5	I_6
T_1	-4.50	4.33	-3.30	3.07	-2.29	2.30
T_2	2.31	-4.50	4.22	-3.39	3.17	-2.40
T_3	-2.37	2.26	-4.45	4.18	-3.17	3.17
T_4	3.16	-2.38	2.44	-4.29	4.33	-3.14
T_5	-3.32	3.14	-2.49	2.36	-4.28	4.22
T_6	4.15	-3.21	3.17	-2.41	2.33	-4.34

TABLE VI
PROTOTYPE SPECIFICATIONS (FOUR-LEVEL)

Parameter	Value
Input voltage	36 V
Output voltage	3.3–12 V
Output current	7 A
Flying capacitance	$2 \times 4.7\ \mu$F
Inductance	600 nH
Nominal conversion ratio	3:1
Switching frequency	80–550 kHz

density of 0.47 kW/in^3 based on the bounding box volume of powertrain and passive components. Light-load operation can be improved by entering a DCM of operation, as shown in Fig. 16(b). In the CCM (constant switching frequency), operation efficiency drops sharply below a load current of 2 A, while DCM operation can maintain above 75% efficiency down to a load current of 0.1 A.

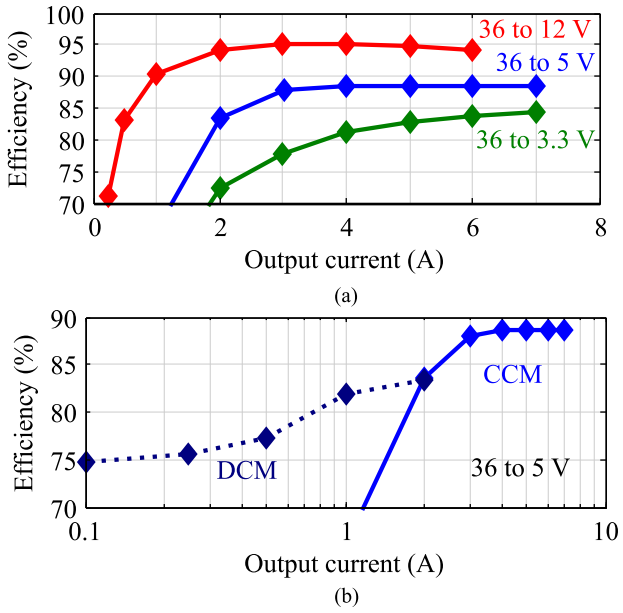


Fig. 16. Measured efficiency of the four-level FCML prototype for various output voltages and load currents.

VII. Conclusion

This paper presented a broader overview of published work on hybrid, resonant, and soft-charging SC converters. An analytical and simulation-based comparison between ReSC and SC converters was presented, and the benefits were discussed. Moreover, a general description of the different regions of operation of hybrid SC converters is provided that includes continuous and discontinuous modes of operation, and a behavioral model is presented that expresses the effective output impedance as a function of relative frequency and equivalent resistance. Moreover, additional operating regimes are discussed, including duty-cycled operation similar to inductive converters, which lead to quasi-resonant and inductive operating regimes. A four-level FCML converter prototype is then used to demonstrate all of the operating modes. The prototype operates with an input voltage of 36 V and achieves up to 95% efficiency in resonant operation. Experimental results show that a single converter can transition between resonant, quasi-resonant, and inductive modes of operation, and that all of them can also be combined with the DCM.

Appendix A

Design Optimization

The optimization procedure for an ReSC design is similar to SC in terms of modeling power loss [29], [40], [41]. The total power loss is computed as the sum of a frequency-dependent portion (switching loss) and a load-dependent portion (conduction loss). With an assumption that the converter is operated at the resonant frequency, and that $Q > 1$, a simplified but reasonably accurate expression follows:

$$P_{\text{loss}} = \frac{\pi^2}{8}\frac{R_{\text{on,sp}}}{W_{\text{sw}}} I_{\text{out}}^2 + E_{\text{g,sp}} W_{\text{sw}} f_{\text{sw}}. \tag{12}$$

In (12), $R_{\text{on,sp}}$ is the specific ON-resistance of the switches, $E_{\text{g,sp}}$ is the specific energy needed to drive the switches, and W_{sw} is the total switch width. In a simplified scenario, $E_{\text{g,sp}} = C_{\text{g,sp}} V_{\text{g}}^2$, with $C_{\text{g,sp}}$ being specific input capacitance and V_{g} being the gate-drive voltage. However, the form with $E_{\text{g,sp}}$ can be appreciated as a more general expression. It should also be noted that (12) has assumed the simplified expression for R_{eff} shown in (2). While a more complicated expression was used in [25], it can be shown that (2) is very accurate for $Q > 3$ and maintains reasonable accuracy for $Q > 1$. Inductor loss is not considered as it is independent of the chosen switch width and does, therefore, not affect the result of the optimization. Based on (12), the optimum switch width W_{opt} and the minimum power loss P_{min} can be derived as

$$W_{\text{opt}} = \frac{\pi I_{\text{out}}}{4\sqrt{f_{\text{sw}}}} \sqrt{\frac{R_{\text{on,sp}}}{E_{\text{g,sp}}}} \tag{13}$$

$$P_{\text{min}} = 2\pi I_{\text{out}} \sqrt{f_{\text{sw}}} \sqrt{R_{\text{on,sp}} E_{\text{g,sp}}}. \tag{14}$$

It should be noted that that (14) represents only the loss in the semiconductor switches, not the inductor loss, which has to be modeled separately.

Appendix B

List of Acronyms

SC	Switched capacitor.
ReSC	Resonant switched capacitor.
SSL	Slow switching limit.
FSL	Fast switching limit.
DCM	Discontinuous conduction mode.
CCM	Continuous conduction mode.

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