Interleaved Operation of Two Neutral-Point-Clamped Inverters With Reduced Circulating Current

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***Abstract*—Parallel inverters are commonly adopted in high-power applications, for instance wind energy systems, smart transformers, and power conditioners. Meanwhile, interleaved pulse width modulation is usually considered as an optimal approach to reduce the current ripple and harmonics of the parallel inverters. However, in the case of a common dc link, the problem of circulating current emerges and leads to performance degradation. This paper aims at investigating the influence of different modulation techniques on the circulating current of two neutral-point-clamped (NPC) inverters under interleaved operation. Two modulation techniques, phase disposition (PD) and alternative phase opposite disposition (APOD), have been studied and compared in terms of current ripple, spectrum quality, and circulating current. Though the PD modulation was regarded as the optimum solution in most of the single-NPC cases, it offers worse performance in the two parallel NPC applications due to higher circulating current. Simulation and experimental validations are provided and show that the APOD leads to much lower circulating current and similar current ripple as well as spectrum quality compared to the PD.**

***Index Terms*—Alternative phase opposite disposition (APOD), circulating current, interleaved operation, neutral-point-clamped (NPC) inverters, parallel inverters, phase disposition (PD).**

I. Introduction

PARALLEL inverters are widely utilized in high-power applications, including multimegawatt wind energy systems [1], smart transformer applications [2], static synchronous compensators [3], active power filters [4], and electric drives [5]. To improve the current waveform quality, interleaved operation is employed to shift the carrier phases among different modules [6], [7]. In this way, the current ripple of the total current can be reduced and, therefore, reduces the size of coupled inductors. Nevertheless, in the case of a common dc link, the circulating current issue raises and would cause critical problems in terms of overcurrent, higher voltage drop, and higher (thermal) stress for both semiconductors and dc capacitors. For parallel two-level inverters, it is well known that modulation is one of the key factors that determine the circulating current [6]. Optimized modulation techniques have been proposed to minimize the circulating current and largely improve the overall performance [8], [9]. However, for the three-level neutral-point clamp (NPC), this issue and the optimum modulation with reduced circulating current were seldom studied in the literature.

Traditionally, two common carrier-based modulation techniques are employed in a three-level NPC inverter: phase disposition (PD) and alternative phase opposite disposition (APOD). The PD modulation is considered as the best solution in the single-NPC inverter, which leads to better waveform and spectrum quality [7], [10]. However, for parallel NPC inverters with a common dc link, the circulating current has to be taken into account during the performance evaluation. With this consideration, it is necessary to reexamine the characteristics of the two well-known modulations in an extensive way.

The main aim of this paper is to investigate the impact of different three-level NPC modulation techniques on the circulating current of two NPC inverters under interleaved operation and to find a superior solution for the medium-voltage (MV) grid impedance measurement application. In these regard, the common-mode voltage and the circulating current of both the PD and the APOD modulation techniques are studied. Mathematical models describing the circulating current are presented with the consideration of various switching sequences. Moreover, the expressions of peak-to-peak (p-2-p) and root-mean-square (rms) values of the circulating current by using both modulation techniques are calculated, which could facilitate the common-mode filter design in two parallel NPC applications. The performance evaluation in the time domain and the phase domain are carried out by simulation and experimental validations.

The rest of this paper is organized as follows. The description of an MV grid impedance measurement system consisting of parallel low-voltage (LV) NPC inverters is given in Section II, with the detailed control and synchronization schemes. Meanwhile, the problem of circulating current between two parallel NPC inverters under interleaved operation is discussed. Then, the two common multilevel modulation techniques are investigated and evaluated in Section III in terms of the common-mode voltage and the circulating current. The models and expressions

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of the circulating current are given in this section as well. Simulation and experimental results are provided in Section IV to validate the theoretical analyses. Conclusions are drawn in Section V.

II. System Configuration and Problem Description

This section describes an MV grid impedance measurement as an example of parallel NPC inverters in high-power applications. In order to improve the quality of the total current, interleaved operation is chosen as an optimal solution. The problem description of the parallel NPC inverters in terms of the common-mode voltage and the circulating current is discussed in this section.

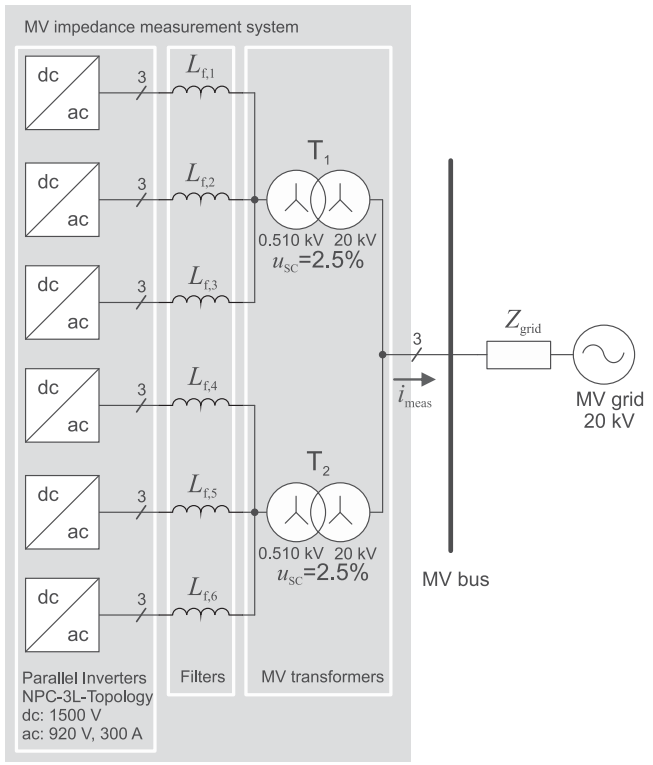
A. MV Grid Impedance Measurement

The system configuration of the grid impedance measurement system is shown in Fig. 1(a), where two MV/LV transformers are connected in parallel and each of them connects to three inverters at the LV side. Filters such as *dv/dt* filters and common-mode filters are adopted between transformers and inverters. A three-level NPC topology is selected because more levels help to track current signals with high frequencies and, at the same time, achieve high power rating. The measurement system is able to inject monofrequency current i_{meas} ranging from 100 Hz to 10 kHz, which excites the MV grid voltage (e.g., 1% nominal voltage excitation) at the corresponding frequencies [11]. The equivalent grid impedance Z_{grid} at the specific frequency can be calculated, and the measuring procedure would be repeatedly carried on with required frequency resolution.

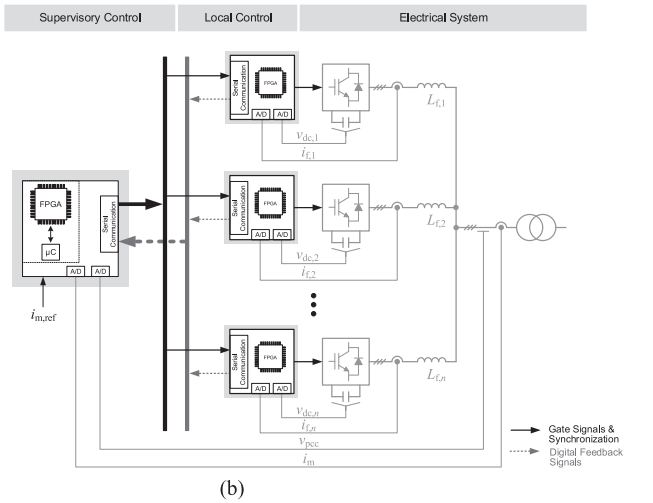
A hierarchical structure is considered for controlling the grid impedance measurement system [shown in Fig. 1(b)]. The control algorithm and grid synchronization are implemented in the master controller, which is a *Xilinix ZC702 Evaluation Board* based on *Xilinx Zynq-7000* that includes a *Dual ARM Cortex-A9*-based processor and a *7-series-fabric*-based programmable logic. A *Xilinx Spartan-3E* is employed for each NPC inverter as the slave controller, and its main functionalities include signal (e.g., ac/dc voltage and ac current) measuring and processing, monitoring, and protection. Serial communication is used to exchange data between the master and the slave controllers.

1) Circulating Current: For parallel inverter applications, the interleaved operation is usually considered as an optimal solution because of the power quality improvement of the total current. The interleaved pulse width modulation operation requires the carriers for adjacent inverters to be phase shifted by 360°/n so that a reduced amplitude of the total current ripple can be achieved [4]. Here, n is the number of the parallel inverters. For instance, if a two-inverter system is considered, a 180° phase shift is used between two inverter carriers. When a shared dc link is used, the common-mode voltage among different inverters will appear, which leads to the circulation of the current among the modules. An example of the cause of the common-mode voltage and the circulating current between two NPC inverters is depicted in Fig. 2. The common-mode voltage v_{cm} can be defined by

$$v_{\mathrm{cm}} = v_{\mathrm{cm1}} - v_{\mathrm{cm2}} = \frac{v_{\mathrm{az1}} + v_{\mathrm{bz1}} + v_{\mathrm{cz1}}}{3} - \frac{v_{\mathrm{az2}} + v_{\mathrm{bz2}} + v_{\mathrm{cz2}}}{3} \quad (1)$$



(a)



(b)

Fig. 1. Grid impedance measurement system. (a) System configuration. (b) Control structure.

where v_{cm1} and v_{cm2} are the common-mode voltages of the two inverters, v_{kz1} and v_{kz2} $(k = a, b, c)$ are the terminal voltages (phase-to-neutral) of inverter 1 and inverter 2, respectively. The circulating current i_{cir} between two inverters can be calculated by

$$i_{\mathrm{cir}} = \frac{3}{2L_f} \int v_{\mathrm{cm}}(t)dt. \quad (2)$$

Here, L_f is the equivalent inductance of the filter of each inverter.

In Fig. 2, the worst case considering the possible modulation is demonstrated, where the switching states of the two inverters are [POP] and [ONO], respectively. Switching state "P" denotes

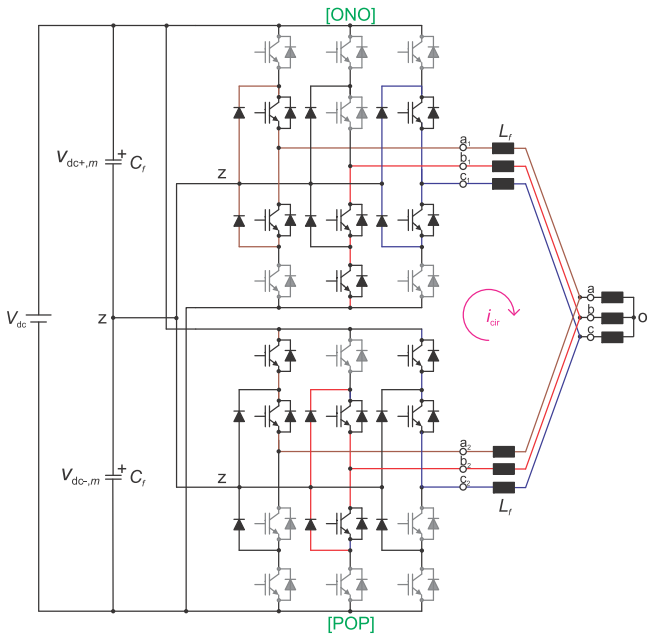


Fig. 2. Example of the common-mode voltage and the circulating current between two parallel NPC inverters.

that the upper two switches in each leg are ON and the inverter terminal voltage at that leg is $+V_{\rm dc}/2$, whereas "N" indicates that the lower two switches conduct, leading to the terminal voltage equals to $-V_{\rm dc}/2$. Switching state "O" represents that the inner two switches are ON and the terminal voltage is clamped to zero through the diodes. The detailed switching states of the worst case are illustrated in the figure with the black ones switched ON and the gray ones be OFF. It can be seen that the common-mode voltage between two inverters in this case is half of the dc-link voltage, which leads to considerable circulating current.

In the previous literature, it is known that the magnitude of the common-mode voltage between two inverters highly depends on the switching sequences of both inverters [8], [12]. As a result, the modulation techniques could be one of the most important factors to determine the common-mode voltage and the circulating current. The relationship between the modulation and the circulating current in two-level inverters has been well studied in the literature [6], [13]. Several optimized modulation techniques have been proposed and aimed at reducing the circulating current while maintaining other grateful features, such as the number of commutations, current spectrum, etc. [6], [13]–[15]. However, in parallel NPC applications, the topic of modulation techniques concerning the circulating current has seldom been investigated. In order to find a best modulation technique for the parallel NPCs, the analysis and validations are given in the following sections.

III. Superior Modulation for Paralleled NPC Inverters

In this section, two well-known carrier-based modulation techniques, PD and APOD, are evaluated for parallel NPC inverters. The common-mode voltage and the circulating current between two parallel inverters are analyzed. The mathematical models of circulating current using two different modulation are presented, and the expressions of the p-2-p and the rms values of the circulating current are calculated for the evaluation.

A. Modulation for a Single Three-Level NPC Inverter

For the multilevel inverter, three level-shifted carrier-based modulation techniques are usually considered: PD, phase opposite disposition (POD), and APOD [7]. For PD, all carriers are in phase; for POD, carriers above the zero point are out of phase with those below zero by 180°; and for APOD, carriers in adjacent bands are phase shifted by 180°. An example of the three modulation techniques is shown in Fig. 3 with a carrier frequency of 500 Hz. Since only two carriers are utilized in the three-level NPC inverter, the POD and the APOD are identical. In the literature, it is shown that the PD modulation strategy provides better performance in terms of harmonic profile and current ripple [7], [16]. As a result, for three-level NPC inverter that uses carrier-based modulation, PD has been employed as a common modulation technique and is even used for optimized space-vector modulation (SVM) [14]. Nevertheless, for the parallel NPCs, this conclusion would be questioned when additional aspects are considered. An example is presented in [17], showing that the PD modulation has bad influence on the current balancing between cells of the same phase, while POD/APOD is better in terms of the differential model of phase current. When a common dc link is implemented, it is necessary to take the circulating current into account as one of the main indices in paralleled NPC inverters under interleaved operation.

B. Division of Sectors and Regions

According to (1) and (2), the common-mode voltage and the terminal voltages of both inverters should be obtained for the calculation of the circulating current. Since the switching sequences determine the terminal voltages, all the switching sequences of both modulation techniques should be enumerated and utilized for evaluation. For analysis convenience, the division of sectors and regions used in the SVM can be utilized for categorizing the switching sequences. In particular, the switching sequences of the PD modulation are identical to that of the SVM given in [14] and [18].

The duty cycles to generate three-phase balanced sinusoidal voltages are given by

$$\begin{aligned} d_a &= m \cdot \sin(\omega t) \\ d_b &= m \cdot \sin\left(\omega t - \frac{2\pi}{3}\right) \\ d_c &= m \cdot \sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{3}$$

where m is the modulation index. For these three-phase signals, six sectors are divided as shown in Fig. 4(a) according to [14]. Depending on the switching sequences, each sector can be further divided into four triangular regions (e.g., 1–4 in Sector I). The division of sectors and regions as well as the

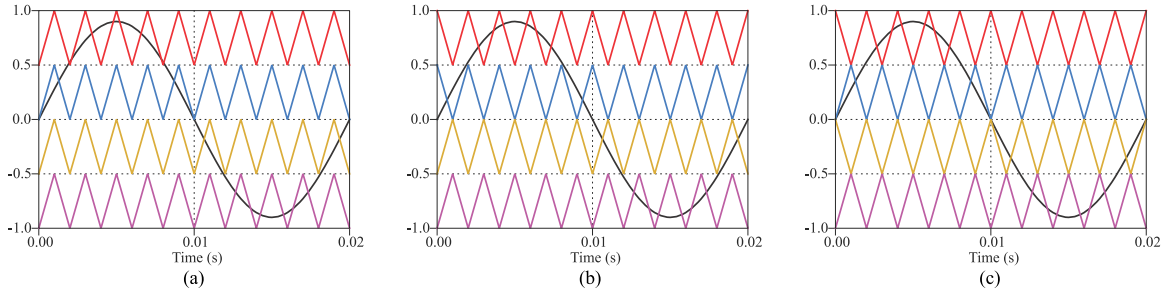


Fig. 3. Carrier-based level-shifted modulation techniques for multilevel inverters: (a) PD, (b) POD, and (c) APOD.

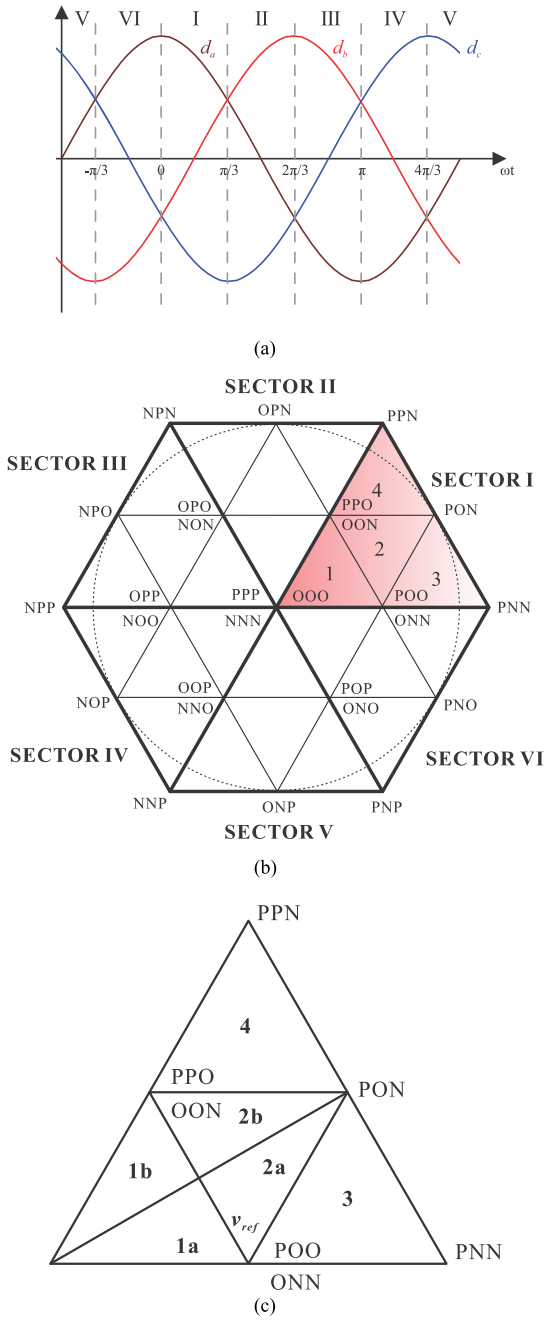


Fig. 4. Fundamental signals and modulation vectors. (a) Fundamental modulation signals. (b) Division of sectors and regions. (c) Division of six regions of Sector I.

switching states is given in Fig. 4(b). Since the characteristics (e.g., switching sequences) of each sector are similar to the others, only Sector I has been taken into account for the sake of simplicity. In the switching sequence design for SVM, one small vector among three selected vectors method is commonly adopted to minimize the neutral-point voltage deviation [7], and a typical seven-segment switching sequence can be obtained. It is worth noting that each small vector has two switching states (e.g., [OON] and [POO]), which leads to the fact that regions 1 and 2 can be further divided into two subregions, as shown in Fig. 4(c). As a result, two types of seven-segment switching sequences will be employed in subregion-a and subregion-b, respectively. For instance, in Sector I region 1, the seven-segment switching sequences in Sector I-2a and Sector I-2b are [ONN], [OON], [PON], [POO], [PON], [OON], [ONN] and [OON], [PON], [POO], [PPO], [POO], [PON], [OON], respectively.

C. PD Versus APOD Under Interleaved Operation

According to the division of Fig. 4(c), the terminal voltages of inverters and the common-mode voltage in each region of Sector I using the PD and the APOD are investigated. An example of the terminal voltages of two inverters of Sector I-1a is given, with two different modulation techniques presented in Fig. 5. In both figures, V_{cp1} and V_{cn1} are the positive and the negative carriers of the first inverter, and V_{cp2} and V_{cn2} are the positive and the negative carriers of the second inverter. d_a, d_b, and d_c represent the duty cycles at that sampling interval, while v_{kz1} and v_{kz2} $(k = a, b, c)$ are the terminal voltages of first and second inverters, respectively. The periods of switch-ON (T_{kz}) and switch-OFF ($\overline{T}_{kz}$) of each phase $(k = a, b, c)$ of Fig. 5 can be easily obtained and shown in (4) and (5), respectively:

$$T_{kz} = |d_k| \cdot T_s, \qquad k = a, b, c \tag{4}$$

$$\overline{T}_{kz} = (1 - |d_k|) \cdot T_s, \qquad k = a, b, c. \tag{5}$$

Based on the terminal voltages, the common-mode voltage between two parallel NPC inverters can be obtained using (1). Depending on the magnitude of the common-mode voltage, seven segments are divided with different gray shades in each half sampling interval. The darker segment represents the higher common-mode voltage, for example, in the middlemost area of PD modulation, two switching states, [ONN] and [POO], were applied to the two inverters, respectively, resulting in the highest common-mode voltage between two modules. It is worth noting that the definition of segments (based on common-mode

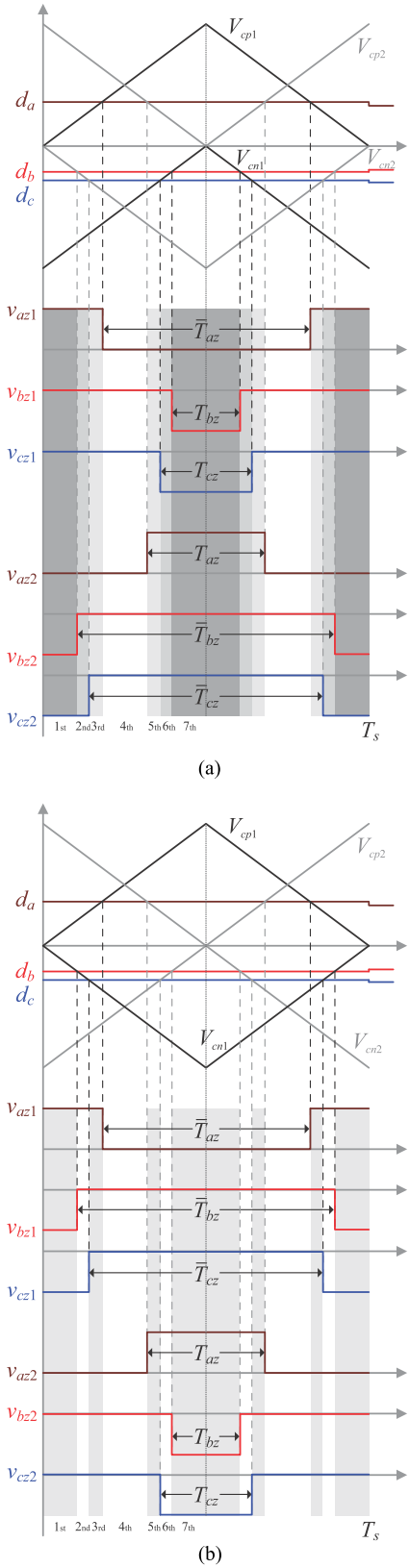


Fig. 5. Terminal voltages of parallel NPC inverters in Sector I-1a with different modulation techniques (the levels of grays are used to highlight the magnitude of common-mode voltage). (a) PD and (b) APOD.

TABLE I
COMPARISONS OF THE COMMON-MODE VOLTAGE OF SECTOR I

PD modulation						
Segment	1a	1b	2a	2b	3	4
First	$3E$	$3E$	$3E$	$3E$	$3E$	$3E$
Second	$2E$	$2E$	$2E$	$2E$	$2E$	$2E$
Third	E	E	E	E	E	E
Fourth	0	0	0	0	0	0
Fifth	$-E$	$-E$	$-E$	$-E$	$-E$	$-E$
Sixth	$-2E$	$-2E$	$-2E$	$-2E$	$-2E$	$-2E$
Seventh	$-3E$	$-3E$	$-3E$	$-3E$	$-3E$	$-3E$
APOD modulation						
Segment	1a	1b	2a	2b	3	4
First	$-E$	E	$-E$	E	$-E$	E
Second	0	0	0	0	$-2E$	$2E$
Third	E	$-E$	$-E$	E	$-E$	E
Fourth	0	0	0	0	0	0
Fifth	$-E$	E	E	$-E$	E	$-E$
Sixth	0	0	0	0	$2E$	$-2E$
Seventh	E	$-E$	E	$-E$	E	$-E$

voltage) here is different from the definition of seven-segment switching sequence (based on the switching states) mentioned before. The common-mode-voltage-related segment sequences (first, second, to seventh) of both modulation techniques are denoted in the time axis of Fig. 5.

The methodology of common-mode voltage calculation used for Sector I-1a is then applied to the rest regions of Sector I. Likewise, seven common-mode-voltage-related segment sequences of each region can be derived, and the corresponding common-mode voltages can be calculated by the terminal voltages using (1). The common-mode voltages of all regions of Sector I for both modulation techniques are listed in Table I, where $E = V_{\rm dc}/6$. It can be seen that the common-mode voltage using the PD technique varies from $-3E$ to $3E$ in all regions, while the common-mode voltage using the APOD varies from $-E$ to E in regions 1 and 2, and from $-2E$ to $2E$ in regions 3 and 4. Comparing the values in each segment, it is seen that the common-mode voltage of the PD technique is higher than that of the APOD technique of all common-mode-voltage-related segments of Sector I, which conjectures that the PD incurs higher circulating current. Especially, with a low modulation index ($m \leq 0.575$), switching sequences of regions 1 and 2 would have a dominant influence on the common-mode voltage and the circulating current.

The detailed common-mode voltage shapes ($v_{\rm cm}$) between two inverters in one sampling interval of all regions using the PD and the APOD are presented in Fig. 6. The circulating current between two modules can be calculated using (2), and the waveforms are shown in figures by the magenta curves. Comparing Fig. 6(a) to Fig. (b)–(d), it can be seen that the common-mode voltage in each sampling interval using the PD is higher than that using the APOD in all regions, which leads to a higher circulating current between two inverters.

Then, to quantify the circulating currents for different modulation techniques in Sector I, the p-2-p value and the rms value in

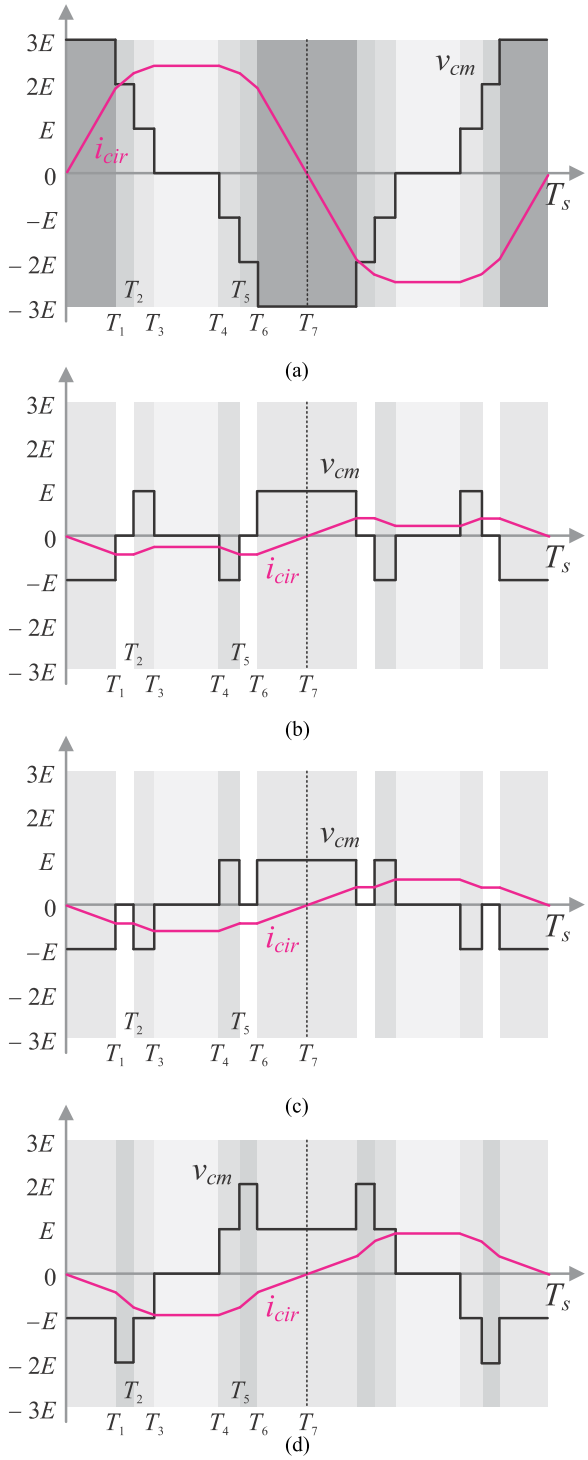


Fig. 6. Common-mode voltage and the circulating current between parallel NPC inverters in Sector I with different modulation techniques: (a) PD (all regions), (b) APOD (region 1), (c) APOD (region 2), and (d) APOD (regions 3 and 4).

each sampling interval are evaluated. Assuming that the initial value of the circulating current at the beginning of each interval is zero, the expressions of the circulating currents in Sector I by using the PD and the APOD are given by (6) and (7)–(9), respectively:

$$i_{\text{cir}}^{\text{PD}} = \begin{cases} \frac{9E}{2L_f}t, & 0 \le t \le T_1 \\ \frac{3E}{2L_f}(T_1 + 2t), & T_1 < t \le T_2 \\ \frac{3E}{2L_f}\left(\sum_{k=1}^{2} T_k + t\right), & T_2 < t \le T_3 \\ \frac{3E}{2L_f}\left(\sum_{k=1}^{3} T_k\right), & T_3 < t \le T_4 \\ \frac{3E}{2L_f}\left(\sum_{k=1}^{4} T_k - t\right), & T_4 < t \le T_5 \\ \frac{3E}{2L_f}\left(\sum_{k=1}^{5} T_k - 2t\right), & T_5 < t \le T_6 \\ \frac{3E}{2L_f}\left(\sum_{k=1}^{6} T_k - 3t\right), & T_6 < t \le T_7 \end{cases} \tag{6}$$

$$i_{\text{cir,region1}}^{\text{APOD}} = \begin{cases} -\frac{3E}{2L_f}t, & 0 \le t \le T_1 \\ -\frac{3E}{2L_f}T_1, & T_1 < t \le T_2 \\ \frac{3E}{2L_f}\left(-\sum_{k=1}^{2} T_k + t\right), & T_2 < t \le T_3 \\ \frac{3E}{2L_f}\left(-\sum_{k=1}^{2} T_k + T_3\right), & T_3 < t \le T_4 \\ \frac{3E}{2L_f}\left(-\sum_{k=1}^{2} T_k + \sum_{k=3}^{4} T_k - t\right), & T_4 < t \le T_5 \\ \frac{3E}{2L_f}\left(-\sum_{k=1}^{2,5} T_k + \sum_{k=3}^{4} T_k\right), & T_5 < t \le T_6 \\ \frac{3E}{2L_f}\left(-\sum_{k=1}^{2,5,6} T_k + \sum_{k=3}^{4} T_k + t\right), & T_6 < t \le T_7 \end{cases} \tag{7}$$

$$i_{\text{cir,region2}}^{\text{APOD}} = \begin{cases} -\frac{3E}{2L_f}t, & 0 \le t \le T_1 \\ -\frac{3E}{2L_f}T_1, & T_1 < t \le T_2 \\ -\frac{3E}{2L_f}(T_1 - T_2 + t), & T_2 < t \le T_3 \\ -\frac{3E}{2L_f}(T_1 - T_2 + T_3), & T_3 < t \le T_4 \\ -\frac{3E}{2L_f}\left(\sum_{k=1}^{3,4} T_k - T_2 - t\right), & T_4 < t \le T_5 \\ -\frac{3E}{2L_f}\left(\sum_{k=1}^{3,4} T_k - T_2 - T_5\right), & T_5 < t \le T_6 \\ -\frac{3E}{2L_f}\left(\sum_{k=1}^{3,4,6} T_k - T_2 - T_5 - t\right), & T_6 < t \le T_7 \end{cases} \tag{8}$$

$$i_{\text{cir,region3,4}}^{\text{APOD}} = \begin{cases} -\dfrac{3E}{2L_f}t, & 0 \le t \le T_1 \\ \dfrac{3E}{2L_f}T_1 - \dfrac{6E}{2L_f}t, & T_1 < t \le T_2 \\ \dfrac{3E}{2L_f}(T_1 - T_2 - t), & T_2 < t \le T_3 \\ \dfrac{3E}{2L_f}(T_1 - \sum_{k=2}^{3} T_k), & T_3 < t \le T_4 \\ \dfrac{3E}{2L_f}(T_1 - \sum_{k=2}^{4} T_k + t), & T_4 < t \le T_5 \\ \dfrac{3E}{2L_f}(T_1 - \sum_{k=2}^{5} T_k + 2t), & T_5 < t \le T_6 \\ \dfrac{3E}{2L_f}(T_1 + T_6 - \sum_{k=2}^{5} T_k + t), & T_6 < t \le T_7 \end{cases} \quad (9)$$

where T_1–T_7 are the time of the seven common-mode-voltage-related segments indicated in Fig. 6 and can be calculated as follows:

$$\begin{aligned} &m \le 0.5: \\ &T_1 = \frac{T_s - \overline{T}_{\text{max,z}}}{2}, T_2 = \frac{T_s - \overline{T}_{\text{mid,z}}}{2}, T_3 = \frac{T_s - \overline{T}_{\text{min,z}}}{2}, \\ &T_4 = \frac{T_s - T_{\text{max,z}}}{2}, T_5 = \frac{T_s - T_{\text{mid,z}}}{2}, T_6 = \frac{T_s - T_{\text{min,z}}}{2}, \\ &T_7 = \frac{T_s}{2} \\ &m > 0.5: \\ &T_1 = \frac{T_s - T_{\text{max,z}}}{2}, T_2 = \frac{T_s - T_{\text{mid,z}}}{2}, T_3 = \frac{T_s - T_{\text{min,z}}}{2}, \\ &T_4 = \frac{T_s - \overline{T}_{\text{max,z}}}{2}, T_5 = \frac{T_s - \overline{T}_{\text{mid,z}}}{2}, T_6 = \frac{T_s - \overline{T}_{\text{min,z}}}{2}, \\ &T_7 = \frac{T_s}{2} \end{aligned} \quad (10)$$

where $T/\overline{T}_{\text{max,mid,min,z}}$ indicate the maximum, middle, minimum values of the switching ON/OFF periods given by (4) and (5). Noting that, if the half sampling interval is considered, the durations of the common-mode-voltage-related segments have reflection symmetry to the quarter of a sampling period. For instance, substituting (4) and (5) into (10), the durations of second and sixth segments are

$$\begin{aligned} T_{1\div 2} = T_2 - T_1 &= \frac{T_s - \overline{T}_{\text{mid,z}}}{2} - \frac{T_s - \overline{T}_{\text{max,z}}}{2} \\ &= \frac{(|d_{k,\text{mid}}| - |d_{k,\text{min}}|) \cdot T_s}{2} \\ T_{5\div 6} = T_6 - T_5 &= \frac{T_s - T_{\text{min,z}}}{2} - \frac{T_s - T_{\text{mid,z}}}{2} \\ &= \frac{(|d_{k,\text{mid}}| - |d_{k,\text{min}}|) \cdot T_s}{2}. \end{aligned} \quad (11)$$

Here, $|d_{k,\text{mid}}|$ and $|d_{k,\text{min}}|$ are the middle and minimum absolute values of the duty cycles. Obviously, the durations of the two intervals are identical, and $T_{0\div 1} = T_{6\div 7}$, $T_{2\div 3} = T_{4\div 5}$, and $T_{3\div\frac{T_s}{4}} = T_{\frac{T_s}{4}\div 4}$ are established as well. With this consideration, for the calculation of the p-2-p value and the rms value, only a quarter of a sampling period ($\frac{T_s}{4}$) needs to be taken into account.

The p-2-p values of circulating current by using the PD and the APOD modulation can be written by

$$i_{\text{cir, p-2-p}}^{\text{PD}} = \begin{cases} \dfrac{3ET_s}{2L_f}(|d_{k,\text{max}}| + |d_{k,\text{mid}}| + |d_{k,\text{min}}|), & \text{Region 1} \\ \dfrac{3ET_s}{2L_f}(3 - |d_{k,\text{max}}| - |d_{k,\text{mid}}| - |d_{k,\text{min}}|), & \text{Regions 2–4} \end{cases} \quad (12)$$

$$i_{\text{cir, p-2-p}}^{\text{APOD}} = \begin{cases} \dfrac{3ET_s}{2L_f}|d_{k,\text{min}}|, & \text{Region 1} \\ \dfrac{3ET_s}{2L_f}(|d_{k,\text{max}}| - |d_{k,\text{mid}}| + |d_{k,\text{min}}|), & \text{Region 2} \\ \dfrac{3ET_s}{2L_f}(|d_{k,\text{max}}| + |d_{k,\text{mid}}| - |d_{k,\text{min}}|), & \text{Regions 3 and 4.} \end{cases} \quad (13)$$

Comparing (12) to (13), it can be evaluated that the p-2-p values of the circulating current between modules using the PD technique are higher in all regions than that if the APOD technique is used. The evaluation procedures for the p-2-p comparisons are presented in the Appendix. Substituting (3) into (12) and (13), the p-2-p values of the circulating current can be obtained, and the plots for the full range of modulation index and the phase angle are presented in Fig. 7. In this case, the dc-link voltage is 750 V ($E = 250$ V), T_s is 100 μs, and L_f is 1.8 mH. Based on (12), it can be calculated that the maximum p-2-p value of the circulating current using the PD modulation would appear at the point ($m = 0.95$, $\theta = \omega t = 0°$). For (15), the p-2-p value using APOD increases monotonously with the increasing of the modulation index. Within the high-modulation-index range, it can be seen that the p-2-p value increases dramatically at the neighborhood of $\theta = 0°$ because higher common-mode voltage is introduced by region 3.

The quarter-cycle rms value of the circulating current by using the PD and the APOD modulation can be written by (14) and (15). Comparing (14) to (15), it can be evaluated that the rms of the circulating current using the PD technique is higher than that if the APOD technique is used. The evaluation procedures for the rms comparisons are presented in the Appendix. Substituting (3) into (14) and (15), the rms values of the circulating current can be obtained, and the plots for the full range of the modulation index and the phase angle are presented in Fig. 8. The parameters T_s, E, and L_f are identical to those used in the p-2-p value evaluation. Based on (14), it can be calculated that the partial derivative of the rms value using PD in the direction of the modulation index equals zero when $m = 0.64$ and in the direction of phase angle equals to zero when $\theta = 0$, which indicates that the maximum rms value of the circulating current using the PD modulation would appear at the point ($m = 0.64$,

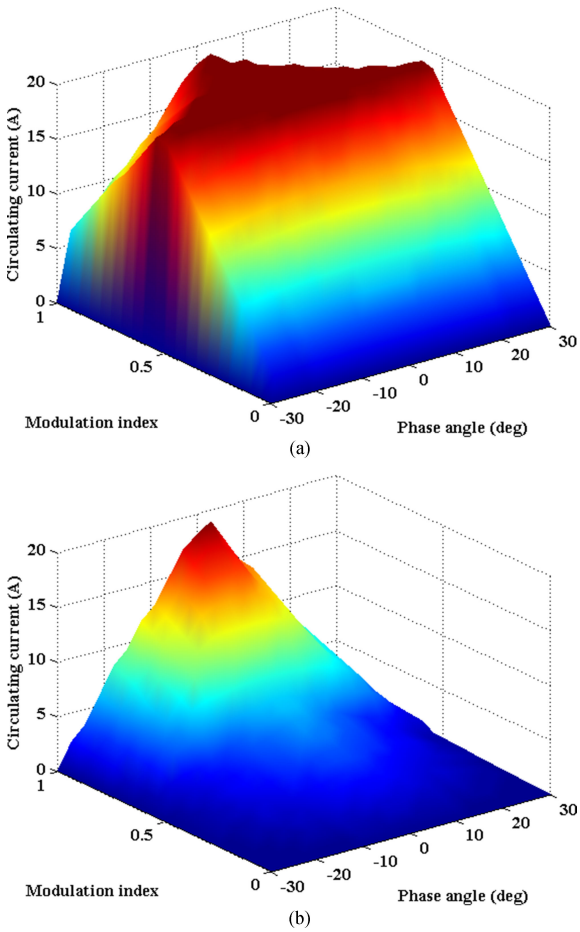


Fig. 7. p-2-p values of the circulating current by using (a) PD and (b) APOD.

$\theta = 0°$). For (15), the partial derivative of the rms value using APOD in the direction of the phase angle is equal to zero when $\theta = 0°$. Meanwhile, the rms value of the circulating current rises monotonously with the increasing of the modulation index, since higher modulation index introduces regions with higher common-mode voltage (e.g., regions 3 and 4).

IV. Simulation and Experimental Results

The performance of two parallel NPC inverters with a common dc link under interleaved operation is validated for different modulation by simulation and experiments. The detailed results and performance evaluation are presented in the following section.

A. Simulation Results

To validate the analyses, two parallel NPC inverters with a common dc link are simulated in the MATLAB/Simulink environment with the PLECS toolbox. Both the PD and the APOD techniques are tested under interleaved operation. The dc-link voltage is 750 V and the nominal ac voltage is 230 V (rms); and the switching frequency is 10 kHz. In the open-loop control case, the modulation index of $m = 0.85$ is considered.

Comparisons in terms of the total current (i_{total}), the common-mode voltage (v_{cm}), and the circulating current (i_{cir}) are shown in Fig. 9. It can be seen that the total currents using two modulation techniques are identical in terms of power quality and current ripple. The total harmonic distortions (THDs) of both waveforms are obtained with 3.04% for both techniques. Nevertheless, the common-mode voltages and the circulating currents

$$i_{\text{cir, rms}}^{\text{PD}} = \begin{cases} \dfrac{\sqrt{3}T_s E}{4L_f}\Big[-4\left|d_{k,\max}\right|^3 - 6\left|d_{k,\text{mid}}\right|^3 + \left|d_{k,\text{mid}}\right|^2\left(3 - 6\left|d_{k,\min}\right|\right) + \left|d_{k,\max}\right|^2\left(3 - 6\left|d_{k,\text{mid}}\right| - 6\left|d_{k,\min}\right|\right) \\ +6\left|d_{k,\text{mid}}\right|\left|d_{k,\min}\right| + \left(3 - 8\left|d_{k,\min}\right|\right)\left|d_{k,\min}\right|^2 + 6\left|d_{k,\max}\right|\left(\left|d_{k,\text{mid}}\right| + \left|d_{k,\min}\right|\right)\Big]^{1/2}, \quad \text{Region 1} \\ \dfrac{\sqrt{3}T_s E}{4L_f}\Big[-9 - 21\left|d_{k,\max}\right|^2 + 8\left|d_{k,\max}\right|^3 - 21\left|d_{k,\text{mid}}\right|^2 + 6\left|d_{k,\text{mid}}\right|^3 + 6\left|d_{k,\text{mid}}\right|\left(3 + \left(\left|d_{k,\min}\right| - 1\right)\left|d_{k,\min}\right|\right) \\ +6\left|d_{k,\max}\right|\left(3 + \left(\left|d_{k,\text{mid}}\right| - 1\right)\left|d_{k,\text{mid}}\right| + \left(\left|d_{k,\min}\right| - 1\right)\left|d_{k,\min}\right|\right. \\ \left. + \left|d_{k,\min}\right|\left(18 + \left|d_{k,\min}\right|\left(4\left|d_{k,\min}\right| - 21\right)\right)\Big]^{1/2}, \quad \text{Regions 2–4} \end{cases} \tag{14}$$

$$i_{\text{cir, rms}}^{\text{APOD}} = \begin{cases} \dfrac{\sqrt{3}T_s E}{4L_f}\Big[-\left(\left|d_{k,\max}\right| - \left|d_{k,\text{mid}}\right|\right)^2\left(-3 + 4\left|d_{k,\max}\right| + 2\left|d_{k,\text{mid}}\right|\right) \\ +6\left(\left|d_{k,\max}\right| - \left|d_{k,\text{mid}}\right|\right)\left(-1 + \left|d_{k,\max}\right| + \left|d_{k,\text{mid}}\right|\right)\left|d_{k,\min}\right| + 3\left|d_{k,\min}\right|^2 - 4\left|d_{k,\min}\right|^3\Big]^{1/2}, \quad \text{Region 1} \\ \dfrac{\sqrt{3}T_s E}{4L_f}\Big[-9\left|d_{k,\max}\right|^2 + 4\left|d_{k,\max}\right|^3 + 3\left|d_{k,\text{mid}}\right|^2 + 2\left|d_{k,\text{mid}}\right|^3 + \left(\left|d_{k,\min}\right| - 1\right)^2\left(4\left|d_{k,\min}\right| - 1\right) \\ -6\left|d_{k,\text{mid}}\right|\left(1 + \left(\left|d_{k,\min}\right| - 1\right)\left|d_{k,\min}\right|\right) + 6\left|d_{k,\max}\right|\left(1 + \left|d_{k,\text{mid}}\right| - \left|d_{k,\text{mid}}\right|^2 + \left(\left|d_{k,\min}\right| - 1\right)\left|d_{k,\min}\right|\right)\Big]^{1/2}, \quad \text{Region 2} \\ \dfrac{\sqrt{3}T_s E}{4L_f}\Big[3\left|d_{k,\max}\right|^2 - 9\left|d_{k,\text{mid}}\right|^2 + 6\left|d_{k,\text{mid}}\right|^3 + \left(\left|d_{k,\min}\right| - 1\right)^2\left(4\left|d_{k,\min}\right| - 1\right) + 6\left|d_{k,\text{mid}}\right|\left(1 + \left|d_{k,\min}\right|\left(\left|d_{k,\min}\right| - 1\right)\right) \\ -6\left|d_{k,\max}\right|\left(1 + \left|d_{k,\text{mid}}\right|\left(\left|d_{k,\text{mid}}\right| - 1\right)\right) + \left|d_{k,\min}\right|\left(\left|d_{k,\min}\right| - 1\right)\Big]^{1/2}, \quad \text{Regions 3 and 4} \end{cases} \tag{15}$$

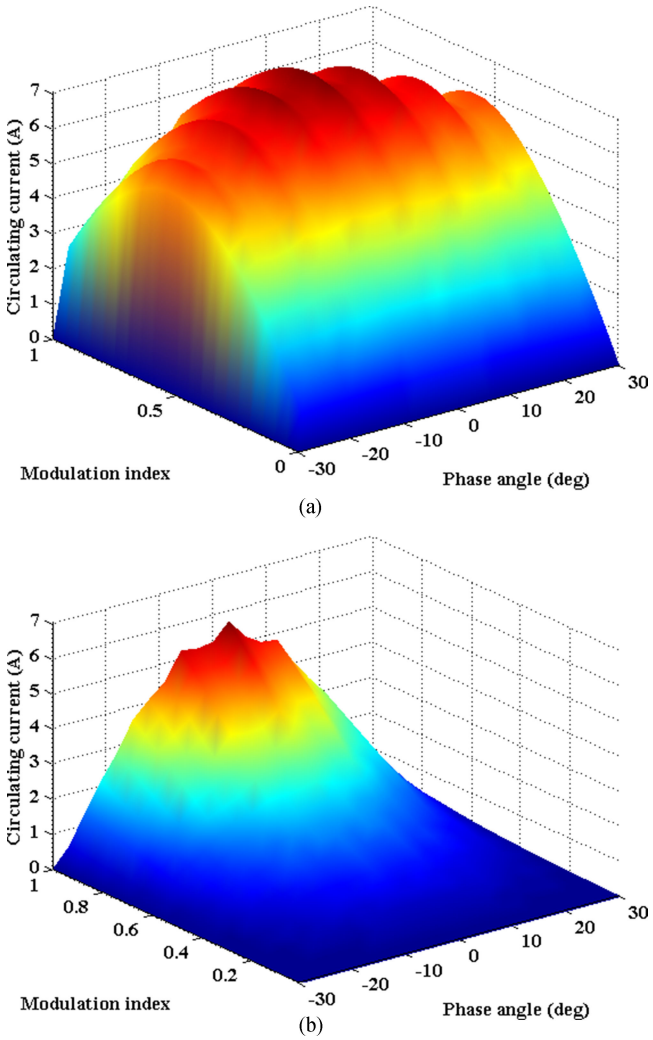


Fig. 8. RMS values of circulating current by using (a) PD and (b) APOD.

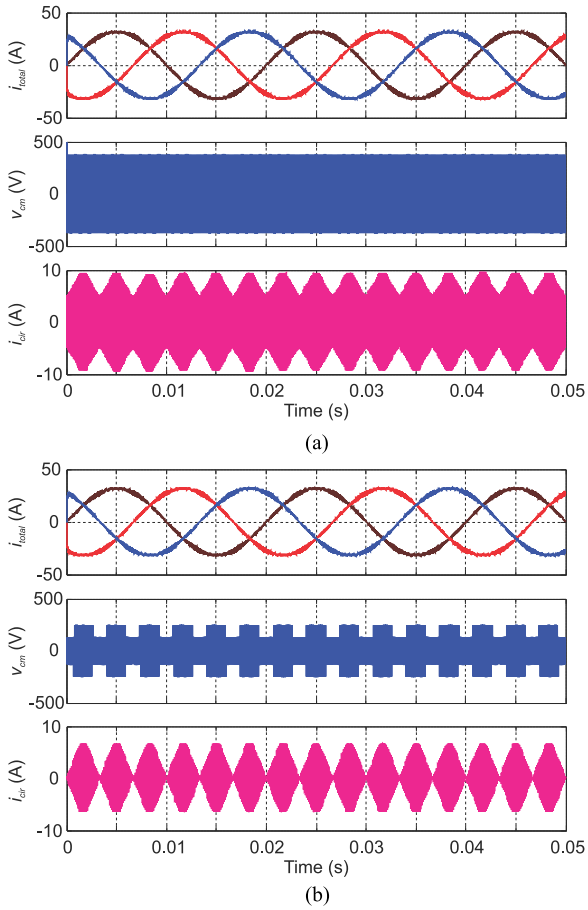


Fig. 9. Performance evaluation of parallel NPCs during interleaved operation using different modulation (modulation index: $m = 0.85$): (a) PD and (b) APOD.

using different modulation techniques are distinct. It is worth noting that the voltage vector is sweeping regions 2, 3, and 4 of every sector in every cycle according to the modulation index. The p-2-p value of the common-mode voltage by using the PD is 750 V for the regions, which is $6E$ or $V_{\rm dc}$, while the p-2-p value of the common-mode voltage by using the APOD is 500 V for regions 3 and 4, which are two-third of that using the PD, and is 250 V for region 2, which is one-third of that using the PD. As a result, it can be expected that the circulating current of the PD modulation would be higher of that of the APOD because of the higher common-mode voltage. In this case, the p-2-p values of the circulating current by using the PD and the APOD are 19.032 and 7.606 A. The rms values of the circulating current by using the PD and the APOD are 6.317 and 1.863 A, respectively.

The shapes of common-mode voltages and circulating currents in different regions are simulated and shown in Fig. 10. For PD modulation, since the shapes of common-mode voltages are similar in all regions, one zoomed plot of the common-mode voltages and circulating currents with the modulation index of $m = 0.85$ is shown in Fig. 10(a). For APOD modulation, to obtain the shapes in region 1, a lower modulation index of $m = 0.35$ is used and the zoomed plot is shown in Fig. 10(b). The zoomed plots of regions 2–4 use the modulation index of $m = 0.85$ and are shown in Fig. 10(c) and (d). Compared to Fig. 6, the theoretical analysis of the common-mode voltage and the circulating current of both modulation techniques is consistent.

B. Experimental Validation

The modulation techniques are also evaluated by the experimental setup shown in Fig. 11. For the preliminary test, a 20-kVA prototype with two paralleled NPC inverters (system configuration of Fig. 2) has been built in the laboratory, and the dc-link voltage is 700 V. The Infineon three-level phase leg insulated-gate bipolar transistor module (F3L75R07W2E3_B11) has been chosen as the candidate of the NPC inverter setup and can handle current up to 75 A. An inductor of 1.8 mH is used in each phase to limit current ripples and circulating currents. Each module is driven by the dedicated evaluation drive board (F3L030E07-F-W2). A high-bandwidth signal processing as well as measurement board is utilized to control each NPC inverter module locally. Meanwhile, the centralized control scheme is implemented in a master control board (Xilinx Zc702 evaluation board). The communication between the master

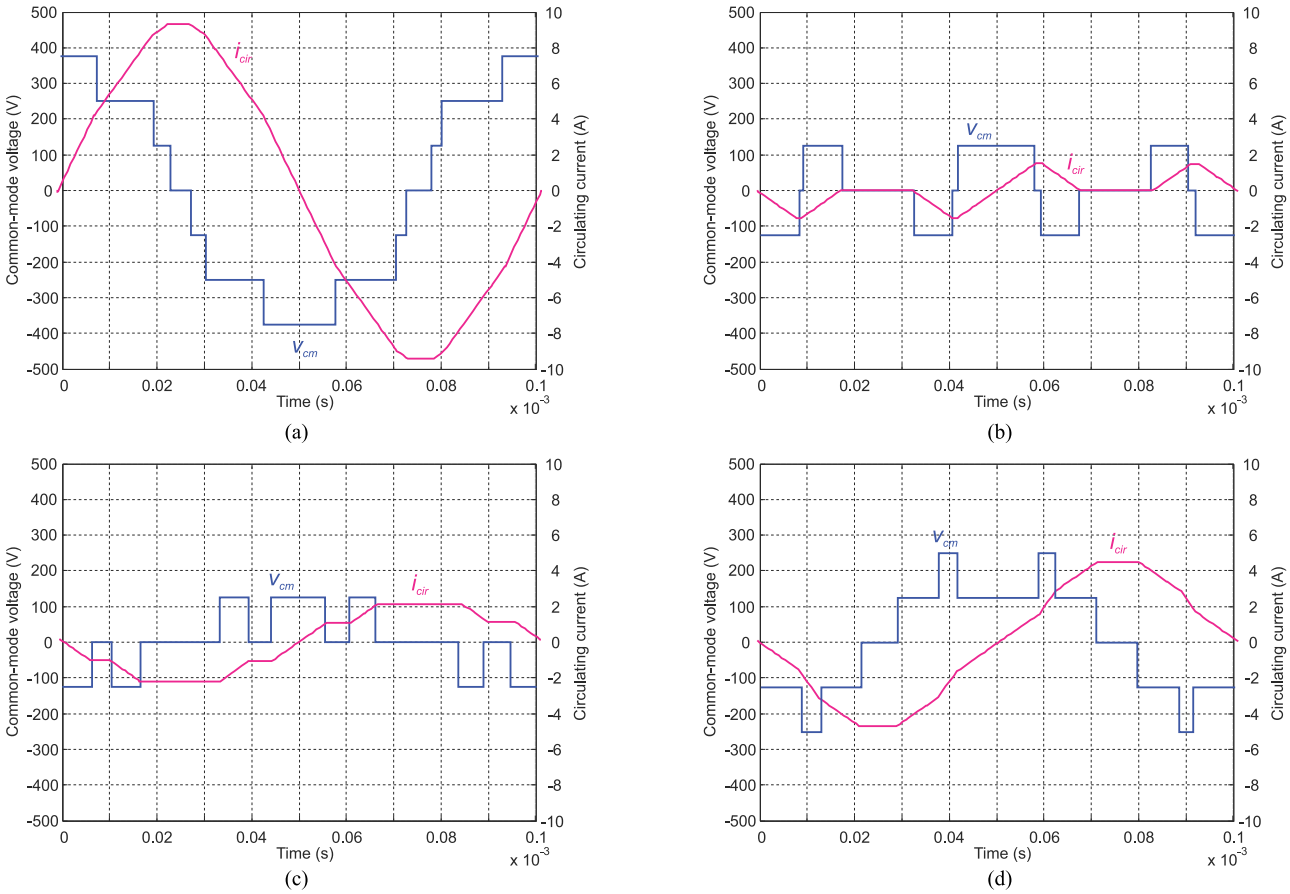


Fig. 10. Common-mode voltage and the circulating current between parallel NPC inverters in one sampling interval with different modulation techniques: (a) PD ($m = 0.85$), (b) APOD ($m = 0.35$, region 1), (c) APOD ($m = 0.85$, region 2), and (d) APOD ($m = 0.85$, regions 3 and 4).

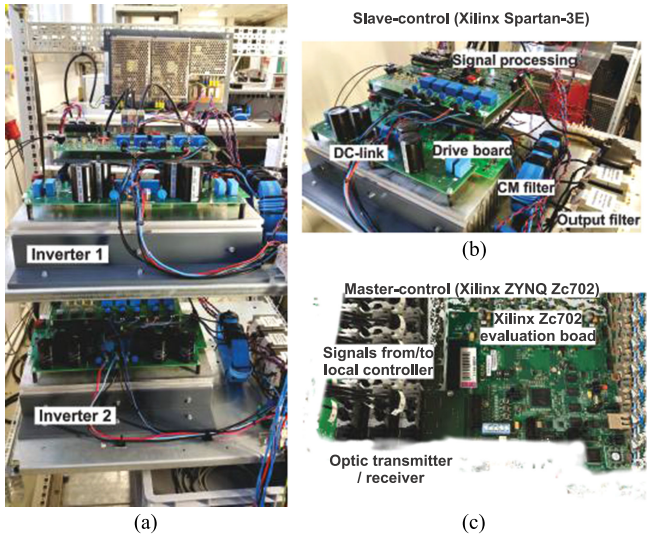


Fig. 11. Experimental setup. (a) Overall prototype. (b) Details of inverter 1 as well as the slave control board. (c) Master control board.

control board and the local control board is achieved through the optic fibers. The detailed system parameters are listed in Table II.

First, the two parallel NPC inverters are performed under interleaved operation with a switching frequency of 10 kHz. An open-loop control is implemented in the master control board, which is able to adjust the modulation index of both inverters online. The three-phase current waveforms by using two different modulation techniques (PD and APOD) are compared as follows. In Fig. 12, the three-phase total currents of both inverters are measured employing the PD and the APOD. It can be seen that the performance of both current waveforms is comparable in terms of current ripple and power quality. The spectrum analysis of the total current of both modulations is presented in Fig. 13. As shown in Fig. 13(b), it is reflected in slightly higher sideband harmonic spectrum around the first carrier harmonics for the APOD modulation. In general, the waveform performance of both techniques in the frequency domain is comparable, and the THD values of Fig. 12 are 5.96% (PD) and 6.80% (APOD).

TABLE II
SYSTEM PARAMETERS

Symbol	Quantity	Value
f_c	Switching frequency	10 kHz
f_s	Baud rate between master/slave boards	75 MBd
$V_{\rm dc}$	DC-link voltage	700 V
S_n	Rated power of each inverter	10 kW
L_f	Filter inductance	1.8 mH
C_f	DC-link capacitance	2000 μF

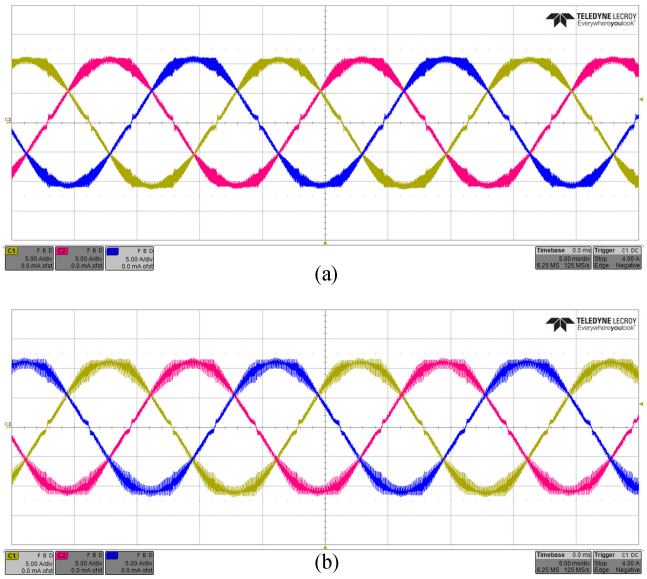


Fig. 12. Three-phase total current of two NPC inverters by using different modulation techniques (modulation index: $m = 0.85$, time: 5 ms/div, and current: 5 A/div): (a) PD and (b) APOD.

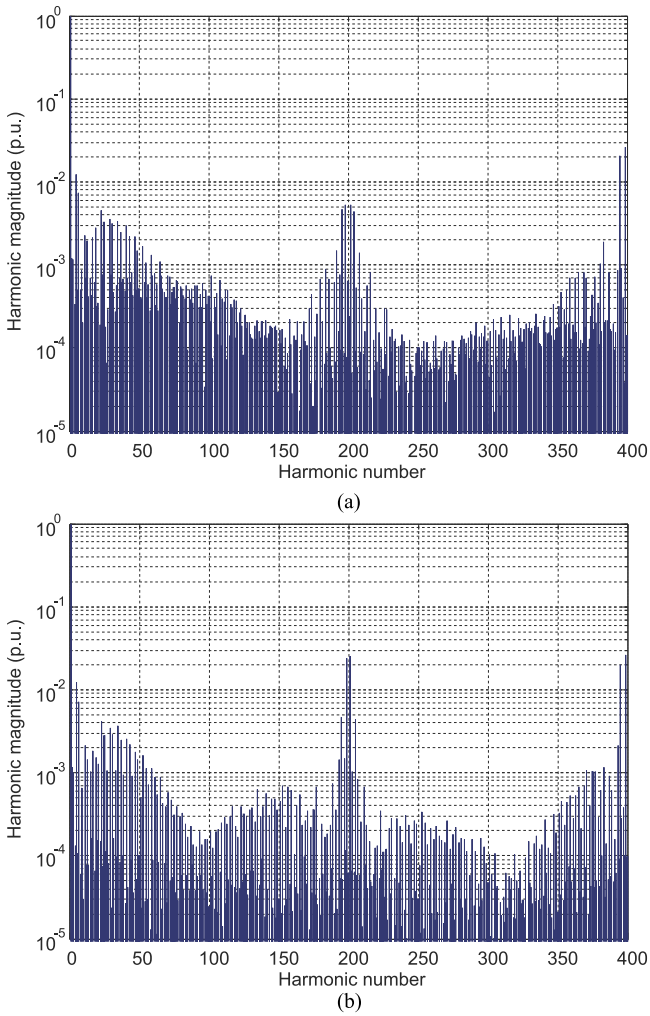


Fig. 13. Amplitude spectrum of total current (Phase A) using different modulation techniques: (a) PD and (b) APOD.

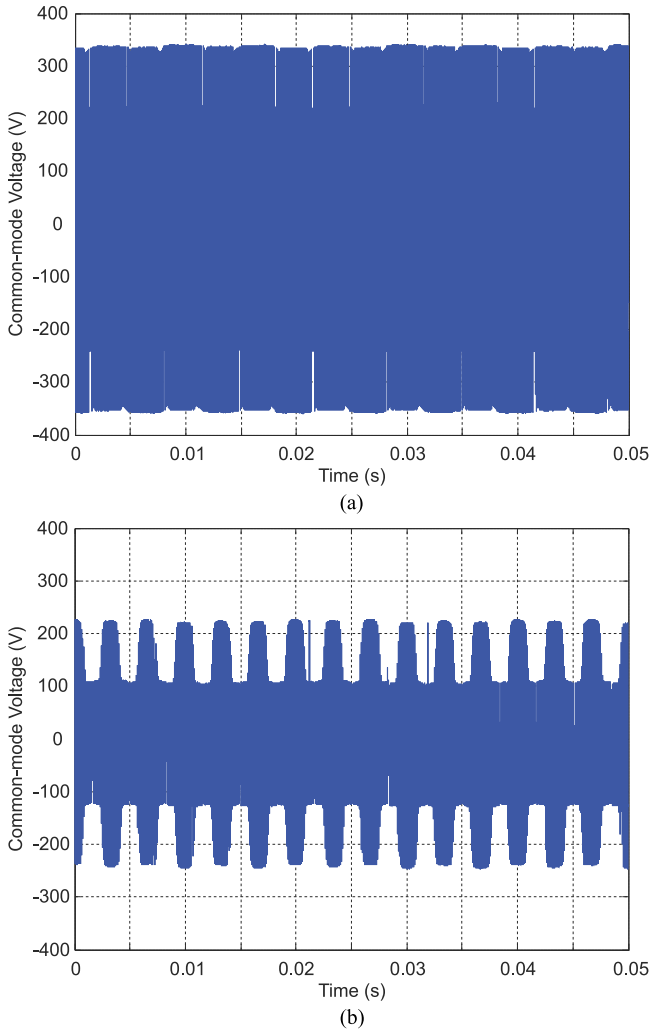


Fig. 14. Common-mode voltage between the parallel NPC inverters using different modulation (modulation index: $m = 0.85$): (a) PD and (b) APOD.

Second, the common-mode voltage and the circulating currents between two NPCs by using two different modulation are investigated. The common-mode voltages between two NPCs are presented in Fig. 14. The modulation index of $m = 0.85$ is implemented for both inverters, indicating that regions 2, 3, and 4 would be swept by the voltage vector. According to the analysis of Section III and Table I, the common-mode voltage of the PD modulation [$\hat{v}_{\rm cm} = 350$ V in Fig. 14(a)] would be 3/2 times to that of the APOD [$\hat{v}_{\rm cm} = 233$ V in Fig. 14(b)] in regions 3 and 4, and three times to that of the APOD in region 2 [$\hat{v}_{\rm cm} = 117$ V in Fig. 14(b)]. The circulating currents between two NPCs are shown in Fig. 15. From the experimental results, the circulating current of the PD [see Fig. 15(a)] is higher than that of the APOD [see Fig. 15(b)] as expected, especially the adjoining areas between two "rhombi" (that related to region 2).

To sum up, during interleaved operation, the performance of the total current of the parallel inverter using the PD is in the same league as that using the APOD. Nevertheless, the circulating current of the PD modulation is much higher than that of the APOD modulation, especially if a small voltage vector is

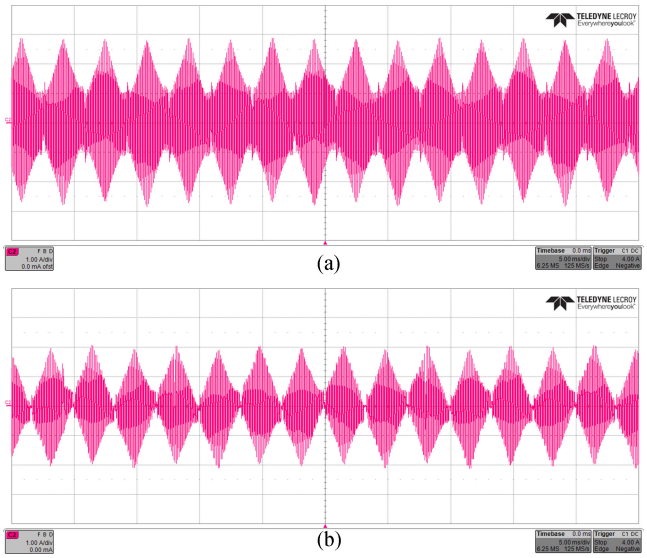


Fig. 15. Circulating current between the parallel NPC inverters using different modulation (modulation index: $m = 0.98$, time: 5 ms/div, and current: 1 A/div): (a) PD and (b) APOD.

performed (regions 1 and 2). As a result, the APOD modulation would be a superior solution for parallel NPC applications.

V. Conclusion

In high-power application, the interleaved operation of parallel NPC inverters has been used for improving the quality of the current waveform. However, in the case of a common dc link, the circulating current issue emerges and could lead to critical problems. To minimize the circulating current of parallel NPCs, two common modulation techniques for NPC inverters (PD and APOD) have been investigated and evaluated in an extensive way. Though it is well known that the PD modulation offers better performance in a single-NPC inverter, the APOD modulation has advantages in the parallel NPCs with interleaved operation. The analyses and results in this paper show that the APOD modulation gives remarkably less common-mode voltage/circulating current (e.g., one-third p-2-p value in some regions) and similar power quality as well as spectrum of the total current compared to those using the PD modulation [e.g., THD: 5.96% (PD) and 6.80% (APOD)]. To conclude, the APOD modulation is a superior solution for the parallel NPC inverters under interleaved operation.

Appendix

The p-2-p and the rms values of the circulating current in all regions by using the PD and the APOD modulation are compared here.

For the duty cycles of (3), it is easy to obtain the ranges of the maximum, middle, and minimum values, which are $|d_{k,\max}| \in [\sqrt{3}/2,\ 1] \cdot m$, $|d_{k,\mathrm{mid}}| \in [0.5,\ \sqrt{3}/2] \cdot m$, and $|d_{k,\min}| \in [0,\ 0.5] \cdot m$, respectively. These constraints will be applied to the following equations.

For p-2-p values, we have the following:

Region 1:

$$i_{\text{cir, p-2-p}}^{\text{PD}} - i_{\text{cir, p-2-p}}^{\text{APOD}} = \frac{3ET_s}{2L_f}(|d_{k,\max}| + |d_{k,\mathrm{mid}}|). \tag{16}$$

Since $|d_{k,\max}| > 0$ and $|d_{k,\mathrm{mid}}| > 0$, one can get that $i_{\text{cir, p-2-p}}^{\text{PD}} - i_{\text{cir, p-2-p}}^{\text{APOD}} > 0$, indicating that the p-2-p value by using the PD is larger than that using the APOD in this region.

Region 2:

$$i_{\text{cir, p-2-p}}^{\text{PD}} - i_{\text{cir, p-2-p}}^{\text{APOD}} = \frac{3ET_s}{2L_f}(1 - |d_{k,\mathrm{mid}}|). \tag{17}$$

Since $|d_{k,\mathrm{mid}}| < 1$, one can get that $i_{\text{cir, p-2-p}}^{\text{PD}} - i_{\text{cir, p-2-p}}^{\text{APOD}} > 0$, indicating that the p-2-p value by using the PD is larger than that using the APOD in this region.

Regions 3 and 4:

$$i_{\text{cir, p-2-p}}^{\text{PD}} - i_{\text{cir, p-2-p}}^{\text{APOD}} = \frac{3ET_s}{2L_f}(1 - |d_{k,\max}|). \tag{18}$$

Since $|d_{k,\max}| \le 1$, one can get that $i_{\text{cir, p-2-p}}^{\text{PD}} - i_{\text{cir, p-2-p}}^{\text{APOD}} \ge 0$, indicating that the p-2-p value by using the PD is larger than that using the APOD in these two regions.

For rms values, we have the following.

Region 1:

$$\begin{aligned}(i_{\text{cir, rms}}^{\text{PD}})^2 - (i_{\text{cir, rms}}^{\text{APOD}})^2 &= -\frac{3T_s^2E^2}{4L_f^2}(|d_{k,\mathrm{mid}}| + |d_{k,\min}|) \\ &\quad \times (3(|d_{k,\max}| - 1)\,|d_{k,\max}| + |d_{k,\mathrm{mid}}|^2 \\ &\quad - |d_{k,\mathrm{mid}}|\,|d_{k,\min}| + |d_{k,\min}|^2) \\ &> \frac{3T_s^2E^2}{4L_f^2}(|d_{k,\mathrm{mid}}| + |d_{k,\min}|)(3\,|d_{k,\mathrm{mid}}|\,(1 - |d_{k,\max}| \\ &\quad - |d_{k,\mathrm{mid}}|/3) + |d_{k,\min}|\,(|d_{k,\mathrm{mid}}| - |d_{k,\min}|)).\end{aligned} \tag{19}$$

Since $|d_k| \le 0.5$ in region 1 (where $m \le 0.5$), and meanwhile $|d_{k,\mathrm{mid}}| \ge |d_{k,\min}|$, one can get that $(i_{\text{cir, rms}}^{\text{PD}})^2 - (i_{\text{cir, rms}}^{\text{APOD}})^2 > 0$, indicating that the rms value by using the PD is larger than that using the APOD in this region.

Region 2:

$$\begin{aligned}(i_{\text{cir, rms}}^{\text{PD}})^2 - (i_{\text{cir, rms}}^{\text{APOD}})^2 &= \frac{3T_s^2E^2}{4L_f^2}\Big(-2 - 3\,|d_{k,\max}|^2 + |d_{k,\max}|^3 \\ &\quad + |d_{k,\mathrm{mid}}|\,(6 + (|d_{k,\mathrm{mid}}| - 6)\,|d_{k,\mathrm{mid}}|) \\ &\quad + 3\,|d_{k,\max}|\,(1 + (|d_{k,\mathrm{mid}}| - 1)\,|d_{k,\mathrm{mid}}|) \\ &\quad + 3\,|d_{k,\min}| - 3\,|d_{k,\mathrm{mid}}|\,|d_{k,\min}| + 3(|d_{k,\mathrm{mid}}| - 1)\,|d_{k,\min}|^2\Big).\end{aligned} \tag{20}$$

By applying the above-mentioned constraints, one can get that $(i_{\text{cir, rms}}^{\text{PD}})^2 - (i_{\text{cir, rms}}^{\text{APOD}})^2 > 0$, indicating that the rms value by using the PD is larger than that using the APOD in this region (a symbolic manipulation program such as Wolfram Mathematica is useful for the calculation).

Regions 3 and 4:

$$(i_{\text{cir, rms}}^{\text{PD}})^2 - (i_{\text{cir, rms}}^{\text{APOD}})^2 = \frac{3T_s^2 E^2}{4L_f^2}(3(|d_{k,\max}| - 1)(2 + 2\,|d_{k,\max}| \times (|d_{k,\max}| - 2) + 3\,|d_{k,\text{mid}}|\,(|d_{k,\text{mid}}| - 1) + 3\,|d_{k,\min}|\,(|d_{k,\min}| - 1))). \quad (21)$$

By applying the above-mentioned constraints, one can get that $(i_{\text{cir, rms}}^{\text{PD}})^2 - (i_{\text{cir, rms}}^{\text{APOD}})^2 > 0$, indicating that the rms value by using the PD is larger than that using the APOD in these two regions (a symbolic manipulation program such as Wolfram Mathematica is useful for the calculation).

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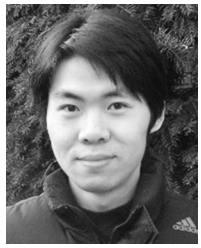

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