Increase in Power Conversion Efficiency of Bidirectional DC–DC Converter Using 1:1 Transformer and Pulse-Frequency Modulation Control

Yoon-Geol Choi, Sang-Won Lee, Hyeon-Seok Lee, Su-Chang Lee, and Bongkoo Kang, *Member, IEEE*

***Abstract*—This paper proposes a circuit structure of bidirectional dc–dc converter. This structure uses two switches, two capacitors, a 1:1 transformer, and a control circuit for pulse-frequency modulation. The windings of the transformer are connected in a series-aiding configuration to reduce current ripples and to increase power conversion efficiency η_e. The capacitors and the leakage inductance of the transformer provide soft-switching conditions. When the proposed converter was designed to operate at a switching frequency of 110–240 kHz, input/output voltages of 100–400 V, and output power P_o of 30–300 W, η_e was ≥97% for $P_o \geq$ 90 W and 93.5% at $P_o =$ 30 W. Experimental results show that the proposed converter is suitable for use in photovoltaic power conversion systems and energy storage systems.**

***Index Terms*—DC–DC power conversion, photovoltaic power, pulse-frequency modulation (PFM).**

I. Introduction

CONCEPTUALLY, the bidirectional dc–dc converter (BDC) is a dc–dc power transformer that matches dc voltage levels between two different systems. BDCs have been used in many applications including between the inverter and the battery pack in energy storage system, between the battery pack and the power train in plug-in hybrid electric vehicles, and between the inverter and the photovoltaic panel in solar power systems [1]–[7].

BDCs have been categorized into isolated and nonisolated types. Isolated BDCs [8]–[16] use a transformer to achieve galvanic isolation and to obtain high voltage conversion ratio.

Manuscript received October 25, 2017; revised January 17, 2018; accepted February 18, 2018. Date of publication February 27, 2018; date of current version September 28, 2018. This work was supported in part by LG Electronics Inc. and in part by the Ministry of Science, ICT and Future Planning, South Korea, under the "IT Consilience Creative Program" (IITP-R0346-16-1007) supervised by the Institute for Information and communications Technology Promotion. Recommended for publication by Associate Editor M. Amirabadi. *(Corresponding author: Bongkoo Kang.)*

Y.-G. Choi, S.-W. Lee, H.-S. Lee, and B. Kang are with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea (e-mail: ygchoi@postech.ac.kr; sangwony1@postech.ac.kr; hsasdf@postech.ac.kr; bkkang@postech.ac.kr).

S.-C. Lee is with the LG Electronics Co., Ltd., Energy Business Center, Gumi 39368, South Korea (e-mail: suchang.lee@lge.com).

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Digital Object Identifier 10.1109/TPEL.2018.2809682

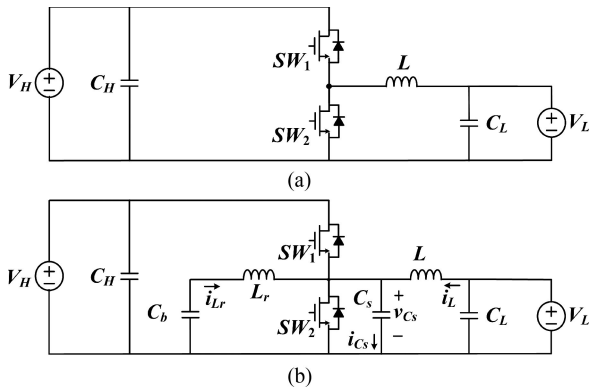

Fig. 1. Schematic diagrams. (a) Conventional nonisolated BDC. (b) Converter of [28].

However, they require more components than the nonisolated BDCs do. Nonisolated BDCs [17]–[32] are relatively simple in structure, have high power conversion efficiency η_e, and can be controlled using simple control circuit, so these BDCs can be small and inexpensive.

The conventional nonisolated BDC [see Fig. 1(a)] is very simple in structure. It can be operated either as a boost converter by using the switch SW_2 and the body diode of SW_1, or as a buck converter by using SW_1 and the body diode of SW_2. This converter has some disadvantages; the switches undergo a hard switching and the body diodes are subject to a reverse recovery, that decreases η_e, causes high current stress on switches, hinders the converter from increasing the power density, and produces electromagnetic interference [17].

Many nonisolated BDCs use the conventional nonisolated BDC as a basic structure, and adopt an auxiliary circuit (either active or passive) to obtain a soft-switching condition. Active auxiliary circuits use either a clamping circuit [22], [23], or a zero-voltage transition circuit [24], [25]. These circuits operate just before the turn-ON of main switches to generate a circulation current that turns on the body diode of the main switch, so zero-voltage turn-ON of switches is ensured. The converter of [26] uses a coupled inductor that has high turn ratio, in conjunction with the active clamp circuit in [22], to achieve both high voltage conversion ratio and zero voltage switching (ZVS). BDCs that use an active auxiliary circuit can increase η_e, but

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require additional components and a complex control circuit for the auxiliary switches.

Passive auxiliary circuits achieve the ZVS condition using either an inductor-capacitor (*LC*) resonance [27] or an auxiliary inductor current [28]–[30]; the switch in the converter of [27] turns ON at the zero-crossing point of the resonance voltage, and the auxiliary inductor current in the converters of [28]–[30] turns ON the body diode of the switch; these arrangement provides a zero-voltage turning-ON of switch. Passive auxiliary circuits can have simpler circuit structure than active ones because passive auxiliary circuits do not use any additional switches and diodes, but the auxiliary inductor current increases the conduction loss and core loss, and increases the current stress on the switch.

The passive auxiliary circuit in the converter of [28] [see Fig. 1(b)] is composed only of one inductor L_r, a dc-blocking capacitor C_b and a snubber capacitor C_s. The converter operates like the conventional nonisolated BDC [see Fig. 1(a)]. The voltage V_{Cs} of C_s is V_H when SW_1 is turned ON for buck conversion, and it is 0 V when SW_2 is turned ON for boost conversion. When the switch is turned OFF, the inductor currents i_L and i_{Lr} charge or discharge C_s, so the slope of V_{Cs} variation is controlled by the inductor currents; because of this relationship, the switch turns OFF with zero voltage. i_L and i_{Lr} flow through the body diode of switch after charging or discharging C_s fully, so the switch also turns ON with zero voltage. The converter increases the switching frequency f_s to decrease the load current; this change also decreases the auxiliary inductor current, so this converter has high η_e even when load is light.

Although the converter of [28] has excellent η_e over a wide range of load variation, the converter has two demerits: first, $i_L + i_{Lr}$ does not change its sign because of the body diode, so full discharge of C_s takes a long time, and V_{Cs} does not drop to 0 V for some voltage conversion ratios V_H/V_L; therefore, the converter operates under ZVS condition only for a limited range of V_H/V_L, and second, the ripples of i_L and i_{Lr} are fairly high; if these ripples could be reduced, the inductors would have less core loss and conduction loss. The converters of [31] and [32] use a coupled inductor to reduce the ripple of i_L, but they require additional switches, diodes, and an auxiliary inductor.

The converter proposed in this paper uses the same circuit structure as the converter of [28], minimizes the inductor current ripples using a 1:1 transformer, and allows $i_L + i_{Lr}$ to change its sign using synchronous switching. The proposed converter uses pulse-frequency modulation (PFM) to accommodate load variation, and uses a pulse-duty control to vary the voltage conversion ratio. The circuit structure, principle of operation, and design considerations of the proposed converter are given in Section II. The control circuit is described in Section III. Experimental results and discussions are given in Section IV-A and conclusion is given in Section V.

II. Proposed BDC

Under the proposed BDC (see Fig. 2) consists of a transformer, a dc blocking capacitor C_b, a snubber capacitor C_s, and

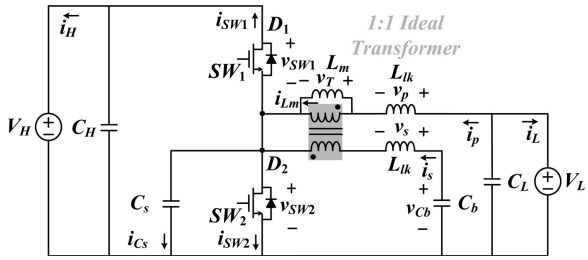

Fig. 2. Schematic diagram of the proposed nonisolated BDC.

two switches SW_1 and SW_2. The transformer has two windings that have turns-ratio 1:1, and it is represented using a 1:1 ideal transformer, a magnetizing inductance L_m, and two leakage inductances L_{lk}. The windings of the transformer are connected in a series-aiding configuration to decrease core loss and core magnetic flux [34]. C_s reduces the switching loss by controlling the turn-ON and turn-OFF slopes of the switch voltages $v_{\mathrm{SW}1}$ and $v_{\mathrm{SW}2}$. To charge and discharge C_s, SW_1 and SW_2 are turned ON alternately with a dead time t_d. C_b acts as a dc blocking capacitor and its voltage v_{Cb} equals to V_L when the converter operates under a steady-state condition. The primary current i_p of the transformer is the sum of the secondary current i_s and the magnetizing current i_{Lm}. The ripple of i_{Lm} is small because the windings are connected in a series-aiding configuration that makes the core magnetic flux almost constant.

The advantages of the proposed converter can be summarized as follows.

1) It uses one transformer and two capacitors to achieve soft switching, so the circuit structure is very simple.
2) It can operate at a high frequency because the switching loss is reduced significantly, so small components can be used.
3) It can use PFM to achieve high η_e over a wide range of load.
4) It reduces the ripple of i_{Lm} significantly by connecting the transformer windings in a series-aiding configuration that reduces the power loss and peak magnetic field in the transformer core.

The converter is assumed to operate at a constant f_s to simplify analysis, although it uses PFM to accommodate for the load variance. Also, the following assumptions have been made to obtain the theoretical waveforms (see Fig. 3: $L_{lkp} = L_{lks} = L_{lk}$; all switches are ideal; and capacitors and inductors are loss free. Then, the voltage and current laws of the circuit give the following equations:

$$v_{Cb} + v_T - v_{\mathrm{SW}2} = L_{lk}\frac{di_s}{dt} \tag{1}$$

$$V_L - v_T - v_{\mathrm{SW}2} = L_{lk}\frac{di_p}{dt} \tag{2}$$

$$\frac{di_m}{dt} = \frac{di_p}{dt} - \frac{di_s}{dt}. \tag{3}$$

The time averages of inductor voltages v_p, v_s, and v_T are zero, so $v_{Cb} \approx V_L$. Using this information and solving (1) and

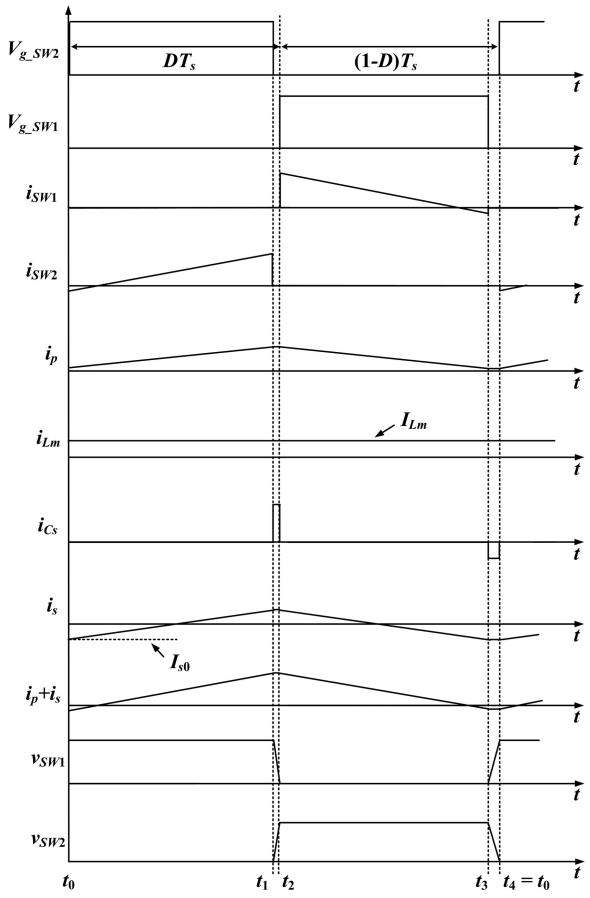

Fig. 3. Theoretical waveforms of currents and voltages of the proposed converter for boost conversion.

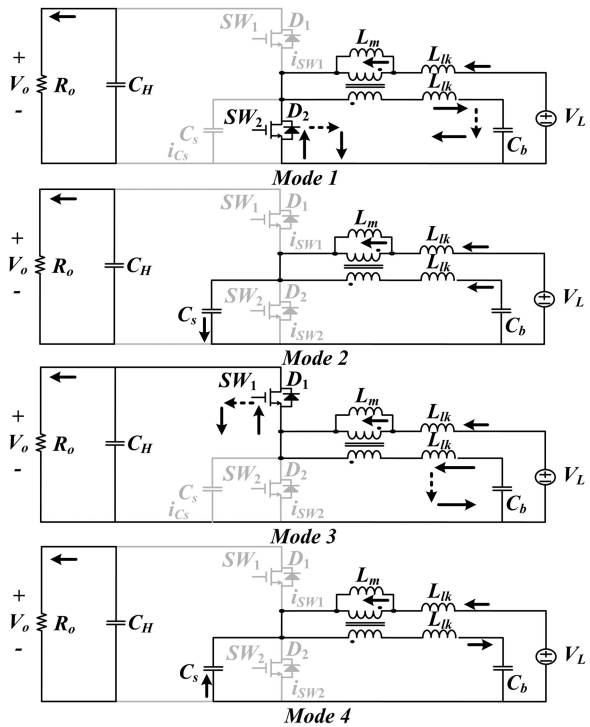

Fig. 4. Equivalent circuits of the proposed converter for boost conversion.

(2) for v_T yields

$$v_T = L_m \frac{di_m}{dt} \cong -\frac{L_{lk}}{2}\frac{di_m}{dt}. \tag{4}$$

Equations (1)–(4) demonstrate that $v_T \approx 0$ V for any $v_{\mathrm{SW}2}$.

A. Boost Conversion

Without Initially, $v_{\mathrm{SW}2} = 0$ V, $i_{\mathrm{SW}2} < 0$ A, and diode D_2 is turned ON. For each switching period $T_s = 1/f_s$, the converter operates in four sequential modes (see Fig. 4).

The first mode (*Mode* 1, Fig. 4) starts when SW_2 is turned ON at $t = t_0$, and ends when SW_2 is turned OFF at $t = t_1$. During this period

$$i_s(t) = I_{s0} + \frac{V_L}{L_{lk}}(t - t_0) \tag{5}$$

and

$$i_p(t) = I_{Lm} + I_{s0} + \frac{V_L}{L_{lk}}(t - t_0)$$

because $v_p = v_s = V_L$, where I_{s0} and I_{Lm} are the initial currents flowing through L_{lk} and L_m, respectively.

The second mode (*Mode* 2, Fig. 4) starts when SW_2 is turned OFF at $t = t_1$. During this mode, C_s charged from 0 V to the output voltage V_H by the current

$$i_{Cs}(t_1) = i_p(t_1) + i_s(t_1) = I_{Lm} + 2I_{s0} + \frac{2V_L}{L_{lk}}(t_1 - t_0).$$

This mode ends at $t = t_2$ when $v_{\mathrm{SW}2} = V_H$, so

$$t_2 - t_1 = \frac{C_s V_H}{I_{Lm} + 2I_{s0} + 2V_L(t_1 - t_0)/L_{lk}}$$

the oscillations in i_p and i_s are prevented by setting $t_2 - t_1 \ll 2\pi\sqrt{C_s L_{lk}}$.

The third mode (*Mode* 3, Fig. 4) starts when the body diode of SW_1 turns ON at $t = t_2$ and SW_1 is turned ON subsequently. During this mode

$$i_s(t) \approx i_s(t_1) - \frac{(V_H - V_L)}{L_{lk}}(t - t_2) \tag{6}$$

and

$$i_p(t) \approx I_{Lm} + i_s(t_1) - \frac{(V_H - V_L)}{L_{lk}}(t - t_2)$$

because $t_s(t_1) \approx i_s(t_1)$, $v_{\mathrm{SW}2} = V_H$ and $v_p = v_s = V_L - V_H$. The energy stored in the transformer is transferred to the load. $i_p + i_s$ decreases from $I_{Lm} + 2i_s(t_1)$ to zero, as t increases. Then, $i_p + i_s$ changes its sign at $t = t_3$, at which time SW_1 is turned OFF and *Mode* 3 ends.

The last mode (*Mode* 4, Fig. 4) starts at $t = t_3$. C_s discharges quickly from V_H to 0 V at a rate of

$$\begin{aligned} i_{Cs}(t_3) &= i_p(t_3) + i_s(t_3) \\ &= I_{Lm} + 2i_s(t_1) - \frac{2(V_H - V_L)}{L_{lk}}(t_3 - t_2) \end{aligned} \tag{7}$$

because $v_{\mathrm{SW}2} = V_H$ at $t = t_3$, $i_p + i_s < 0$ A, and all current paths through switches are turned OFF. This mode ends when

$v_{\mathrm{SW}2} = 0$ V at $t = t_4$, so

$$t_4 - t_3 = \frac{-C_s V_H}{I_{Lm} + 2i_s(t_1) - 2(V_H - V_L)(t_3 - t_2)/L_{lk}} \quad (8)$$

the oscillations in i_p and i_s are prevented by setting $t_4 - t_3 \ll 2\pi\sqrt{C_s L_{lk}}$.

The time average of i_s is zero, so the following equations are obtained using (5) and (6) after setting $t_2 - t_1 \ll T_s$ and $t_4 - t_3 \ll T_s$

$$I_{s0} \approx -\frac{V_L}{2L_{lk}} DT_s = -\frac{(V_H - V_L)}{2L_{lk}}(1-D)T_s \quad (9)$$

$$\frac{V_H}{V_L} \cong \frac{1}{1 - D}. \quad (10)$$

The output current I_o equals the time average of $i_{\mathrm{SW}1}$, i.e.,

$$I_o = \int_{t_2}^{t_3} (i_p(t) + i_s(t))dt \approx (1-D)I_{Lm}.$$

Accordingly, I_{Lm} is given by

$$I_{Lm} \cong \frac{I_o}{(1-D)}. \quad (11)$$

B. Buck Conversion

The V_H is input and V_L is output for the buck conversion. The theoretical waveforms (see Fig. 5) were calculated for the equivalent circuits (see Fig. 6). Initially, $i_s(t_0) = I_{s0}$, $i_p(t_0) = -I_{Lm} + I_{s0}$, and $v_{\mathrm{SW}2} = V_H$ because the body diode D_1 has been turned ON.

The first mode (*Mode* 1, Fig. 6) starts when SW_1 is turned ON at $t = t_0$, and ends when SW_1 is turned OFF at $t = t_1$. During this period, $v_p = v_s = V_H - V_L$, so

$$i_s(t) = I_{s0} - \frac{(V_H - V_L)}{L_{lk}}(t - t_0) \quad (12)$$

and

$$i_p(t) = -I_{Lm} + I_{s0} - \frac{(V_H - V_L)}{L_{lk}}(t - t_0).$$

The second mode (*Mode* 2, Fig. 6) starts when SW_1 is turned OFF at $t = t_1$. During this mode, C_s discharges from V_H to 0 V by the current

$$i_{Cs}(t_1) = i_p(t_1) + i_s(t_1)$$
$$= -I_{Lm} + 2I_{s0} - \frac{2(V_H - V_L)}{L_{lk}}(t_1 - t_0).$$

This mode ends at $t = t_2$ when $v_{\mathrm{SW}2} = 0$ V, so

$$t_2 - t_1 = \frac{-C_s V_H}{-I_{Lm} + 2I_{s0} - 2(V_H - V_L)(t_1 - t_0)/L_{lk}}.$$

The third mode (*Mode* 3, Fig. 6) starts at $t = t_2$ when the body diode of SW_2 is turned ON and SW_2 is turned ON subsequently. During this mode

$$i_s(t) \approx i_s(t_1) + \frac{V_L}{L_{lk}}(t - t_2) \quad (13)$$

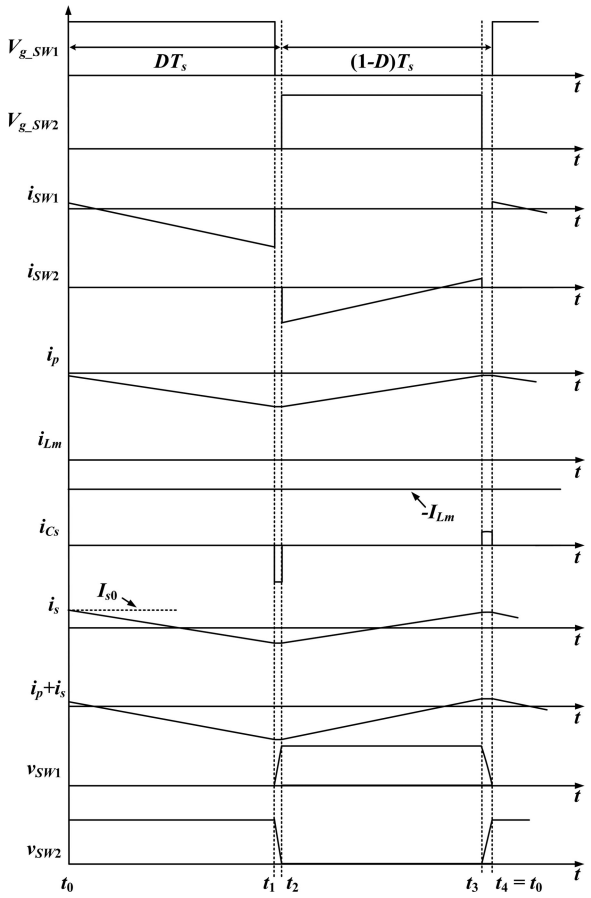

Fig. 5. Theoretical waveforms of currents and voltages of the proposed converter for buck conversion.

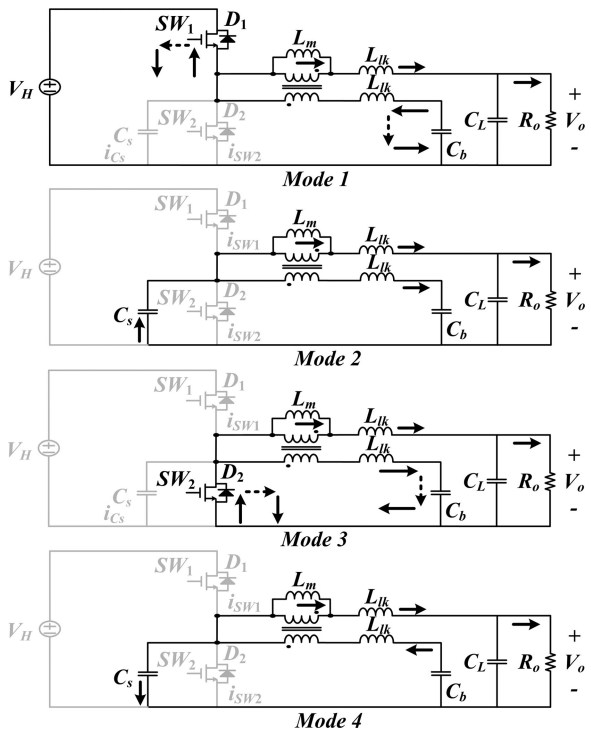

Fig. 6. Equivalent circuits of the proposed converter for buck conversion.

and

$$i_p(t) \approx -I_{Lm} + i_s(t_1) + \frac{V_L}{L_{lk}}(t - t_2)$$

because $i_s(t_2) \approx i_s(t_1)$, $v_{\mathrm{SW}2} = 0$ V and $v_p = v_s = V_L$. As t increases, $i_p + i_s$ increases from $-I_{Lm} + 2i_s(t_1)$ to 0. Then, $i_p + i_s$ changes its sign at $t = t_3$, at which time SW_2 is turned OFF and *Mode* 3 ends.

The last mode (*Mode* 4, Fig. 6) starts at $t = t_3$. C_s charges quickly from 0 V to V_H at a rate of

$$i_{Cs}(t_3) = i_p(t_3) + i_s(t_3) = -I_{Lm} + 2i_s(t_1) + \frac{V_L}{L_{lk}}(t_3 - t_2)$$

because $v_{\mathrm{SW}2} = 0$ V at $t = t_3$, $i_p + i_s > 0$ A, and all current paths through switches are turned OFF. This mode ends at $t = t_4$ when $v_{\mathrm{SW}2} = V_H$, so

$$t_4 - t_3 = \frac{C_s V_H}{-I_{Lm} + 2i_s(t_2) + 2V_L(t_3 - t_2)/L_{lk}}.$$

Using (12) and (13), and the fact that the time average of i_s is zero, the following equations are obtained after setting $t_2 - t_1 \ll T_s$ and $t_4 - t_3 \ll T_s$

$$I_{s0} \approx \frac{(V_H - V_L)}{2L_{lk}} DT_s = \frac{V_L}{2L_{lk}}(1 - D)T_s$$

$$\frac{V_L}{V_H} \cong D. \tag{14}$$

As the time average value of i_p equals I_o, and the time average of i_s is zero, the magnetizing current I_{Lm} is obtained as

$$I_o \cong \frac{1}{T_s}\int_{t_0}^{t_1} -(i_p(t) - i_s(t))dt - \int_{t_2}^{t_3}(i_p(t) - i_s(t))dt \cong I_{Lm}.$$

C. Design Considerations

Under light load, to achieve zero-voltage turn-ON of switches for boost conversion, $i_{Cs}(t_1) > 0$ and $i_{Cs}(t_3) < 0$ are required to charge/discharge C_s fully. From (5), (7), (9), and (11), the condition $i_{Cs}(t_1) > 0$ is satisfied because

$$i_p(t_1) + i_s(t_1) = I_{Lm} + V_L DT_s/L_{lk} > 0$$

and the condition $i_{Cs}(t_3) < 0$ is represented for $t_2 - t_1 \ll 2\pi\sqrt{C_s L_{lk}}$ as

$$i_p(t_3) + i_s(t_3) \approx I_{Lm} - \frac{V_L}{L_{lk}} DT_s < 0.$$

The requirement of L_{lk} for zero-voltage turning-ON of switches is obtained using (11) as

$$L_{lk} < \frac{V_L}{I_o} D(1 - D)T_s. \tag{15}$$

This condition results in $L_{lk} < 102\ \mu$H when the converter operates at $V_L = 100$ V, $150 \le V_H \le 400$ V, $0.34 \le D \le 0.75$, $110 \le f_s \le 240$ kHz, and $0.075 \le I_o \le 2$ A.

The value of L_{lk} should be determined after considering I_{s0} and the structure of the core. An increase of L_{lk} decreases I_{s0} so the conduction loss of switches decreases, but dead time increases so the available D decreases. Transformer T_1 (see Fig. 7) was fabricated using an EER 4042 ferrite core that has a window width $W_w = 3.15$ cm, turns-number $N = 29$, a space $S = 2$ cm between two windings, an air-gap length $S_a = 0.12$ mm, a relative permeability $\mu_r = 3000$, and a mean-length-per-turn $MLT = 9$ cm. L_{lk} for T_1 was obtained as [35]

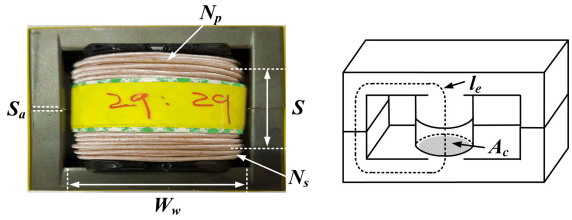

Fig. 7. Core and winding structures of the 1:1 transformer.

$$L_{lk} = \frac{\mu_0 \mu_a N^2 (MLT)(S + S_a)}{W_w} = 60.7\ \mu\mathrm{H}$$

where μ_0 is the vacuum permeability and $\mu_a = 1$ is the relative permeability of air gap; the fabricated T_1 had $L_{lk} = 56.5\ \mu$H, which resulted in $-6.02 < i_p(t_4) + i_s(t_4) < -2.40$ A.

The self-inductance L for a given S_a is given by [36] and [37]

$$L = L_m + L_{lk} = \frac{\mu_0 N^2 A_c}{2S_a + l_e/\mu_r} = 677.7\ \mu\mathrm{H}$$

where $A_c = 1.75\ \mathrm{cm}^2$ is the effective cross-sectional area of the core and $l_e = 9.87$ cm is the mean magnetic path length. To prevent core saturation, L_m should satisfy

$$kL = L_m < \frac{2S_a A_c B_{\mathrm{sat}}^2}{I_{Lm.\max}^2 \mu_0}$$

where $I_{Lm,\max}$ is the highest value of magnetizing current, and $0 < k < 1$ is the coupling coefficient. The above equation gives $L_m < 820\ \mu$H for $I_{Lm,\max} = 3$ A, $S_a = 0.12$ mm, $A_c = 1.75\ \mathrm{cm}^2$, and the saturation magnetic field $B_{\mathrm{sat}} = 0.47$ T; $L_m = 510\ \mu$H was used in the experiment to prevent core saturation.

The proposed converter is assumed to operate under the condition

$$f_s \gg f_r = \frac{1}{2\pi\sqrt{C_b L_{lk}}}$$

so that i_p and i_s vary linearly in time. The ripple voltage ΔV_{Cb} of C_b is estimated using (5) as

$$\Delta v_{Cb} = \frac{1}{2}\frac{V_L}{C_b L_{lk}}(DT_s)^2.$$

Allowing $\Delta v_{Cb} < 0.02 V_L$, C_b should satisfy

$$C_b > \frac{25}{L_{lk}}(DT_s)^2.$$

From (10), the longest $D = 0.75$ when $V_L = 100$ V and $150 \le V_H \le 400$ V, so $C_b > 13\ \mu$F for $L_{lk} = 56.5\ \mu$H, and $110 \le f_s \le 240$ kHz; the experimental converter used $C_b = 20\ \mu$F.

When the switches have a rising time t_r and a falling time t_f, the condition $t_4 - t_3 > t_r + t_f$ is required to reduce the

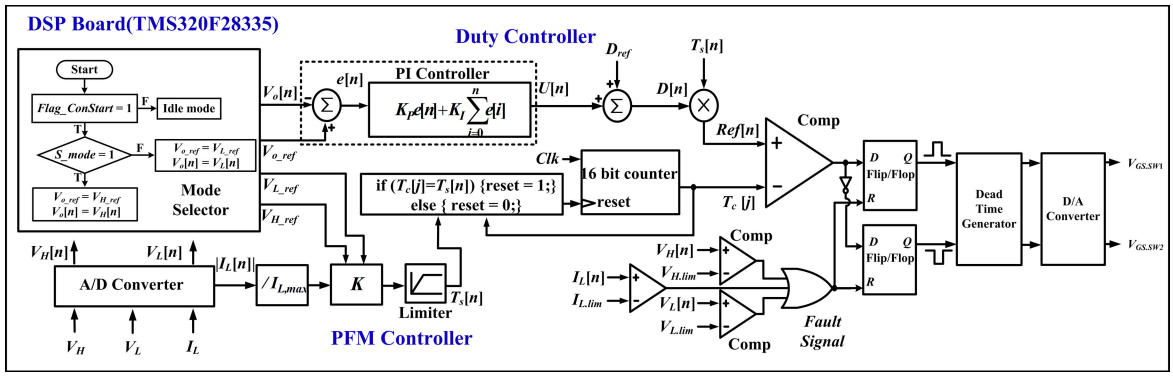

Fig. 8. Block diagram of the digital controller for the proposed converter.

switching loss. Also, to increase the available duty D, C_s should have a discharging time $t_4 - t_3 < T_s/10$. Using (8), (9), and (11) yields

$$\left|\frac{I_o}{V_L} - \frac{(1-D)DT_s}{L_{lk}}\right|(t_r + t_f) < C_s < \left|\frac{I_o}{V_L} - \frac{(1-D)DT_s}{L_{lk}}\right|\frac{T_s}{10}. \quad (16)$$

Considering that the experimental switches (FCH110N65F nMOSFET from Fairchild) have $t_r + t_f = 26.7$ ns, condition (16) results in $0.45 \le C_s \le 5.44$ nF for $V_L = 100$ V, $150 \le V_H \le 400$ V, $0.34 \le D \le 0.75$, $110 \le f_s \le 240$ kHz, and $0.075 \le I_o \le 2$ A; the converter had $C_s = 2.2$ nF to shorten the duration of *Mode* 4.

III. Digital Controller

The main switch and output voltage for the boost conversion are SW_2 and V_H, respectively, and those for the buck conversion are SW_1 and V_L. The digital controller for the proposed converter (see Fig. 8) was implemented using a 32-b digital signal processor (TMS320F28335 from Texas Instruments with 150-MHz clock, 12-b ADC, and 12-ch PWM). The inputs for the controller are the low-side current I_L, the reference voltages $V_{H,\mathrm{ref}}$ and $V_{L,\mathrm{ref}}$, the measured voltages V_H and V_L, and the type of operation (buck or boost). The voltage selector selects $V_{H,\mathrm{ref}}$ and V_H when the type of operation is boost (Flag_ConStart = 1, S_mode = 1), and selects $V_{L,\mathrm{ref}}$ and V_L otherwise. After calculating the error signal $V_{H,\mathrm{ref}} - V_H$ or $V_{L,\mathrm{ref}} - V_L$ and obtaining the proportional–integral (PI) controller output $U[n]$, a PWM reference duty $\mathrm{Ref}[n]$ is obtained by multiplying $U[n]$ with the time-base switching period $T_s[n]$.

The low-side current I_L was measured and normalized with the low-side maximum current $I_{L,\max}$. Then, the normalized current was multiplied with a constant K to obtain a signal that determines the switching period

$$T_s[n] = \frac{f_{\mathrm{clk}}}{f_s} - 1$$

where $f_{\mathrm{clk}} = 150$ MHz is the clock frequency for the 16-b counter; PFM is achieved by resetting the 16-b counter when the counter output $T_c(j)$ reaches to $T_s[n]$; f_s decreases as I_L increases. The switch control pulses are obtained by comparing $T_c(j)$ with $\mathrm{Ref}[n]$ and using the flip/flops and the dead time generator.

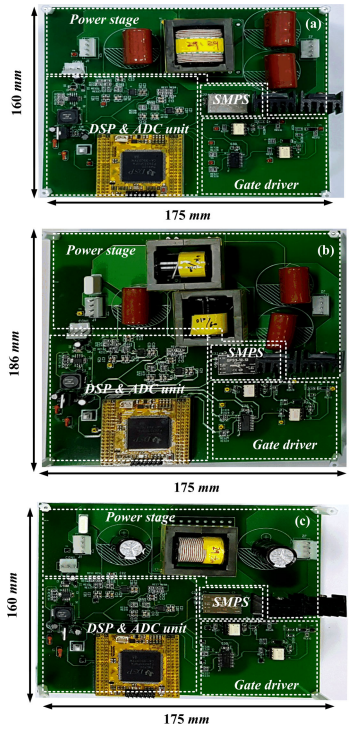

Fig. 9. Photographs of the (a) proposed BDC, (b) converter of [28], and (c) conventional bidirectional converter.

IV. Experimental Results

The proposed converter [see Fig. 9(a)] was built using the circuit parameters in Table I, and tested. It was designed to operate at $V_L = 100$ V, $150 \le V_H \le 400$ V, $0.34 \le D \le 0.75$, $110 \le f_s \le 240$ kHz, and $0.075 \le I_o \le 2$ A. The PI coefficients of the controller were $k_p = 0.02$ and $k_i = 0.2$, and the data sampling rate was 20 kHz. The switching frequency f_s was varied in the range of 140–240 kHz as P_o varied in the range of 30–300 W at $V_L = 100$ V, $V_H = 200$ V. The dead time was 0.266 μs.

TABLE I
POWER LOSSES IN THE LLC RESONANT CONVERTER UNDER DIFFERENT CONTROLS

Parameter	Symbol	Value
N-MOSFET	SW_1, SW_2	FCH110N65F
Magnetizing inductance	L_m	510 μH
Leakage inductance	L_{lk}	56.5 μH
DC blocking capacitor	C_b	20 μF
Snubber capacitor	C_s	2.2 nF
Filter capacitor	C_H, C_L	4.4 μF

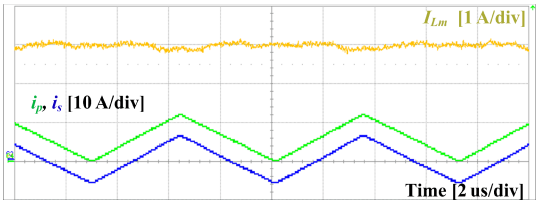

Fig. 10. Waveforms for i_{Lm}, i_p, and i_s; measured at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 300$ W, while the converter operated in boost mode.

For a comparison, the converter of [28] [see Fig. 9(b)] and the conventional bidirectional converter [17] [see Fig. 9(c)] were also built and tested. To ensure fair comparison, these converters used the same switches (FCH110N65F nMOSFET from Fairchild) as the proposed one. The inductor L for the conventional converter was fabricated using the EER 4042 ferrite core with $N = 29$, which resulted in an inductance of 1.2 mH. The conventional converter was operated in continuous conduction mode (CCM) to reduce the current ripple; it operated at $f_s = 140$ kHz to ensure CCM operation at $P_o = 30$ W. The converter of [28] used two identical inductors, instead of the 1:1 transformer in the proposed converter. These inductors were also fabricated using the EER 4042 ferrite cores with $N = 12$, that resulted in $L_r = 56$ μH. $C_b = 20$ μF and $L_r = 56$ μH for the converter of [28]; these are the same as the C_b and L_{lk} in the proposed converter.

The waveforms for i_{Lm}, i_p, and i_s (see Fig. 10) were measured at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 300$ W, while operating the converter in boost mode; they show that i_{Lm} varied much less than i_p and i_s. Considering that the core loss decreases as the ripple of i_{Lm} decreases, the proposed converter is expected to minimize core loss.

The waveforms for $v_{GS,\mathrm{SW}1}$, $v_{GS,\mathrm{SW}2}$, v_{Cb}, and $i_p + i_s$ were measured at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 300$ W, while operating the converter either in boost mode [see Fig. 11(a)], or in buck mode [see Fig. 11(b)]. The waveforms show that $v_{Cb} \approx V_L$, $i_p + i_s < 0$ A at the turn-ON instance of SW_2 for the boost conversion, and $i_p + i_s > 0$ A at the turn-ON instance of SW_1 for the buck conversion; these are required to operate the converter properly.

The waveforms for $v_{\mathrm{SW}1}$, $v_{\mathrm{SW}2}$, $i_{\mathrm{SW}1}$, and $i_{\mathrm{SW}2}$ (see Fig. 12) were measured at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 30 - 300$ W, while operating the converter either in boost mode or in buck mode. The waveforms for boost mode [see Fig. 12(a)] show the following.

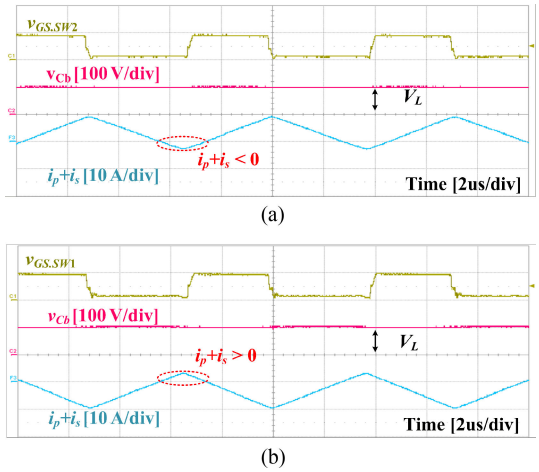

Fig. 11. Waveforms for $v_{GS,\mathrm{SW}1}$, $v_{GS,\mathrm{SW}2}$, v_{Cb}, and $i_p + i_s$; measured at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 300$ W, while the converter operated in (a) boost mode and (b) buck mode.

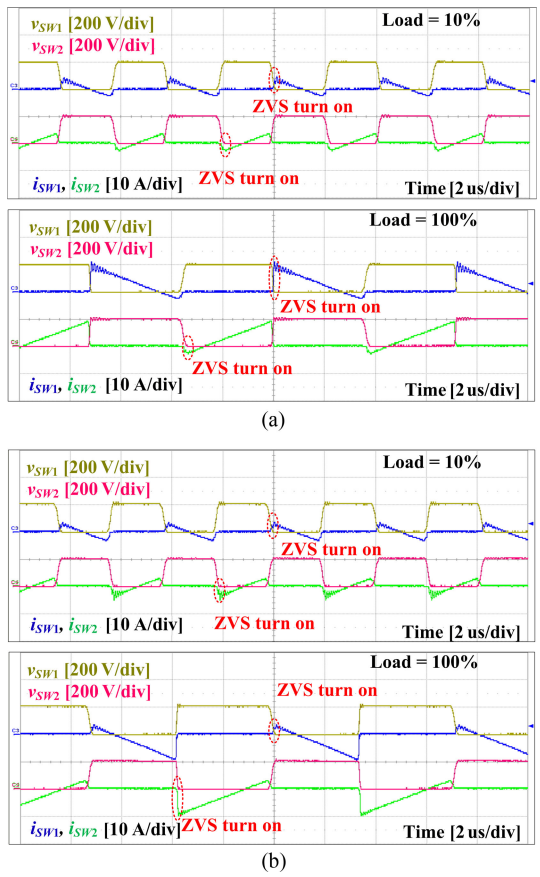

Fig. 12. Waveforms for $v_{\mathrm{SW}1}$, $v_{\mathrm{SW}2}$, $i_{\mathrm{SW}1}$, and $i_{\mathrm{SW}2}$; measured at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 30 \sim 300$ W, while the converter operated in (a) boost mode and (b) buck mode.

1) C_s discharged fully and $i_{\mathrm{SW}2} < 0$ A ($i_{\mathrm{SW}2}$ flowed through D_2) before the turn-ON of SW_2; this behaviors indicate that SW_2 had ZVS turn-ON for *Mode* 1 of boost operation.

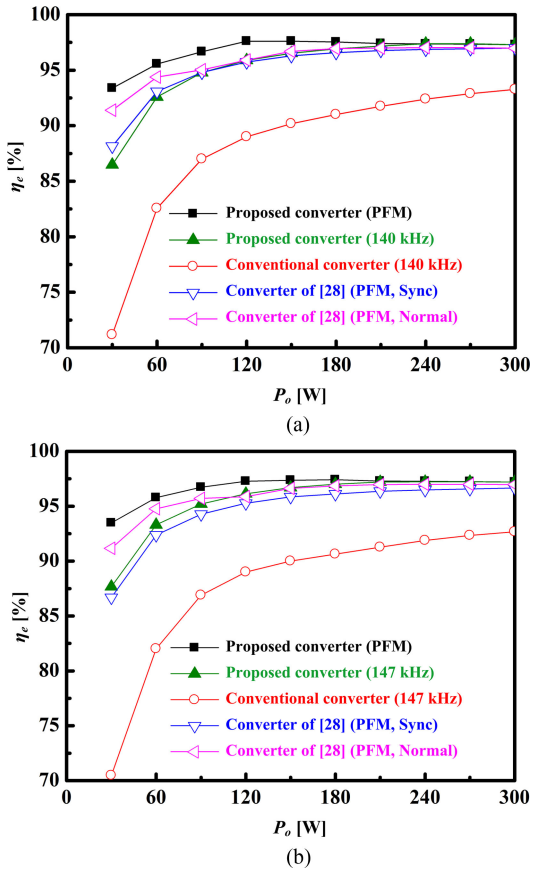

Fig. 13. η_e versus P_o at $V_L = 100$ V and $V_H = 200$ V. (a) Boost. (b) Buck conversions.

2) V_{Cs} increased to V_H when SW_2 was turned OFF; this result indicates that SW_1 had ZVS turn-ON for *Mode* 3 of boost operation.
3) f_s decreased as the load increased. The waveforms for buck mode [see Fig. 12(b)] also show that SW_1 and SW_2 had ZVS turn-ON.

η_e versus P_o for the boost conversion [see Fig. 13(a)] was measured at $V_L = 100$ V and $V_H = 200$ V while the proposed converter was operated either in the PFM mode with a synchronous switching, or was operated at $f_s = 140$ kHz; for comparison, η_e versus P_o was also measured for the conventional bidirectional converter [17] and the converter of [28] under the same measurement condition. When the proposed converter was operated in PFM mode, $\eta_e \geq 97\%$ for $P_o > 120$ W, but decreased as P_o decreased from 120 to 30 W ($\eta_e = 93.5\%$ at $P_o = 30$ W). When the proposed converter was operated at $f_s = 140$ kHz, $\eta_e \geq 97\%$ for $P_o > 210$ W, but decreased to 87.7% at $P_o = 30$ W. The conventional bidirectional converter had $\eta_e = 93.3\%$ at $P_o = 300$ W, but its η_e decreased gradually to 71.2% at $P_o = 30$ W because the switching loss was independent of P_o. The converter of [28] had η_e vs. P_o that was very close to one of the proposed converter operating at $f_s = 140$ kHz: $\eta_e = 97\%$ at $P_o = 300$ W, and 88.1% at $P_o = 30$ W. When the converter of [28] was operated in PFM mode without synchronous switching (the converter of [28]: normal-switching, using SW_2 and the body diode of SW_1), complete discharge of C_s took a fairly long time. The available duty cycle was reduced and the range of f_s was $170 \leq f_S \leq 380$ kHz at $V_L = 100$ V, $V_H = 200$ V and $30 \leq P_o \leq 300$ W. This type of operation had η_e slightly lower than that of the proposed converter: $\eta_e = 97\%$ at $P_o = 300$ W, and 91.4% at $P_o = 30$ W. When the converter of [28] was operated in PFM mode with synchronous switching (the converter of [28]: sync-switching, using both SW_2 and SW_1), C_s discharged fully in a short time, but η_e decreased further when load was light. η_e versus P_o for the buck conversion [see Fig. 13(b)] was quite similar to that for the boost conversion.

The switching loss could be minimized by operating the proposed converter at $f_s = 140$ kHz, which was the lowest f_s for PFM operation, but the current through switches and transformer increased, so the conduction loss increased. Because of this, η_e at $f_s = 140$ kHz was lower than that of PFM operation. η_e of the converter of [28]: sync-switching was lower than that of the proposed converter operating in PFM mode, because the converter of [28] had higher inductor current ripples than the proposed one, which increased the core and conduction losses. The core loss influenced η_e less at $P_o = 300$ W for which $f_s = 140$ kHz, than that at $P_o = 30$ W for which $f_s = 240$ kHz; η_e of the converter of [28]: sync-switching was lower than that of the proposed converter by 5.2% at $P_o = 30$ W and by 0.2% at $P_o = 300$ W. Without synchronous switching, f_s of the converter of [28] increased, but the circulating current was minimized at $V_H/V_L = 2$, so η_e was lower than that of the proposed converter by 2% at $P_o = 30$ W, and by 0.3% at $P_o = 300$ W.

η_e versus P_o for boost conversion was measured also at $V_L = 100$ V and $V_H = 400$ V [see Fig. 14(a)]. The proposed converter under PFM control had $\eta_e \geq 95\%$ at $P_o > 210$ W, but η_e decreased as P_o decreased ($\eta_e = 81\%$ at $P_o = 30$ W). When the proposed converter was operated at $f_s = 147$ kHz, $\eta_e < 95\%$ for $P_o < 300$ W and decreased to 74.25% at $P_o = 30$ W. η_e of the converter of [28]: normal-switching was very close to that of the proposed converter operating at $f_s = 147$ kHz: $\eta_e = 94.63\%$ at $P_o = 300$ W, and 76.5% at $P_o = 30$ W. η_e of the converter of [28]: sync-switching was 93.44% at $P_o = 300$ W and 67.29% at $P_o = 30$ W. η_e of the conventional bidirectional converter was 73.7% at $P_o = 120$ W, but it decreased rapidly to 42.52% at $P_o = 30$ W; this converter failed at $P_o > 120$ W. η_e versus P_o for the buck conversion at $V_H = 400$ V [see Fig. 14(b)] was also similar to that for the boost conversion, except that the converter of [28]: normal-switching failed at any P_o because $V_H/V_L = 4$.

η_e versus V_H at $P_o = 300$ W and $V_L = 100$ V (see Fig. 15) shows that η_es for the boost and buck conversions decreased slightly as the voltage conversion ratio V_H/V_L increased. D increased as V_H/V_L increased, as given in (10) and (14), so both i_p and i_s increased as V_H/V_L increased. η_e for boost conversion was 97.9% at $V_H = 150$ V, 97.3% at $V_H = 200$ V, 96.1% at $V_H = 300$ V, and 95% at $V_H = 400$ V, whereas that for buck conversion was 97.7%, 97.2%, 96%, and 95.1%, respectively. the converter of [28]: normal-switching could not be operated for $V_H < 190$ V in boost mode conversion, and only for $V_H < 210$ V in buck mode conversion, because v_{SW1} and v_{SW2} did not reach to 0 V; switches were destroyed by the current peak due to

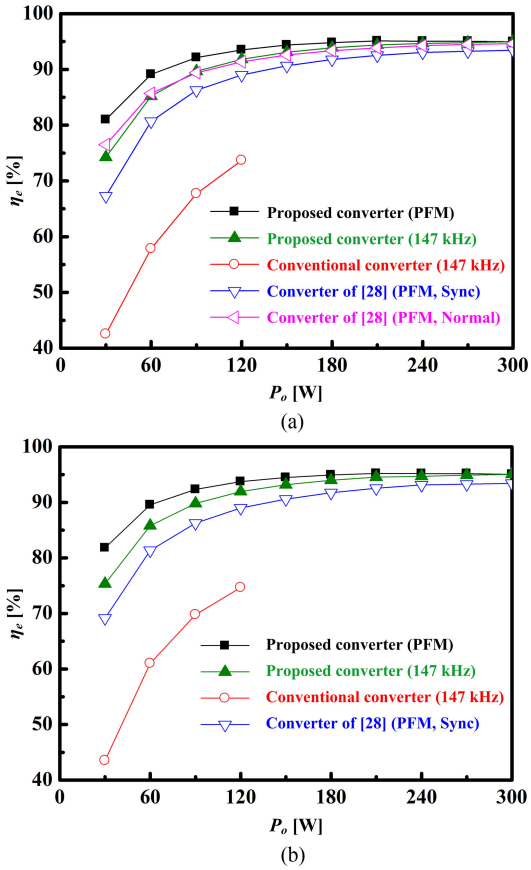

Fig. 14. η_e versus P_o at $V_L = 100$ V and $V_H = 400$ V. (a) Boost. (b) Buck conversions.

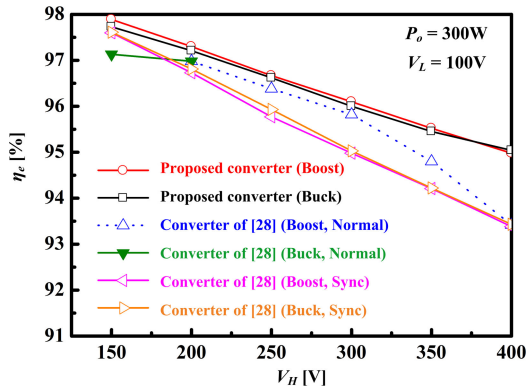

Fig. 15. η_e versus V_H for boost and buck mode conversions.

the hard switching, so the converter could operate bidirectionally only for $V_H/V_L \approx 2$. With synchronous switching, the converter of [28] operated properly at $150 \le V_H \le 400$ V; η_e for the boost conversion was 97.6% at $V_H = 150$ V, 96.7% at $V_H = 200$ V, 95% at $V_H = 300$ V, and 93.4% at $V_H = 400$ V, whereas that for the buck conversion was 97.6%, 96.8%, 95%, and 93.4%, respectively.

the converter of [28]: normal-switching could not be operated for $V_H < 190$ V in boost mode conversion, and only for $V_H < 210$ V in buck mode conversion. The cause of failure could be understood from the waveforms at $V_L = 100$ V,

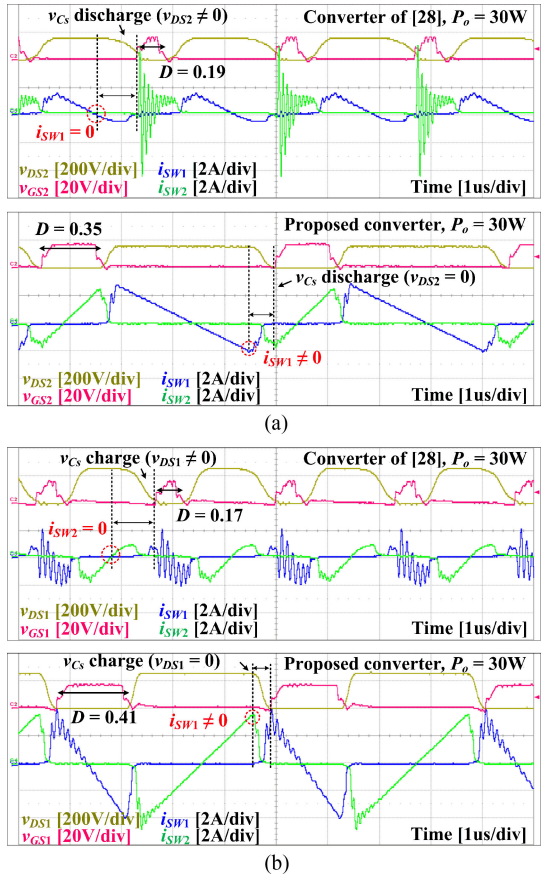

Fig. 16. Waveforms of $i_{\mathrm{SW}1}$, $i_{\mathrm{SW}2}$, v_{DS1}, v_{DS2}, v_{GS1}, and v_{GS2} at $V_L = 100$ V and $P_o = 30$ W. (a) Boost conversion for $V_H = 150$ V. (b) Buck conversion for $V_H = 250$ V.

$V_H = 150$ V, and $P_o = 30$ W for boost conversion, and at $V_L = 100$ V, $V_H = 250$ V, and $P_o = 30$ W for buck conversion. For boost conversion at $V_H/V_L = 1.5$ [see Fig. 16(a)], the converter of [28]: normal-switching could not discharge C_s fully. This remnant charge in C_s produced high-frequency ringing in $i_{\mathrm{SW}2}$, because C_s and the parasitic inductance of SW_2 formed a resonance circuit when SW_2 was turned ON. This high frequency ringing caused a switch failure at $P_o = 300$ W; the high frequency ringing in $i_{\mathrm{SW}2}$ was reduced significantly in the proposed converter. For buck conversion at $V_H/V_L = 2.5$ and $P_o = 30$ W [see Fig. 16(b)], the converter of [28]: normal-switching could not charge C_s to V_H. In this case, the remnant charge in the output capacitor of SW_1 produced high frequency ringing in $i_{\mathrm{SW}1}$ and caused a switch failure at $P_o = 300$ W; the proposed converters achieved ZVS condition, although they also had some ringing in $i_{\mathrm{SW}1}$.

The power losses in the proposed converter, the converter of [28]: normal-switching, and the conventional converter were analyzed at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 300$ W using a circuit simulator. The total power losses for boost conversion (see Fig. 17) were 5.76 W (proposed), 9.53 W (converter of [28]), and 18.82 W (conventional). The percentile core, winding, switch, and capacitor losses in the proposed converter were 3.5%, 51.2%, 43.9%, and 1.4%, respectively, and the ones in

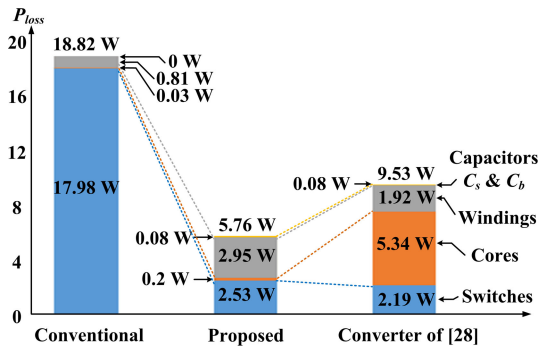

Fig. 17. Power losses in the proposed converter, the converter of [28], and the conventional converter for boost conversion at $V_L = 100$ V, $V_H = 200$ V, and $P_o = 300$ W.

the converter of [28] were 56%, 20.2%, 23%, and 0.8%, respectively. In contrast to these, the switch loss took 95% of the power loss in the conventional converter. (The lower losses for buck conversion were similar to those for boost conversion.)

The switch loss in the conventional converter was highest, because the switches were subjected to a hard switching. The switch loss in the proposed converter was slightly higher than that in the converter of [28] because the synchronous switching allowed the reverse current of switch. The core loss in the proposed converter was as low as 0.2 W because the ripple of magnetic flux was minimized by connecting the windings of transformer in a series-aiding configuration, but the winding loss was 1.5 times higher than that in the converter of [28] because the number of turns for the transformer was increased. The core loss in the converter of [28] was 5.34 W, which is 27 times higher than the core loss in the proposed converter.

V. Conclusion

This paper has proposed a circuit structure of a BDC that can achieve high power conversion efficiency over a wide range of output power. The proposed converter uses a 1:1 transformer, two switches, two capacitors, and a control circuit for PFM. The windings of transformer are connected in a series-aiding configuration to reduce inductor current ripples and to improve power conversion efficiency η_e. The capacitors and the leakage inductance of transformer provide soft-switching conditions. Experimental results at a switching frequency of 110–240 kHz, an input/output voltages of 100–400 V, and an output power P_o of 30–300 W, achieved $\eta_e \geq 97\%$ for $P_o \geq 90$ W, and $\eta_e = 93.5\%$ even at $P_o = 30$ W; these results demonstrate that the proposed converter is well suited to photovoltaic power-conversion and energy-storage systems.

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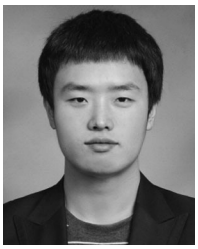
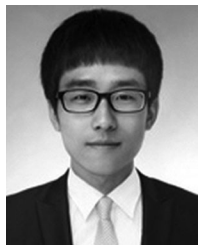


Yoon-Geol Choi received the B.S. degree in electrical engineering from Dongguk University, Seoul, South Korea, in 2013, and the M.S. degree in electrical engineering in 2015 from Pohang University of Science and Technology, Pohang, South Korea, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include dc–dc converters, PV micro inverters, power factor correction, and active cell balancing circuits for automotive batteries.

Sang-Won Lee received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, South Korea, in 2014 and the M.S. degree in electrical engineering in 2016 from Pohang University of Science and Technology, Pohang, South Korea, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include high-power converters, wireless power transfer system, battery management system, and active cell balancing circuits for automotive batteries.

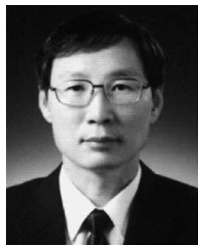


Hyeon-Seok Lee received the B.S. degree in electrical engineering from Chungnam National University, Daejeon, South Korea, in 2013 and the M.S. degree in electrical engineering in 2015 from Pohang University of Science and Technology, Pohang, South Korea, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include the LED driving circuit, soft-switching techniques in dc-dc converter, and microinverter.

Su-Chang Lee received the B.S. degree in electrical engineering from Hanyang University, Ansan, South Korea, in 2003 and the M.S. and Ph.D. degrees in electrical engineering from Pohang University of Science and Technology, Pohang, South Korea, in 2005 and 2008, respectively.

He is currently an Engineer with LG Electronics Co., Ltd., Energy Business Center, Gumi, South Korea. His research interests include PV micro inverters, new converter topologies, and soft-switching techniques in ac-dc and dc-dc converters.



Bongkoo Kang (S'83–M'86) received the Ph.D. degree in electrical engineering from the University of California Berkeley, Berkeley, CA, USA, in 1986.

Following his graduation, he was with the Electronics and Telecommunication Research Laboratory, Daejeon, South Korea, where he worked on developing semiconductor processing equipment. Since 1989, he has been a Professor with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, South Korea. His current research interests include the design of drive circuits for display devices and the modeling and characterization of semiconductor devices.