High Power Density Z-Source Resonant Wireless Charger With Line Frequency Sinusoidal Charging

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***Abstract*—Wireless charger for electric vehicles (EVs) is an offline application and it needs power factor correction (PFC) function, which usually consists of a front-end boost PFC and a cascaded dc–dc converter. Z-source resonant converter (ZSRC), a single-stage solution with low cost and high efficiency, was proposed for EV wireless charger lately. The Z-source capacitors in the ZSRC are designed to absorb the double-line frequency ripple in this single-phase application. Sinusoidal charging, which allows the double-line frequency ripple propagate to the output, is another solution aiming at reducing the bulky capacitors. Recently, a comparison of low-frequency (120 Hz) sinusoidal charging and dc charging shows a negligible impact on Li-ion batteries' performance. Therefore, the ZSRC's capacitor, the biggest component, can be reduced dramatically from millifarad to several microfarads with a sinusoidal charging technique, which features the ZSRC high power density. Also, it keeps the Z-source's benefit of boost ability and being immune to shoot-through problems. In this paper, the sinusoidal charging behavior for the ZSRC is modeled, and a control scheme that has both PFC function and load regulation for sinusoidal charging is proposed. This control scheme can pass IEC61000-3-2 Class A criterion. Experimental results based on a 1-kW prototype with 20 cm air gap between the primary and secondary side are presented to illustrate the proposed control scheme.**

***Index Terms*—Power factor correction (PFC), resonant converter, sinusoidal charging, wireless power transfer (WPT), Z-source.**

I. Introduction

RESEARCH on wireless power transfer (WPT) for electric vehicle (EV) battery charger is actively carrying on, for the sake of its advantages of convenience, reliability, and environmental adaptation [1]. A proper energy storage and charging system design could reduce to about 20% battery capacity of the online electric vehicle [2], minimizing the weight and cost.

Conventional on-board battery charger (OBC) is usually a two-stage structure, front-end power factor correction (PFC) and cascaded dc–dc converter, with a high-frequency transformer, as shown in Fig. 1. Two-stage structure separates the optimization goals for PFC function and load regulation. Recently, a low-cost high-efficiency single-stage solution with the Z-source resonant converter (ZSRC) was proposed in [3] (see Fig. 2).

Manuscript received July 7, 2017; revised December 27, 2017; accepted February 9, 2018. Date of publication February 16, 2018; date of current version September 28, 2018. Recommended for publication by Associate Editor Wing-Hung Ki. *(Corresponding author: Hulong Zeng.)*

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Digital Object Identifier 10.1109/TPEL.2018.2806919

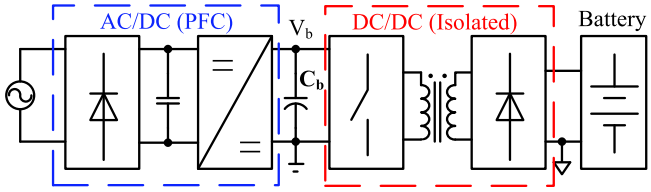

Fig. 1. Block diagram of a conventional OBC.

The ZSRC has a Z-source [4] network between the input rectifier and the H-bridge inverter of the conventional dc–dc system. The Z-source network (ZSN) provides the unique feature of inherent PFC without adding extra switches such as conventional two-stage solutions do. In addition, the ZSN has immunity to shoot-through damage of the H-bridge inverter, which makes the system more reliable [4]. In the previous literature, the ZSN capacitors served as the bulky double-line frequency filter as the conventional two-stage structure does, which is one of the major power density barriers in the system. By decoupling the double-line frequency ripple to an extra capacitor with more voltage fluctuation [5]–[7], the total size can be reduced greatly. However, most of these solutions need extra switches, which is against the ZSRC's low-cost feature.

On the other hand, sinusoidal charging, which had already been brought out in the early 1990s [8], allows the low-frequency ripple to propagate to the battery and does not require energy storage component for the low-frequency ripple. Research done on a lead-acid battery [9] shows that there is no significant influence on battery temperature and capacity by utilizing sinusoidal charging. Recently, a comparison of low-frequency (120 Hz) sinusoidal charging and dc charging shows a negligible impact on the performance of Li-ion batteries [10]–[12], which is the mainstream energy storage component for the EV [13], [14]. Therefore, sinusoidal charging is a promising technique for EV battery charger. In OBC application, sinusoidal charging can be easily realized by changing the algorithm on the PFC stage [13]–[19]. However, most of these solutions still maintain the two-stage structure with the only benefit of reducing the bulky bus capacitor. ZSRC, as a single-stage solution, can maximize the volume and cost reduction of utilizing sinusoidal charging.

In the previous literature [3], the control scheme for the ZSRC can only have good PF at full load and poor PF at half load. In this paper, the sinusoidal charging technique is introduced to the ZSRC for the first time. It can overcome previous low PF issue and pass IEC61000-3-2 Class A criterion for all loads with all the double-line frequency power directly to the output. The following sections are organized as below. In Section II, the ZSRC's sinusoidal charging behavior is modeled, and two approaches

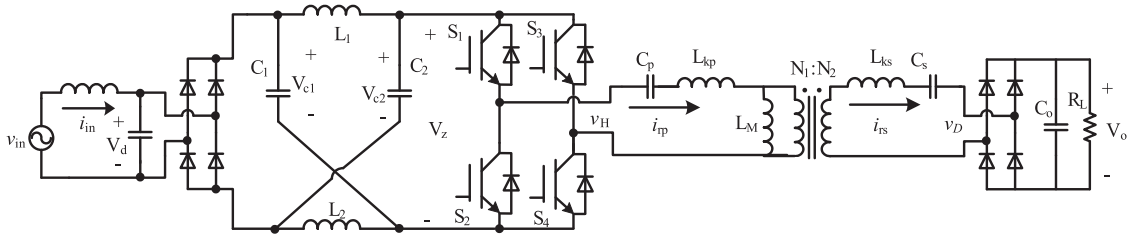

Fig. 2. Circuit schematic of the ZSRC (I-type core shape for the coils [21]).

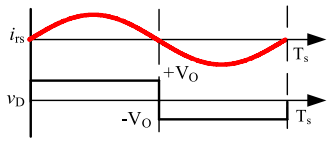

Fig. 3. Secondary side waveform in one switching period.

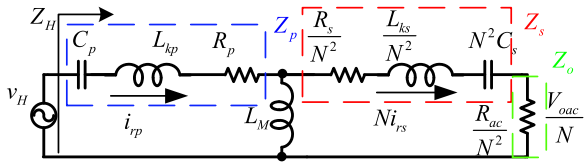

Fig. 4. Simplified circuit of the resonant network.

are brought out for implementing the control schemes. In Section III, two specific control schemes that have both PFC function and load regulation for sinusoidal charging are proposed from the two approaches. In Section IV, based on the proposed control scheme, the exact values for the ZSN are calculated with the desired ripple requirement. In Section V, experimental results based on a 1-kW prototype with 20 cm air gap between the primary and secondary side are presented to illustrate the proposed control scheme. Soft startup has been tested for the proposed control scheme. Section VI concludes the paper.

II. Modeling of Sinusoidal Charging

In PFC application, the source is usually a voltage source from the grid. To achieve unity PF, one can directly control the input current to follow the input voltage simultaneously. The other way is to control the input power such that the current matches automatically. In this section, the equations for these two approaches are derived.

A. Input Current Approach

The dc characteristic of the ZSRC can be found in detail in [20]. The secondary side rectifier can be modeled as an ac resistor ($R_{\rm ac}$) by fundamental harmonic approximation, as shown in Fig. 3. Assuming all the power is carried by the fundamental component, the expression of $R_{\rm ac}$ is

$$R_{\rm ac} = \frac{v_{D(1)}}{i_{\rm rs}} = \frac{V_o^2}{P_o} \tag{1}$$

where $v_{D(1)}$ is the fundamental component of v_D. For conventional dc charging, the output power P_o is constant. However, in sinusoidal charging, the output power follows the input power simultaneously, and battery voltage V_o is constant. Therefore, $R_{\rm ac}$ changes over one line frequency period. The expression of $R_{\rm ac}$ is revised to

$$R_{\rm ac}(t) = \frac{V_o^2}{P_{o\_\rm peak}|\sin(120\pi t)|^2} = \frac{R_{\rm ac\_peak}}{|\sin(120\pi t)|^2}. \tag{2}$$

The WPT system can be simplified as one voltage source v_H and a resonant network with all the parameters reflected to the primary side, as Fig. 4 shows. The voltage source v_H is the output of the H-bridge and v_H contains different frequency components. Z_p and Z_s are primary side impedance and secondary side impedance, respectively. Z_o represents the output impedance. N is the turn ratio. The impedance from the output terminals of the H-bridge is Z_H. Also, at resonant frequency ω_0, with certain compensation [21], the impedance Z_H is purely resistive (R_H). According to [20], the input current of traditional phase shift control is

$$i_{\rm in} = \left[\frac{2\sqrt{2}v_{\rm in}}{\pi(1-2D_{\rm st})}\sin\left(\frac{\pi D_{\rm act}}{2}\right)\right]/R_H \tag{3}$$

where

$$R_H = Z_H(\omega_0) = R_p + \frac{(\omega_0 L_M)^2}{(R_{\rm ac}+R_s)/N^2} \approx \frac{(N\omega_0 L_M)^2}{R_{\rm ac}}. \tag{4}$$

Considering $R_{\rm ac}$ is no longer a constant, $i_{\rm in}$ can be derived by inserting (2) and (4) into (3) as

$$i_{\rm in}(t) = \frac{v_{\rm in}(t)\cdot\sin(\pi D_{\rm act}(t)/2)}{[1-2D_{\rm st}(t)]\,|\sin(120\pi t)|^2}\frac{2\sqrt{2}R_{\rm ac\_peak}}{\pi(N\omega_0 L_M)^2}. \tag{5}$$

For the ideal unity PF case, $i_{\rm in}(t)$ should follow $v_{\rm in}(t)$ and the rest of the terms in (5) should be constant. The PFC control scheme is illustrated in the next section.

B. Input Power Approach

Similar to the input current approach, assuming a lossless system, the input power expression in [20] should be modified with a time-varying $R_{\rm ac}$. For phase shift control, we have

$$P_{\rm in}(t) = \left[\frac{2\sqrt{2}v_{\rm in}}{\pi(1-2D_{\rm st}(t))}\sin\left(\frac{\pi D_{\rm act}(t)}{2}\right)\right]^2 \times \frac{R_{\rm ac\_peak}}{(N\omega_0 L_M)^2|\sin(120\pi t)|^2}. \tag{6}$$

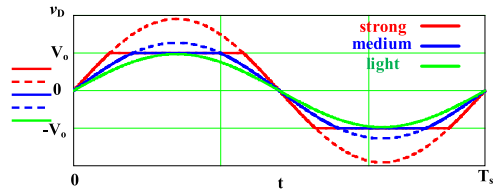

Fig. 5. Secondary side waveform in one switching period with different excitations.

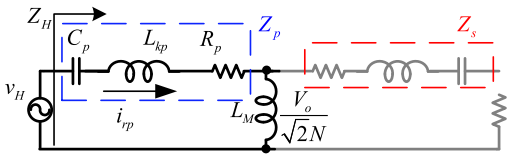

Fig. 6. Simplified circuit of the resonant network at the power discontinuous mode.

Adopting the per-unit concept in [20], a unit-power variable $P_{o,\text{uni}}$ is introduced for (6) as

$$P_{o,\text{uni}}(t) = \left[\frac{\sin(\pi D_{\text{act}}(t)/2)}{(1-2D_{\text{st}}(t))}\right]^2. \tag{7}$$

Then, (6) can be reduced to

$$P_{\text{in}}(t) = \frac{8v_{\text{in\_peak}}^2 R_{\text{ac\_peak}}}{(\pi N\omega_0 L_M)^2} \cdot P_{o,\text{uni}}(t). \tag{8}$$

It is worth emphasizing that (8) is a general expression regardless of a specific control scheme. The two control methods, phase shift control and pulse notch control in [20], differ in unit power $P_{o,\text{uni}}$ expression. Even for one control method, continuous mode and discontinuous mode have different $P_{o,\text{uni}}$ expressions. However, all of these cases can be unified to (8) with specific $P_{o,\text{uni}}$ functions. Moreover, $P_{o,\text{uni}}$ is not related to any input or output information. Therefore, $P_{o,\text{uni}}$ can be calculated offline and stored in one lookup table. This allows us to apply and test different control methods rapidly by updating just one lookup table.

C. Secondary Side Power Discontinuous Phenomenon

The modeling of the secondary side in Fig. 3 is an ideal case. The diode bridge input voltage v_D changes with a limited slope, as Fig. 5 shows (ignoring harmonics). With strong excitation from the primary side, v_D is clamped at the output voltage most of the time in one period while delivering power to output capacitor C_o. As the excitation intensity decreases to medium, the on-time of the diode bridge reduces with less output power. Furthermore, light excitation as shown in Fig. 5 even cannot drive the diode bridge; therefore, no power is flowing between the resonant circuit and the output capacitor. At this power discontinuous point, an equivalent circuit of the resonant network is shown in Fig. 6. As there is no current flowing through Z_s, there is no voltage drop on Z_s and the peak voltage on magnetizing inductor L_m is the dc output voltage V_o over N at a discontinuous mode boundary. The fundamental component of v_D is marked as $v_{D(1)}$, and the peak value of $v_{D(1)}$ is $4V_o/\pi$ where v_D is a square wave at full load.

Based on this boundary value, one can predict when the ZSRC enters this power discontinuous mode at the dc steady state.

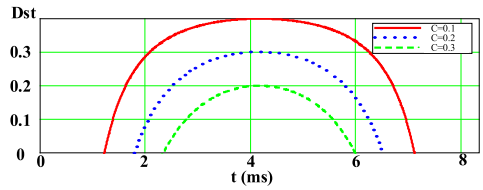

Fig. 7. D_{st} in a half-line period with different values of constant C.

However, in PFC application, the power is time-varying and the resonant network serves as an energy buffer. The true boundary point in one line cycle has a minor error if determined only by this dc method as the time constant for this energy buffer is closed to line frequency and the ac transient exists in every line cycle. Another explanation is that the resonant network is compensated to be pure resistive at the resonant frequency. However, the resonant network is capacitive at line frequency. The dc method only holds true for a resistive case. For example, when the ac input voltage is rising from zero, the resonant network needs some time to be charged to the boundary point; and when the ac input voltage is decreasing from the peak, the resonant network can still provide power to the output for some time even without sufficient input voltage. In a power discontinuous mode, the resonant network continuously draws some amount of current from the input to support its conduction loss. This input current is called "tail current." On one hand, this tail current helps improving power factor by increasing the fire angle; on the other hand, it is uncontrollable as it depends on the system's efficiency. More detail discussion of its effect on PFC would be presented in the next section.

III. PFC for the ZSRC With Sinusoidal Charging

In the ZSRC, there are two control freedoms, which are active state duty cycle (D_{act}) and shoot-through state duty cycle (D_{st}). For the input current approach, these two control freedoms are independent, with the only constraint that the sum of them should be less than 1. On the other hand, D_{act} and D_{st} are dependent on the input power approach, as there is only one variable, input power, in (8). In this section, two specific control schemes are picked up from each approach to illustrate the implementation of the two approaches.

A. Input Current Control

One easy way of control freedoms distribution is to do load regulation with D_{act} and to achieve PFC function by controlling D_{st}. As shown in (5), the input current monotonically increases with D_{act}. Therefore, D_{act} can be used for load regulation and left as a constant over one line period. On the other hand, the denominator of (5) also should be a constant to achieve unity power factor, and we have

$$D_{\text{st}}(t) = 0.5 - \frac{C}{|\sin(120\pi t)|^2} \tag{9}$$

where C is a constant. Fig. 7 shows a D_{st} curve over a half-line period with different parameter C. Since D_{st} must be above zero, part of the curve loses tracking to the sinusoidal term. Smaller C results in higher D_{st} and higher voltage stress on the switching device, while larger C has less controllable region and more

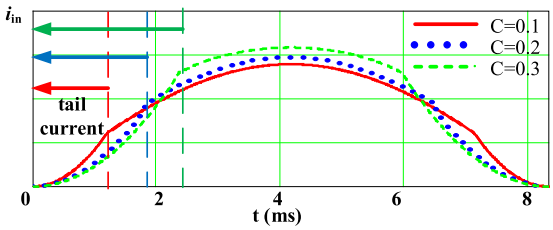

Fig. 8. Input current waveform with different constant *C*.

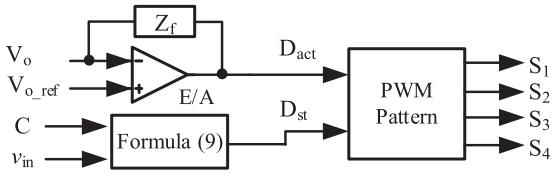

Fig. 9. Block diagram of input current control.

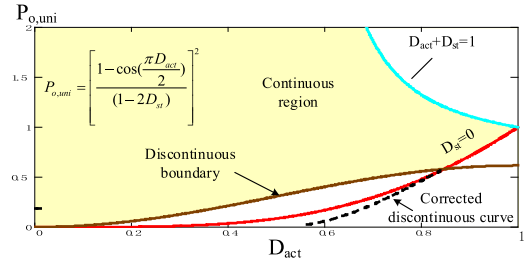

Fig. 10. Unified power curves for pulse notch control with power correction.

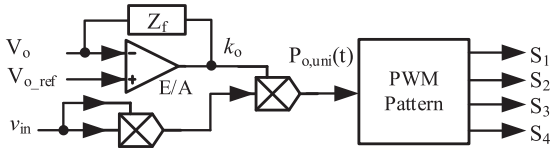

Fig. 11. Block diagram of input power control.

distortion in the input current. It is a tradeoff to determine the constant *C*.

By inserting (9) into (5), we have the input current expression as

$$i_{\text{in}}(t)=\frac{\sqrt{2}v_{\text{in\_peak}}\sin(\pi D_{\text{act}}/2)R_{\text{ac\_peak}}}{C\cdot\pi(N\omega_0 L_M)^2}\cdot\left|\sin(120\pi t)\right|. \tag{10}$$

The first term in (10) is constant over one line period and the second term shapes the input current to pure sinusoidal. However, (10) only holds true when the secondary side is drawing power. When the output rectifier is OFF, tail current is observed on the input side. Fig. 8 shows the input current waveform with different values of constant *C*. The conclusion is coordinate with the previous discussion, where a smaller *C* leads to larger D_{st} and larger portion of controllable i_{in}. On the opposite, a larger *C* results in smaller D_{st} and lower voltage stress on the switch, but the tail current portion is longer in one line period. The boundary of the secondary side power discontinuous mode is roughly around the instant that D_{st} goes to zero. That is because shoot-through duty cycle can still pump energy into the resonant network regardless of the reflection of the output voltage.

The control block diagram for input current control is shown in Fig. 9. Two input signals are needed from the circuit. One is the output voltage indicating the output power. Impedance Z_f has a bandwidth lower than line frequency. The output of the error amplifier is the D_{act} signal for load regulation. The other input signal is the input voltage. Constant *C* is predetermined by the required shape of the input current shown in Fig. 8. The output of (9) serves as D_{st}. The pulse width modulation (PWM) pattern is required to generate arbitrary D_{act} and D_{st}. In this case, the phase shift control in [20] is adopted as the PWM pattern. The input current control is essentially a feed-forward control.

B. Input Power Control

For input power approach, $P_{o,\text{uni}}$ actually is a specific combination of D_{st} and D_{act}, which are stored in a look-up table. As mentioned in [20], some control schemes may involve the need of solving transcendental equation, and therefore, there is no expression for online calculation. Here, we adopt the pulse notch control in [20] as an example since pulse notch control is able to regulate the power all the way down to zero. From (8), the first term is constant and $P_{o,\text{uni}}$ is required to track the double-line frequency power ripple all the way down to zero as

$$P_{o,\text{uni}}(t)=\left|\sin(120\pi t)\right|^2. \tag{11}$$

Fig. 10 from [20] gives a clear image of $P_{o,\text{uni}}$ for pulse notch control. The dashed line below the discontinuous boundary and the two solid lines above the discontinuous boundary are the working points, which are stored in a look-up table. The definition of the discontinuous boundary is when the current peak in the resonant network reaches twice of the Z-source inductor current. More discussion could be found in [20].

The section below the discontinuous boundary (dash line) has shoot-through duty cycle, which can pump energy to the resonant network even at low line voltage. As a result, the tail current phenomenon is not that serious as the input current approach. This can be proved in the experimental section mentioned below.

The control block diagram for input power control is shown in Fig. 11. Two input signals are needed from the circuit. One is the output voltage indicating the output power. Impedance Z_f has a bandwidth lower than line frequency. The output of the error amplifier is a scaler signal (k_o) for load regulation. The other input signal is the input voltage. The square of the input voltage together with the scaler signal contributes to $P_{o,\text{uni}}(t)$, which is the sole input of the PWM pattern block. In this case, the pulse notch control in [20] has been adopted as the PWM pattern. The input power control is also essentially a feed-forward control.

IV. Z-Source Network Design for the ZSRC With Sinusoidal Charging

To design the ZSN, we can analyze the circuit by studying it under different operation modes [4] such as shoot-through state and non-shoot-through state, as shown in Fig. 12.

The ZSN is symmetrical; therefore, $V_c=V_{c1}=V_{c2}$ and $v_L=v_{L1}=v_{L2}$. From [4], we have

$$V_C=\frac{1-D_{\text{st}}}{1-2D_{\text{st}}}V_d. \tag{12}$$

As the phase shift control's shoot-through duty cycle is distributed evenly over one switching cycle [22], as shown in

TABLE I
PROTOTYPE PARAMETERS AND VALUES

Parameter	Value	Parameter	Value
Input voltage ($V_{\rm ac}$)	115 V	Primary side compensating capacitor (C_p)	164 nF
Output	200 V/5 A	Primary side leakage inductance ($L_{\rm kp}$)	0.414 mH
Resonant frequency	18.2 kHz	Magnetizing inductance (L_M)	63 μH
Transformer turns ratio	15:20	Secondary side leakage inductance ($L_{\rm ks}$)	1.07 mH
ZSN capacitors (C_1, C_2)	20 μF	Secondary side compensating capacitor (C_s)	66 nF
ZSN inductors (L_1, L_2)	50 μH	Output filter capacitor (C_o)	4.7 mF
H-bridge	6MBP100VEA120	Input rectifier (SiC)	GHXS020A060S
Output rectifier	15ETH03PBF		

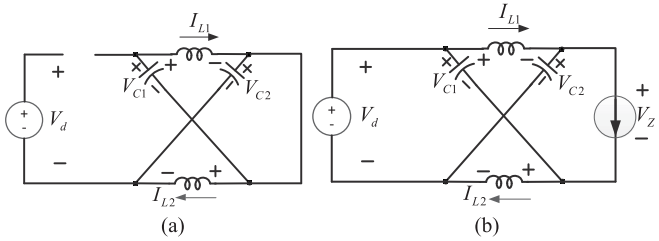

Fig. 12. Equivalent circuits of the Z-source network. (a) Shoot-through state. (b) Non-shoot-through state.

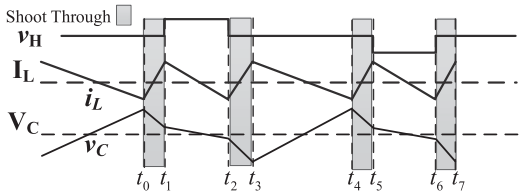

Fig. 13. Z-source inductor current and capacitor voltage in one switching period.

Fig. 13, the Z-source inductor's current bounces back and forth four times in one switching cycle.

To find the maximum current ripple on the Z-source inductor, we focus on the shoot-through section from t_0 to t_1. We have

$$L = \frac{V_c \cdot 0.25 D_{\rm st} \cdot T_{\rm sw}}{\Delta i} = \frac{1 - D_{\rm st}}{(1 - 2D_{\rm st})} \cdot \frac{V_d \cdot 0.25 D_{\rm st}}{\Delta i \cdot f_{\rm sw}} \quad (13)$$

where "$0.25D_{\rm st}$" is used here due to the phase shift control. By choosing the current ripple to be 10 A at ac peak (110 $V_{\rm ac}$) and $D_{\rm st}$ as 0.2 with the prototype parameters in Table I, we can derive the inductance to be

$$L = \frac{1 - 0.2}{(1 - 2 \times 0.2)} \cdot \frac{110 \times 1.414 \times 0.05}{10 \times 18200} H = 57\ \mu{\rm H}. \quad (14)$$

For the Z-source capacitor design, we can follow the same ripple approach. The difference from inductor design is that the capacitor voltage bounces only twice in one switching cycle. Considering the zero state (t_3–t_4), we have the capacitor current as

$$i_C = i_L = P_{\rm in}/V_d. \quad (15)$$

And the maximum voltage ripple happens at ac peak (110 $V_{\rm ac}$) as

$$\Delta V_c = \frac{i_C}{C} \Delta t = \frac{\sqrt{2} P_{\rm in}}{V_Z C} \cdot \frac{0.5 D_{\rm zero}}{f_{\rm sw}} \quad (16)$$

where "$0.5D_{\rm zero}$" represents the zero state (t_3–t_4). To maintain that the ripple is less than 5%, one has

$$\Delta V_C \le 5\% \cdot \left(\frac{1 - D_{\rm st}}{1 - 2D_{\rm st}} \sqrt{2} V_d \right). \quad (17)$$

By pulping in the parameters from Table I into (10) with constant $C = 0.3$, we have $D_{\rm st} = 0.2$, $D_{\rm act} = 0.4$, and $D_{\rm zero} = 0.4$. Then, the minimum capacitance for 5% ripple would be

$$C \ge \frac{P_{\rm in}}{V_Z^2} \cdot \frac{(1 - 2D_{\rm st}) 0.5 D_{\rm zero}}{5\%(1 - D_{\rm st}) f_{\rm sw}} = \frac{1000}{110^2} \cdot \frac{(1 - 2 \times 0.2) \times 0.2}{5\%(1 - 0.2) \times 18200} F = 13.6\ \mu{\rm F}. \quad (18)$$

In summary, the Z-source inductor is 50 μH and the Z-source capacitor is 20 μF for the experimental prototype. Compared to the conventional Z-source inverter [3], the Z-source capacitor is tremendously reduced from 4.7 mF to 20 μF. Moreover, the corresponding Z-source inductor is shrunk from 1 mF to 50 μH as the stability issue at line frequency no longer exists [22].

V. EXPERIMENTAL RESULT

The analysis and design guidelines of the proposed ZSRC system are verified on a 1-kW prototype, whose parameters are summarized in Table I.

A. Steady-State Waveforms

Fig. 14 shows the ac side waveforms for the proposed input current and input power approaches at full load and half load. Constant duty cycle control was tested as a comparison in Fig. 14(a). The input current of the constant duty cycle control appears to be a square waveform and is full of harmonics. Also, the ZSN is not active when $D_{\rm st} = 0$, and the ZSRC reduces to the normal SRC. If a single-stage dc–dc converter is directly fed with the ac source, the power factor is low. From Fig. 14(b)–(e), both of the proposed controls can reshape the input current to be symmetric and less harmonics. In terms of the input current quality, the two proposed controls have similar performance both at full load and half load.

Figs. 15 and 16 show more key waveforms for the two proposed controls at full load. The peak H-bridge voltage v_H is higher in the input current control as the shoot-through duty cycle is allocated only around the ac peak. The input current approach actually is phase shift control in [20], and the voltage stress is high when it enters deep light load, which is the case of low input voltage points around zero crossing. That is

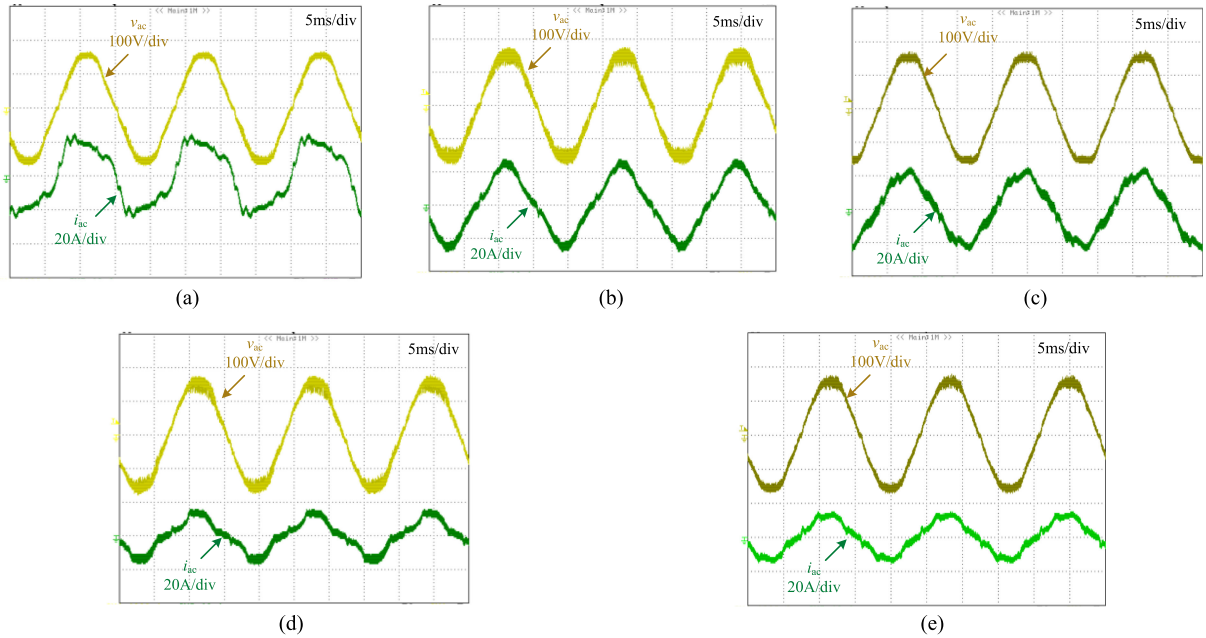

Fig. 14. Experimental waveforms of ac side voltage and current (a) Constant $D_{st} = 0$ and $D_{act} = 0.52$ @full load. (b) Proposed input current approach, $D_{act} = 0.39$ and $C = 0.3$ @full load. (c) Proposed input power approach, pulse notch control @full load. (d) Proposed input current approach, $D_{act} = 0.29$ and $C = 0.35$ @half load. (e) Proposed input power approach, pulse notch control @half load.

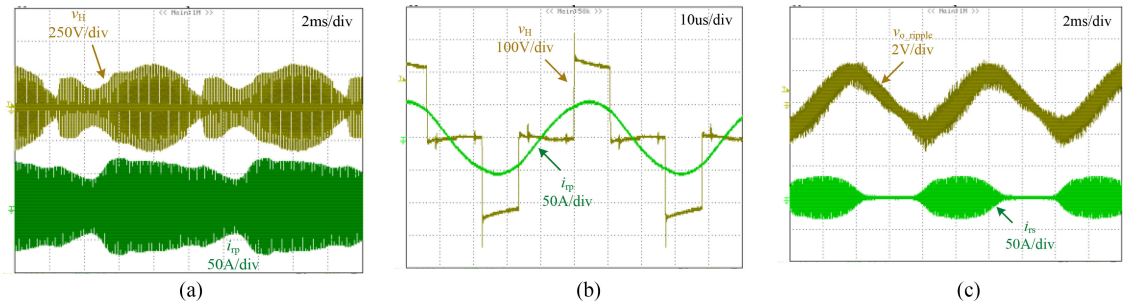

Fig. 15. Key experimental waveforms for the proposed input current control ($D_{act} = 0.39$ and $C = 0.3$) at full load (200 V/1 kW). (a) H-bridge output voltage and current. (b) Zoom-in of (a). (c) Secondary side output voltage ripple.

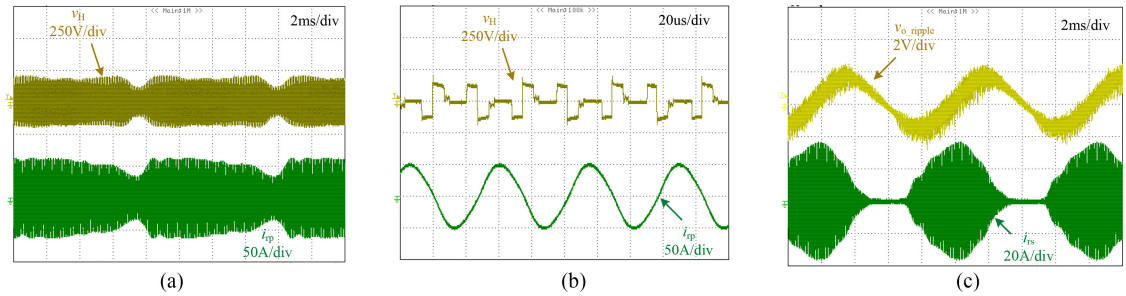

Fig. 16. Key experimental waveforms for the proposed input power control at full load (200 V/1 kW). (a) H-bridge output voltage and current. (b) Zoom-in of (a). (c) Secondary side output voltage ripple.

the reason why the envelop of v_H in Fig. 15(a) bounces up several times in one line period. On the other hand, the example of the input power approach is pulse notch control in [20], and it can regulate the load smoothly all the way down to zero. The envelop of v_H in Fig. 16(a) is symmetric and smooth.

Figs. 15(b) and 16(b) show the switching pattern for the two proposed controls, which correspond to phase shift control and pulse notch control in [20].

Figs. 15(c) and 16(c) show the output voltage ripple and secondary side current for both controls. The secondary side rectifier's off time in the first proposed control is longer than

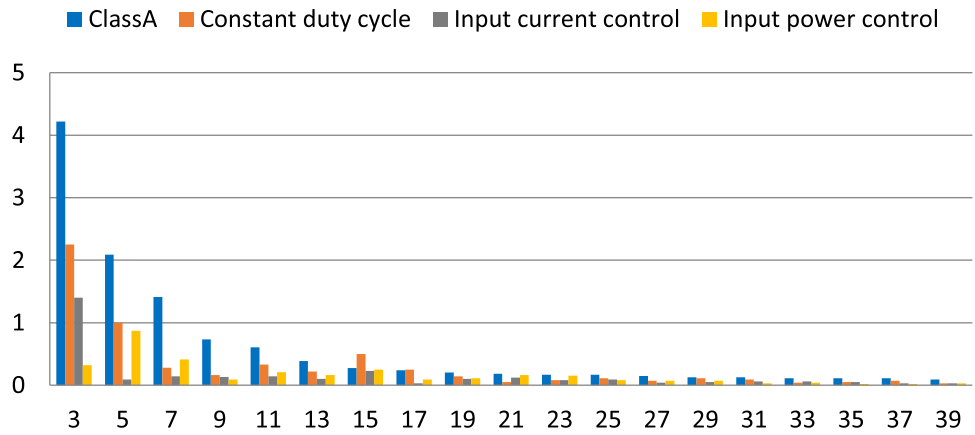

Fig. 17. Input current spectrum at full load (200 V/1 kW).

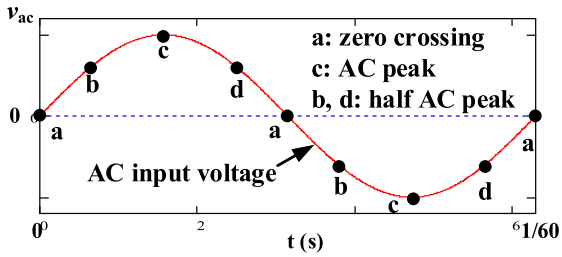

Fig. 18. Four candidates of soft startup instant in one line cycle.

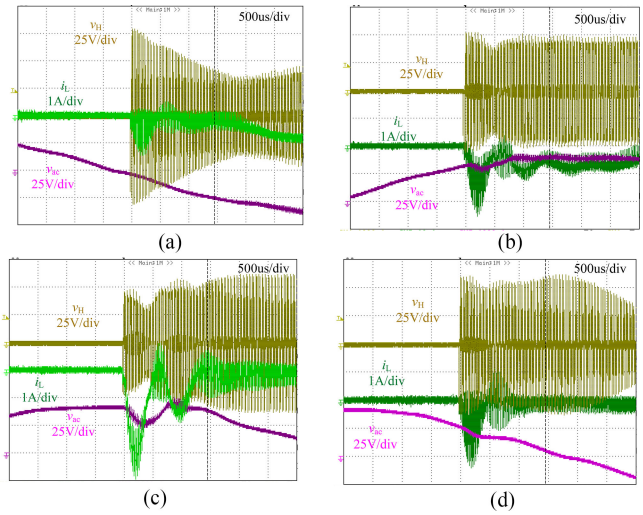

Fig. 19. Soft startup waveforms for the proposed input power control at 32-V ac input voltage. (a) Startup at the ac voltage zero crossing. (b) Startup at the rising edge of the ac voltage. (c) Startup at the ac voltage peak. (d) Startup at the falling edge of the ac voltage.

the second one as the shoot-through duty cycle is allocated all around one line period for the second one.

Fig. 17 shows the input current spectrum of these two control schemes. IEC61000-3-2 Class A criterion is transformed from 220 to 115 V and plotted in Fig. 17 as a reference. Constant duty cycle control fails in the 15th and the 17th harmonics with 23% total harmonic distortion (THD), while the proposed controls pass Class A criterion with 12% THD (input current control) and 10% THD (input power control).

B. Soft Startup Issue

Soft startup for the traditional boost PFC is always an issue and it needs an extra diode to charge the output capacitor before startup. Since there is no bulky energy storage component for sinusoidal charging, the inrush current at startup would be substantially smaller than conventional dc charging. Furthermore, the ZSN can limit the shoot-through current or inrush current inherently. Therefore, the ZSRC does not need any extra hardware or delicate engineering solution for soft startup. However, there are four possible instants in one line period to start up the circuit. It is worth examining all candidates to find the best one.

Before the circuit starts up, the Z-source capacitors are charged to ac peak voltage. In Fig. 19(a), if the ZSRC starts up at the ac voltage zero crossing (point a in Fig. 18), the voltage across the H-bridge would be twice of the ac peak voltage as v_H is the difference between the sum of the Z-source capacitors' voltage and the ac input voltage. In this case, the Z-source inductor current is almost zero as the input voltage experiences zero crossing. In Fig. 19(b), if the ZSRC starts up at the rising edge of the ac voltage (point b in Fig. 18), the voltage across the H-bridge would be around two-third of the voltage of point a. The inrush current is higher than the current of point a but it is still small compared to the steady-state current. In Fig. 19(c), if the ZSRC starts up at the ac voltage peak (point c in Fig. 18), the voltage across the H-bridge would be minimum among these candidates. However, the inrush current is the highest and the sudden change of high *di/dt* would cause some voltage drop due to line impedance from variac. In Fig. 19(d), if the ZSRC starts up at the falling edge of the ac voltage (point d in Fig. 18), the initial voltage across the H-bridge and the inrush current are similar to those of point b. However, as the ac input voltage falls, not much energy is being drawn from the output, and the Z-source capacitor's voltage is still around the ac peak. Therefore, v_H rises when the ac voltage falls to zero and introduces higher voltage stress on the switches than that of point b. In summary, startup at the rising edge of ac voltage (point b in Fig. 18) is the best option with minimum voltage stress on the switches and acceptable inrush current. Fig. 20 shows the start-up waveforms at rated input voltage and full load, which is coordinated with the discussion above.

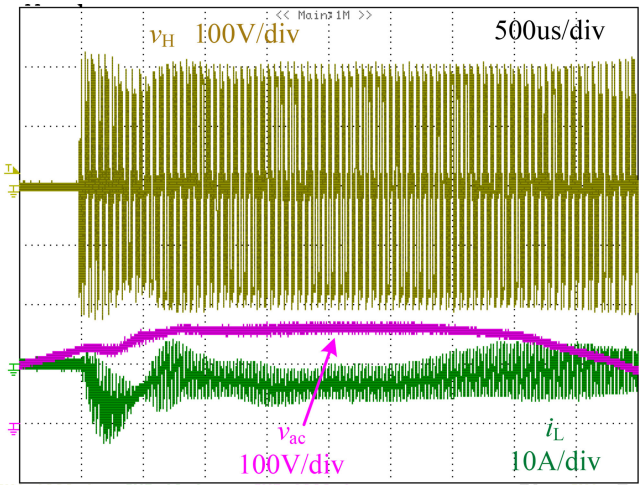

Fig. 20. Soft startup waveforms for the proposed input power control at full load (120 V_{ac}/1 kW).

VI. Conclusion

ZSRC is a single-stage solution with low cost and high efficiency for EV wireless charger application. To further reduce the size of bulky capacitors in single-phase application, the sinusoidal charging technique has been applied to the ZSRC. The Z-source capacitor has been reduced from 4.7 mF to 20 μF to handle the switching ripple only. Both PFC and load regulation functions have been successfully achieved with the two proposed control schemes. They have a relatively good performance in THD and pass IEC61000-3-2 Class A. The input power control has less voltage stress on the switches than the input current control, and therefore, is preferable. Moreover, the ZSRC has inherent soft startup capability. The limitation of these controls is that the input current cannot be perfectly compensated as sinusoidal wave without distortion due to the tail current. For future research, loss analysis would be performed and the efficiency would be improved.

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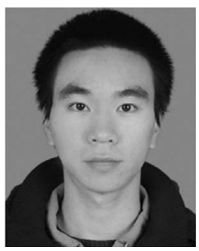

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