Fully ZVS, Minimum RMS Current Operation of the Dual-Active Half-Bridge Converter Using Closed-Loop Three-Degree-of-Freedom Control

Shiladri Chakraborty, *Student Member, IEEE* and Souvik Chattopadhyay, *Member, IEEE*

***Abstract*—This paper discusses how duty ratios of the primary and secondary half-bridge legs of a dual-active half-bridge converter can be used in conjunction with phase-shift control to operate the converter with the least possible transformer rms current at a given power. Following introduction of all possible operational modes arising due to such three-degree-of-freedom control, results from a numerical-optimization-based approach are used to identify the best mode. Using information gleaned from careful observation of simulation results corresponding to the minimum current trajectory in this mode, key insights regarding circuit conditions to be satisfied for optimal operation are obtained. This information is used to propose the framework of a 3-D modulation strategy, which results in globally minimum rms current operation and is remarkably also found to satisfy the necessary conditions for zero-voltage-switching operation of all devices. The proposed strategy is implemented through closed-loop control and, hence, does not have the demerits associated with a lookup-table-based approach involving offline precomputation of optimal duty ratios. Simulation and experimental results on a 625-W laboratory prototype demonstrate the significant efficiency advantages of the proposed modulation scheme compared to simple phase-shift (1-D) control or 2-D asymmetric control, particularly at light loads in applications with widely varying voltage ratios.**

***Index Terms*—Bidirectional power flow, dual-active half-bridge (DAHB), minimum rms current, zero-voltage switching (ZVS).**

I. Introduction

THE dual-active-bridge (DAB) dc–dc converter [2], [3] remains a popular choice in high-power-density, isolated, bidirectional dc–dc power conversion applications because of its advantages such as low passive count, inherent zero-voltage-switching (ZVS) turn-ON of switches in both directions of power flow and voltage-clamped operation of switches, which obviates the need for auxiliary turn-OFF snubber circuitry. The half-bridge version of such a converter, shown in Fig. 1, offers the additional benefits of low device count, reduced size, and operation with zero steady-state dc offset of transformer magnetizing current and can be considered a suitable alternative in the low-power (sub-750-W) regime.

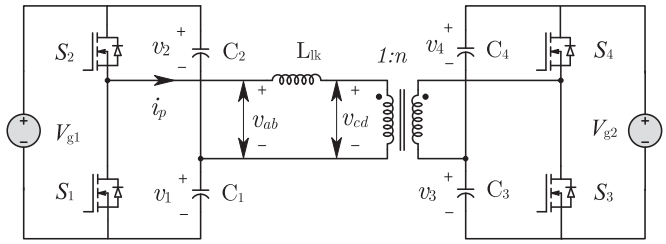

Fig. 1. DAHB converter.

The simplest way to control power flow in DAB and dual-active half-bridge (DAHB) converters is to drive the primary- and secondary-side bridges with a duty ratio of 0.5, and to vary the phase overlap between the resulting square waves. However, such a single-degree-of-freedom-based control (referred to as simple-phase-shift control (SPC) in this paper) results in high circulating current, especially under light-load conditions. Another critical limitation is that ZVS operation over the entire power range is possible only when the effective voltage conversion ratio is unity [2]. In view of the above limitations, several modulation techniques [4]–[16] and topological modifications [17]–[21] have been proposed in contemporary literature, which try to mitigate the problems of high reactive power and loss of ZVS of DAB converters at light loads. Control-oriented solutions do not introduce additional hardware complexity and improve the converter performance by simply changing switching strategies of primary and/or secondary bridges. Some of these modulation schemes employ a two-degree-of-freedom-based approach by either combining square-wave operation of one bridge with phase modulation of the other [4]–[6] or operating both bridges with the same phase-modulation duty ratio [7], [8]. Similar two-degree-of-freedom-based approach has been reported for DAHB converters as well [9].

Maximal improvement in the performance of full-bridge DAB converters is possible by utilizing all three available degrees of freedom, viz., the two duty ratios representing phase overlap among the legs of each of the primary and secondary bridges and the phase shift between the resulting quasi-square-wave voltage waveforms [10]–[16]. In a DAHB converter, the duty ratios of the primary and secondary half-bridges represent two similar additional control handles along with the phase shift between the

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The authors are with the Power Electronics Project Laboratory, Department of Electrical Engineering, Indian Institute of Technology Kharagpur, Kharagpur 721302, India (e-mail: shiladri@ee.iitkgp.ernet.in; souvik@ee.iitkgp.ernet.in).

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rectangular primary and secondary voltage waveforms. Though triple-phase-shift control of DAB converters has been extensively addressed in recent literature, there has been no similar work in the realm of DAHB converters. The exact approach discussed in [15] and [16] for analyzing triple-phase-shift operation of DAB converters cannot be directly applied to DAHB converters because of the fundamentally different nature of the transformer voltage waveforms in the two cases (rectangular in DAHB versus quasi-square wave in DAB), which leads to different operating modes. The fundamental-harmonic-analysis-based strategy discussed in [13] and [14] can be adopted for DAHB converters as well, but such an approach is only accurate for near-resonance operation in converters with a resonant tank network. Hence, this paper takes up the problem of investigating operation of a DAHB converter following three-degree-of-freedom control, which can lead to considerable enhancement of the converter performance compared to square-wave or previously proposed 2-D control.

An important aspect related to optimal operation of DAB or DAHB converters is the actual implementation of the chosen modulation scheme. Some researchers adopt a lookup-table-based approach [14], [15], wherein the optimal values of the duty ratios at discrete points across the power range are precomputed offline based on numerical optimization results or analytically developed closed-form expressions. Though this method is simple, as mentioned in [10] and [17], it may result in errors because of change in operating conditions, parameter variations, etc. The implementation strategy discussed in this paper is similar to the closed-loop-control-based online tracking approach outlined in [16], and hence, it does not have the aforementioned demerits of the lookup-table-based approach.

The remaining part of this paper is organized as follows. In Section II, all possible modes of operation for 3-D control are introduced, followed by analysis of active power output and rms current variation. The optimal search space vis-a-vis least rms current operation is identified in Section III, and ZVS performance under optimal operation is investigated. In Section IV, details of the closed-loop implementation strategy for optimal operation are presented. Simulation and experimental results presented in Section V validate the analysis and highlight the significant efficiency advantages gained at light loads by adopting the proposed control scheme.

II. Steady-State Analysis

A. Modes of Operation

Typical steady-state waveforms of the converter for a generic case of operation with triple duty-ratio control are depicted in Fig. 2. D_1 and D_2 are the duty ratios of the high-side devices (S_2 and S_4) on the primary side (port 1) and the secondary side (port 2), respectively. This results in rectangular voltage waveforms v_{ab} and v_{cd} being impressed across the transformer, whose positive and negative magnitudes can be obtained from volt–second balance of L_{lk} and L_m. These values are listed in Table I. Referring to Fig. 2, the phase-shift duty ratio D_ϕ is defined as the angle (normalized to 2π rad) between the fundamentals of v_{ab} and v_{cd}. Furthermore, the transformer current

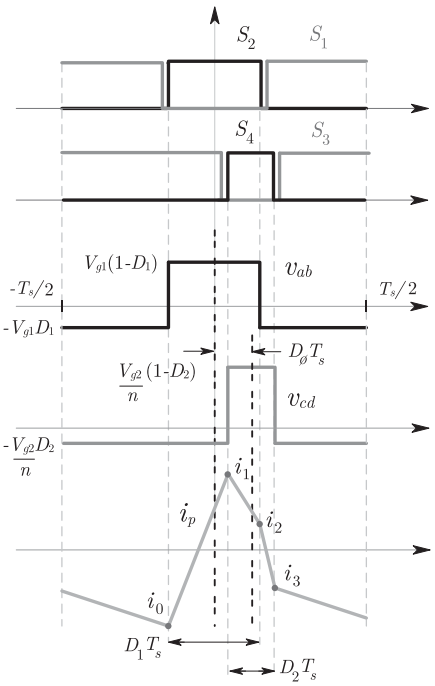


Fig. 2. Generic steady-state waveforms of transformer voltage and current with triple duty-ratio control. Waveforms are for mode 1b.

TABLE I
Average Values of Capacitor Voltages in the Steady State

Voltage	Expression	Voltage	Expression
V_1	$V_{g1}D_1$	V_2	$V_{g1}(1-D_1)$
V_3	$V_{g2}D_2$	V_4	$V_{g2}(1-D_2)$

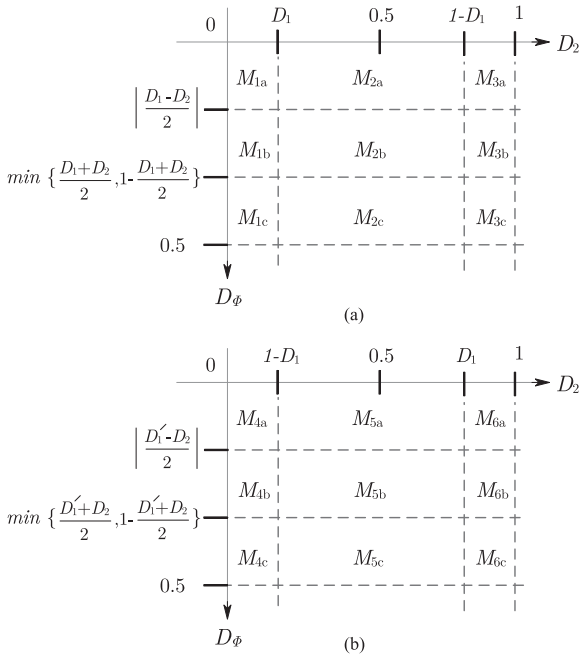


Fig. 3. Explaining the definition of the different operating modes possible for different values of the three control variables D_1, D_2, and D_ϕ for $P > 0$. (a) For $D_1 < 0.5$. (b) For $D_1 > 0.5$. $D_1' = 1 - D_1$, e.g., for $D_2 < D_1$ and $D_\phi < |D_1 - D_2|/2$, the circuit operates in mode 1a.

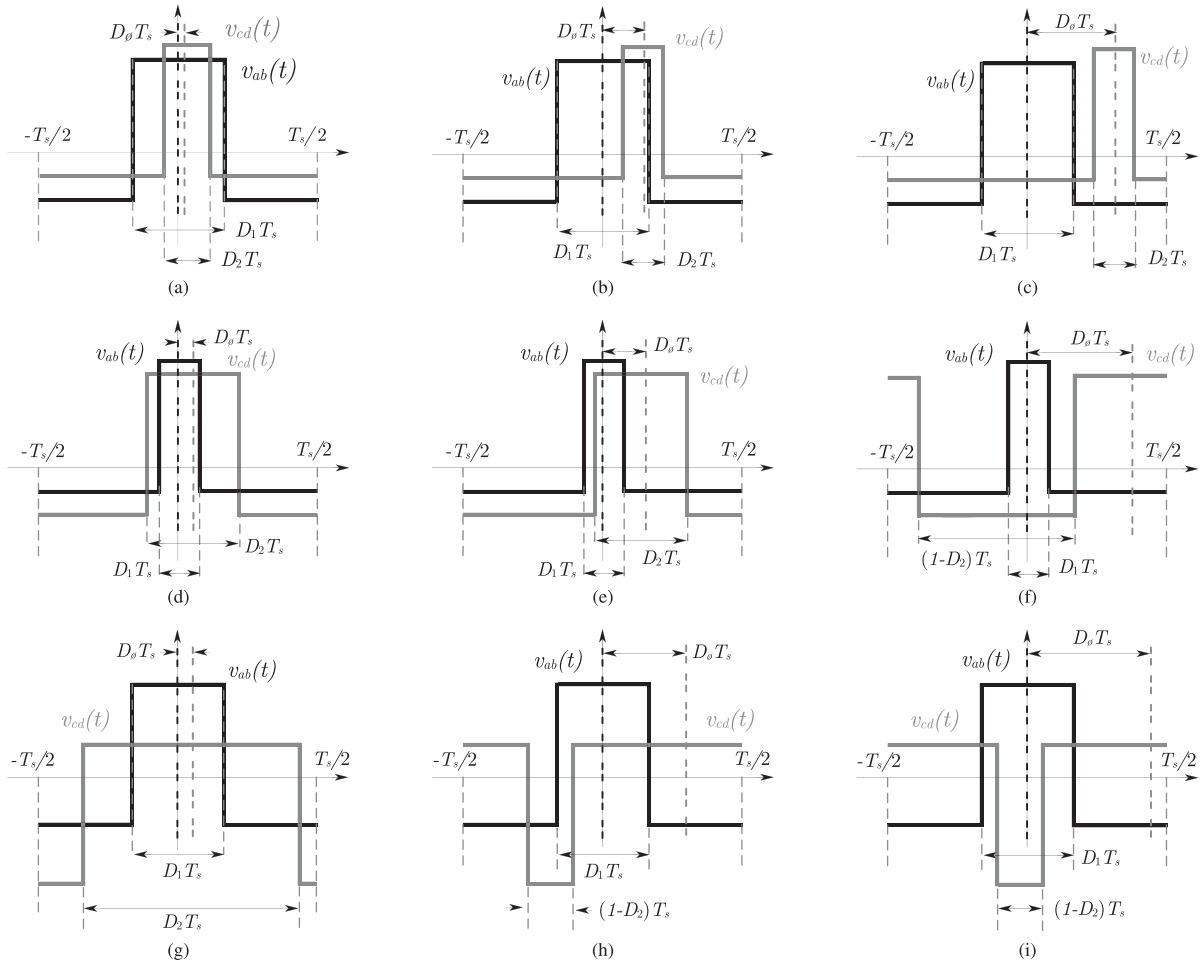


Fig. 4. Representative waveforms of transformer primary (v_{ab}) and reflected secondary (v_{cd}) voltages in different modes for $D_1 < 0.5$. Each mode can be denominated by a schema or a string pattern representing the sequence of rising and falling edge transitions of the transformer voltage waveforms. (a) Mode 1a ($r_1 r_2 f_2 f_1$). (b) Mode 1b ($r_1 r_2 f_1 f_2$). (c) Mode 1c ($r_1 f_1 r_2 f_2$). (d) Mode 2a ($r_1 f_1 f_2 r_2$). (e) Mode 2b ($r_1 r_2 f_1 f_2$). (f) Mode 2c ($r_1 f_1 r_2 f_2$). (g) Mode 3a ($r_1 f_1 f_2 r_2$). (h) Mode 3b ($r_1 r_2 f_1 f_2$). (i) Mode 3c ($r_1 f_2 r_2 f_1$). Similar modes exist for $D_1 > 0.5$.

(i_p) at the instant $t = -D_1 T_s/2$ is denoted by i_0. Currents at the next three successive switching instants are denoted by i_1, i_2, and i_3, respectively.

Assuming two cases where the voltage of port 1 is either greater or lesser than the reflected voltage of port 2, i.e., $M = V_{g2}/nV_{g1} < 1$ and > 1, respectively, it is evident that analysis of the complete operating region of the converter can be performed by assuming positive power flow from port 1 to port 2. With this assumption, depending on the relative values of D_1, D_2, and D_ϕ, 18 different modes of operation are possible, with nine such modes occurring for $D_1 < 0.5$ and the remaining nine for $D_1 > 0.5$. The defining conditions for these modes in the D_2–D_ϕ plane are pictorially represented in Fig. 3, while representative transformer voltage waveforms for modes 1–3 are depicted in Fig. 4. Each mode can be represented by a schema, which indicates the sequence of rising and falling edges of the transformer voltage waveforms at ports 1 and 2. For instance, modes 1b, 2b, and 3b are expressed by the schema $\{r_1 r_2 f_1 f_2\}$. Modes having the same schema pattern have the same expressions for steady-state active power and rms current. Furthermore, it can be shown that the modes for $D_1 > 0.5$ have similar power and rms current expressions to corresponding modes for $D_1 < 0.5$. Hence, for simplicity, these modes are not considered in further analysis.

B. Expressions for Active Power and RMS Current

Following the generic approach outlined in [9] and using the symbolic computation feature of a software package like MATLAB or Maple, expressions for active power and rms current in different modes can be easily obtained. Closed-form expressions for steady-state active power (normalized to the global maximum) along with respective maximum values and rms current in different nodes are listed in Tables II and III, respectively. It is observed that the maximum power corresponds to modes 1b and 2b.

III. Minimum RMS Current Operation

A. Identification of Mode With the Lowest RMS Current

In order to identify the mode/modes with the least rms current at a given power, a numerical-optimization-based approach

TABLE II
EXPRESSIONS FOR $i_{p(rms)}{}^2$ IN DIFFERENT MODES
($k = L_{lk} f_s$, $D_1' = 1 - D_1$, $D_2' = 1 - D_2$, $D_\phi' = 1 - D_\phi$, $M = V_{g2}/(nV_{g1})$)

Mode	Expression
M1a	$(V_{g1}^2/12k^2)[(D_1 D_1')^2 + (M D_2 D_2')^2 + 12M D_1' D_2 D_\phi^2 + M D_1' D_2 (D_1^2 + D_2^2 - 2D_1)]$
M1b, M2b, M3b	$(V_{g1}^2/24k^2)[M(D_1^3 + D_2^3) - 8M D_\phi^3 + 2(D_1 D_1')^2 + 2(M D_2 D_2')^2 + 12M D_\phi^2 (D_1 + D_2)$ $-2M(D_1^2 + D_2^2)(3D_\phi + D_1 D_2) + 3M D_1 D_2 (D_1 + D_2) - 4M D_1 D_2 (6D_\phi^2 - 3D_\phi + 1)]$
M1c, M2c	$(V_{g1}^2/12k^2)[(D_1 D_1')^2 + (M D_2 D_2')^2 - M D_1 D_2 (D_1^2 + D_2^2 + 2 - 12M D_\phi D_\phi')]$
M2a, M3a	$(V_{g1}^2/12k^2)[(D_1 D_1')^2 + (M D_2 D_2')^2 + 12M D_1' D_2 D_\phi^2 + M D_1 D_2' (D_1^2 + D_2^2 - 2D_2)]$
M3c	$(V_{g1}^2/12k^2)[(D_1 D_1')^2 + (M D_2 D_2')^2 - M D_1' D_2' (D_1'^2 + D_2'^2 + 2 - 12M D_\phi D_\phi')]$

TABLE III
EXPRESSIONS FOR ACTIVE POWER (NORMALIZED TO $P_{\max}$) IN DIFFERENT MODES
($P_{\max} = (V_{g1} V_{g2})/(32nL_{lk} f_s)$, $D_1' = 1 - D_1$, $D_2' = 1 - D_2$, $D_{\text{eq}} = D_1 + D_2 - 2D_1 D_2$)

Mode	Normalized power	Maximum power
M1a	$32 D_1' D_2 D_\phi$	$(1/2)P_{\max}$
M1b, M2b, M3b	$4[4D_\phi (D_{\text{eq}} - D_\phi) - (D_1 - D_2)^2]$	$P_{\max}$
M1c, M2c	$16 D_1 D_2 (1 - 2D_\phi)$	$(16/27)P_{\max}$
M2a, M3a	$32 D_1 D_2' D_\phi$	$(16/27)P_{\max}$
M3c	$16 D_1' D_2' (1 - 2D_\phi)$	$(1/2)P_{\max}$

TABLE IV
PARAMETER VALUES FOR OPERATION WITH $M = 1/2$ AND $M = 2$

V_{g1}	V_{g2}	Turns ratio (n)	M	L_{lk}	f_s	$P_{\max}$
200 V	50 V	1/2	1/2	20 μH	50 kHz	625 W
50 V	200 V	2	2	5 μH	50 kHz	625 W

is adopted. Using MATLAB's "fmincon" function, which numerically calculates the optimum value of a constrained optimization problem, the least rms current solution in each mode is computed for a given power reference. For this, rms current and active power output expressions of each mode, listed in Tables II and III, respectively, are used, while ensuring that variable bounds satisfy the inequality constraints in that particular mode. The exercise is performed for two pairs of values of $M(= V_{g2}/nV_{g1}) - M = \{2, 1/2\}$ and $M = \{5, 1/5\}$. Parameter values corresponding to $M = \{2, 1/2\}$ are noted in Table IV and are more commonly used in the rest of this paper, unless otherwise mentioned.

Results of this numerical optimization exercise are illustrated in Fig. 5, where D_{HV} and D_{LV} refer to the duty ratios of the top switches on the high-voltage (HV) and low-voltage (LV) sides of the converter. It is evident that for $M > 1$ and $M < 1$, the optimal trajectory corresponds to operation in modes 1b and 2b, respectively. Furthermore, it may be observed that the optimal values of D_1 and D_2 are equal to 0.5 (SPC) above a certain power limit P_{lim}, which is around 82% and 98% for $M = \{2, 1/2\}$ and $M = \{5, 1/5\}$, respectively. By considering other design values of M, it may be shown that the aforementioned observations regarding optimal operation in modes 1b and 2b are generic. It

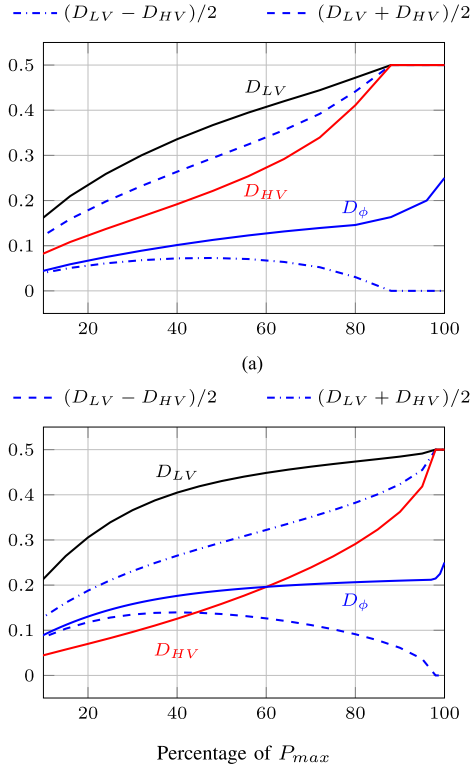


Fig. 5. Trajectories of D_1, D_2, and D_ϕ for minimum current operation obtained using "fmincon" for two pairs of values of $M = V_{g2}/nV_{g1}$. (a) $M = 2$ or $M = 1/2$, $P_{\text{lim}} = 0.82$ p.u. (b) $M = 5$ or $M = 1/5$, $P_{\text{lim}} = 0.98$ p.u. For $M > 1$, $D_{\text{LV}} = D_1$ and $D_{\text{HV}} = D_2$. Operation is in mode 1b. For $M < 1$, $D_{\text{LV}} = D_2$ and $D_{\text{HV}} = D_1$. Operation is in mode 2b.

can be further shown that the critical power P_{lim} decreases and approaches zero as M moves closer to unity, which points to the well-established fact that for $M = 1$, SPC is the most optimal control strategy over the full power range [9].

B. Investigation of ZVS Performance

In this section, ZVS performance of the switches of the converter, when operated under minimum rms current control, is investigated. The necessary condition to ensure ZVS of any switch is that just prior to its turn-ON, the corresponding switch node current should be in a direction such that it discharges the parasitic capacitor across the switch. This directional require-

TABLE V
NECESSARY CONDITIONS FOR ZVS TURN-ON OF INDIVIDUAL SWITCHES IN MODES 1b AND 2b

Mode	S_1	S_2	S_3	S_4
1b	$i_2(i_{\mathrm{LVf}})>0$	$i_0(i_{\mathrm{LVr}})<0$	$i_3(i_{\mathrm{HVf}})<0$	$i_1(i_{\mathrm{HVr}})>0$
2b	$i_2(i_{\mathrm{HVf}})>0$	$i_0(i_{\mathrm{HVr}})<0$	$i_3(i_{\mathrm{LVf}})<0$	$i_1(i_{\mathrm{LVr}})>0$

TABLE VI
EXPRESSIONS FOR i_0, i_1, i_2, AND i_3 IN MODES 1b AND 2b
$(D_1' = 1 - D_1, D_2' = 1 - D_2, k = L_{lk} f_s)$

Current	Expression
i_0	$(1/2nk)(-nV_{g1}D_1D_1' + V_{g2}D_2(D_1' - 2D_\phi))$
i_1	$(1/2nk)(-nV_{g1}D_1'(D_2 - 2D_\phi) + V_{g2}D_2D_2')$
i_2	$(1/2nk)(nV_{g1}D_1D_1' - V_{g2}D_2'(D_1 - 2D_\phi))$
i_3	$(1/2nk)(nV_{g1}D_1(D_2' - 2D_\phi) - V_{g2}D_2D_2')$

ment for ZVS of each switch can be related to the polarity of the corner values i_0, i_1, i_2, and i_3 of the inductor current and is noted in Table V for modes 1b and 2b. The terms within brackets signify whether the given switching instant corresponds to the rising/falling edge transition on the HV/LV side. Closed-form expressions for i_0–i_3 in modes 1b and 2b are listed in Table VI. Using these expressions and the duty-ratio and phase-shift data obtained from "fmincon" results, values of i_0–i_3 under 3-D optimal operation can be computed. These values are plotted in Fig. 6(a) and (b) for $M = \{2, 1/2\}$ and $M = \{5, 1/5\}$, respectively. Comparing Fig. 6 and Table V, it may be concluded that in both cases, the necessary conditions for ZVS for all switches is satisfied over the full power range of the converter. Hence, 3-D optimal control not only achieves the theoretically least rms current at a given power, but also eliminates switching loss of all devices by ensuring their ZVS across the converter's power range.

IV. CLOSED-LOOP OPTIMIZATION CONTROL STRATEGY

A. Condition for Minimum RMS Current Operation

Because of the complex form of the power and rms current expressions in modes 1b and 2b, finding closed-form expressions for the minimum rms current trajectory at a given power using standard constrained optimization techniques (like the Lagrange multiplier method [22]) is a mathematically intractable task. Even if exact closed-form expressions can be deduced, as the authors of [15] manage to do for the full-bridge DAB, their likely cumbersome form would make them unsuitable for real-time implementation in an embedded controller. In this work, a closed-loop-control-based online optimization strategy is proposed, which is based on the following simple but key insight gained from careful inspection of simulation waveforms of the converter. Circuit simulations of the converter, operated with optimal duty ratios (obtained from "fmincon" predictions), reveal that till $P = P_{\mathrm{lim}}$, the transformer current (i_p) at the LV-side

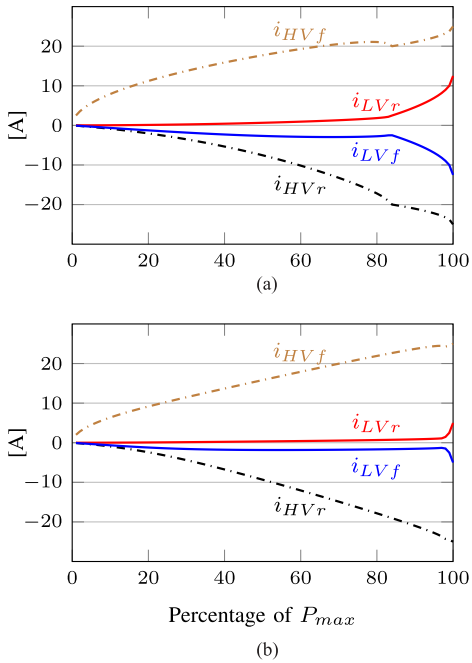


Fig. 6. Plot of the transformer current (on the LV side) at the switching instants for 3-D minimum rms current operation. (a) $M = \{2, 1/2\}$. (b) $M = \{5, 1/5\}$. The suffixes denote the switching instant, e.g., "$\mathrm{LV_r}$" denotes the rising edge of the LV-side voltage waveform. It is observed that across the full power range, all switches satisfy the necessary conditions for ZVS. Also note that the LV-side switches turn ON at close to zero current up to P_{lim}.

switching instants is close to zero, i.e.,

$$i_{\mathrm{LVr}}, i_{\mathrm{LVf}} \approx 0 \tag{1}$$

where i_{LVr} and i_{LVf} denote the values of i_p at the rising and falling edges, respectively, of the transformer voltage on the LV side. The validity of this assertion is readily verified from the transformer corner currents (LV side) plotted in Fig. 6, which clearly show that the LV-side switching instant currents are nearly zero till about 80% and 98% of the maximum power for $M = 2$ (or 1/2) and $M = 5$ (or 1/5), respectively, which correspond to the critical power P_{lim} for these two values.

Thus, using the aforementioned conditions, the classical constrained optimization problem of minimizing rms current at a given power can be translated into an equivalent three-loop tracking problem. The scheme, which is similar to the approach outlined in [16], is depicted in the block diagram of Fig. 7. The phase shift (D_ϕ) is varied by a fast proportional–integral (PI) controller, which ensures that the power reference P_{ref} is tracked with adequate speed. Two slower control loops drive converter operation toward the optimal point by regulating the duty ratios (D_1, D_2) so as to ensure that the transformer current at the LV-side switching instants is close to zero. In a practical circuit, i_{LVr} and i_{LVf} should have suitable nonzero values so as to ensure that the leakage inductor has adequate energy to discharge the output capacitance of the incoming device. It can be easily seen that for the top and bottom LV switches, these values should be (small) positive and (small) negative, respectively, as denoted by $+\epsilon$ and $-\epsilon$, respectively, in Fig. 7. The saturation blocks on

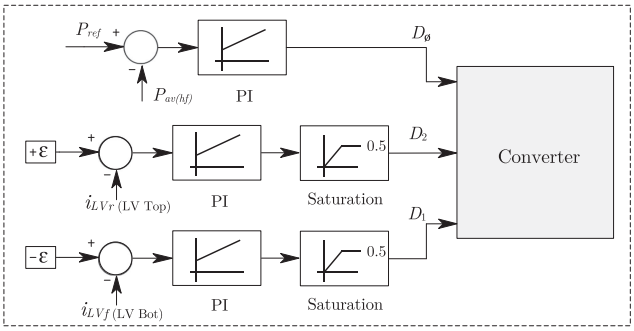


Fig. 7. Closed-loop implementation scheme of the 3-D control strategy to minimize RMS current. The power-loop (phase-shift) controller is considerably faster compared to the other two (duty-ratio) loops.

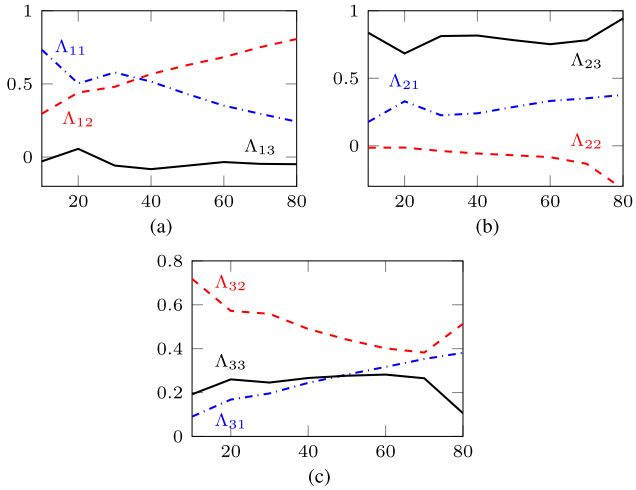


Fig. 8. Plot of elements of the RGA matrix $\mathbf{\Lambda}$ for operation around the steady-state optimum operating points. The x-axis is power in percentage of $P_{\max}$. (a) Elements of row 1 of $\mathbf{\Lambda}$ corresponding to P. (b) Row 2 (corresponding to i_{LVr}). (c) Row 3 (corresponding to i_{LVf}). $j = 1, 2, 3$ in Λ_{ij} correspond to D_ϕ, D_1, and D_2, respectively. The plots indicate that the most suitable variable pairing to limit interaction among the loops is $\{P - D_\phi, i_{\mathrm{LVr}} - D_2,$ and $i_{\mathrm{LVf}} - D_1\}$.

D_1 and D_2 clamp the duty ratios to 0.5 at higher power levels ($P > P_{\mathrm{lim}}$), when the $i_{\mathrm{LVr}} = 0$ or $i_{\mathrm{LVf}} = 0$ conditions cannot be satisfied, thereby driving the circuit to operation with SPC.

An important advantage of the proposed solution is that unlike similar real-time optimal tracking strategies for DAB converters [10]–[13], [16], the proposed scheme does not need information about the voltage conversion ratio (M) of the converter. This obviates the need for having dc voltage sensors at the two ports (when active sources are employed).

B. Choice of Variable Pair for Closed-Loop Control

The closed-loop framework described above consists of three individual control loops, which are assumed to function independently. However, since each of the controlled variables (P, i_{LVr}, and i_{LVf}) are dependent on the manipulated variables (D_ϕ, D_1, and D_2), it is evident that the three loops are coupled and the converter represents a multi-input multi-output (MIMO) system. A possible method to decouple the control loops in such cases is to use a static decoupling network [25]. But this approach has the drawback of requiring a lookup table for storing the elements of the decoupling matrix, which need to be computed offline for all possible operating points. An alternate approach to mitigate control-loop coupling in MIMO systems is to use the relative gain array (RGA) method [23], which provides a guideline for recommended pairing of the controlled and manipulated variables, so that loop interactions are minimized. The method, which uses the steady-state gain matrix ($\mathbf{G}$) of the system, is based on computation of the RGA matrix ($\mathbf{\Lambda}$), defined as [24]

$$\Lambda_{ij} = G_{ij} H_{ij} \tag{2}$$

where H_{ij} is the $\{i, j\}$th element of $\mathbf{H} = (\mathbf{G}^{-1})^T$. Once the values of Λ_{ij} are determined, the method suggests pairing the variables so that the corresponding Λ_{ij} is positive and as close to unity as possible [24]. In the present case, the small-signal control-to-output model of the converter is given by

$$\hat{\mathbf{x}} = \mathbf{G_{ss}}.\hat{\mathbf{u}} \tag{3}$$

where $\mathbf{x} = \{P, i_{\mathrm{LVr}}, i_{\mathrm{LVf}}\}^T$ and $\mathbf{u} = \{D_\phi, D_1, D_2\}^T$ are the output and input vectors, respectively, while $\mathbf{G_{ss}}$ denotes the small-signal transfer function matrix. As in [25], at low frequency, the elements of $\mathbf{G_{ss}}$ can be derived by linearizing the static control-to-output relationships (obtained from Tables III and VI) around the steady-state operating point. This yields the steady-state gain matrix $\mathbf{G}$, which is given by (4) shown at the bottom of this page, for operation in mode 2b. Based on this matrix, the elements of the corresponding RGA can be obtained using (2). These values are plotted in Fig. 8 for operation with optimal duty ratios across the power range. It is observed that Λ_{23} is very close to unity throughout, while for the third manipulated variable (i_{LVf}), the relative gain Λ_{32} has the value closest to unity. Hence, the recommended variable pairing based on the RGA method is $\{P - D_\phi, i_{\mathrm{LVr}} - D_2, i_{\mathrm{LVf}} - D_1\}$.

C. Design of the Controllers

For design of the three controllers depicted in Fig. 7, the sequential loop tuning method [24], [26] is adopted, which involves designing the controller for the fastest loop first and

$$\mathbf{G_{2b}} = \begin{bmatrix} 16P_{\max}(D_1 + D_2 - 2D_1D_2 - 2D_\phi) & 8P_{\max}(2D_\phi(1-2D_2) - (D_1 - D_2)) & 8P_{\max}(2D_\phi(1-2D_1) + (D_1 - D_2)) \\ (1/2nk).2nV_{g1}(1 - D_1) & (1/2nk).nV_{g1}(D_2 - 2D_\phi) & (1/2nk).(V_{g2}(1-2D_2) - nV_{g1}(1 - D_1)) \\ (1/2nk).(-2nV_{g1}D_1) & (1/2nk).nV_{g1}(D_2' - 2D_\phi) & (1/2nk).(-V_{g2}(1-2D_2) - nV_{g1}D_1) \end{bmatrix} \tag{4}$$

closing it. Thereafter, the controllers for the slower loops are tuned with the first loop closed.

In the present scenario, the phase shift to power or output voltage control loop evidently demands the fastest dynamic response and, hence, is designed first. Considering a passive *RC* load to be connected at port 2 (instead of V_{g2}), designated the output port, the relevant small-signal control to output transfer function is given by $\widehat{v}_0(s)/\widehat{d}_\phi(s)$, where v_0 is the output voltage. As discussed in [27] and [28], ignoring the fast dynamics of the inductor current, this transfer function has a predominantly first-order form given by

$$G_{vd_\phi}(s) = \frac{G_0}{1 + s/\omega_0} \tag{5}$$

where expressions for G_0 and ω_0 are noted in Table VII. A PI compensator is sufficient to ensure satisfactory dynamic response for such a plant [29]. For improved performance, the compensator may also contain a high-frequency pole for attenuating switching noise in the control loop [29]. Hence, the compensator transfer function is given by

$$H_v(s) = \frac{K_p + K_i/s}{1 + s/\omega_{hp}}. \tag{6}$$

Bode plots illustrating design of the phase-shift control loop for a nominal power of $0.3P_{\max}$ are shown in Fig. 9. For the chosen design values of H_v (listed in Table VIII), the crossover frequency ($f_{\rm co}$) and phase margin (Φ_m) of the compensated loop gain are 5 kHz ($f_s/10$) and 90°, respectively, indicating satisfactory and stable performance. Satisfactory performance of the control loop over a broad load range is also verified in Fig. 10, which shows worst-case values of 3 kHz and 80° for $f_{\rm co}$ and Φ_m, respectively.

Design of the $\widehat{d}_2$ to $\widehat{i}_{\rm LVr}$ and $\widehat{d}_1$ to $\widehat{i}_{\rm LVf}$ controllers is simplified by the fact that the corresponding loop crossover frequencies should be considerably lower than that of the phase-shift loop in order to mitigate loop interactions. The duty-ratio loops of [12] have a bandwidth of 1/20 of the faster loop, which translates to a value of 100–200 Hz in the present case. With such a reduced bandwidth, the plant transfer functions can be approximated by corresponding steady-state gains G_{01} (for $\widehat{i}_{\rm LVf}/\widehat{d}_1$) and G_{02} (for $\widehat{i}_{\rm LVr}/\widehat{d}_2$), which are noted in Table VII. Hence, simple integral controllers may be used to obtain the desired closed-loop bandwidth with a ϕ_m of 90°. Thus, the compensators for the duty-ratio loops are given by

$$H_{d1(s)} = K_{id1}/s, \qquad H_{d2(s)} = K_{id2}/s. \tag{7}$$

It may be noted that since the value of G_{02} is negative, finally, a negative value of K_{id_2} should be used, or the polarity of reference and feedback signals for the $i_{\rm LVr}$ loop, shown in Fig. 7, should be reversed. For the chosen values of K_{id1} and K_{id2} (listed in Table VIII), a closed-loop bandwidth of around 150 Hz is achieved, as Fig. 11 illustrates.

TABLE VII
EXPRESSIONS OF THE TRANSFER FUNCTION PARAMETERS, $k = L_{lk} f_s$

Term	Expression	Value at $0.3P_{\max}$
G_0	$1/(2nk).V_{g1}R(D_1 + D_2 - 2D_1D_2 - 2D_\phi)$	494
ω_0	$1/(RC)$	7.5 krad/s
G_{01}	$(1/2k).V_{g1}(1 - D_2 - 2D_\phi)$	54
G_{02}	$(1/2nk).(V_{g2}(1 - 2D_2) - nV_{g1}(1 - D_1))$	− 79

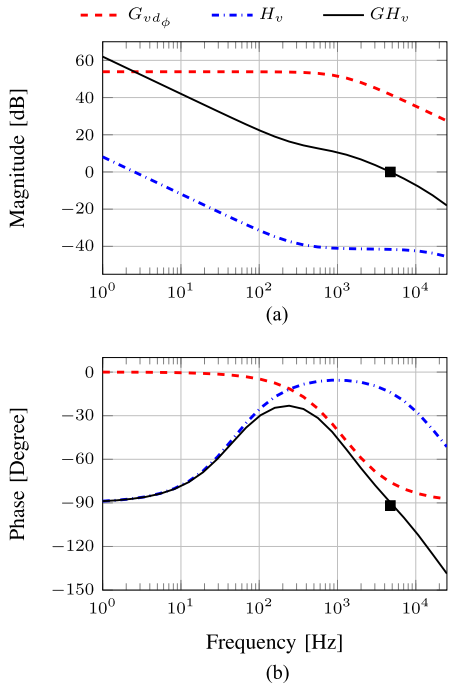


Fig. 9. Bode plots of the uncompensated loop gain (G_{vd_ϕ}) (computed at $0.3P_{\max}$), the compensator (H_v) (PI with a high-frequency pole) and the compensated loop gain (GH_v) for the phase shift ($\widehat{d}_\phi$) to output voltage ($\widehat{v}_0$) transfer function. (a) Magnitude plot. (b) Phase plot. The gain crossover frequency is around 5 kHz and the phase margin is close to 90°.

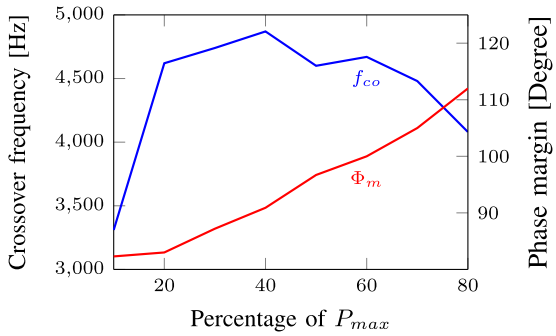


Fig. 10. Plot illustrating satisfactory phase margin (Φ_m) and gain crossover frequency ($f_{\rm co}$) characteristics of the phase shift to output voltage control loop with the designed compensator over a broad load range of the converter.

V. RESULTS

A. Simulation Results

In order to highlight the advantages of the 3-D optimal control scheme, circuit simulation of the DAHB converter, with specifications listed in Table IV (for $M = 1/2$), was carried out in

TABLE VIII
PARAMETER VALUES OF THE CONTROLLERS OF (6) AND (7)

K_p	Ki	ω_{hp}	K_{id_1}	K_{id_2}
0.00835	16	$(2\pi.20)$ kHz	18	10

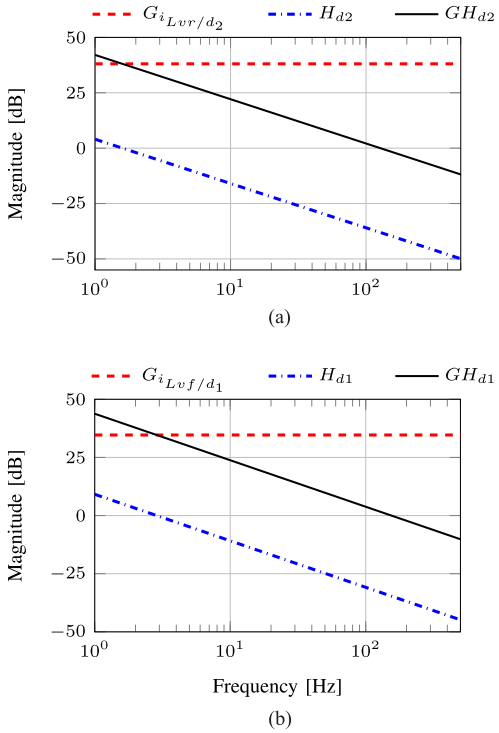


Fig. 11. Bode magnitude plots relevant to the design of the duty-ratio control loops. (a) Plots for $\widehat{d}_2$ to $\widehat{i}_{\mathrm{LVr}}$. (b) Plots for $\widehat{d}_1$ to $\widehat{i}_{\mathrm{LVf}}$. The plant, compensator, and compensated loop gains are denoted by G, H, and GH, respectively. The design bandwidths of the duty-ratio loops are much smaller ($<1/20$) than the phase-shift loop. This allows the plant transfer functions to be approximated by their steady-state gains.

PLECS. A resistive load was used on the LV side and the circuit was operated with output (LV side) voltage control (controlled by varying D_ϕ).

Steady-state simulation results at a power of 187.5 W (which corresponds to 30% of the maximum power) are presented in Figs. 12 and 13, which compare optimal 3-D operation with square wave control (SPC) and the 2-D optimal strategy discussed in [9]. It is observed from Fig. 12 that with 3-D optimal control, the LV-side transformer rms current is 9.2 A, which is significantly lower than the value of 14.5 A obtained with SPC. Furthermore, Fig. 13 shows that, as predicted by analysis, 3-D optimal control results in ZVS turn-ON of all devices, which follows from the observation that current through each switch is in the negative direction (source to drain) at its turn-ON instant. In contrast, one of the LV-side switches for 2-D optimal control and both LV-side switches for SPC are hard-switched.

Closed-loop dynamic simulation results of the converter for a step increase (from 30% to 40%) in load and back are depicted in Fig. 14. It is observed that the overall response is stable and the settling time of the output voltage tracking loop is around

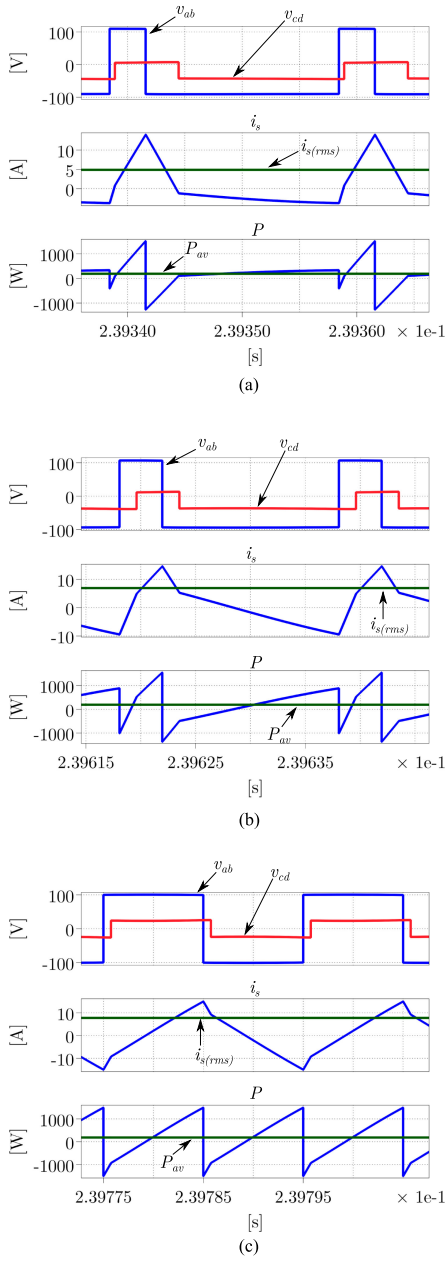


Fig. 12. Steady-state simulation results comparing rms currents of the three strategies at $P = 187.5$ W (30% of $P_{\max}$) for the specifications of Table IV. (a) Optimal 3-D control: $D_1 = 0.1575$, $D_2 = 0.2904$, $D_\phi = 0.0855$; $i_{s\,(\mathrm{rms})} = 9.2$ A. (b) Optimal 2-D control [9]: $D_1 = D_2 = 0.1952$, $D_\phi = 0.0801$; $i_{s\,(\mathrm{rms})} = 10.9$ A. (c) 1-D control (SPC): $D_1 = D_2 = 0.5$, $D_\phi = 0.04$; $i_{s\,(\mathrm{rms})} = 14.5$ A.

1 ms with a maximum undershoot/overshoot of around 5%, which indicates satisfactory dynamic performance. Also, the duty ratios are automatically adjusted to track the optimal values in less than 10 ms, following the step changes.

B. Experimental Results

Effectiveness of the 3-D optimal scheme has been validated by performing closed-loop tests on a 625-W laboratory prototype (see Fig. 15) having the same nominal specifications, as listed in Table IV, i.e., 200 V – 50 V with a switching frequency of 50 kHz. Details of the components used in the prototype are

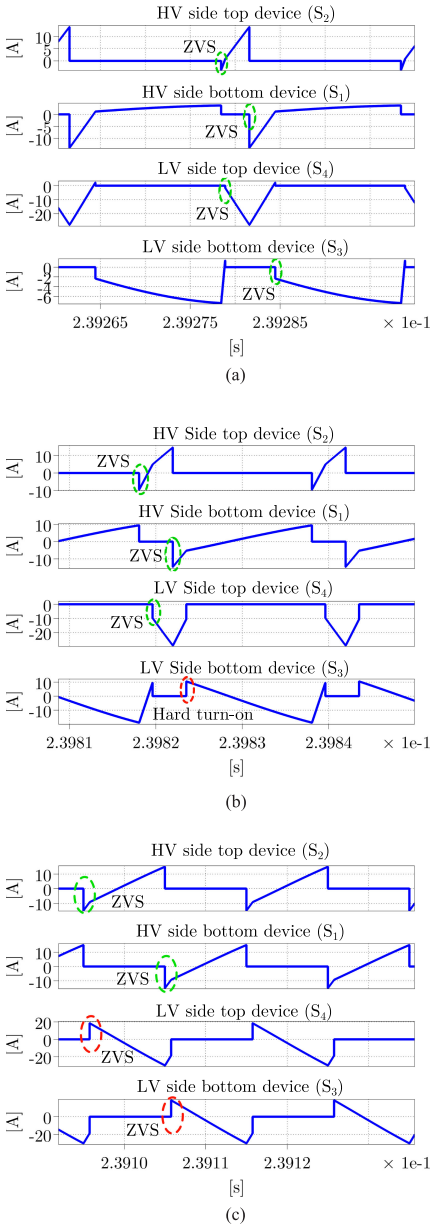


Fig. 13. Steady-state simulation results comparing ZVS performance of the three strategies at $P = 187.5$ W for the specifications of Table IV. (a) Optimal 3-D control: ZVS of all devices. (b) 2-D control in [9]: Hard turn-ON of bottom device on LV side. (c) 1-D control (SPC): Hard turn-ON of LV-side devices.

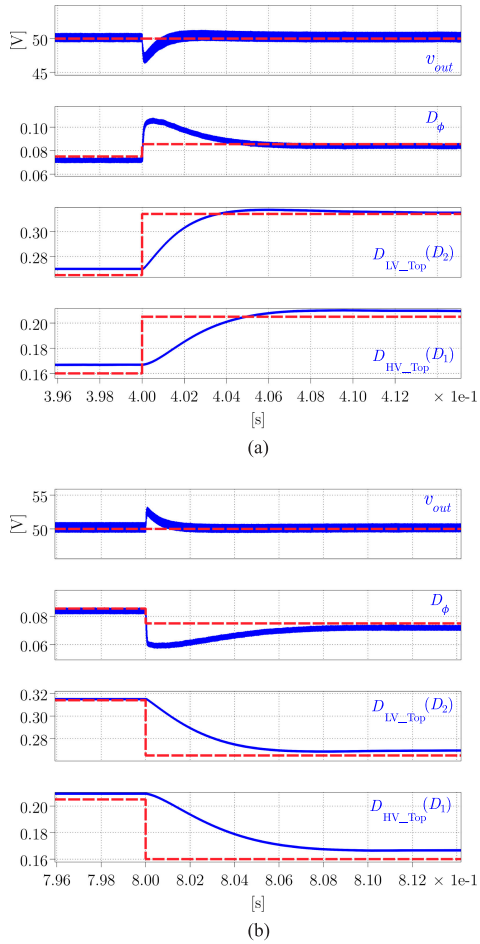


Fig. 14. Simulation result demonstrating satisfactory dynamic performance of the phase-shift-controlled (D_ϕ) output voltage regulation loop ($t_{\rm sett} \approx 1$ ms) and online tracking of the optimal operating point for (a) a step increase (from 30% to 40%) and (b) a step decrease (from 40% to 30%) in load. The reference voltage and optimal duty ratios are shown by dotted lines.

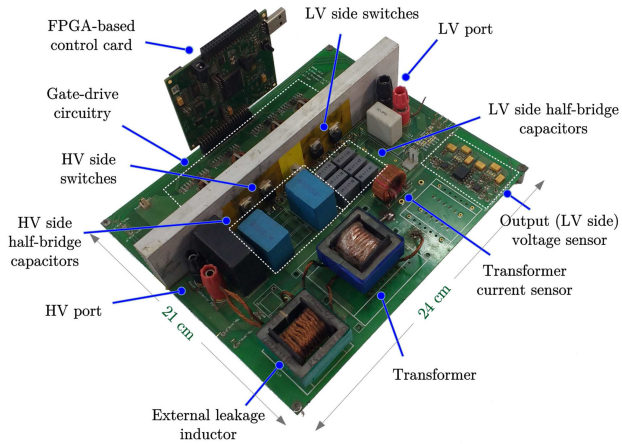


Fig. 15. Photograph of the 200 V–50 V, 625 W (max) hardware prototype.

provided in Table IX. The control algorithm is implemented using a Xilinx Spartan 3 (XC3S400) field-programmable gate array (FPGA)-based control card. A toroidal current transformer (CT) with a turn ratio of 1:100 is employed for sensing the transformer current because of the inherent high bandwidth of CT-based solutions [30].

A critical consideration related to hardware implementation of the proposed control method is the correctness of sensing the high-frequency transformer current at the turn-OFF instants of the LV-side switches. Error in this process can lead to deviation from the optimal operating condition and more importantly loss of ZVS operation of the LV switches. As illustrated in Fig. 16, in a practical circuit, due to the gate-drive turn-OFF delay of the outgoing switch, the real instant (t_1) at which the switch begins to turn OFF is delayed by a duration $T_{\rm doff}$. A further delay arises from the fact that the pipeline analog-to-digital converter (ADC) used in the control board for digital conversion of the sensed analog current has a conversion latency $T_{\rm dADC}$.

TABLE IX
DETAILS OF COMPONENTS USED IN THE HARDWARE PROTOTYPE

Component	Description
HV-side switches	IPA60R125C6 (600 V, 125 mΩ)
LV-side switches	FDP075N15A (150 V, 7.5 mΩ)
HV-side half-bridge capacitors	10 μF, 300 V dc, film
LV-side half-bridge capacitors	14.1 μF, 63 V dc, film
Leakage inductor (L_{1k})	20 μH placed on HV side, 10 T/ 30 strands of 32 wire gauge on EE 42/15, $R_{ac} = 27$ mΩ at 50 kHz
Transformer	Primary: 20 T/ 28 strands of 32 wire gauge, Secondary: 10 T/ 66 strands of 32 wire gauge on EE 42/15, $R_{ac(HV)} = 112$ mΩ at 50 kHz, $L_{1k(HV)} = 2$ μH, $L_{m(HV)} = 275$ μH
HV-side filter capacitor	20 μF, 500 V dc, film
LV-side filter capacitor	10 μF, 100 V dc, film

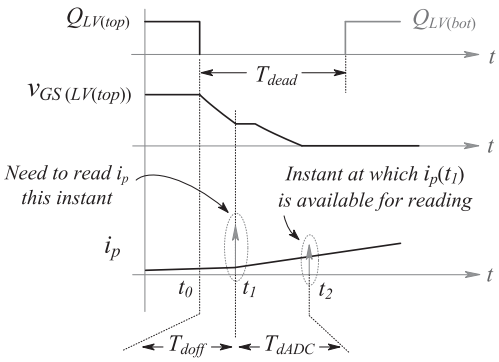


Fig. 16. Explaining the delay necessary for correctly reading the transformer current at the turn-OFF of one of the LV-side switches, owing to the gate-drive turn-OFF delay (T_{doff}) and the conversion latency (T_{dADC}) of the ADC.

Hence, as Fig. 16 shows, the ADC output should be read in the FPGA at the instant t_2, which corresponds to a total delay of ($T_{\mathrm{doff}} + T_{\mathrm{dADC}}$) after the pulse-width modulation signal of the outgoing switch goes low, ensuring that the sensed transformer current at the proper turn-OFF instant (t_1) is ultimately used in the FPGA. The values of T_{doff} for the two LV switches can be ascertained from device datasheet and experimental gate–source waveforms, while the employed ADC chip (ADC12010) has a fixed latency of six ADC clock cycles [31].

Steady-state experimental waveforms for the 3-D scheme and SPC at 187.5 W are shown in Figs. 17 and 18, respectively. It is seen that the transformer rms currents closely match the values obtained from simulation. Also, the switching waveforms illustrate ZVS occurrence of all devices for 3-D optimal control and hard switching of the LV-side devices for the SPC scheme.

Performance of the converter following a step increase in load (from 30% to 40% of P_{max}) is illustrated in Fig. 19, which shows stable response with an undershoot of less than 5% and an output voltage regulation time of around 1 ms. Fig. 19(a) and (b) shows the zoomed view of the relevant high-frequency waveforms before and after the load change was applied. It is observed that the circuit transitions from one optimum steady-state operating point to another, as can be inferred from the shape of the transformer current.

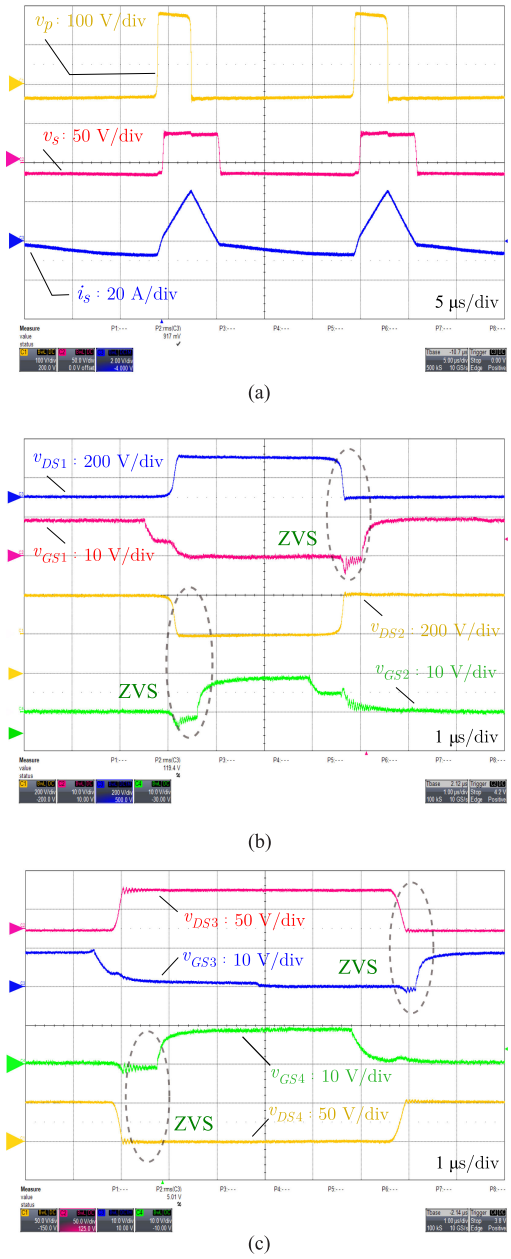
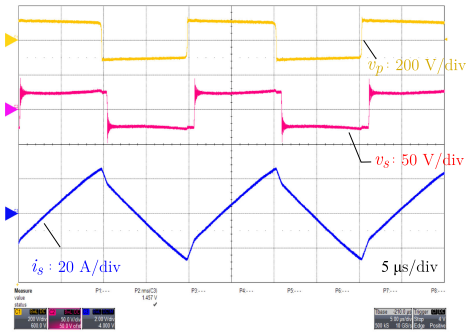
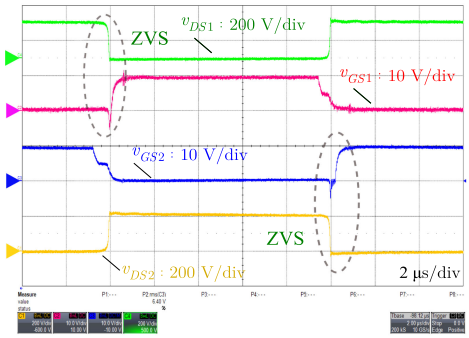


Fig. 17. Steady-state experimental results for 3-D control: $D_1 = 0.1575$, $D_2 = 0.2904$, $D_\phi = 0.0855$; $i_{s\,(\mathrm{rms})} = 9.2$ A, and $P = 187.5$ W. (a) Transformer primary and secondary voltages and LV-side current. (b) ZVS turn-ON of the HV-side devices. (c) ZVS turn-ON of the LV-side devices.

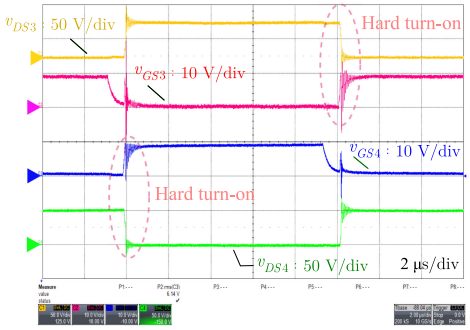
Experimentally measured efficiency figures and the rms values of the LV-side transformer current for the SPC, 2-D optimal phase-shift control (OPC) [9], and 3-D optimal schemes are compared in Fig. 20. Since for the parameter values of Table IV, SPC is optimal above the critical power limit of 80%, results under light-load conditions (up to 40%) are presented in order to highlight the advantages of 3-D control. It is observed that 3-D control leads to remarkable reduction in rms current and improvement in efficiency compared to the other strategies.



(a)



(b)

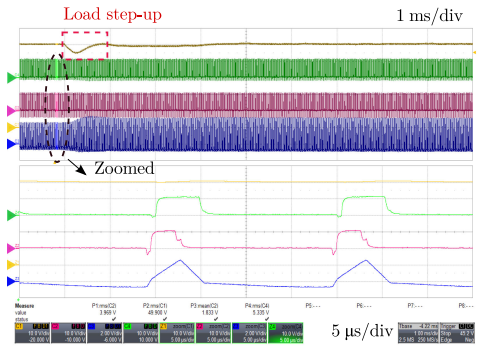


(c)

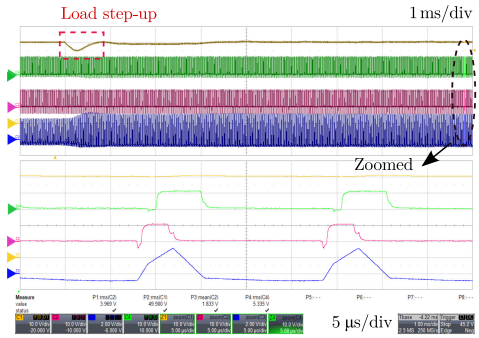
Fig. 18. Steady-state experimental results for SPC: $D_1 = D_2 = 0.5$, $D_\phi = 0.04$; $i_{s(\mathrm{rms})} = 14.5$ A, and $P_{\mathrm{av}} = 187.5$ W. (a) Transformer primary and secondary voltages and LV-side current. (b) ZVS turn-ON of the HV-side devices. (c) Hard turn-ON of the LV-side devices.

VI. Conclusion

This paper has presented extensive steady-state analysis of the operation of a DAHB converter controlled utilizing all three available degrees of freedom, viz., duty ratios of the two half-bridges and phase shift between them. Active power output and rms current expressions in each mode are derived, which are used by MATLAB's "fmincon" function to numerically calculate the minimum rms current solution at a given power. From scrupulous observations of circuit waveforms under optimal conditions, a lookup-table-less, closed-loop-control-based, real-time rms current minimization strategy is proposed. Unlike other online optimal tracking strategies for the DAB converter, the proposed method does not require knowledge of the converter's voltage gain, and thus, dc voltage sensors are obviated (when active sources are employed). Remarkably, operation at

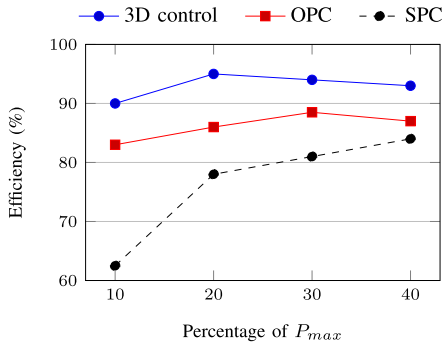


(a)

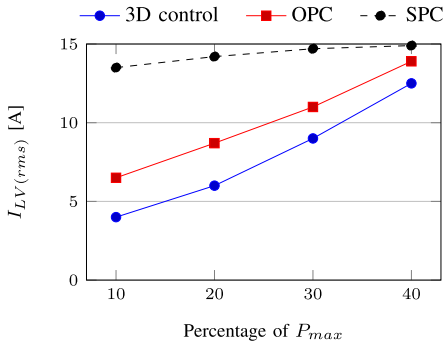


(b)

Fig. 19. Illustrating the excellent dynamic response of the converter for a step change in load from 30% to 40% of the maximum power. Traces from top to bottom are output (LV side) voltage: 10 V/div, v_{GS} of the HV-side top switch: 10 V/div, v_{GS} of the LV-side top switch: 10 V/div, and transformer current: 20 A/div. (a) Zoomed view in the steady state before load change. (b) Zoomed view in the steady state after load change.



(a)



(b)

Fig. 20. Experimentally measured efficiency and rms currents for the SPC, 2-D OPC [9], and 3-D control schemes. (a) Efficiency. (b) Transformer LV-side current rms value.

the optimal point is also found to satisfy the necessary conditions for ZVS turn-ON of all devices across the power range of the converter. Stable and satisfactory dynamic response of the converter has been experimentally verified, and the proposed method is found to offer significant efficiency advantages over conventional square-wave control or 2-D optimization strategy, particularly at light loads.

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Shiladri Chakraborty (S'14) received the B.E. degree in electrical engineering from Jadavpur University, Kolkata, India, in 2008, and the M.Tech. degree from the Indian Institute of Technology (IIT) Kanpur, Kanpur, India, in 2012, both in electrical engineering. He is currently working toward the Ph.D. degree with the Department of Electrical Engineering, IIT Kharagpur, Kharagpur, India.

From 2008 to 2010, he was with Tata Motors Limited, Mumbai, India. His research interests include dual-active-bridge converters, resonant converters, gate-drive techniques, and high-frequency magnetics.

Souvik Chattopadhyay (M'04) received the B.E. degree from the Bengal Engineering College, Howrah, India, in 1988, and the M.Sc. and Ph.D. degrees in electrical engineering from the Indian Institute of Science, Bangalore, India, in 1990 and 2002, respectively.

He is currently an Assistant Professor with the Department of Electrical Engineering, Indian Institute of Technology Kharagpur, Kharagpur, India. From 1991 to 1995, he was with the M/s Crompton Greaves, Ltd., Mumbai, India, and from 1996 to 1998, with M/s Cegelec India, Ltd., New Delhi, India. From 2002 to 2003, he was an Assistant Professor with the Department of Electronics Engineering, Jalpaiguri Government Engineering College, Jalpaiguri, India. From 2003 to 2004, he was an Assistant Professor with the Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai. His research interests include design, analysis, control, and modeling of power converters.