Effect of Gate-Oxide Degradation on Electrical Parameters of Power MOSFETs

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***Abstract*—Gate oxide in power metal–oxide–semiconductor field effect transistors (MOSFETs) degrades over time. The degradation leads to an accumulation of oxide-trapped charges within the gate oxide and an accumulation of interface-trapped charges at the oxide–semiconductor surface of power MOSFETs. Overtime, such charges significantly alter the electrical parameters of power MOSFETs; to observe this, the electrical parameters are utilized as precursors of gate-oxide degradation. The purpose of this paper is threefold: 1) to propose a new online precursor of gate-oxide degradation—the gate plateau time; 2) to demonstrate a simultaneous dip-and-rebound variation pattern of four precursors of gate-oxide degradation: threshold voltage, gate plateau voltage, gate plateau time, and on-resistance; and 3) to compare the shift tendencies of each precursor over the course of gate-oxide degradation. The existing studies of gate-oxide degradation mechanisms and their effects on threshold voltage and mobility reduction were extended to correlate a variation of all four precursors using analytical expressions. The variation patterns were experimentally verified using high-electric field stressing in two different commercial power MOSFETs. The new precursor, the gate plateau time, was found to be a competitive gate-oxide degradation precursor, as it had a higher positive shift than threshold voltage and gate plateau voltage. In addition, the threshold voltage was found to be the most sensitive indicator of the negative shift (dip), while the on-resistance and gate plateau time were found to be the most sensitive indicators of the positive shift (rebound).**

***Index Terms*—Gate oxide, metal–oxide–semiconductor field effect transistor (MOSFET), oxide degradation, precursor, turn around.**

I. Introduction

THE power metal–oxide–semiconductor field effect transistor (MOSFET) is recognized as a crucial component of power electronic systems. It has a relatively thick gate oxide layer as a dielectric material between its gate terminal and semiconductor surface. The gate oxide material, which is predominantly silicon dioxide (SiO_2), slowly degrades over time. The degradation of gate oxide under an electric field has been a subject of extensive investigation for nearly two decades [1]–[7]. These studies have established that the degradation of SiO_2 introduces two primary charges that significantly alter the electrical parameters of a power MOSFET: 1) oxide-trapped charge (Q_{ot}) within gate oxide, and 2) interface-trapped charge (Q_{it}) at the oxide–silicon interface.

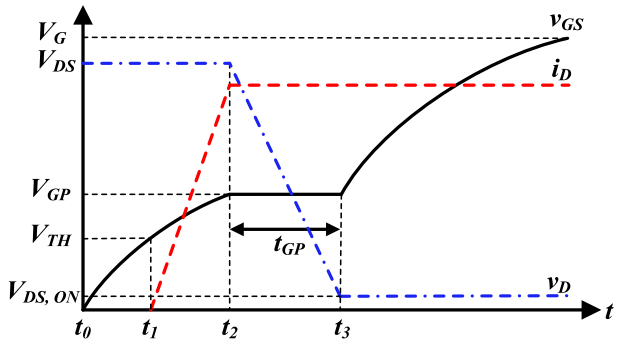

Fig. 1. Typical turn-on waveform of power MOSFETs.

The electrical parameters serve as precursors (or indicators) of gate-oxide degradation in power MOSFETs. However, in terms of observing the effects of gate-oxide degradation, very few precursors have been identified. The threshold voltage (V_{TH}) is the most commonly studied precursor of gate-oxide degradation in power MOSFETs [2], [4]–[10]. The on-resistance (R_{ON}), though a well-known precursor, has mostly been studied for assessing package-related failures during thermal or power cycling of power MOSFETs [11]–[14], and thus, very few studies have assessed its role as a precursor of gate-oxide degradation [15], [16]. However, it is shown later that R_{ON} varies significantly over the stress period, and should therefore be considered an important precursor of gate-oxide degradation. Recently, the gate plateau (or miller) voltage (V_{GP}) was proposed as an online precursor of gate-oxide degradation for power MOSFETs [17]. In this paper, the gate plateau time (t_{GP}) is proposed as a new online precursor of gate-oxide degradation. In comparison to V_{GP}, this new precursor is shown to be a more sensitive indicator of Q_{it}. It is interesting to note that online precursors, unlike off-line precursors, can be extracted without affecting system operation. The extraction of online precursors V_{TH}, V_{GP}, and t_{GP} can all be done from the same turn-on waveform of a power MOSFET shown in Fig. 1.

The precursors exhibit a distinct variation pattern due to accumulation of Q_{ot} and Q_{it} over the course of gate-oxide degradation. In [2] and [4]–[6], it is reported that the threshold voltage initially decreases (i.e., dips) due to a buildup of positive Q_{ot}, but it rises back to its initial value and beyond (i.e., rebounds) due to an accumulation of negatively charged Q_{it}. This dip-and-

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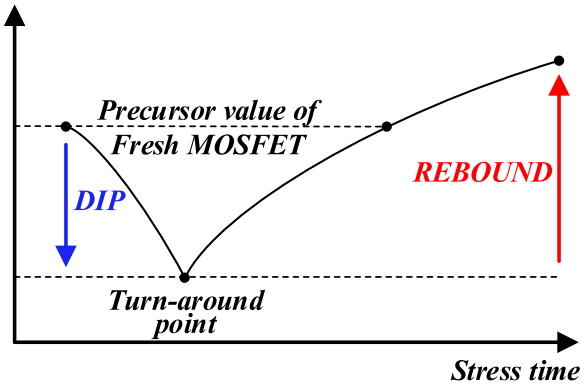

Fig. 2. Expected variation of precursors over time.

rebound variation is also known as the turnaround effect [2], [8], [18], [19]. Recently, a similar dip-and-rebound variation pattern was also observed in gate plateau (or miller) voltage [17]. On the other hand, some literatures have reported that precursors only increase (or rebound) over time. For instance, the threshold voltage and the on-resistance have been reported to only increase due to gate-oxide degradation [9], [10], [16], [20]. While confirming the dip-and-rebound variation pattern of precursors, we observed that, if measurements were not taken at brief intervals especially during initial stages of degradation, the initial dip might not be observed at all. This is because the effect of $Q_{\rm ot}$ is dominant during initial stages of degradation [1], [8], [17], [21], and depending upon the electrical stress, its effect may be observable for a relatively short time. It is important to note that all electrical parameters mentioned earlier, i.e., $V_{\rm TH}$, $R_{\rm ON}$, $V_{\rm GP}$, and $t_{\rm GP}$, bear a strong analytical relationship with $Q_{\rm ot}$ and $Q_{\rm it}$ through the threshold voltage (to be discussed later). Therefore, we can expect the variation of other precursors to replicate the dip-and-rebound variation pattern of $V_{\rm TH}$ over the course of gate-oxide degradation, as shown in Fig. 2. The precursors initially dip, reach their minimum values at turnaround point, and then rebound to their initial values and beyond.

The dip-and-rebound variation of electrical parameters due to gate-oxide degradation can be detrimental to device performance, reliability, and efficiency. The dip may cause the threshold voltage to shift to negative values (as shown in the experimental results later), which may cause a "normally OFF" (or enhancement type) MOSFET to become a "normally ON" (or depletion type) MOSFET, or may result in a MOSFET with high OFF-state leakage current [6], [22]. This is a very serious problem as it can lead to unintended operation of power electronic devices. In a similar manner, the rebound causes simultaneous increase of $R_{\rm ON}$, $V_{\rm GP}$, and $t_{\rm GP}$, which correspond to an increase in on-state loss, switching loss, and switching time of the MOSFET, respectively. A holistic approach that predicts the dip-and-rebound variation of all four precursors is therefore necessary to understand the effect of gate-oxide degradation on power MOSFETs.

The purpose of this paper is threefold: 1) to propose a new online precursor of gate-oxide degradation—the gate plateau time; 2) to demonstrate a simultaneous dip-and-rebound variation pattern of all four precursors of gate-oxide degradation ($V_{\rm TH}$, $R_{\rm ON}$, $V_{\rm GP}$, and $t_{\rm GP}$); and 3) to compare the shift tendencies of each precursor over the course of gate-oxide degradation. It is shown that all four precursors reflect the gate-oxide degradation status with a simultaneous negative and positive shift from their initial values. The threshold voltage was found to be the most suitable precursor for observing the negative shift (dip), while $R_{\rm on}$ and $t_{\rm GP}$ were found to be the most suitable precursors for observing the positive shift (rebound). Such an understanding of the nature of variation of these precursors will enable an effective and redundant monitoring of gate-oxide degradation process in power MOSFETs while being used in real power-electronic systems.

The organization of the paper is as follows. Section II provides background information about the effect of gate-oxide degradation in power MOSFETs. Section III investigates the variation of all four precursors with respect to the type of trapped charges. Section IV explains the experimental setup and precursors' measurement methods in detail. The subsequent sections provide experimental verification of variation patterns in two commercially available power MOSFETs (IRF510 and IRF520).

II. Effects of Gate-Oxide Degradation

The two well-known vertical structures of power MOSFETs, vertical-diffused (VD) structure and trench-gate (or U-MOSFET) structure, are shown in Fig. 3. These MOSFETs have a relatively thick gate oxide layer as a dielectric material between the gate terminal and semiconductor surface. The metal–oxide–semiconductor (MOS) sandwich thus formed is shown within dotted rectangles in Fig. 3.

The degradation of gate oxide under electric field has been a subject of extensive investigation for nearly two decades. Several researches have been devoted to the theoretical and analytical study of the effects of trapped charges on threshold voltage and mobility [1], [2], [4]–[7]. Based on these studies, the gate-oxide degradation generates two primary types of charges: 1) oxide-trapped charge ($Q_{\rm ot}$) within gate oxide, and 2) interface-trapped charge ($Q_{\rm it}$) at the oxide–silicon interface. The present understanding of the effect of trapped charges on threshold voltage can be summarized into three stages, as shown in Fig. 4.

Stage I: This represents the MOS structure before the initiation of gate-oxide degradation. It is assumed that there are no $Q_{\rm ot}$ or $Q_{\rm it}$ within gate oxide prior to degradation.

Stage II: During the initial phase of degradation, $Q_{\rm ot}$ begins to build up within gate oxide. These oxide-trapped charges exhibit donor like behavior and are positively charged. The presence of positive $Q_{\rm ot}$ increases effective electric field across gate oxide and contributes to the inversion of the channel. This leads to a decrease of threshold voltage in power MOSFETs. The threshold voltage may even decrease (dip) to a negative value causing a "normally OFF" (or enhancement type) MOSFET to become a "normally ON" (or depletion type) MOSFET.

Stage III: After a buildup of a certain threshold of $Q_{\rm ot}$, interface traps begin to form at oxide–silicon interface. Since there is a time delay between the creation of $Q_{\rm ot}$ and the creation of interface traps, the effects of $Q_{\rm ot}$ is observable at early stages of degradation. However, after a certain time, the increase of

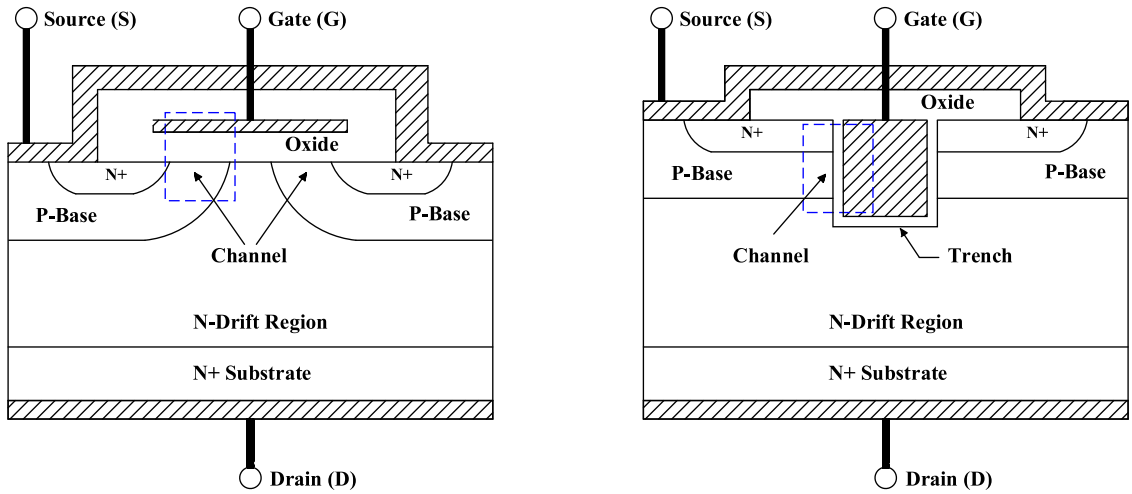

Fig. 3. Elementary cell cross section of (a) VD-MOSFET structure and (b) U-MOSFET structure.

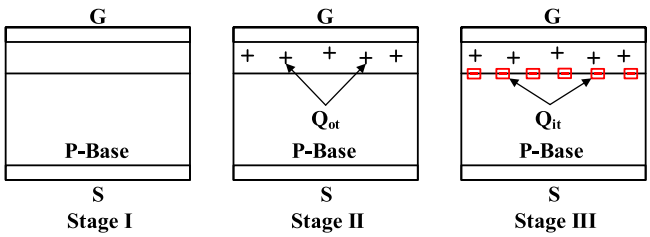

Fig. 4. Stages of gate-oxide degradation.

interface traps become very dominant. Since the interface traps can interact electrically with the charge carriers, they begin to capture electrons and in the process, become negatively charged in an n-channel MOSFET. Additionally, the build-up of negatively charged $Q_{\rm it}$ compensates the effect of oxide field. Thus, a higher electric field is required across the oxide for channel inversion. This leads to an increase (rebound) of threshold voltage in power MOSFETs. Upon prolonged stress, the threshold voltage rises to back its initial value and beyond, allowing the power MOSFET to regain its "normally OFF" state.

Based on above discussion, the threshold voltage shift can be represented as a sum of the shifts due to positive oxide-trapped charges (during stage II) and negative interface-trapped charges (during stage III). The positive oxide-trapped charges have an effect of reducing the threshold voltage while the negative interface-trapped charges have an effect of increasing the threshold voltage. It is also important to mention that accumulation of both $Q_{\rm ot}$ and $Q_{\rm it}$ reduce channel carrier mobility. But the mobility reduction is primarily due to scattering from charges in interface traps [22]–[24]. The empirical expression modeling the effect of gate-oxide degradation mechanism on threshold-voltage shift and channel carrier mobility reduction is given by [5], [6]

$$V_{\rm TH} = V_{\rm TH0} - \frac{qN_{\rm ot}}{C_{\rm ox}} + \frac{qN_{\rm it}}{C_{\rm ox}} \tag{1}$$

and

$$\mu = \frac{\mu_o}{1 + \alpha_{\rm ot} N_{\rm ot} + \alpha_{\rm it} N_{\rm it}} \tag{2}$$

where $V_{\rm TH0}$ and μ_o are the initial values of threshold voltage and mobility, respectively; $N_{\rm ot}$ and $N_{\rm it}$ are the stress-induced changes in densities of $Q_{\rm ot}$ and $Q_{\rm it}$, respectively; and $\alpha_{\rm ot}$ and $\alpha_{\rm it}$ are the coefficients describing the effects of $Q_{\rm ot}$ and $Q_{\rm it}$, respectively.

III. Investigation of Variation of Precursors

The other electrical parameters, i.e., $V_{\rm GP}$, $t_{\rm GP}$, and $R_{\rm ON}$, bear a strong analytical relationship with threshold voltage. Therefore, we can expect these precursors to replicate the dip-and-rebound variation pattern of $V_{\rm TH}$ over the course of gate-oxide degradation. In this section, the analytical expressions of four precursors are analyzed to show their respective dip-and-rebound variations.

A. Variation of Threshold Voltage

The partial derivative of $V_{\rm TH}$ in (1) with respect to (w.r.t.) $N_{\rm it}$ and $N_{\rm it}$ results in

$$\frac{\partial V_{\rm TH}}{\partial N_{\rm ot}} = -\frac{q}{C_{\rm ox}} < 0 \tag{3}$$

and

$$\frac{\partial V_{\rm TH}}{\partial N_{\rm it}} = \frac{q}{C_{\rm ox}} \quad > 0. \tag{4}$$

The partial derivative of $V_{\rm TH}$ w.r.t. $N_{\rm ot}$ in (3) is negative. Similarly, the partial derivative of $V_{\rm TH}$ w.r.t. $N_{\rm it}$ is positive. This follows our previous discussion that $V_{\rm TH}$ decreases with increase of $N_{\rm ot}$ and increases with increase of $N_{\rm it}$, indicating a dip-and-rebound variation pattern.

B. Variation of Gate Plateau Voltage

Recently, $V_{\rm GP}$ was proposed as a precursor of gate-oxide degradation and its analytical relationship with respect to trapped charges was derived for power MOSFETs in [17]. The gate plateau voltage of a power MOSFET is given by [25]

$$V_{\rm GP} = V_{\rm TH} + \sqrt{\frac{I_D L_{\rm CH}}{\mu C_{\rm ox} Z}} \tag{5}$$

where I_D is the drain current, $L_{\rm CH}$ is the channel length, Z is the channel width, and $C_{\rm ox}$ is the specific gate oxide capacitance.

The partial derivative of $V_{\rm GP}$ w.r.t. $N_{\rm ot}$ and $N_{\rm it}$ results in

$$\frac{\partial V_{\rm GP}}{\partial N_{\rm ot}} = \frac{\partial V_{\rm TH}}{\partial N_{\rm ot}} - \frac{1}{2{\mu_o}^{3/2}} \sqrt{\frac{I_D L_{\rm CH}}{C_{\rm ox} Z}} \frac{\partial \mu}{\partial N_{\rm ot}} \tag{6}$$

and

$$\frac{\partial V_{\rm GP}}{\partial N_{\rm it}} = \frac{\partial V_{\rm TH}}{\partial N_{\rm it}} - \frac{1}{2{\mu_o}^{3/2}} \sqrt{\frac{I_D L_{\rm CH}}{C_{\rm ox} Z}} \frac{\partial \mu}{\partial N_{\rm it}}. \tag{7}$$

Since the manufacturing parameters of commercial power MOSFETs are not always provided in the datasheet, an appreciable effort was made to determine the sign of (6) in [17]. As mentioned before, the presence of both $Q_{\rm ot}$ and $Q_{\rm it}$ reduce the channel carrier mobility. Because the mobility reduction is primarily due to interface trapped charges [22]–[24], we can assume that the decrease of mobility due to $N_{\rm ot}$ in (6) is negligible. This assumption simplifies the analytical expressions of (6) and (7) to

$$\frac{\partial V_{\rm GP}}{\partial N_{\rm ot}} \simeq \frac{\partial V_{\rm TH}}{\partial N_{\rm ot}} \quad < 0 \tag{8}$$

and

$$\frac{\partial V_{\rm GP}}{\partial N_{\rm it}} = \frac{\partial V_{\rm TH}}{\partial N_{\rm it}} - \frac{1}{2{\mu_o}^{3/2}} \sqrt{\frac{I_D L_{\rm CH}}{C_{\rm ox} Z}} \frac{\partial \mu}{\partial N_{\rm it}} \quad > 0. \tag{9}$$

The partial derivative of $V_{\rm GP}$ w.r.t. $N_{\rm ot}$ in (8) is negative. Also, since $V_{\rm TH}$ increases w.r.t. $N_{\rm it}$ and μ decreases w.r.t. $N_{\rm it}$, the partial derivative of $V_{\rm GP}$ w.r.t. $N_{\rm it}$ in (9) is positive. This means that $V_{\rm GP}$ initially decreases due to accumulation of $N_{\rm ot}$. As the formation of $N_{\rm it}$ begins to compensate the effect of $N_{\rm ot}$, $V_{\rm GP}$ rebounds to its initial value and beyond. The shift tendency of $V_{\rm GP}$ due to trapped charges is illustrated in Fig. 5, where $V_{\rm GP2} > V_{\rm GP0}$ (Fresh MOSFET) $> V_{\rm GP1}$. This indicates that $V_{\rm GP}$ dips initially, and then rebounds like $V_{\rm TH}$.

C. Variation of the Gate Plateau Time

In this paper, the gate plateau time ($t_{\rm GP}$) is proposed as a new online precursor of gate-oxide degradation. This is the time span where the gate voltage remains constant and equal to $V_{\rm GP}$. During this time span (time span (t_3–t_2) in Fig. 1), the drain voltage (v_D) gradually decreases at a rate given by [25]

$$\frac{dv_D}{dt} = -\frac{V_G - V_{\rm GP}}{R_G C_{\rm GD,av}} \tag{10}$$

where R_G is the gate resistance, V_G is the gate voltage, and $C_{\rm GD,av}$ is an assumed average value of gate-drain capacitance during the transient.

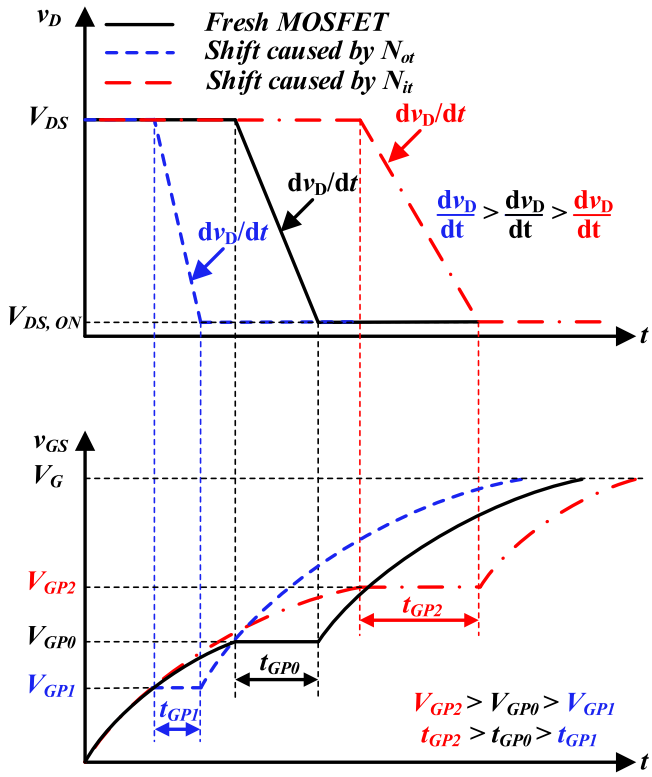

Fig. 5. Shift tendencies of $V_{\rm GP}$ and $t_{\rm GP}$.

As seen from expression (10), the rate of change of v_D depends on the magnitude of R_G and $V_{\rm GP}$. For a given R_G, a smaller $V_{\rm GP}$ results in a larger dv_D/dt and vice versa. Furthermore, a larger dv_D/dt corresponds to a smaller $t_{\rm GP}$ and vice versa. The presence of $Q_{\rm ot}$ leads to a smaller $V_{\rm GP}$, and thus, a smaller $t_{\rm GP}$, while the presence of $Q_{\rm it}$ leads to a larger $V_{\rm GP}$, and thus, a larger $t_{\rm GP}$. This is illustrated in Fig. 5 where $t_{\rm GP2} > t_{\rm GP0}$ (Fresh MOSFET) $> t_{\rm GP1}$. This indicates that $t_{\rm GP}$ dips and rebounds like $V_{\rm TH}$ and $V_{\rm GP}$.

The variation of $t_{\rm GP}$ can also be explained using quantitative method. The time interval (t_3–t_2) of a power MOSFET is given by [25]

$$t_{\rm GP} = t_3 - t_2 = \frac{R_G C_{\rm GD,av}}{V_G - V_{\rm GP}} \left[V_{\rm DS} - v_{D(t3)} \right]. \tag{11}$$

As shown in the turn-on waveform in Fig. 1, at the end of time t_3, the drain voltage $v_D(t_3)$ becomes nearly equal to the on-state voltage drop of the power MOSFET. Thus, $v_D(t_3)$ can be considered negligible. Therefore, the expression for $t_{\rm GP}$ in (11) can be rewritten as

$$t_{\rm GP} = t_3 - t_2 = R_G C_{\rm GD,av} \frac{V_{\rm DS}}{V_G - V_{\rm GP}}. \tag{12}$$

The partial derivative of $t_{\rm GP}$ w.r.t. $N_{\rm ot}$ and $N_{\rm it}$ results in

$$\frac{\partial t_{\rm GP}}{\partial N_{\rm ot}} = R_G C_{\rm GD,av} \frac{V_{\rm DS}}{\left(V_G - V_{\rm GP}\right)^2} \frac{\partial V_{\rm GP}}{\partial N_{\rm ot}} \quad < 0 \tag{13}$$

and

$$\frac{\partial t_{\mathrm{GP}}}{\partial N_{\mathrm{it}}} = R_G C_{\mathrm{GD,av}} \frac{V_{\mathrm{DS}}}{(V_G - V_{\mathrm{GP}})^2} \frac{\partial V_{\mathrm{GP}}}{\partial N_{\mathrm{it}}} \quad > 0 \qquad (14)$$

respectively. Since the partial derivative of V_{GP} w.r.t. N_{it} is negative in (8), the partial derivative of t_{GP} w.r.t. N_{ot} in (13) is also negative. This indicates that t_{GP} decreases with increase of N_{ot}. Similarly, since the partial derivative of V_{GP} w.r.t. N_{it} is positive in (9), the partial derivative of t_{GP} w.r.t. N_{it} in (14) is also positive. This indicates that t_{GP} increases with increase of N_{it}. Thus, t_{GP} follows a dip-and-rebound variation pattern like V_{TH} and V_{GP}.

D. Variation of On-Resistance

The on-resistance of the power MOSFET shown in Fig. 3 is mainly composed of four resistances: channel resistance R_{CH}, accumulation layer resistance R_A, drift resistance R_D, and contact resistance R_C [16], [25]. The presence of trapped charges due to gate-oxide degradation mainly affects R_{CH} and R_A [16]. Thus, the variation of R_{CH} and R_A reflects the variation of R_{ON} in power MOSFETs due to gate-oxide degradation. These resistances are given by [25]

$$R_{\mathrm{CH}} = \frac{L_{\mathrm{CH}}}{2Z\mu C_{\mathrm{ox}}(V_G - V_{\mathrm{TH}})} \qquad (15)$$

and

$$R_A = \frac{L_A}{2Z\mu_{nA} C_{\mathrm{ox}}(V_G - V_{\mathrm{TH}})} \qquad (16)$$

where Z is the length of the cell in the orthogonal direction to the cross section shown in Fig. 3, L_{CH} is the channel length, L_A is the accumulation layer path, μ is the inversion-layer mobility, μ_{nA} is the accumulation-layer mobility, and C_{ox} is the specific gate oxide capacitance.

As mentioned before, the effect of N_{ot} on mobility is assumed to be negligible. Thus, the derivative of R_{CH} w.r.t. N_{ot} and N_{it} can be simplified to

$$\frac{\partial R_{\mathrm{CH}}}{\partial N_{\mathrm{ot}}} = \frac{L_{\mathrm{CH}}}{2Z\mu C_{\mathrm{OX}}(V_G - V_{\mathrm{TH}})^2} \frac{\partial V_{\mathrm{TH}}}{\partial N_{\mathrm{ot}}} < 0 \qquad (17)$$

and

$$\frac{\partial R_{\mathrm{CH}}}{\partial N_{\mathrm{it}}} = \frac{L_{\mathrm{CH}}}{2Z\mu^2 C_{\mathrm{OX}}(V_G - V_{\mathrm{TH}})^2} \left[\mu \frac{\partial V_{\mathrm{TH}}}{\partial N_{\mathrm{it}}} - (V_G - V_{\mathrm{TH}}) \frac{\partial \mu}{\partial N_{\mathrm{it}}} \right] > 0. \qquad (18)$$

The field dependence of accumulation-layer mobility is very similar to inversion-layer mobility [24]. Thus, the presence of trapped charges can be expected to bring a similar reduction in both μ and μ_{nA}. Therefore, the derivative of R_A w.r.t. N_{ot} and N_{it} can be calculated (with similar assumptions made for R_{CH}) as

$$\frac{\partial R_A}{\partial N_{\mathrm{ot}}} = \frac{L_A}{2Z\mu_{na} C_{\mathrm{OX}}(V_G - V_{\mathrm{TH}})^2} \frac{\partial V_{\mathrm{TH}}}{\partial N_{\mathrm{ot}}} < 0 \qquad (19)$$

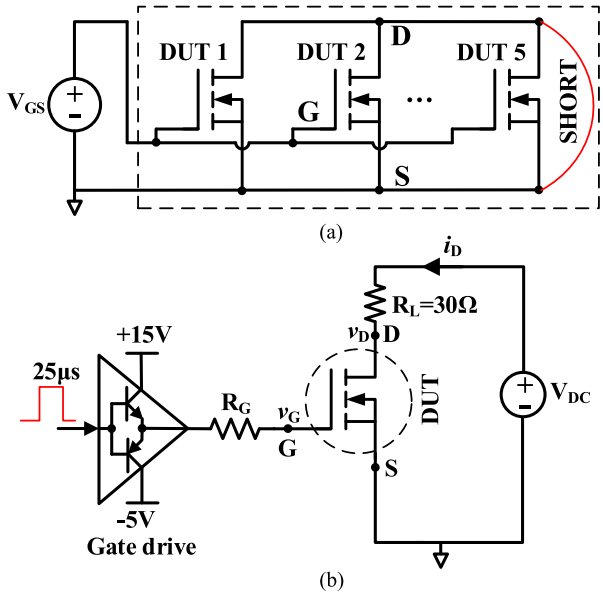

Fig. 6. Circuit schematic for (a) HEF-stress platform and (b) switching-test platform.

and

$$\frac{\partial R_A}{\partial N_{\mathrm{it}}} = \frac{L_A}{2Z\mu_{na}{}^2 C_{\mathrm{OX}}(V_G - V_{\mathrm{TH}})^2} \left[\mu_{nA} \frac{\partial V_{\mathrm{TH}}}{\partial N_{\mathrm{it}}} - (V_G - V_{\mathrm{TH}}) \frac{\partial \mu_{nA}}{\partial N_{\mathrm{it}}} \right] > 0. \qquad (20)$$

As seen from expression (17) and (19), the derivative of both R_{CH} and R_A w.r.t. N_{OT} are negative, which indicates that R_{ON} decreases with increase of N_{ot}. Similarly, the derivative of both R_{CH} and R_A w.r.t. N_{it} in (18) and (20) are positive, which indicates that R_{ON} increases with increase of N_{it}. Thus, Ron follows a dip-and-rebound variation pattern like V_{TH}, V_{GP}, and t_{GP}.

IV. Experiment Details

Experiments were performed on two different commercial power MOSFETs: IRF510 (100 V, 5.6 A) and IRF520 (100 V, 9.2 A) [26], [27] in order to validate the analysis made in previous section.

A. Experimental Setup

The experimental circuit schematic and overall setup are shown in Figs. 6 and 7, respectively. The setup mainly consists of a high-electric-field (HEF) stress platform [see Fig. 6(a)] to induce accelerated gate-oxide degradation of MOSFETs, a switching-test platform [see Fig. 6(b)] to obtain the MOSFETs' turn-on waveform, and a B2912A device analyzer to obtain device characteristics.

A total of five MOSFETs [DUT 1 through DUT 5 in Fig. 6(a)] were inserted into the sockets of the HEF-stress platform for accelerated aging. Electrical stressing was performed by applying positive bias to the gate electrode at ambient temperature (25 °C)

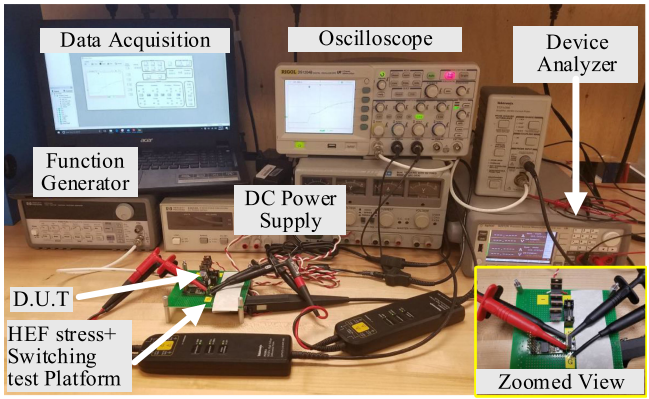

Fig. 7. Experimental setup.

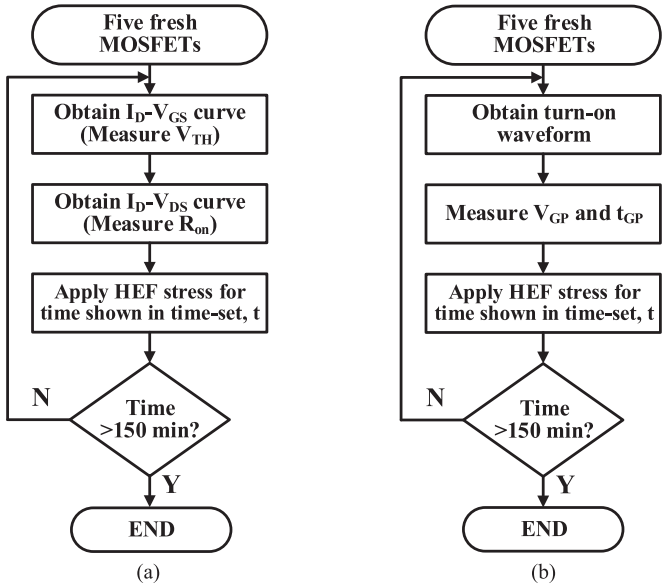

Fig. 8. Experimental process flowchart for measurement of (a) V_{TH} and R_{ON} and (b) V_{GP} and t_{GP}.

with the drain and source terminals grounded. The stress voltage was chosen (fixed 65 V for both devices) such that it was sufficient to initiate observable gate-oxide degradation, but low enough not to cause gate oxide breakdown.

To obtain the turn-on waveforms, each MOSFET was driven by a gate driver with a gate bias voltage of -5 V/$+15$ V [see Fig. 6(b)]. Since, it is easier to observe switching characteristics with a larger gate resistance, an external 100 Ω resistance was inserted between the gate driver and the gate terminal of the MOSFET. To minimize self-heating of the MOSFET during the test, a single 25 μs pulse was provided to the gate driver. A dc voltage of 30 V and a load resistance (R_L) of 30 Ω were used to ensure a drain current of 1 A.

B. Experimental Process

The experimental process mainly comprises the following: 1) the application of HEF stress for accelerated aging of gate oxide, and 2) the measurement of precursors after the stress. The stress-and-measurement of precursors were carried out for variable times represented by the time set, $t = \{0, 2, 2, 2, 2, 2, 20, 40, 40, 40\}$ for 150 min. It is important to mention that a brief stress-and-measurement pattern of 2-min interval during the initial stages of stress was necessary to observe the "dip" effect of Q_{ot} on precursors.

Fig. 8(a) shows the experimental process followed to determine V_{TH} and R_{on} for the batch of five MOSFETs. The pulsed $I_D - V_{GS}$ transfer characteristics and $I_D - V_{DS}$ characteristics graphs were obtained using a B2912A device analyzer. The threshold voltage was determined from the pulsed $I_D - V_{GS}$ characteristics using linear extrapolation method [28]–[30], and the on-resistance was determined from the pulsed $I_D - V_{DS}$ characteristics (@ $I_D = 1$ A and $V_G = 10$ V). Then, the batch of five MOSFETs was transferred into the sockets of HEF-stress platform for accelerated aging for a specific duration listed in the time set earlier. Upon subsequent aging, the precursors were measured again. This stress-and-measurement process was carried out for a total duration of 150 min.

Fig. 8(b) shows the experimental process followed to obtain V_{GP} and t_{GP}. The individual MOSFETs were inserted into the socket of switching-test platform. The gate plateau voltage and gate plateau time were obtained from the turn-on waveform. Upon subsequent aging, these precursors were measured again. This stress-and-measurement process was carried out for a total duration of 150 min.

V. Results and Discussion

A total of 20 MOSFETs (ten of each MOSFET type) were tested to confirm the variation pattern of electrical parameters. The names of different samples followed the format: KP-510-xx for IRF510 sample group and KP-520-xx for IRF520 sample group, where xx denoted each sample's number. Figs. 9 and 10 show the variation of precursors with HEF stress for all the samples, where the bottom horizontal axis corresponds to the order of measurement and the top horizontal axis corresponds to the specific time at which each measurement was taken. As aforementioned, an initial dip was predominantly due to a buildup of Q_{ot}, while the rebound in the later stages was predominantly due to an accumulation of Q_{it}.

A. Variations of Threshold Voltage

Figs. 9(a) and 10(a) show the variation of V_{TH} that occurred in both the IRF510 (KP-510-11 through KP-510-15) and IRF520 (KP-520-51 through KP-520-55) samples when the samples were subjected to HEF stress. Fresh KP-510-xx and KP-520-xx samples had average initial positive V_{TH} of nearly $+3.2$ and $+3.1$ V, respectively. During an initial four min of stress, V_{TH} decreased to negative values (nearly -3.1 V for KP-510-xx samples and -3.2 V for KP-520-xx samples). After the turnaround point, V_{TH} returned to and surpassed its initial positive value. The 'positive to negative to positive' transition of V_{TH} indicated "normally OFF to normally ON to normally OFF" transitions in power MOSFETs over the course of gate-oxide degradation.

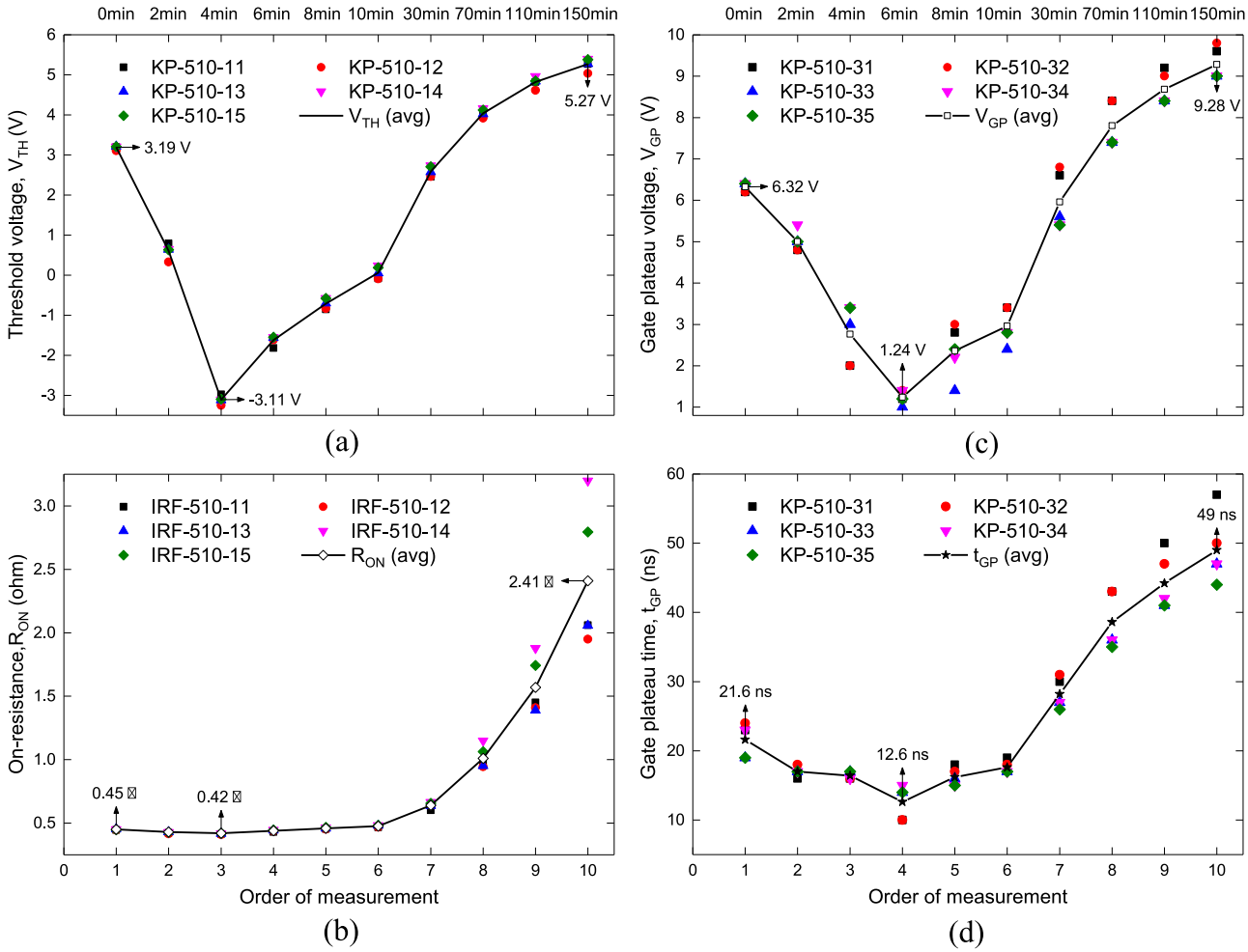

Fig. 9. Variations of (a) threshold voltage, (b) on-resistance, (c) gate plateau voltage, and (d) gate plateau time for five samples of IRF510 over time.

B. Variations of On-Resistance

Figs. 9(b) and 10(b) show the variation of R_{ON} that occurred in both the IRF510 (KP-510-11 through KP-510-15) and IRF520 (KP-520-51 through KP-520-55) samples. It was observed that R_{ON} decreased very slightly in the initial stage. However, it rebounded significantly in the later stages of degradation (exceeding 4 times for IRF510 samples and 6 times for IRF520 samples). Thus, it was observed that R_{ON} followed the dip-and-rebound variation pattern like V_{TH}.

C. Variations of Gate Plateau Voltage

Figs. 9(c) and 10(c) show the variation of V_{GP} that occurred in both the IRF510 (KP-510-31 through KP-510-35) and IRF520 (KP-520-71 through KP-520-75) samples. It was observed that V_{GP} dipped and rebounded in a manner similar to V_{TH} and R_{ON}. Fig. 11 shows gate voltage (V_G) waveforms for samples KP-510-31 and KP-520-74. The solid black arrows point to an initial V_{GP} decrease, which was followed by a V_{GP} increase during later stages. Tabulated V_{GP} values show that V_{GP} @ 150 min $>$ V_{GP} @ 0 min (Fresh MOSFET) $>$ V_{GP} @ 6 min for KP-510-31 sample (or V_{GP} @ 4 min for KP-520-74 sample).

D. Variations of Gate Plateau Time

Figs. 9(d) and 10(d) show the variation of t_{GP} that occurred in both the IRF510 (KP-510-31 through KP-510-35) and IRF520 (KP-520-71 through KP-520-75) samples. It was observed that t_{GP} dipped and rebounded in a manner similar to other precursors: V_{TH}, R_{ON}, and V_{GP}. Such a variation can also be observed in the waveform in Fig. 11, in which dotted black lines show t_{GP} at different stress times. Tabulated t_{GP} values show that t_{GP} @ 150 min $>$ t_{GP} @ 0 min (Fresh MOSFET) $>$ t_{GP} @ 6 min for KP-510-31 sample (or t_{GP} @ 4 min for KP-520-74 sample).

E. Precursor Comparison

The experiment's results confirmed that all four precursors reflected the gate-oxide degradation status with simultaneous negative and positive shifts from their initial values. The shift tendency of each precursor was different; the average shifts from the respective initial values of the precursors in both sample groups are provided in Table I. The percentage shifts were computed for a stress period of 150 min. For longer stress periods, the percentage positive shifts can be expected to increase. Three observations were noted:

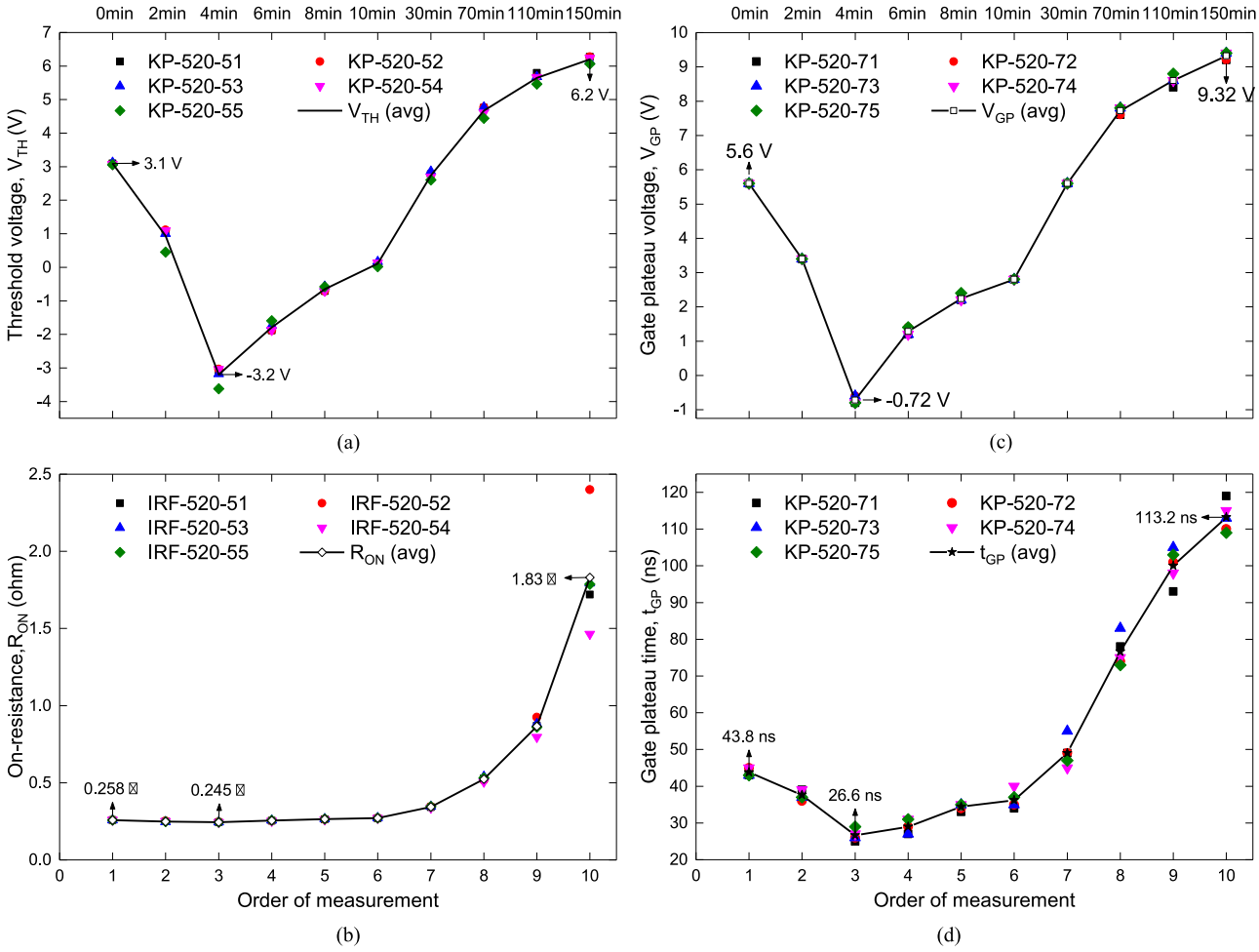

Fig. 10. Variations of (a) threshold voltage, (b) on-resistance, (c) gate plateau voltage, and (d) gate plateau time for five samples of IRF520 over time.

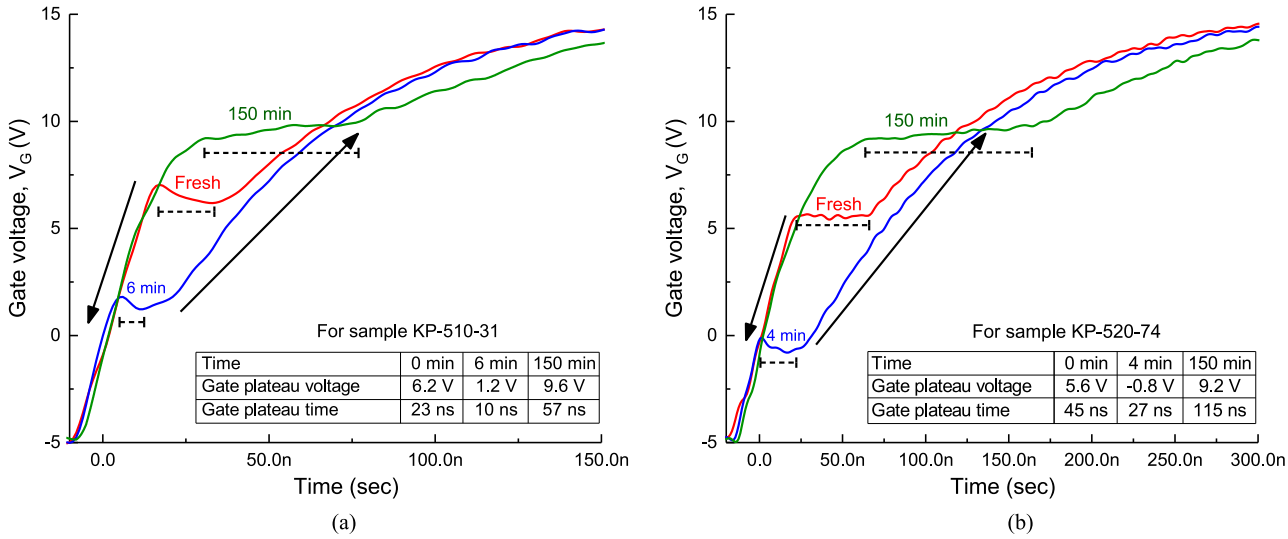

Fig. 11. Variations of V_{GP} and t_{GP} shown in gate voltage waveform of (a) sample KP-510-31 and (b) sample KP-520-74.

TABLE I
PERCENTAGE SHIFT OF PRECURSORS

Precursors	IRF510 Samples		IRF520 Samples	
	% Negative Shift	% Positive Shift	% Negative Shift	% Positive Shift
Threshold voltage	200%	65%	200%	100%
On-resistance	7%	440%	5%	610%
Gate plateau voltage	80%	50%	115%	70%
Gate plateau time	40%	130%	40%	160%

1) In both sample groups, V_{TH} had the highest negative shift at nearly 200% each, while R_{ON} exhibited the least negative shifts at 7% and 5% for the IRF510 and IRF520 samples, respectively. In addition, for both groups, V_{GP} had a higher negative shift than t_{GP}.
2) In both sample groups, R_{ON} had the highest positive shift at nearly 440% and 610% for IRF510 and IRF520 samples, respectively. Moreover, t_{GP} had the highest positive shift (nearly 130% for IRF510 samples and 160% for IRF520 samples) compared to V_{TH} (nearly 65% for IRF510 samples and 100% for IRF520 samples) and V_{GP} (nearly 50% for IRF510 samples and 70% for IRF520 samples). Although it was found that the off-line precursor R_{ON} had a maximum positive shift, the online precursors (V_{TH}, V_{GP}, and t_{GP}) have an additional advantage over R_{ON} (off-line precursor) in that they can be extracted without affecting a system's operation.
3) The threshold voltage was the most suitable precursor for observing the negative shift while R_{on} and t_{GP} were more suitable precursors for observing the positive shift.

VI. CONCLUSION

In this paper, the effect of gate-oxide degradation on four electrical parameters of power MOSFETs were examined qualitatively and quantitatively. It was demonstrated that the electrical parameters of power MOSFETs vary with a dip-and-rebound pattern over the course of gate-oxide degradation. The pattern, which results from the presence of oxide-trapped charges and interface-trapped charges, was confirmed by inducing gate-oxide degradation in two different commercial power MOSFETs. The results of all samples were very consistent and repeatable. Furthermore, shift tendencies, which occurred throughout gate-oxide degradation in the online and off-line precursors, i.e., V_{TH}, V_{GP}, R_{ON}, and t_{GP}, were compared. The new online precursor t_{GP} was found to be a competitive precursor of gate-oxide degradation, as it had a higher positive shift than the other online precursors (V_{TH} and V_{GP}). Additionally, V_{TH} was found to be the most sensitive precursor for observing the negative shift, while R_{on} and t_{GP} were found to be the most sensitive precursors for observing the positive shift.

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