

Duty Cycle and Frequency Modulations in Class-E DC–DC Converters for a Wide Range of Input and Output Voltages

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Abstract—We present an operation scheme for a dc–dc converter consisting of a class-E inverter and a class-E rectifier to always achieve zero-voltage zero- dv/dt switching at a wide range of input and output voltages. To cope with the high sensitivity due to load variations, previous approaches either forgo the zero- dv/dt turn-ON switching conditions or required additional components and topological changes. Instead, the proposed strategy modulates the duty cycles and switching frequencies depending on the input and output voltages to always achieve zero- dv/dt turn-ON switching and, thus, minimizes switching losses, while preserving the structural simplicity of the converter. Experiments demonstrate the prototype converter maintaining the desired soft-switching condition under 80–200-V input voltage and 5–20-V output voltage variations. In an additional prototype, we implemented a similar design with synchronous rectification that achieves a peak efficiency of 92.3% at an input voltage of 80 V, an output voltage of 12 V, and an output power of 26.9 W.

Index Terms—DC-DC power converters, power conversion, resonant converters.

I. INTRODUCTION

HIGH-FREQUENCY power conversion enables system size and weight reductions, new applications [1], [2], and new ways to build power converters [3]. Among many resonant converter topologies that eliminate switching loss for high-frequency operation, class-E [4]–[6] is a popular choice for its circuit simplicity, ease of design, tuning, and because it only needs a simple ground-referenced gate drive. Just as many other types of resonant converters, conventional class-E converters operate efficiently only on a narrow range of input and output voltages. This paper presents an operation scheme to overcome this limitation by changing the transistor duty cycle and switching frequency.

The main disadvantage of the class-E converter is its sensitivity to variations on the input and output conditions [7]. When the inverter is designed to operate at 50% duty cycle, Raab [8]

reports 5% inverter efficiency drop by a twofold increase or decrease in the load resistance. Drain voltage waveforms in [8]–[10] show severe switching losses introduced by load variations in a class-E amplifier. This high sensitivity is problematic when the circuit is to be used for applications that demand flexible input and output conditions, such as a universal mobile battery charger in which the input voltage should typically range from 85 to 265 V_{ac} and the output voltage from 5 to 20 V_{dc}.

The design outlined in [10] overcomes this problem by tuning the converter such that the zero crossing of the voltage across the switch always occurs at a constant timing. This tuning method guarantees zero-voltage switching under varying input and output voltage conditions, provided that the gate drive signal has an accurate and precise duty cycle, as well as fast rise time. Because this strategy forgoes the zero- dv/dt during the turn-ON transition, a slight deviation in the switching timing may lead to significant switching loss, especially at high frequency. Using a resistance compression network [9] is another effective strategy to tackle the sensitivity issue in these converters. The impedance network consisting of inductors and capacitors significantly reduces the range of the load variations when seen from the input of the network. Although this method adds several passive components to the system and requires two identical loads, this solution is generally applicable beyond class-E to other topologies to deal with the load variation problem.

This paper presents a new method to deal with the sensitivity of a class-E converter to the input and output conditions. For a dc–dc converter consisting of a class-E inverter and a class-E rectifier [11], we use different duty cycles and frequencies depending on the input and output voltages to always achieve zero-voltage zero- dv/dt switching. This strategy adds no additional components on the power stage, although at the expense of potentially more complicated design of the gate drive unit. Since the proposed method only handles input and output voltage conditions, a proper control strategy such as ON–OFF control [12], [13] is necessary to maintain the desired output current level.

The remainder of this paper is organized as follows. Section II explains how to calculate the duty cycle and frequency values for the desired soft switching. We perform the analysis on an example converter to illustrate the calculation steps. Section III shows the experimental verification and achievements. We build a converter and test it to validate the theoretical analysis, identify sources of power loss, and improve the efficiency by synchronous rectification. We also briefly introduce

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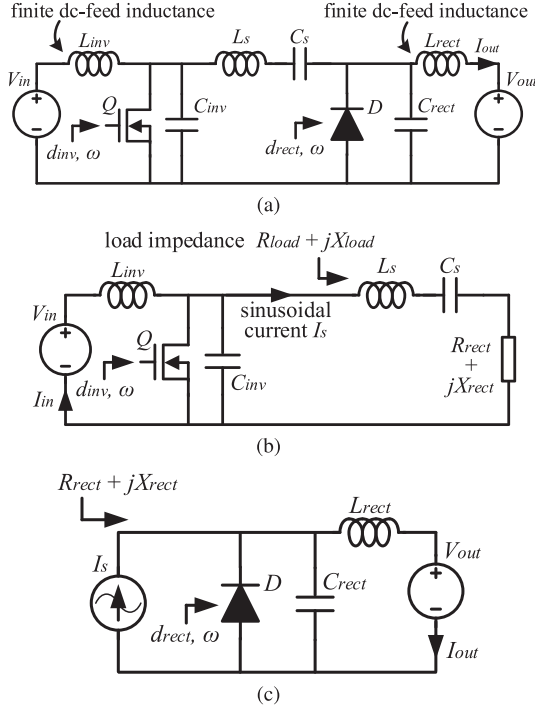


Fig. 1. Class-E dc-dc converter that is the subject of our study. Instead of large (ideally infinite) choke inductance [4], [11], a finite dc-feed inductance [5] is used in both the inverter and the rectifier. (a) DC-DC converter consisting of a class-E inverter and a class-E rectifier [11]. A series LC filter lies between them. (b) Class-E inverter under the assumption that only sinusoidal ac current with I_s half peak-to-peak amplitude flows into the LC filter branch and the rectifier. (c) Class-E rectifier [5], [11] under the assumption that it is driven by a sinusoidal input current with I_s half peak-to-peak amplitude.

a new way to design a class-E converter with a loosely coupled transformer [12]–[16] and describe its benefit. Section IV concludes this paper.

II. DUTY CYCLE AND FREQUENCY CALCULATIONS

A. Calculation Steps

The dc-dc converter that is the subject of our study consists of a class-E inverter and a class-E rectifier [11], both of which have finite dc-feed inductance [5]. Fig. 1(a) shows the schematic of the circuit. Analyses throughout this section are based on following assumptions. First, Q and D are ideal switches. They have zero forward voltage drop, zero ON-resistance, as well as zero turn-ON and turn-OFF time. Their junction capacitances are absorbed to the parallel capacitance C_{inv} and C_{rect} , and their nonlinearity is negligibly small. Second, all passive elements are ideal. Especially, series resistances of inductors L_{inv} , L_s , and L_{rect} are negligibly small. Finally, the current flowing through the L_s - C_s branch is sinusoidal.

We explain how to determine the switching frequency ω , the inverter duty cycle d_{inv} , and the rectifier duty cycle d_{rect} that achieve zero-voltage zero- dv/dt switching for a given converter design. By a given converter design, we mean the following values are given: the input dc voltage V_{in} , the inverter-side resonant inductance L_{inv} and capacitance C_{inv} , the filter inductance L_s and capacitance C_s , the rectifier-side resonant inductance L_{rect} and capacitance C_{rect} , and the output dc voltage V_{out} .

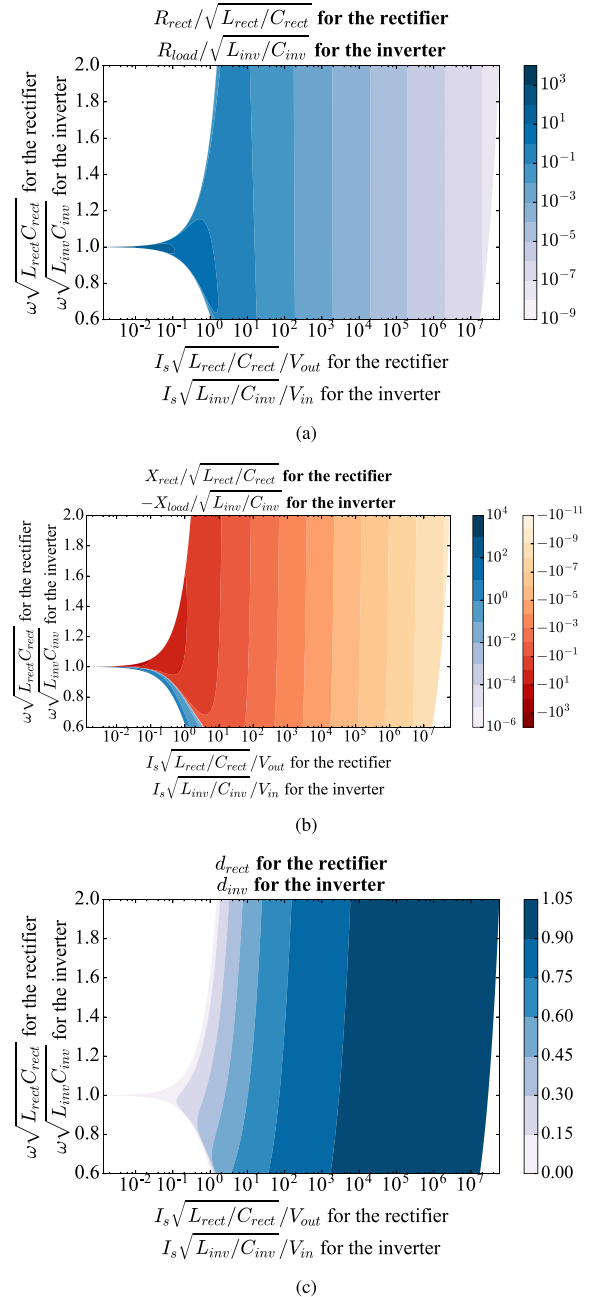


Fig. 2. General solution maps of equivalent impedance and duty cycles for zero-voltage zero- dv/dt switching. For the rectifier, solution maps describe the equivalent input impedance of the rectifier. For the inverter, these maps describe the load impedance that the inverter needs to drive. (a) Equivalent resistance. (b) Equivalent reactance. (c) Switch duty cycle.

Assuming that a sinusoidal ac current flows between the inverter and the rectifier, we can divide the circuit of Fig. 1(a) into two parts: an inverter driving a load impedance $R_{load} + jX_{load}$ with a sinusoidal load current of I_s half-peak-to-peak amplitude [see Fig. 1(b)], and a rectifier presenting an input impedance $R_{rect} + jX_{rect}$ and being driven by a sinusoidal current source with I_s half-peak-to-peak amplitude [see Fig. 1(c)][11].

Fig. 2 shows general solution maps of d_{inv} , d_{rect} , R_{rect} , R_{load} , X_{rect} , and X_{load} for zero-voltage zero- dv/dt switching (derivation details are in Appendix IV; the *Python* code that

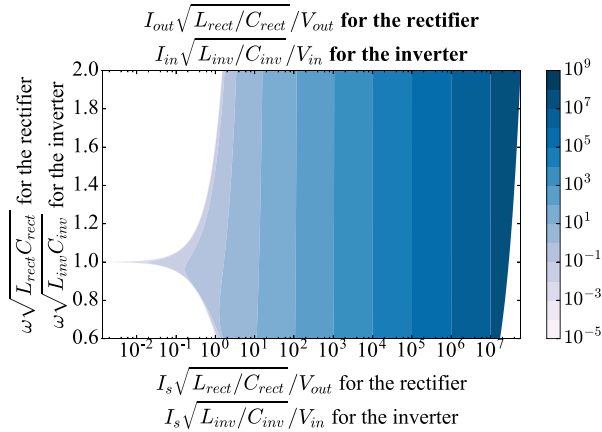


Fig. 3. General solution map of the dc-dc converter output current. This plot is used to predict the output current of the dc-dc converter at the desired operating point (I_s, ω) .

calculates and plots the solution map is in Appendix B; basic ideas of the derivation are from [17]–[20]). Because a class-E inverter operation is time reversal of a class-E rectifier operation [21], [22], the solution map for X_{load} equals that for X_{rect} times negative one [see Fig. 2(b)]. Those solution maps give specific values of six parameters mentioned above as a function of I_s and ω , all of which are scaled by a simple function of resonant inductance, resonant capacitance, and dc voltages, as shown on the plot titles and axes labels of Fig. 2. The reason for choosing I_s and ω as variables is that only those two parameters are shared by both the inverter [see Fig. 1(b)] and the rectifier [see Fig. 1(c)].

When a converter design is given, we calculate scaling factors and turn general solution maps into specific solution maps that show necessary impedance and duty cycles for the inverter and the rectifier. Once we obtain specific solution maps for the given converter, we find the point (I_s, ω) that makes $R_{load}(I_s, \omega)$ equal to $R_{rect}(I_s, \omega)$ and $X_{load}(I_s, \omega)$ equal to $X_{rect}(I_s, \omega) + \omega L_s - 1/\omega C_s$. This is to match the impedance the inverter needs to drive and the one presented by the load branch, which is the LC filter connected in series with the rectifier. The found (I_s, ω) is the point that achieves zero-voltage zero- dv/dt switching for both the inverter and the rectifier. Then, we find d_{inv} and d_{rect} that correspond to the (I_s, ω) point on the specific solution maps derived from Fig. 2(c).

Fig. 3 is used to find the rectifier output current. Similar to what we have explained for Fig. 2, we convert the plot to the specific solution map by multiplying appropriate scaling factors to horizontal and vertical axes and, then, read the output current value that corresponds to the found (I_s, ω) point.

B. Calculation Example

In order to illustrate the calculation procedure outlined above, consider an example converter in structure of Fig. 1(a) with component values given in Table I. Fig. 4 illustrates the steps for finding duty cycles and the frequency, which we describe in detail in the following.

TABLE I
COMPONENT VALUES OF THE EXAMPLE CONVERTER WITH VARIABLE NAMES IN REFERENCE TO FIG. 1(A)

V_{in} [V]	V_{out} [V]	L_{inv} [μ H]	C_{inv} [nF]	L_s [μ H]	C_s [nF]	L_{rect} [μ H]	C_{rect} [nF]
100	50	2	1	2.5	1	1	1

First, obtain specific solution maps of R_{load} and R_{rect} as a function of I_s and ω . In order to do that, in Fig. 2(a), scale the horizontal axis by $V_{in}/\sqrt{L_{inv}/C_{inv}} = 2.24$ A and the vertical axis by $1/\sqrt{L_{inv}C_{inv}} = 2.24 \times 10^7$ rad/s and multiply the general solution map by $\sqrt{L_{inv}/C_{inv}} = 44.7 \Omega$ to obtain Fig. 4(a) and the specific solution map of R_{load} . Similarly for R_{rect} , scale Fig. 2(a) horizontally by $V_{out}/\sqrt{L_{rect}/C_{rect}} = 1.58$ A and vertically by $1/\sqrt{L_{rect}C_{rect}} = 3.16 \times 10^7$ rad/s and multiply the solution map by $\sqrt{L_{rect}/C_{rect}} = 31.6 \Omega$ to obtain Fig. 4(b).

Second, subtract Fig. 4(b) from Fig. 4(a). The result is plotted in Fig. 4(c). The curve on which $R_{load} - R_{rect}$ equals 0 is the set of (I_s, ω) that matches the resistance needed by the inverter and the resistance presented by the rectifier.

Third, obtain specific solution maps of X_{load} and X_{rect} from Fig. 2(b) in a similar fashion as for R_{load} and R_{rect} . Results are shown in Fig. 4(d) and (e). Note that the sign of X_{load} is the opposite of Fig. 2(b).

Fourth, add $(\omega L_s - 1/\omega C_s)$ to Fig. 4(e) and subtract it from Fig. 4(d). The set of (I_s, ω) that satisfies $X_{load} - (X_{rect} + \omega L_s - 1/\omega C_s) = 0$ are points that equalize the reactance needed by the inverter with that presented by the load branch.

Fifth, find the point that matches both the resistance and the reactance between the inverter and the load branch, as shown in Fig. 4(g). In this example, I_s of 3.856 A and ω of $2\pi(4.903$ MHz) is such a point.

Sixth, find the duty cycles. Obtain specific solution maps of d_{inv} and d_{rect} from Fig. 2(c) by a similar method described in the first step. The results are in Fig. 4(h) and (i). Read the values that correspond to the point found in the fifth step. Here, we find $d_{inv} = 0.300$ and $d_{rect} = 0.456$.

Finally, find the output current by scaling Fig. 3 horizontally by 1.58 A and vertically by 3.16×10^7 rad/s, as explained in the first step, multiplying the map by 1.58 A, and then finding the point that corresponds to $(I_s, \omega) = (3.856$ A, $2\pi(4.903$ MHz)). The resulting output current is 2.51 A.

Simulation confirms that zero-voltage zero- dv/dt switching occurs in both the inverter and the rectifier switches when $f = 4.903$ MHz, $d_{inv} = 0.300$, and $d_{rect} = 0.475$, which are in good agreement with the calculations. The reason for the discrepancy is that in simulation, I_s is not perfectly sinusoidal. Table II summarizes the result. Fig. 5 shows simulated waveforms of the voltage across Q [see Fig. 5(a)] and D [see Fig. 5(b)].

III. EXPERIMENTAL VERIFICATION

A. Experimental Setup

We build a class-E dc-dc converter in a structure that uses a loosely coupled transformer [12]–[16] to verify the calculation

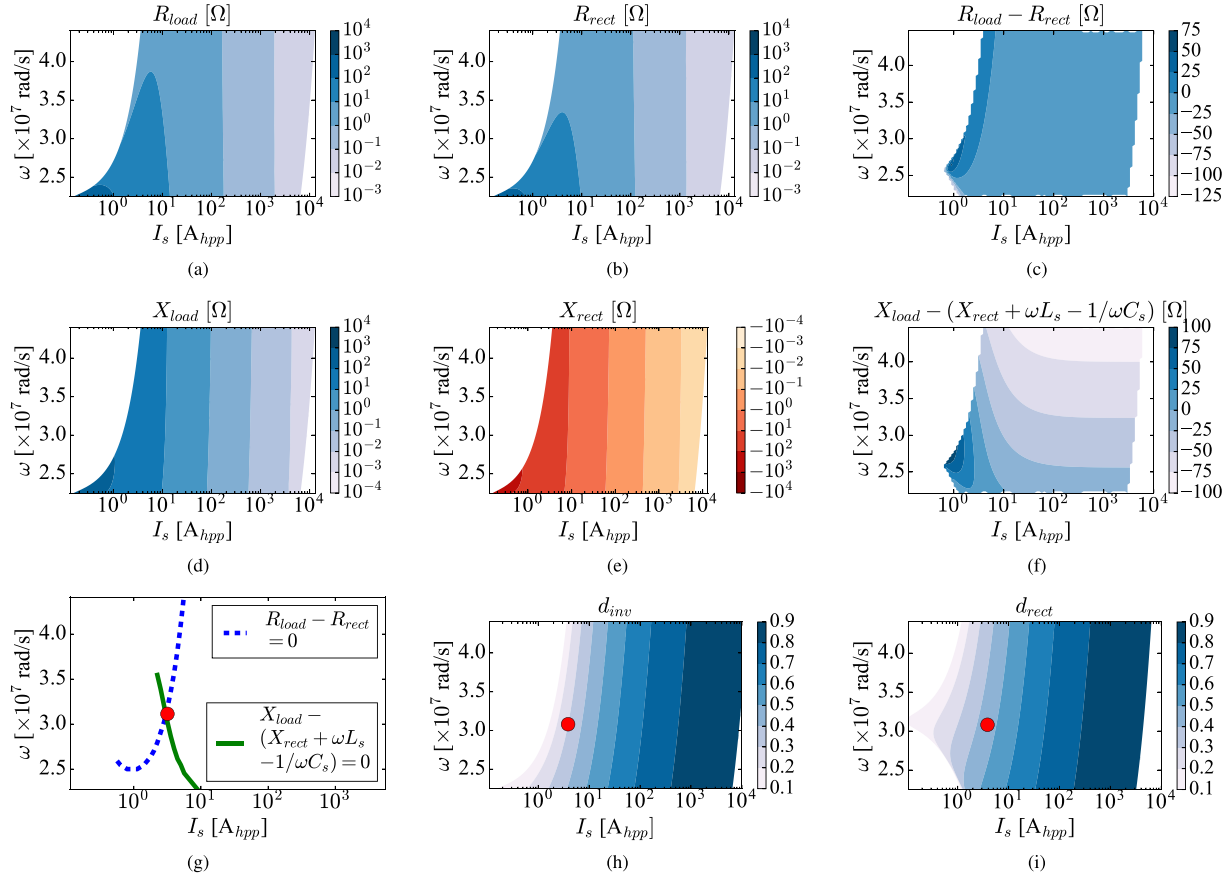


Fig. 4. Calculations steps to find duty cycles d_{inv} , d_{rect} , and the frequency ω to achieve zero-voltage zero- dv/dt switching in both the inverter and the rectifier. (a) Specific solution map of R_{load} obtained from Fig. 2(a). (b) Specific solution map of R_{rect} obtained from Fig. 2(a). (c) R_{rect} subtracted from R_{load} . The curve on which $R_{load} - R_{rect} = 0$ is where the resistance matches between the inverter and the rectifier. (d) Specific solution map of X_{load} obtained from Fig. 2(b). (e) Specific solution map of X_{rect} obtained from Fig. 2(b). (f) $X_{rect} + \omega L_s - 1/\omega C_s$ subtracted from X_{load} . The curve on which the result equals to zero is where the reactance matches between the inverter and the load branch. (g) Two curves extracted from (c) and (f) of which the intersection is marked by a red dot. This dot denotes I_s and ω that achieve soft switching. (h) Point in (g) overlaid on the specific solution map of d_{inv} for the inverter duty cycle. (i) Point in (g) overlaid on the specific solution map of d_{rect} for the rectifier duty cycle.

TABLE II
COMPARISON OF CIRCUIT PARAMETERS PREDICTED BY THE
CALCULATIONS IN SECTION II-B AND THOSE FOUND IN SIMULATION

	Calculation	Simulation
I_s	3.86 A_{hpp}	3.68 A_{hpp}
f	4.90 MHz	4.90 MHz
d_{inv}	0.30	0.30
d_{rect}	0.46	0.48
I_{out}	2.51 A	2.44 A

method in Section II. Although previous publications [13], [15], [16] describe various design methods, we find it convenient to design the converter of such a structure by following the transformation steps in Fig. 6 [23]. The transformation steps are as follows: first, the conventional structure [see Fig. 6(a)] is altered so that the ac-ground connection bridges the converter input and output nodes [see Fig. 6(b)]; next, dc-blocking capacitors are replaced by an ideal transformer [see Fig. 6(c)]; then, the ideal transformer turn ratio is changed to $n:m$ and parameters are adjusted accordingly [see Fig. 6(d)]; and finally, the inductive

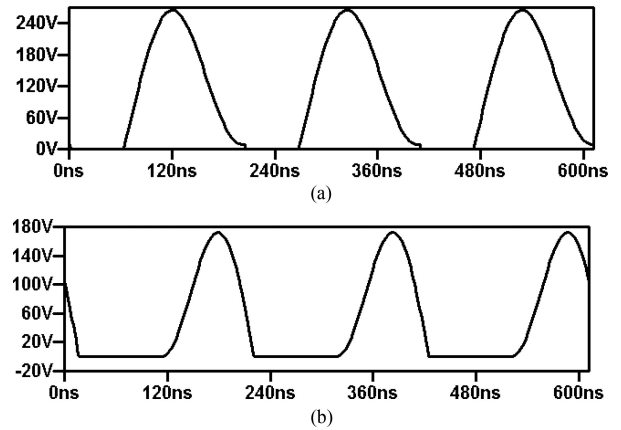


Fig. 5. Simulated waveforms of the voltage across the inverter switch Q and the rectifier diode D of a converter in structure of Fig. 1(a) and with parameters in the Simulation column in Table II. (a) Voltage across Q . (b) Voltage across D .

two-port network within the dashed lines of Fig. 6(d) is replaced by an equivalent coupled inductor pair [see Fig. 6(e)]. Because these steps preserve equivalence of the circuit operation, design

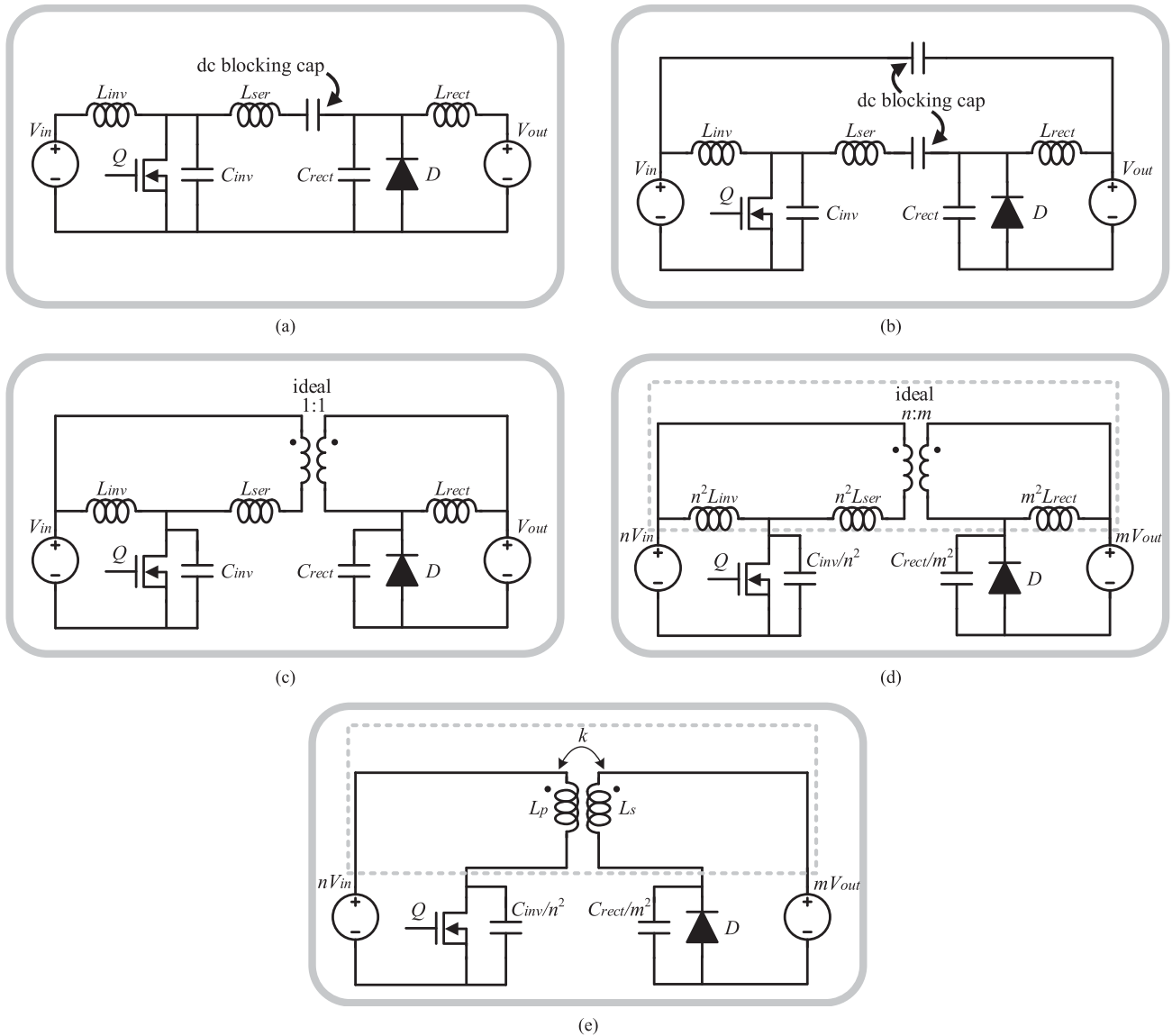


Fig. 6. Transformation steps of the isolated resonant dc-dc converter consisting of a class-E inverter and a class-E rectifier. Because those steps preserve equivalence of the circuit operation, design methods and analyses developed for the conventional structure are directly applicable to any other structures in the transformation steps. (a) First step shows the conventional structure. (b) Second step is where the ac-ground connection is relocated. (c) Third step is where dc-blocking capacitors are replaced by an ideal transformer. (d) In the fourth step, the ideal transformer turn ratio is changed to $n:m$ and parameters are adjusted accordingly. (e) In the final step, the inductive two-port network within the dashed lines is replaced by an equivalent coupled inductor pair.

methods and analyses developed for the conventional structure of Fig. 6(a) are directly applicable to the structure in use [see Fig. 6(e)].

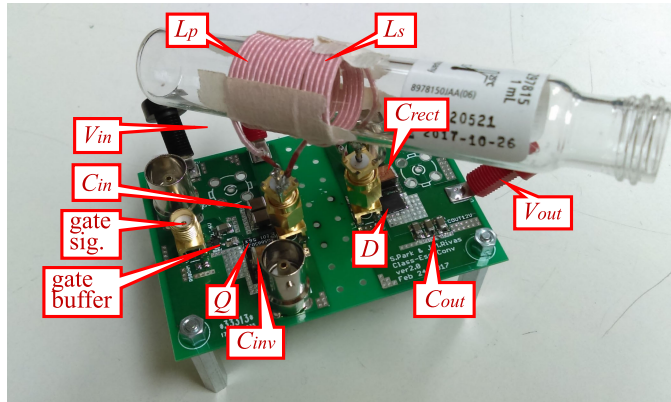
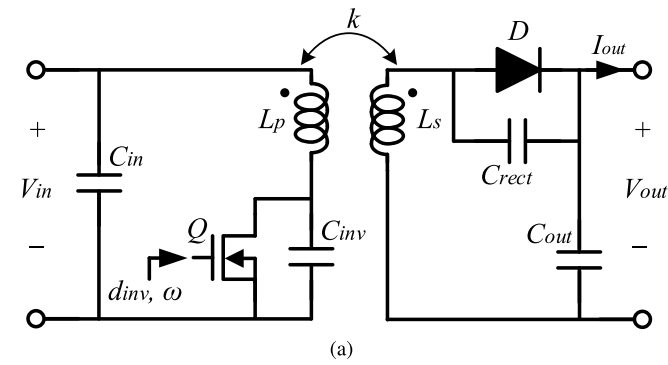
Compared to the equivalent circuit of the conventional design, Fig. 6(e) has several advantages, including: input-output galvanic isolation; less number of components; more flexibility in choosing the input-to-output voltage gain; and in the case of using an air-core transformer, the relatively low coupling coefficient that eases the implementation when the primary and secondary inductances are different.

Fig. 7 describes the experimental setup. Fig. 7(a) and (b) shows the schematic and picture of the implemented converter. Nonlinear junction capacitances of Q and D are denoted by $C_{j,Q}$ and $C_{j,D}$, which we assume to be 36 and 120 pF, respectively. Table III shows the implementation details of the converter.

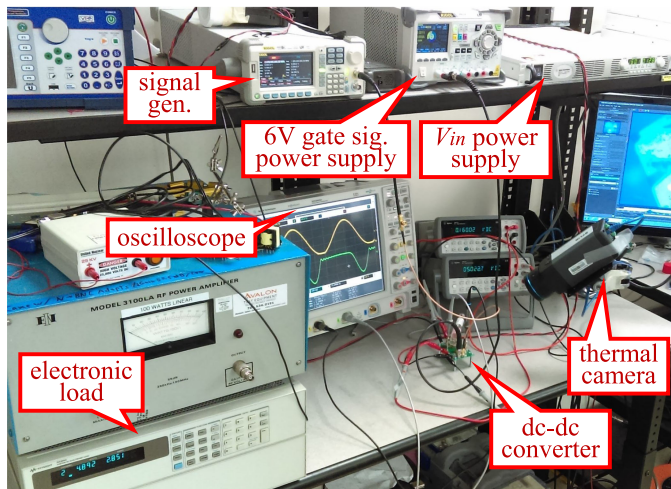
Fig. 7(c) shows the test equipment setup for this experiment. A gate drive chip (SN74LVC1G17, Texas Instruments) receives the gate drive signal from an external signal generator and drives Q .

Compared to Fig. 6(e), D and C_{rect} in Fig. 7(a) are connected to the output node instead of the ground node. This is because the diode we use has a thermal pad on the cathode side just as many other rectifier diodes. The configuration in Fig. 7(a) allows us to add a diode heat sink without its stray capacitance influencing the circuit operation.

We design the converter to operate at switching frequencies close to 2 MHz because such a frequency level has the following advantages: first, 48-AWG litz wire becomes very effective in reducing the winding losses; second, 2 MHz is high enough to implement air-core inductors and thus completely avoid core



(b)



(c)

Fig. 7. Experimental setup to verify the calculation method in Section II. (a) Schematic of the class-E dc-dc converter. (b) Implemented converter. (c) Test equipment setup.

losses; third, C_{inv} and C_{rect} we need are significantly larger than nonlinear $C_{j,Q}$ and $C_{j,D}$, yielding an almost-linear resonant capacitance and thereby making the circuit operation in line with the analysis in Section II; and finally, 2 MHz is slow enough to avoid the power losses of the GaN transistor under high- dv/dt condition [24], namely when the applied voltage stress is hundreds of volts peak-to-peak at tens of megahertz.

In consideration of a high-frequency transformer model [25], nonideal behaviors of our transformer design that can possibly have a significant effect on the converter operation are

TABLE III
IMPLEMENTATION DETAILS OF THE CONVERTER IN FIG. 7(B)

Parameter	Value	Description
C_{inv}	3 nF	CDE mica capacitance
C_{rect}	6 nF	CDE mica capacitance
L_p	2000 nH	675×48 AWG litz; air core
L_s	499 nH	675×48 AWG litz; air core
k	0.257	Air-core coupling
Q	GS66502B	GaN transistor
D	MBR5H100MFS	Si Schottky diode
C_{in}	0.2 μ F	X7R capacitance
C_{out}	0.3 μ F	X7R capacitance
$C_{j,Q}$	36 pF	Approximate nonlinear capacitance
$C_{j,D}$	120 pF	Approximate nonlinear capacitance

interwinding capacitance and frequency-dependent winding resistance. Since our transformer is air core, the core loss or saturation are guaranteed to be nonexistent. The interwinding capacitance in our transformer is in the order of a few picofarads, which is less than 1% of the parallel-connected resonant capacitances C_{inv} and C_{rect} . Frequency dependence of the winding resistance from the skin effect and the proximity effect is taken into account in the simulation-based analysis in Figs. 14 and 15 and the relevant text.

B. Duty Cycle and Frequency Modulation

We change V_{in} from 80 to 200 V by a step of 40 V, and V_{out} from 5 to 9 V, 12 V, and 20 V. For each combination of input and output voltages, we find the frequency and the duty cycle for the converter to achieve zero-voltage zero- dv/dt switching and compare them with the theoretical expectations. In all comparisons between theoretical and experimental results, we suspect the differences are mostly attributed to the voltage drop across the diode, series resistance of inductors, and the nonlinear junction capacitance of semiconductor switches.

Figs. 8 and 9 plot the duty cycles of the inverter switch Q and the switching frequencies, respectively, at different input and output voltages. In both figures, when the input-to-output voltage gain increases (toward the top left of figures), the switching frequency does too, while the duty cycle decreases.

By modulating the duty cycle and the switching frequency, we achieve the desired soft-switching conditions throughout all experiments. As an example, we show in Fig. 10 the experimental waveforms of the voltage across Q [see Fig. 10(a)] and D [see Fig. 10(b)] when we fix V_{out} to 12 V and change V_{in} from 80 to 200 V while modulating the duty cycle and frequency, as indicated in Figs. 8 and 9.

C. Output Current and Regulation

Continuous output currents are plotted in Fig. 11. Due to the lack of design freedom, it is impossible to make the output current deviate from the values of Fig. 11 without giving up zero-voltage or zero- dv/dt switchings and without changing the input or output voltages. As experimentally demonstrated in [12] and [13], a proper control strategy such as ON-OFF control

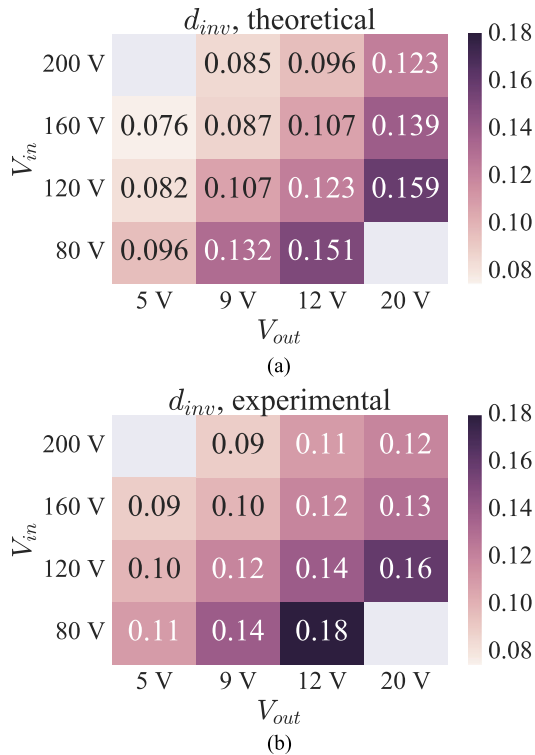


Fig. 8. Duty cycles of the inverter switch Q for zero-voltage zero- dv/dt switching at different input and output voltages. (a) Theoretical. (b) Experimental.

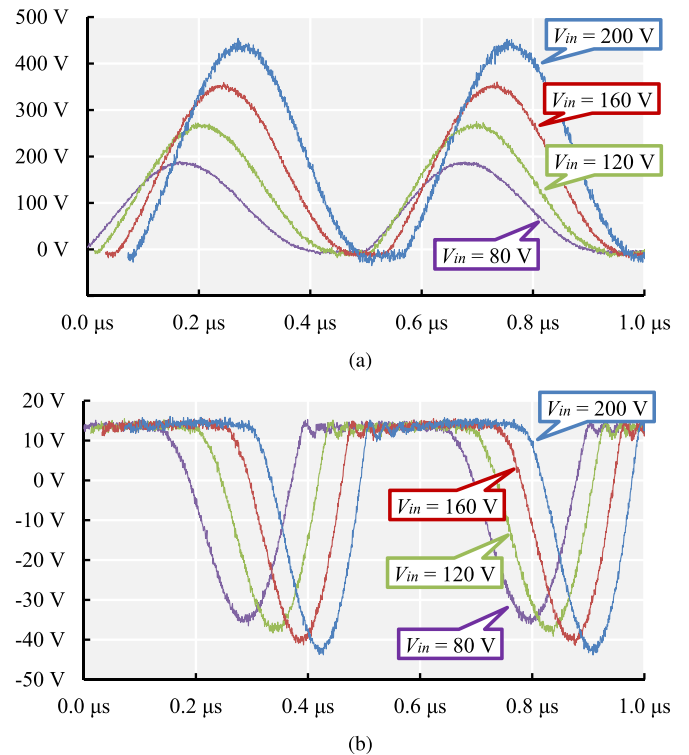


Fig. 10. Experimental waveforms of the voltage across semiconductor devices when we fix V_{out} to 12 V and change V_{in} from 80 to 200 V, while modulating the duty cycle and frequency, as indicated in Figs. 8 and 9. (a) Voltage across the inverter transistor Q . (b) Voltage across the rectifier diode D .

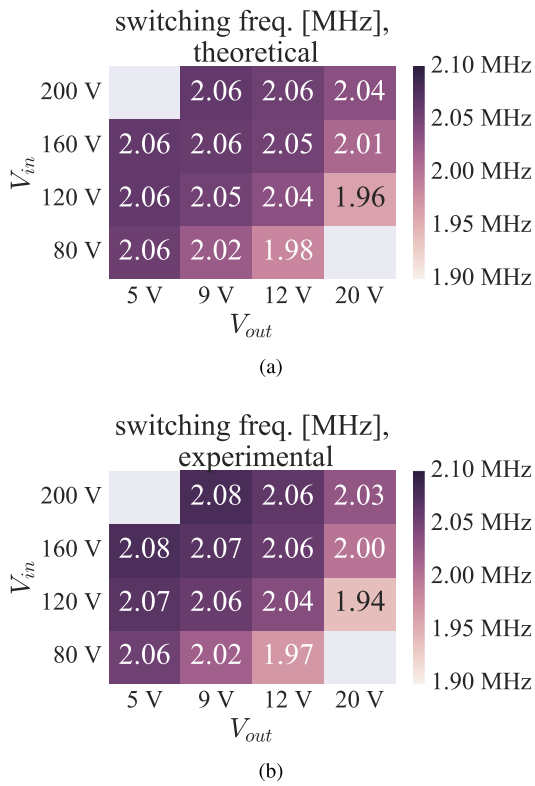


Fig. 9. Switching frequencies for zero-voltage zero- dv/dt switching at different input and output voltages. (a) Theoretical. (b) Experimental.

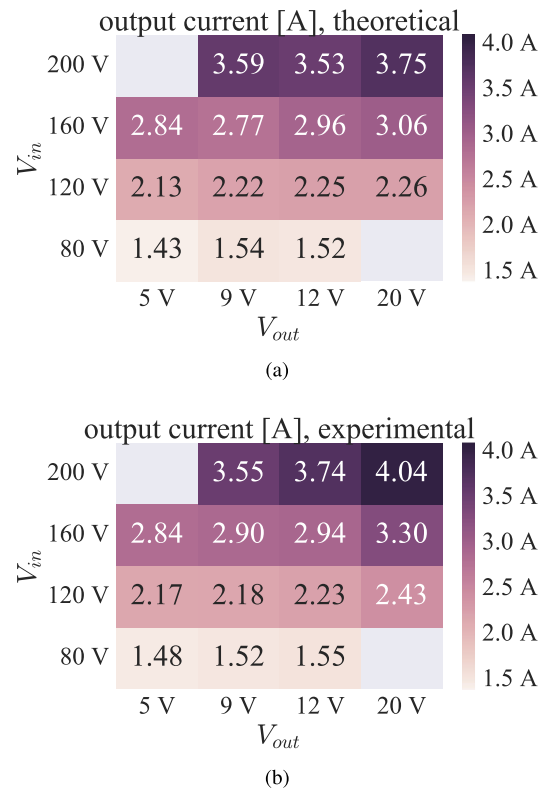


Fig. 11. Output current variation when duty cycle and frequency are modulated as in Figs. 8 and 9. (a) Theoretical. (b) Experimental.

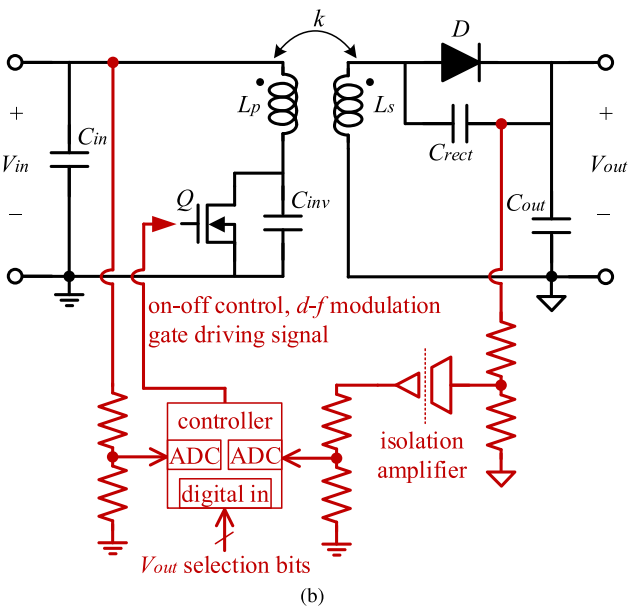
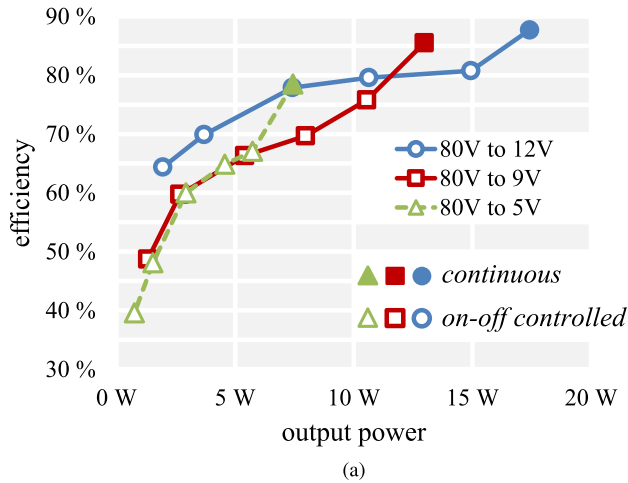


Fig. 12. Experimental demonstration of ON-OFF control and a possible closed-loop controller design. (a) Experimental efficiency versus output power when the output voltage is regulated by ON-OFF control. (b) Concept schematic of a closed-loop controller and an auxiliary circuitry.

should be used to cope with load variations at given input and output voltages.

Fig. 12(a) depicts the measured dc-dc efficiency for different output powers when we try ON-OFF control to regulate the output voltage. The output power of the converter can be adjusted from the maximum level under continuous operation (indicated by filled markers) down to near-zero power level under the ON-OFF control scheme (indicated by hollow markers) at the expense of degraded efficiency and increased input and output voltage ripple. Designers should choose parameters of the converter so that the maximum output power they need is smaller than or equal to the output power under continuous converter operation. We show the concept schematic of the closed-loop controller and the auxiliary circuitry in Fig. 12(b), but without implementation. Should anyone interested in building one, the shown schematic can be one possible way to carry out the task.

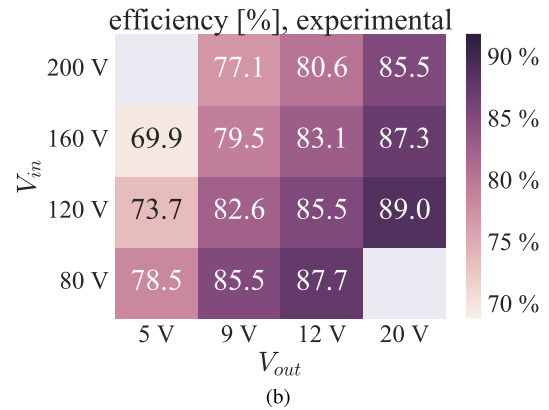
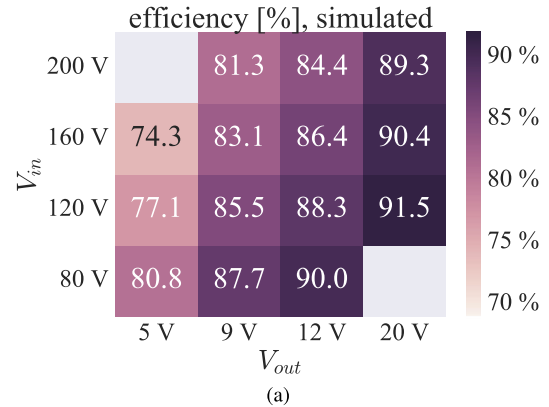


Fig. 13. Converter efficiency at different input and output voltages. Experimental efficiency includes the gate buffer power drawn from the external power supply and excludes the power consumption of the signal generator. (a) Simulated. (b) Experimental.

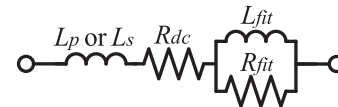
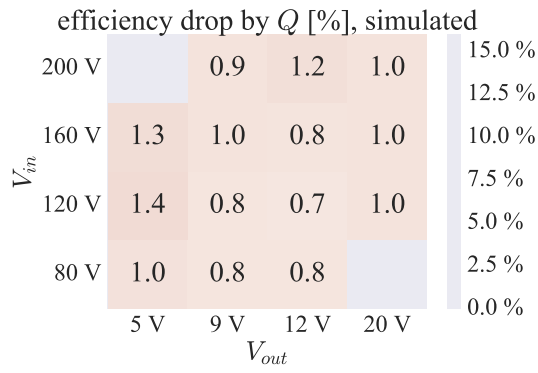


Fig. 14. Inductor with an RL network to emulate the series resistance that increases with frequency due to dielectric and skin effect losses. We use this circuit in place of L_p and L_s while simulating the converter in Fig. 7(a) to estimate inductor losses.

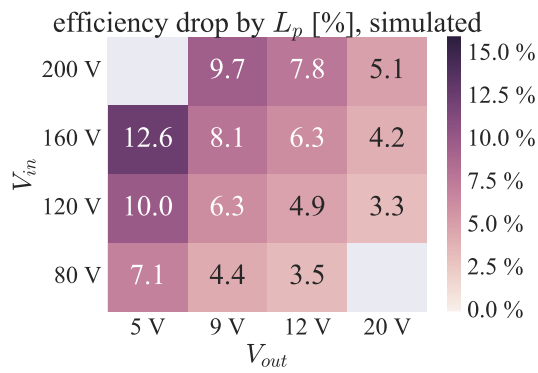
D. Efficiency Variation

The efficiency of the converter changes when the duty cycle and the frequency are adjusted for different input and output voltages. As shown in Fig. 13, the efficiency decreases with increasing input-to-output voltage gain both in simulations [see Fig. 13(a)] and experiments [see Fig. 13(b)]. Experimental efficiency includes 0.024-W gate buffer power drawn from the 6-V external power supply and excludes the power consumption of the signal generator.

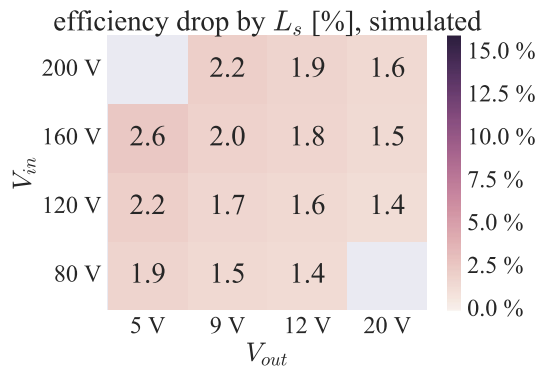
We simulate the dc-dc converter in order to estimate how much efficiency drops are caused by each circuit components in Fig. 7(a). For Q , we use the manufacturer-provided SPICE model for power loss estimation [26]. For D , losses are simulated by a constant forward voltage drop of 0.5 V and a ON-resistance of 0.02 Ω to fit the I - V curve for 25 $^\circ\text{C}$ in the datasheet [27]. Capacitors C_{in} , C_{inv} , C_{rect} , and C_{out} are



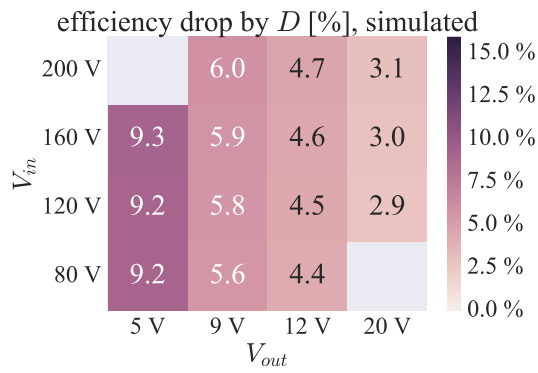
(a)



(b)

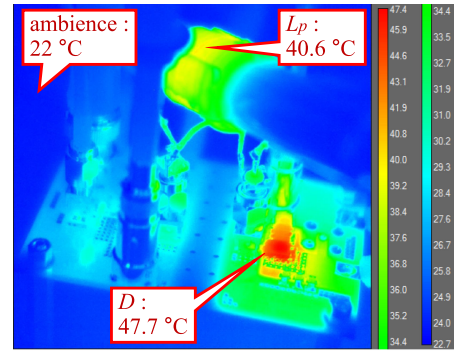


(c)

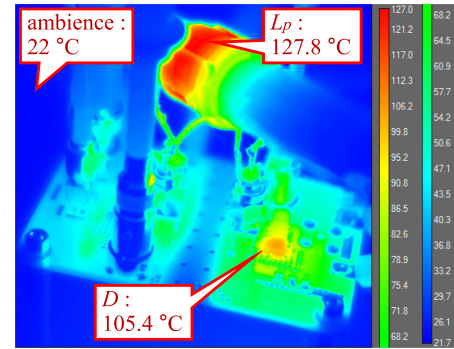


(d)

Fig. 15. Simulated efficiency drops caused by (a) the inverter transistor Q , (b) the primary winding L_p , (c) the secondary winding L_s , and (d) the rectifier diode D .

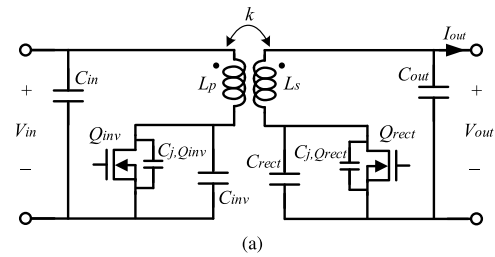


(a)

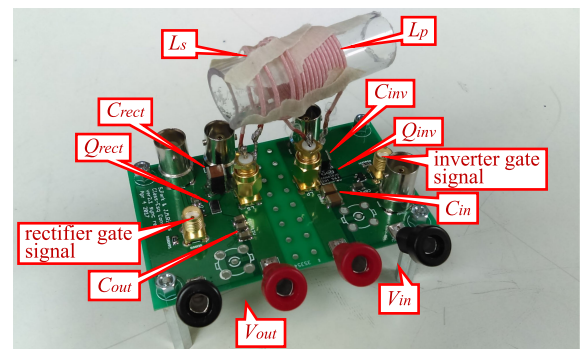


(b)

Fig. 16. Thermal images of the converter at thermal equilibrium. Temperatures of L_p and D agree with the simulated loss breakdown in Fig. 15. (a) Thermal image when $V_{in} = 80$ V and $V_{out} = 12$ V, in which the loss breakdown predicts similar loss levels in L_p and D . (b) Thermal image when $V_{in} = 200$ V and $V_{out} = 12$ V, in which the loss breakdown predicts twice as much loss in L_p than in D .



(a)



(b)

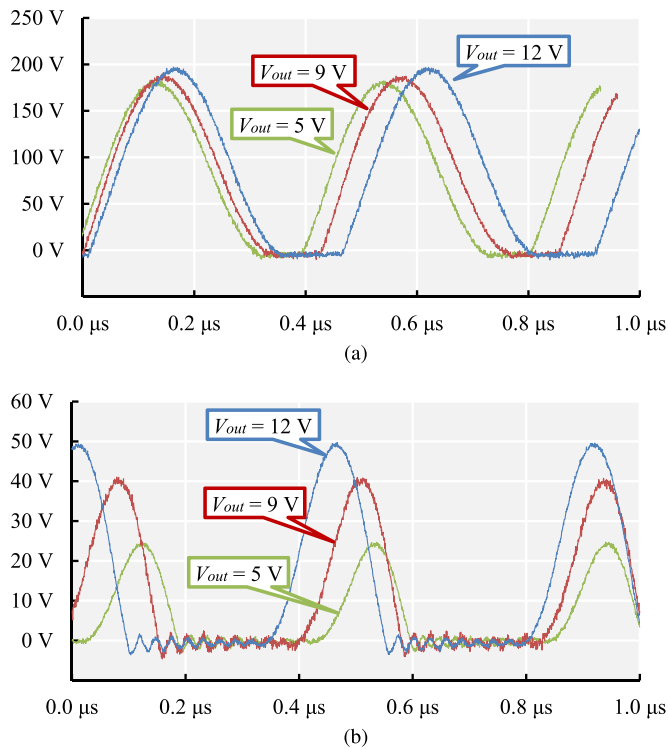
Fig. 17. Class-E dc-dc converter with synchronous rectification. (a) Schematic. (b) Implementation.

TABLE IV
 IMPLEMENTATION DETAILS OF THE CONVERTER IN FIG. 17

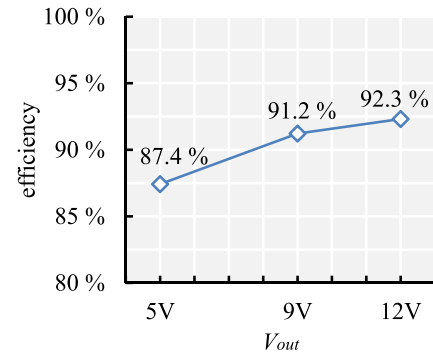
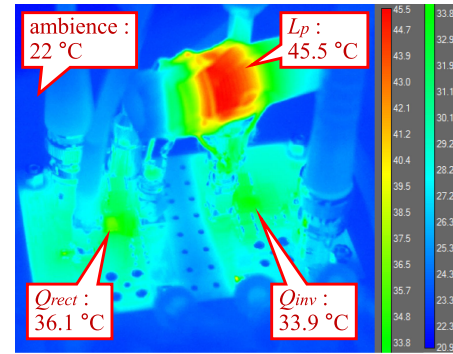
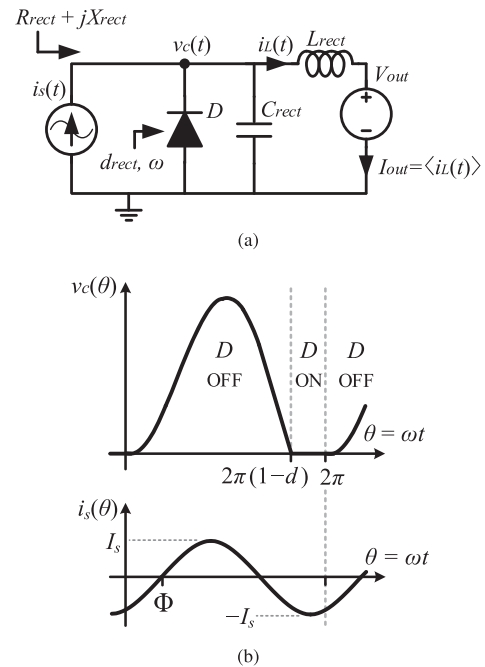
Parameter	Value	Description
C_{inv}	2 nF	CDE Mica capacitance
C_{rect}	5.4 nF	CDE Mica capacitance
L_p	2560 nH	675 × 48 AWG litz; air core
L_s	329 nH	675 × 48 AWG litz; air core
k	0.416	Air-core coupling
Q_{inv}	GS66502B	GaN transistor
Q_{rect}	EPC2033	GaN transistor
C_{in}	0.2 μF	X7R capacitance
C_{out}	0.3 μF	X7R capacitance
$C_{j,Q_{inv}}$	36 pF	Approximate nonlinear capacitance
$C_{j,Q_{rect}}$	720 pF	Approximate nonlinear capacitance

 TABLE V
 OPERATING CONDITIONS OF THE CONVERTER WITH SYNCHRONOUS RECTIFICATION WHEN $V_{in} = 80$ V AND $V_{out} = 5, 9, 12$ V

V_{out}	d_{inv}	d_{rect}	Frequency	I_{out}
5 V	0.20	0.60	2.44 MHz	2.62 A
9 V	0.22	0.55	2.34 MHz	2.80 A
12 V	0.25	0.52	2.20 MHz	2.24 A


 Fig. 18. Experimental waveforms of the voltage across the inverter- and the rectifier-side transistors when $V_{in} = 80$ V and $V_{out} = 5, 9, 12$ V. (a) Voltage across Q_{inv} . (b) Voltage across Q_{rect} .

assumed lossless. For L_p and L_s , we should model the resistance that increases with frequency due to dielectric losses and skin effect. We measure the resistance-versus-frequency curve of L_p and L_s and, then, construct an inductor model with an RL network (see Fig. 14) of which the resistance profile


 Fig. 19. Experimental results of the converter with synchronous rectification. (a) Thermal image that shows the reduced power loss in the rectifier-side switch when $V_{in} = 80$ V and $V_{out} = 12$ V. The image demonstrates a clear improvement when compared with Fig. 16(a). L_p shows a higher temperature because this converter processes higher power, namely 26.9 W versus 18.6 W in the output. (b) Efficiency of the converter with synchronous rectification. The peak efficiency is 92.3% when V_{out} is 12 V.

 Fig. 20. Class-E rectifier schematic and relevant waveforms for solution map derivations. (a) Rectifier schematic. (b) Waveforms of the capacitor voltage $v_c(t)$ and the sinusoidal input current $i_s(t)$ over one cycle of the periodic operation.

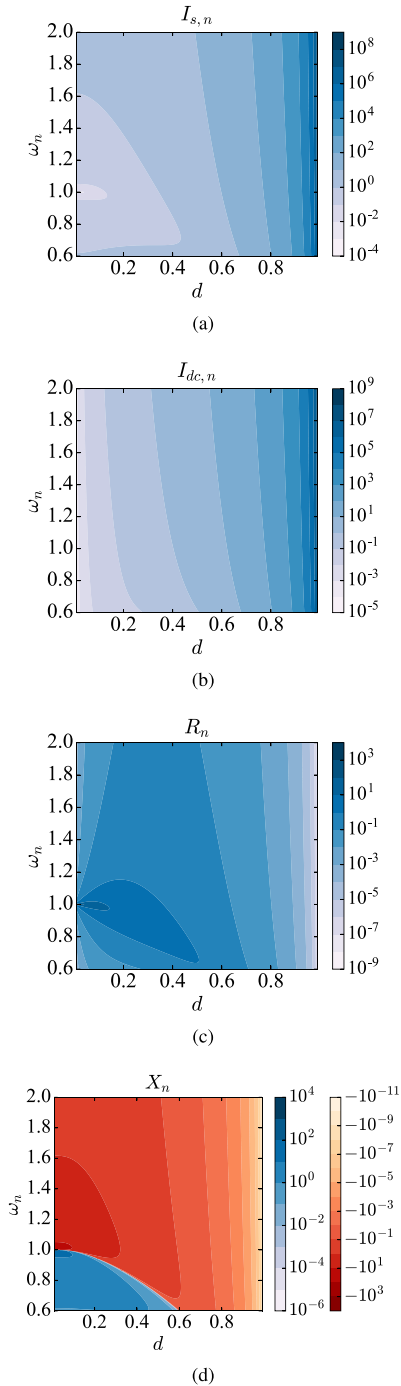


Fig. 21. General solution maps of a class-E topology derived in Appendix IV. The derivation follows a similar manner as that in previous works [17]–[19]. (a) Normalized sinusoidal ac current. Variables here are circuit parameters normalized by the dc voltage, resonant inductance, and capacitance. (b) Normalized dc current. (c) Equivalent resistance. (d) Equivalent reactance.

fits the measured curve. The constructed circuits emulate the frequency-dependent resistance within $\pm 15\%$ accuracy up to the third harmonic of the switching frequency and are used in place of L_p and L_s for the simulation. Duty cycles and switching frequencies for the simulation follow the experimental values in Fig. 9(b) and Fig. 8(b), respectively.

Fig. 15 shows the simulation results. Efficiency drops are mainly attributed to the loss in the primary transformer winding L_p and the diode D . L_p and D degrade the efficiency by as much as 12.6% and 9.3%, respectively, while other two components are not as significant in terms of their impact. Diode losses shows a tendency to increase only with V_{out} because most of the losses are caused by the diode forward voltage drop.

Thermal measurements in Fig. 16 agree with the simulated power loss breakdown in Fig. 15. Fig. 16(a) shows the thermal image when V_{in} is 80 V and V_{out} is 12 V, in which D is slightly hotter than L_p . When V_{in} changes to 200 V while V_{out} remains the same at 12 V, Fig. 16(b) shows L_p becoming noticeably hotter than D . This is in accordance with the simulated loss breakdown, in which L_p has a similar loss as D in the former case and twice as much loss than D in the latter case.

E. Synchronous Rectification

To eliminate the diode loss and improve the efficiency, we build a converter with synchronous rectification and compare it to the converter above. Fig. 17 shows the schematic and the implementation of the circuit. $C_{j,Q_{inv}}$ and $C_{j,Q_{rect}}$ denote the nonlinear junction capacitance of Q_{inv} and Q_{rect} , respectively. Table IV gives the implementation details. As in the previous section, the gate drive signal is provided by an external signal generator.

We fix V_{in} at 80 V and change V_{out} from 5 to 9 V and 12 V. When we modulate the frequency and duty cycles as in Table V, both the inverter- and the rectifier-side transistors achieve zero-voltage zero- dv/dt switching as can be seen in Fig. 18.

Fig. 19 verifies the effectiveness of synchronous rectification in reducing the rectifier loss and thereby boosting the efficiency. Thermal images in Fig. 19(a) demonstrate that the temperature of Q_{rect} is significantly reduced when compared with Fig. 16(a), and hence the power loss. The peak efficiency is 92.3% when V_{out} is 12 V.

IV. CONCLUSION

The duty cycle and frequency modulations presented here achieve zero-voltage zero- dv/dt switching in a class-E dc-dc converter to retain high efficiency under a wide range of input and output voltage conditions. The duty cycle, frequency, and the expected output current can be calculated by a few simple mathematical operations that use predetermined general solution maps. We built a prototype converter in a structure that uses a loosely coupled transformer for simplicity, isolation, and high efficiency. We suggested equivalent circuit transformation steps to design such a converter. Theoretically calculated duty cycle and frequency for soft switching matched well with the experimental data. We experimentally demonstrated the ON-OFF control scheme for output voltage regulation and suggested a concept schematic of the controller and the peripheral circuitry. We identified the transformer and the rectifier diode as a major contributor to the power loss and improved the performance by implementing synchronous rectification to achieve 92.3% peak efficiency.

APPENDIX A

DERIVATIONS OF GENERAL SOLUTION MAPS IN FIGS. 2 AND 3

This section derives general solution maps for a class-E topology as a function of two design variables, namely the normalized switching frequency ω_n and the switch duty cycle d . The derivation resembles those published in [17]–[19].

Consider a class-E rectifier [see Fig. 20(a)] of which the capacitor voltage $v_c(t)$ and the sinusoidal input current $i_s(t)$ follow periodic waveforms depicted in Fig. 20(b). We define parameters listed in as follows.

- 1) $d = d_{\text{rect}}, L = L_{\text{rect}}, C = C_{\text{rect}}$.
- 2) $\omega_n = \omega\sqrt{LC}$.
- 3) $\theta = \omega t$.
- 4) $I_{s,n} = I_s\sqrt{L/C}/V_{\text{out}}$.
- 5) $I_{dc,n} = I_{\text{out}}\sqrt{L/C}/V_{\text{out}}$.
- 6) $R_n = R_{\text{rect}}/\sqrt{L/C} = R_{\text{rect}} \cdot (I_s/V_{\text{out}})/I_{s,n}$.
- 7) $X_n = X_{\text{rect}}/\sqrt{L/C} = X_{\text{rect}} \cdot (I_s/V_{\text{out}})/I_{s,n}$.

Analytical equations for $i_s(t)$, $v_c(t)$, and the inductor current $i_L(t)$ are described as follows:

$$i_s(\theta) = I_s \sin(\theta - \Phi) \quad (1)$$

$$v_c(\theta) = \begin{cases} V_{\text{out}} \left(A \sin\left(\frac{\theta}{\omega_n} + \phi\right) + \left(\frac{I_{s,n}\omega_n}{1-\omega_n^2}\right) \cos(\theta - \Phi) + 1 \right) & \text{if } 0 < \theta \leq 2\pi(1-d) \\ 0, & \text{if } 2\pi(1-d) < \theta \leq 2\pi \end{cases} \quad (2)$$

$$i_L(\theta) = \begin{cases} \frac{V_{\text{out}}}{\sqrt{L/C}} \left(A \cos\left(\frac{\theta}{\omega_n} + \phi\right) + \frac{I_{s,n}}{1-\omega_n^2} \sin(\theta - \Phi) \right) & \text{if } 0 < \theta \leq 2\pi(1-d) \\ i_L(2\pi(1-d)) - \frac{V_{\text{out}}}{\omega L} (\theta - 2\pi(1-d)), & \text{if } 2\pi(1-d) < \theta \leq 2\pi \end{cases} \quad (3)$$

where L , C , and V_{out} are given constants, ω_n and d are variables, and A , ϕ , $I_{s,n}$, and Φ are unknowns. We need four conditions in order to determine four unknowns. The first condition to be met is the zero-voltage turn-OFF

$$v_c(0) = 0. \quad (4)$$

The second and third are from the zero- dv/dt turn-OFF

$$i_s(0) = i_L(0) \quad (5)$$

$$i_s(2\pi) = i_L(2\pi). \quad (6)$$

The last condition is from the zero-voltage turn-ON

$$v_c(2\pi(1-d)) = 0. \quad (7)$$

We use (4)–(7) to analytically solve for unknowns in (1)–(3). Plotting $I_{s,n}$, one of four unknowns, as a function of ω_n and d yields the general solution map in Fig. 21(a). Calculating the time average of $i_L(\theta)$ as described in (6) and plotting it gives us the map in Fig. 21(b).

We find R_n and X_n by calculating the fundamental Fourier coefficient $v_c(\theta)$ and dividing it by that of $i_s(\theta)$ as shown in the

following:

$$\tilde{v}_{c,1} = \frac{1}{2\pi} \int_0^{2\pi} v_c(\theta) e^{-j\theta} d\theta = V_{\text{out}} f \quad (8)$$

$$\tilde{i}_{s,1} = I_s e^{-j\Phi} \quad (9)$$

$$R_n + jX_n = \left(\frac{1}{\sqrt{L/C}} \right) \frac{\tilde{v}_{c,1}}{\tilde{i}_{s,1}} = \left(\frac{I_s/V_{\text{out}}}{I_{s,n}} \right) \frac{\tilde{v}_{c,1}}{\tilde{i}_{s,1}} = \frac{f}{I_{s,n}} e^{-j\Phi} \quad (10)$$

in which f , $I_{s,n}$, and Φ are all functions of ω_n and d . Plugging (2) into (8) and performing the calculation in (10), we obtain the plots in Fig. 21(c) and (d).

Fig. 21(a) reveals that designating the value of $I_{s,n}$ and ω_n is enough to uniquely determine every different point on the (d, ω_n) plane. We use this property to reconstruct Fig. 21(a) as a function of $I_{s,n}$ and ω_n and thereby obtain Fig. 2(c). Using $I_{s,n}$ values that correspond to each (d, ω_n) points in Fig. 21(a), we rearrange the solution fields of Fig. 21 onto the new mapping with respect to $I_{s,n}$ and ω_n , thereby obtaining plots in Figs. 2 and 3.

For a class-E inverter [see Fig. 1(b)], same equations and derivation process apply when we use the following parameter definitions instead.

- 1) $d = d_{\text{inv}}, L = L_{\text{inv}}, C = C_{\text{inv}}$.
- 2) $I_{s,n} = I_s\sqrt{L/C}/V_{\text{in}}$.
- 3) $I_{dc,n} = I_{\text{in}}\sqrt{L/C}/V_{\text{in}}$.
- 4) $R_n = R_{\text{load}}/\sqrt{L_{\text{inv}}/C_{\text{inv}}}$.
- 5) $X_n = -X_{\text{load}}/\sqrt{L_{\text{inv}}/C_{\text{inv}}}$.

The sign of X_n is changed to negative and all the voltage and current waveforms are flipped horizontally because the inverter operation is time reversal of the rectifier operation [21], [22].

APPENDIX B

PYTHON CODE THAT CALCULATES GENERAL SOLUTION MAPS OF A CLASS-E TOPOLOGY

```
import numpy as np
from numpy import sin, cos, pi, sqrt
import matplotlib.pyplot as plt
from matplotlib import ticker, cm

##### class-E rectifier solution #####

numstep_d = 100
numstep_wn = 100

d_linsp = np.linspace(.01, .99, numstep_d)
wn_linsp = np.linspace(.6, 2., numstep_wn)

wn, d = np.meshgrid(wn_linsp, d_linsp)
theta = (1 - d) * 2*pi
tau1 = theta / wn

ww0 = 1 / (1 - wn**2)
ww1 = wn*ww0
ww2 = wn*ww1
```

```

cos_tau1 = cos(tau1)
sin_tau1 = sin(tau1)
cos_theta = cos(theta)
sin_theta = sin(theta)

X1 = ww1*sin_theta - ww2*sin_tau1
X2 = 1 - cos_tau1
X3 = ww1*(cos_tau1 - cos_theta)

Y1 = ww2*cos_tau1 - ww0*cos_theta + 1
Y2 = tau1 - 2*pi/wn - sin_tau1
Y3 = ww1*sin_tau1 - ww0*sin_theta

B1 = ((Y2/Y1-X2/X1)/(X3/X1-Y3/Y1))
B2 = ((X2/X3-Y2/Y3)/(X1/X3-Y1/Y3))

A1 = -ww2*B2
A2 = 1 - ww1*B1

PHI = np.arctan2(B2, B1)
PHI = PHI - (PHI > 0).astype(int) * (2*pi)

#### values obtained in a closed form ####

Is_hpp_n = sqrt(B1**2 + B2**2)
Is_rms_n = Is_hpp_n/sqrt(2)
IL_avg_n = ((1/2/pi*(B1*(cos_theta-1)+
    B2*sin_theta)-(-A1*cos_tau1+
    A2*sin_tau1+ww0*(B1*sin_theta-
    B2*cos_theta)-tau1)*(1-
    theta/2/pi)-1/2*(2*pi/wn-
    (wn/2/pi)*tau1**2)))

Rrect_n = 1/Is_rms_n**2
C_n = wn/IL_avg_n
L_n = wn*IL_avg_n

##### Xrect_n #####

a1n = (2*A1*wn**2*sin(tau1)*sin(tau1*wn)/
    (2*wn**3-2*wn)+2*A1*wn*cos(tau1)*
    cos(tau1*wn)/(2*wn**3-2*wn)-2*A1*
    wn/(2*wn**3-2*wn)+2*A2*wn**2*sin(
    tau1*wn)*cos(tau1)/(2*wn**3-2*wn)-
    2*A2*wn*sin(tau1)*cos(tau1*wn)/(2*
    wn**3-2*wn)+B1*taul*wn**3*ww1*sin(
    tau1*wn)**2/(2*wn**3-2*wn)+B1*taul*
    wn**3*ww1*cos(tau1*wn)**2/(2*wn**3-
    2*wn)-B1*taul*wn*ww1*sin(tau1*wn)**
    2/(2*wn**3-2*wn)-B1*taul*wn*ww1*
    cos(tau1*wn)**2/(2*wn**3-2*wn)+B1*
    wn**2*ww1*sin(tau1*wn)*cos(tau1*
    wn)/(2*wn**3-2*wn)-B1*ww1*sin(tau1*
    wn)*cos(tau1*wn)/(2*wn**3-2*wn)-B2*
    wn**2*ww1*cos(tau1*wn)**2/(2*wn**3-
    2*wn)+B2*wn**2*ww1/(2*wn**3-2*wn)+
    B2*ww1*cos(tau1*wn)**2/(2*wn**3-2*
    wn)-B2*ww1/(2*wn**3-2*wn)-sin(tau1*
    wn)/wn)

b1n = (-2*A1*wn**2*sin(tau1)*cos(tau1*wn)/
    (2*wn**3-2*wn)+2*A1*wn*sin(tau1*
    wn)*cos(tau1)/(2*wn**3-2*wn)-2*A2*
    wn**2*cos(tau1)*cos(tau1*wn)/(2*
    wn**3-2*wn)+2*A2*wn**2/(2*wn**3-2*
    wn)-2*A2*wn*sin(tau1)*sin(tau1*wn)/
    (2*wn**3-2*wn)-B1*wn**2*ww1*
    cos(tau1*wn)**2/(2*wn**3-2*wn)+B1*
    wn**2*ww1/(2*wn**3-2*wn)+B1*ww1*
    cos(tau1*wn)**2/(2*wn**3-2*wn)-B1*
    ww1/(2*wn**3-2*wn)+B2*taul*wn**3*
    ww1*sin(tau1*wn)**2/(2*wn**3-2*wn)+
    B2*taul*wn**3*ww1*cos(tau1*wn)**2/
    (2*wn**3-2*wn)-B2*taul*wn*ww1*sin
    (tau1*wn)**2/(2*wn**3-2*wn)-B2*taul*
    wn*ww1*cos(tau1*wn)**2/(2*wn**3-2*
    wn)-B2*wn**2*ww1*sin(tau1*wn)*cos
    (tau1*wn)/(2*wn**3-2*wn)+B2*ww1*sin
    (tau1*wn)*cos(tau1*wn)/(2*wn**3-2*
    wn)+(cos(tau1*wn)-1)/wn)

PHIv = np.arctan2(a1n,b1n)
PHIv = PHIv + (PHIv < 0).astype(int)*2*pi

argZin = PHIv + PHI
argZin = (argZin +
    (argZin < -pi).astype(int)*2*pi)
argZin = (argZin -
    (argZin > pi).astype(int)*2*pi)
Xrect_n = Rrect_n * np.tan(argZin)
Xload_n = -Xrect_n

##### Plots #####

def fmt(x, pos):
    a, b = ':.2e'.format(x).split('e')
    b = int(b)
    return r'10'+str(b)+r''

def fmt_neg(x, pos):
    a, b = ':.2e'.format(x).split('e')
    b = int(b)
    return r'-10'+str(b)+r''

plt.figure()
plt.xscale('log')
plt.contourf(Is_hpp_n, wn,
    Rrect_n*IL_avg_n,
    locator=ticker.LogLocator(),
    cmap=cm.PuBu)

plt.colorbar()
plt.title('Fig. 2a')
plt.show()

plt.figure()
plt.xscale('log')

```

```

plt.contourf(Is_hpp_n, wn,
             -Xrect_n*IL_avg_n,
             locator=ticker.LogLocator(),
             cmap=cm.OrRd)
clb = plt.colorbar(
    format=plt.FuncFormatter(fmt_neg))
plt.contourf(Is_hpp_n, wn, Xrect_n*IL_avg_n,
             locator=ticker.LogLocator(),
             cmap=cm.PuBu)
plt.colorbar(
    format=plt.FuncFormatter(fmt_neg))
plt.title('Fig. 2b')
plt.show()

plt.figure()
plt.xscale('log')
plt.contourf(Is_hpp_n, wn, d, cmap=cm.PuBu)
plt.colorbar()
plt.title('Fig. 2c')
plt.show()

plt.figure()
plt.xscale('log')
plt.contourf(Is_hpp_n, wn,
             IL_avg_n,
             locator=ticker.LogLocator(),
             cmap=cm.PuBu)
plt.colorbar()
plt.title('Fig. 3')
plt.show()

plt.figure()
plt.contourf(d, wn, Is_hpp_n,
             locator=ticker.LogLocator(),
             cmap=cm.PuBu)
plt.colorbar()
plt.title('Fig. 21a')
plt.show()

plt.figure()
plt.contourf(d, wn, IL_avg_n,
             locator=ticker.LogLocator(),
             cmap=cm.PuBu)
plt.colorbar()
plt.title('Fig. 21b')
plt.show()

plt.figure()
plt.contourf(d, wn, Rrect_n*IL_avg_n,
             locator=ticker.LogLocator(),
             cmap=cm.PuBu)
plt.colorbar()
plt.title('Fig. 21c')
plt.show()

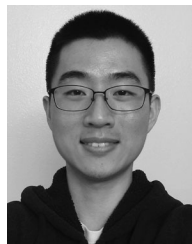
plt.figure()
plt.contourf(d, wn, -Xrect_n*IL_avg_n,
             locator=ticker.LogLocator(),
             cmap=cm.OrRd)
clb = plt.colorbar(
    format=plt.FuncFormatter(fmt_neg))
clb.ax.invert_yaxis()
plt.contourf(d, wn, Xrect_n*IL_avg_n,
             locator=ticker.LogLocator(),
             cmap=cm.PuBu)
plt.colorbar(
    format=plt.FuncFormatter(fmt_neg))
plt.title('Fig. 21d')
plt.show()

```

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