Direct Single-Phase AC–AC Converters Based on Series Impedance Networks

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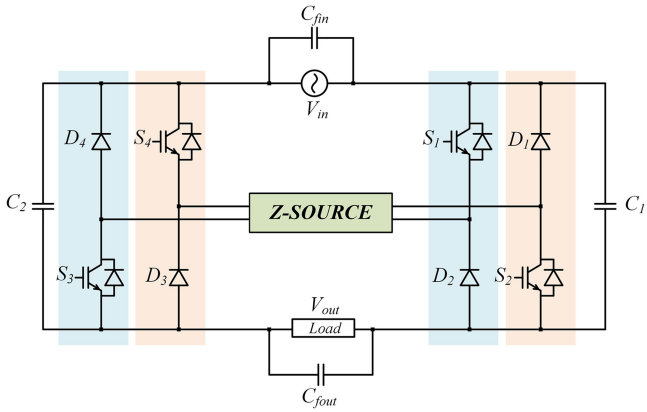
***Abstract*—In this paper, a novel direct ac–ac converter based on the coupled inductor Z-source networks is proposed that offers a wide range of buck–boost operation. A total of two Z-source networks, called the coupled switched inductor and the modified switched coupled inductor, are employed that enable the ac–ac converter to deliver a wide voltage range. The proposed converter with both networks provides free-wheeling current paths for the inductors currents during the state transitions, which results in solving the commutation problems and the need for snubber circuits. A simple switching strategy is then proposed that helps to share a common magnetic core between the coupled inductors. For any particular voltage gain, the proposed structures require a smaller duty cycle compared to the conventional ones; therefore, a smaller inductance is required. Simulation and experimental results are provided to confirm the theoretical achievements.**

***Index Terms*—AC–AC converter, single phase, Z-source impedance network.**



I. Introduction

STATIC ac voltage regulators are commonly utilized in some industrial applications, including dynamic voltage regulators (DVRs), induction machine adjustable speed drives, light dimming circuits, and electric heaters. Among different voltage regulator circuits, the pulsewidth-modulated (PWM) ac choppers have already attracted a lot of attention mainly due to their simple structure, high efficiency, small size, and improved power quality [1]–[7].

On the other hand, one of the recent advances in the power electronics is the introduction of Z-source impedance networks [8]. Different topologies for these networks are already proposed, which are successfully applied to dc–ac [9]–[18], dc–dc [19]–[24], and ac–ac converters [25]–[30] that all offer very high voltage conversion gains. The most recent successful implementation of an ac–ac converter is reported in [31], which solves the shoot-through and dead-time problems and operates with a simple PWM control. Lately, the performance of the Z-source impedance networks has significantly improved by employing the coupled inductors in their structures that leads to higher conversion gains with lower shoot-through durations.

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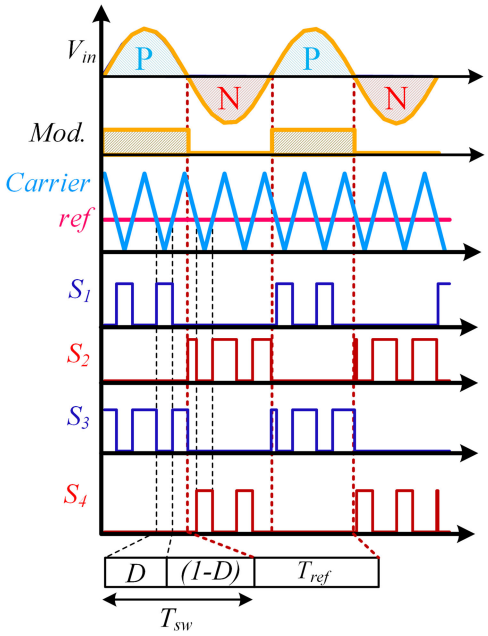

Fig. 2. Proposed PWM scheme.

common circuit. So, the magnetic circuit, as a major part of the proposed converter, has the main advantages of reduced number of magnetic cores and a simple structure.

The paper is organized as follows. Section II describes the proposed topologies and the switching algorithm. Section III discusses the design of the converter parameters. Experimental results illustrating the performance of the converters are presented in Section IV. Section V presents the comparative analysis and Section VI concludes the paper.

II. Proposed Topology and Control Algorithm

Fig. 1 shows the proposed topology, in which the circuits on the right and left sides of the Z-source impedance network, positive and negative legs, are basically double-ended forward choppers. The impedance network is a combination of capacitors, inductors, and semiconductors. The proposed switching strategy and the impedance network circuits are explained in the following sections.

A. Switching Strategy

Fig. 2 shows the proposed switching scheme, in which the gating signals are generated by a conventional carrier-based PWM method. The switching operation requires a modulating signal ("Mod." in Fig. 2) that distinguishes the positive and negative half-cycles of the input voltage, when either the switch pairs (S_1, S_3) or (S_2, S_4) are active. Also, during each half-cycle, the two active switches are turned ON and OFF complementary that even more simplifies the modulation scheme. As a result, two operation modes for each positive and negative half-cycles are possible, which are shown in Fig. 3(a)–(d). In mode I [referring to Fig. 3(a) and (c)], the capacitors C_1 and C_2 provide the output current path, while in mode II [referring to Fig. 3(b) and (d)], the input current flows through them.

The conducting semiconductors during each state are only one IGBT and a diode, which reduces the losses. In addition, this strategy separates the proposed converter into two unidirectional circuits for positive and negative half-cycles.

B. Proposed Impedance Network Circuits

According to the possibility of unidirectional operation of the proposed converter, series impedance network circuits can be used for the Z-source block in Fig. 1. Employing the series Z-source networks offers a wide range of possible output to input voltage gains. In this work, two series Z-source networks are used, hereafter called the coupled switched inductor (CSL) of [11] and the proposed modified switched coupled inductor (MSCL) structures. The configurations of the proposed converters with the CSL and the MSCL are shown in Fig. 4(a) and (b), respectively. For the proposed converters, the principles of operations in both positive and negative half-cycles are the same. Thus, for the sake of simplicity, only the negative cell (with yellow background in Fig. 4) is analyzed in the following.

1) CSL Structure: As can be seen in Fig. 4(a), each positive and negative cell of this structure includes three diodes and two coupled inductors. The turn numbers of both windings are the same ($N_1 = N_2$). Employing the coupled inductors helps reduce the volume and size of the magnetic components. During both negative and positive half-cycles of the input voltage, two distinct operation states can be recognized described as follows.

a) Mode I: Figs. 3(c) and 5(a) show the current paths through the main converter and the CSL negative cell, respectively. According to Fig. 5(a), the diodes D_{z1} and D_{z2} conduct and the source charges the coupled inductors, while D_{z3} is reverse-biased and does not conduct. The voltages across the inductors can be obtained as

$$V_{N_1} = V_{N_2} = V_{\text{in}}. \tag{1}$$

b) Mode II: Figs. 3(d) and 5(b) show the current paths of the main converter and the CSL negative cell, respectively. As shown in Fig. 5(b), the diodes D_{z1} and D_{z2} are reverse-biased and the coupled inductors are connected in series and discharge through D_{z3}. The following KVL holds:

$$V_{N_1} + V_{N_2} = V_{\text{out}}. \tag{2}$$

Applying the volt-second balance to (1) and (2) results in the voltage gain equation given as follows, in which D is the duty cycle of the charging switches (S_1 for positive and S_4 for negative half-cycles)

$$V_{\text{out}} = \frac{2D}{1-D} V_{\text{in}}. \tag{3}$$

2) MSCL Structure: Each cell of the MSCL structure comprises three coupled inductors, two diodes, and a capacitor. The turn numbers N_1 and N_2 are equal, while N_3 is different and $n = N_3/N_1$. Similar to the CSL, two operation modes can be recognized for the MSCL structure.

a) Mode I: Based on Figs. 3(c) and 5(c), the MSCL diodes D_{z1} and D_{z2} conduct and the source charges the coupled

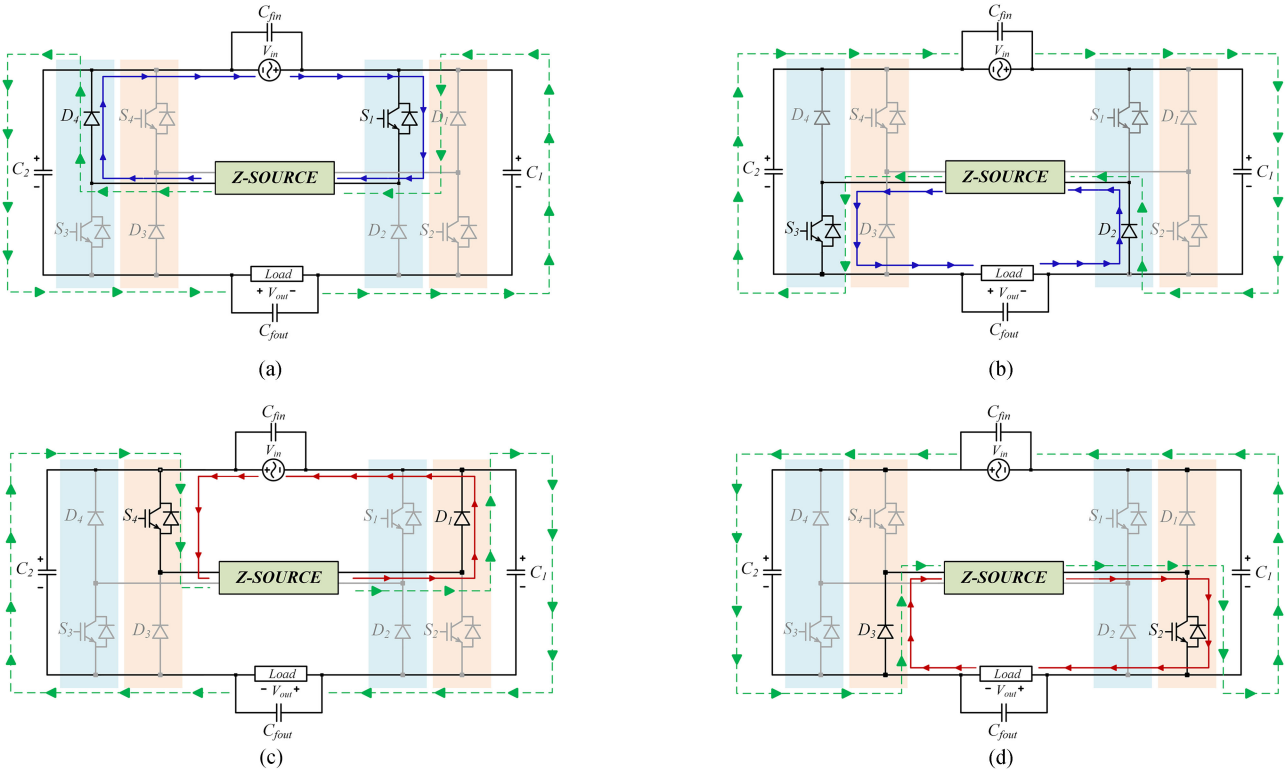

Fig. 3. Operation modes (a) I and (b) II during the positive half-cycle, and (c) I and (d) II during the negative half-cycle.

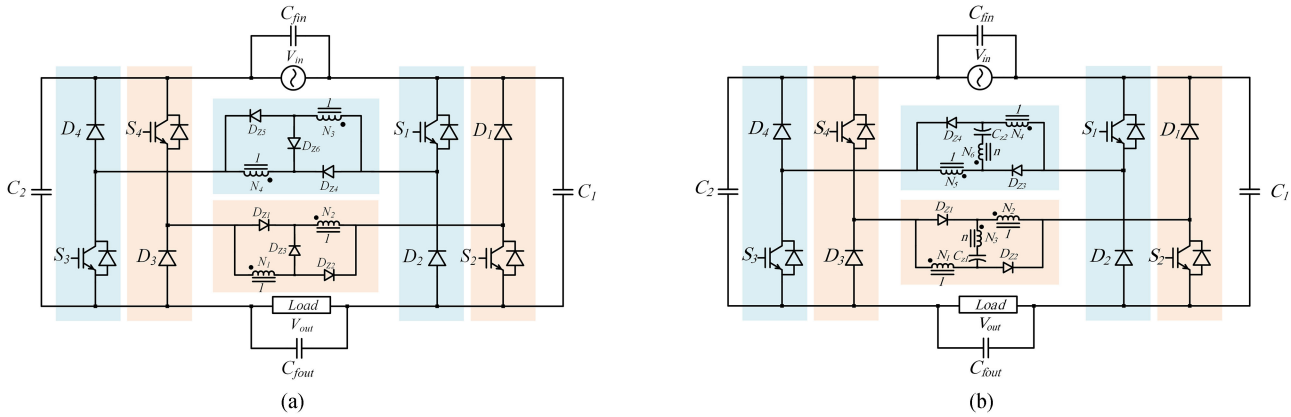

Fig. 4. Proposed converters with (a) CSL and (b) MSCL Z-source networks.

inductors. Furthermore, C_{z1} is also charged due to the coupling among N_1, N_2, and N_3. Voltage equations are obtained as follows:

$$V_{N_1} = V_{N_2} = V_{\text{in}} \tag{4}$$

$$V_{N3} = nV_{N_1} = nV_{N_2} \tag{5}$$

$$V_{C_{Z1}} = (1-n)\,V_{\text{in}}. \tag{6}$$

b) Mode II: Based on Figs. 3(d) and 5(d), the diodes D_{z1} and D_{z2} are reverse-biased and the coupled inductors and C_{z1} are all connected in series and discharge. Voltage equations are obtained as follows:

$$V_{N_1} + V_{N_2} - V_{N_3} + V_{C_{Z1}} = V_{\text{out}} \tag{7}$$

$$V_{N_3} = nV_{N_1}, \quad V_{N_1} = V_{N_2} \tag{8}$$

$$V_{N_1} = V_{N_2} = \frac{V_{\text{out}} - (1-n)\,V_{\text{in}}}{(2-n)}. \tag{9}$$

Finally, from the volt-second balance, the voltage gain can be obtained as follows from (4) and (9):

$$V_{\text{out}} = \frac{1-n+D}{1-D} V_{\text{in}}. \tag{10}$$

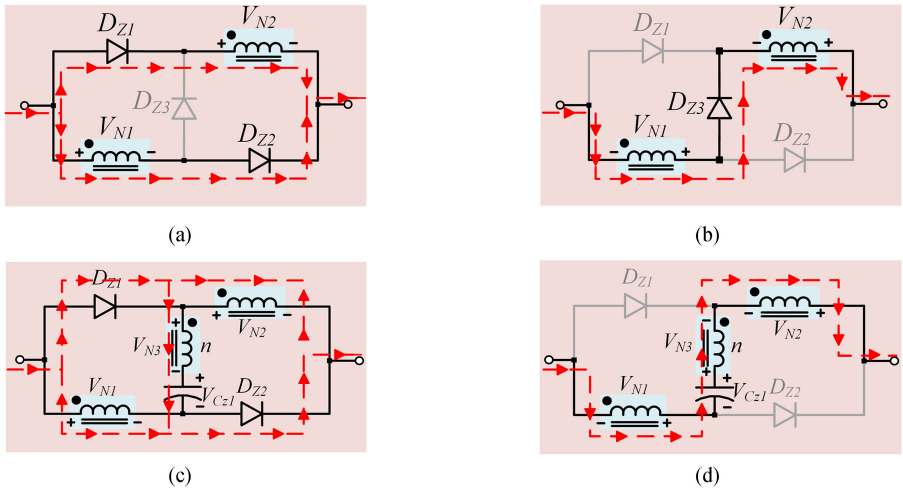

Fig. 5. Current paths of negative cells. (a) Mode I and (b) mode II of the CSL. (c) Mode I and (d) mode II of the MSCL.

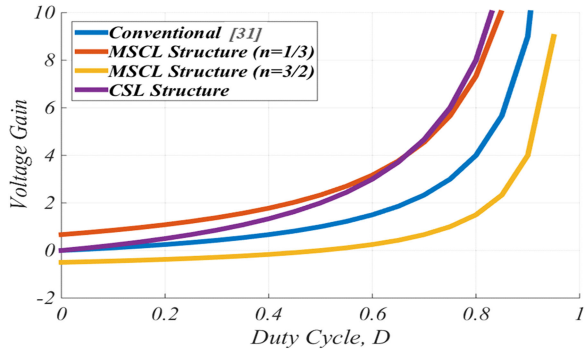

Fig. 6. Voltage gain versus duty cycle for the proposed Z-source networks and the conventional buck–boost ac chopper.

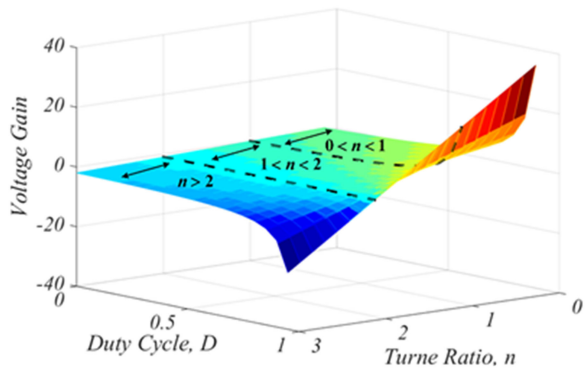

Fig. 7. Voltage gain versus duty cycle and turn ratio for the MSCL.

Fig. 6 compares the voltage gain ability for the series Z-source networks, based on the results presented in (3) and (10). As can be seen, both proposed structures have the buck–boost ability. In addition, for the reference of comparison, the gain plot of the conventional buck–boost ac–ac converter of [31] is also plotted.

Based on (3) and its plot in Fig. 6, the CSL structure provides voltage gains twice the conventional buck–boost structure for the same duty cycle. In other words, for the same voltage gain, the CSL requires a lower duty cycle compared to the conventional converter. As a result, the charging interval and consequently the current ripple of inductors decrease significantly, resulting in a smaller magnetic core size and lower losses.

According to (10), the voltage gain of the MSCL depends on the turn ratio n as well as the duty cycle, which offers a high degree of freedom in the voltage gain equation, presented in Fig. 7. The voltage gain curves in Fig. 6 are already plotted for $n = 1/3$ and $3/2$. In general, the MSCL can offer the same advantages as the CSL with more flexibility to satisfy the design compromise through proper selection of n. As an advantage, by choosing the turn ratio in the range $1 < n < 2$, the high gain buck operation can also be achieved.

III. Parameter Design of the Proposed Converter

A. Magnetic Design

As mentioned in Section II, the proposed switching strategy makes it possible for the main converter to independently operate in each half-cycle. For example, in the positive half-cycle, just the positive cell operates, while the negative cell is out of work. Consequently, the magnetic circuit of the negative cell is not in use during the positive half-cycle. This means that the windings of positive and negative cells can share a common magnetic core, as depicted in Fig. 8. This method is called the together cell winding from now on. Despite having this advantage, a volume and size optimization of the magnetic cores is required for the proposed converters, which follows. The core size of a set of coupled inductors can be determined from the geometrical constant (K_g) presented as [32]

$$K_g = \frac{A_c^2 W_A}{(MLT)} \geq \frac{\rho L_m^2 I_{\text{tot}}^2 I_{m-\max}^2}{B_{\max}^2 R K_u}. \tag{11}$$

In (11), A_c, W_A, and MLT are the core cross-sectional area, the winding area, and the mean length per turn, respectively. Also, ρ is the copper resistivity, L_m is the required magnetizing inductance, I_{tot} is the total rms of the windings currents referred

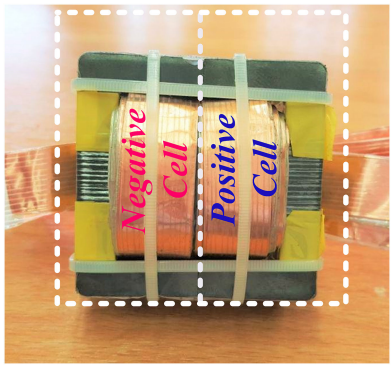

Fig. 8. Coupled inductors on a common EE core.

to the primary, $I_{m-\max}$ is the peak magnetizing current, $B_{\max}$ is the core maximum flux density, R is the primary winding resistance, and K_u is the winding fill factor. The right-hand side of (11) represents the electrical characteristics of the magnetic element, while the left-hand side shows the core size parameter. The left-hand side of (11) must always be larger than or equal to the right-hand side, thus avoiding the core from saturation.

The CSL and the MSCL structures have two operation modes (refer to Fig. 5) where their windings currents are the sum of input and output currents in both I and II modes, as shown in Fig. 3. It can be readily shown that the peak magnetizing currents of the CSL and the MSCL are, respectively, as follows:

$$I_{m-\max(\mathrm{CLS})} = 2\sqrt{2}\left(\frac{1}{1-D}\right) I_{\mathrm{out}-(\mathrm{rms})} \tag{12}$$

$$\mathrm{I}_{m-\max(\mathrm{MSCL})} = \sqrt{2}\left(\frac{2-n}{1-D}\right) I_{\mathrm{out}-(\mathrm{rms})}. \tag{13}$$

It is important to note that for the same number of turns, the cell-winding method (separate or together) does not affect the total rms current (I_{tot}) for the rated power and the specified gain. Consequently, the core geometrical constant (K_g) has the same value for either separate or together cell winding, then the same core size can be used for the together cell-winding method as the separate method while requiring only one core instead of two. Therefore, as shown in Fig. 8, both positive and negative cell windings are wound on the middle leg of one EE ferrite core.

Assuming the magnetizing current ripple $x\%$ of (12) and (13) for the CSL and the MSCL, respectively, then the magnetizing inductances can be calculated from the following equations:

$$L_{m\_\mathrm{CSL}} = \frac{(1-D)^2}{4} \times L_{m\_\mathrm{base}} \tag{14}$$

$$L_{m\_\mathrm{MSCL}} = \frac{D(1-D)^2}{(2-n)(1-n+D)} \times L_{m\_\mathrm{base}} \tag{15}$$

$$L_{m\_\mathrm{base}} = \frac{V^2_{\mathrm{out}-(\mathrm{rms})}}{x\%P_{\mathrm{out}} f_{\mathrm{sw}}}. \tag{16}$$

The variations of the magnetizing inductances in terms of duty cycle are presented in Fig. 9. The magnetizing inductances are in per-unit, based on (16). Evidently, for the duty cycles above 0.2, the conventional structure requires the largest L_m compared to the proposed ones. For high duty cycles, the CSL and the MSCL structures require almost the same L_m but for low duty cycles, the MSCL magnetizing inductance demand is much lower than the CSL to achieve an equal I_m ripple current. On the other hand, for the MSCL, with decreasing turn ratio (n), the magnetizing inductance requirement reduces.

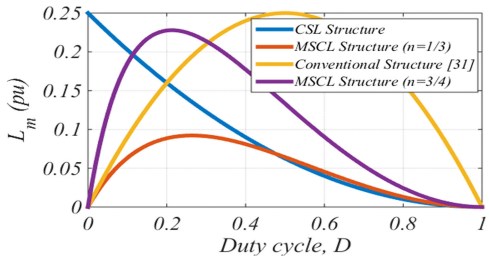

Fig. 9. Per-unit of magnetizing inductance versus duty cycle.

B. Capacitor Design

The capacitors are designed from (17) with the capacitor voltage ripple assumed as the design constraint. By considering $y\%$ as the percent of tolerable capacitor voltage ripple, the capacitor can be designed as

$$C_1 = C_2 = \frac{I_{\mathrm{out}}}{y\%V_{C_{1/2}}} DT_s \tag{17}$$

where I_{out} is the peak output current. Replacing for the capacitor voltages and the output peak currents for both structures (CSL and MSCL) in (17) results in

$$\begin{cases} C_1^{\mathrm{MSCL}} = C_2^{\mathrm{MSCL}} = \frac{D(1-n+D)}{((1-n)(3+D)-n^2)} \times C_b \\ C_1^{\mathrm{CSL}} = C_2^{\mathrm{CSL}} = \frac{2D^2(1+D)}{(9D^2+1)} \times C_b \\ C_b = \frac{P_{\mathrm{out}}}{y\% f_{\mathrm{sw}} V^2_{\mathrm{out}-(\mathrm{rms})}}. \end{cases} \tag{18}$$

Rewriting (17) for the MSCL-cell capacitors gives

$$C_{z1,2} = \frac{I^I_{N3}}{x\%V_{Cz1,2}} DT_s. \tag{19}$$

By substituting I^I_{N3} and $V_{Cz1,2}$ into (19) and performing some manipulations, then the following equation is obtained for the capacitors $C_{z1,2}$ as a design constraint

$$C_{z1,2} = \frac{1}{(1-n)}\left(\frac{1-D}{1-n+D}\right)^3 \times C_b. \tag{20}$$

C. Voltage Rating of Semiconductors

1) IGBTs: The blocking voltages of different IGBTs are provided in (21) and (22) for S_1 and S_4 and (23) and (24) for S_2

TABLE I
EXPERIMENTAL PARAMETERS

Description		Values
Input Voltage		110 V_{rms}/60 Hz
Output Gain:	CSL (Buck, Boost)	Buck: 0.63 , Boost: 1.6
	MSCL (Buck, Boost)	Buck: 0.85 , Boost: 1.8
Output Power		500 W
Load Resistance		10-80 Ω
Switching Frequency		30 kHz
Input & Output Filter Capacitors (C_{fin}, C_{fout})		2.2 μF , 4.4 μF
Converter Capacitors (C_1 , C_2)		6.8 μF
Magnetizing Inductance (L_m)		100 μH
MSCL Winding (N_1:N_2:N_3)		(15:15:5) ;for each cell
MSCL Capacitor ($C_{Z1,2}$)		2.2 μF

and S_3 for the CSL and the MSCL structures

$$V_{\text{stress }S_1,S_4\,(\text{CSL})} = \frac{\sqrt{2}\left(9D^2+1\right)V_{\text{out}-(\text{rms})}}{2D\left(1+D\right)} \tag{21}$$

$$V_{\text{stress }S_1,S_4\,(\text{MSCL})} = \frac{\sqrt{2}\left((1-n)\left(3+D\right)-n^2\right)V_{\text{out}-(\text{rms})}}{1-n+D} \tag{22}$$

$$V_{\text{stress }S_2,S_3\,(\text{CSL})} = \frac{\sqrt{2}\left(7D^2+1\right)V_{\text{out}-(\text{rms})}}{2D\left(1+D\right)} \tag{23}$$

$$V_{\text{stress }S_2,S_3\,(\text{MSCL})} = \frac{\sqrt{2}\left(5+D-3n\right)V_{\text{out}-(\text{rms})}}{2\left(1-n+D\right)}. \tag{24}$$

2) Diodes: The blocking voltages of the main converter diodes are given as follows:

$$V_{\text{stress }D_1,D_4\,(\text{CSL})} = \frac{\sqrt{2}\left(7D^2+1\right)V_{\text{out}-(\text{rms})}}{2D\left(1+D\right)} \tag{25}$$

$$V_{\text{stress }D_1,D_4\,(\text{MSCL})} = \frac{\sqrt{2}\left(5+D-3n\right)V_{\text{out}-(\text{rms})}}{2\left(1-n+D\right)} \tag{26}$$

$$V_{\text{stress }D_2,D_3\,(\text{CSL})} = \frac{\sqrt{2}\left(9D^2+1\right)V_{\text{out}-(\text{rms})}}{2D\left(1+D\right)} \tag{27}$$

$$V_{\text{stress }D_2,D_3\,(\text{MSCL})} = \frac{\sqrt{2}\left((1-n)\left(3+D\right)-n^2\right)V_{\text{out}-(\text{rms})}}{1-n+D}. \tag{28}$$

The Z-source diodes block the peak voltages as follows:

$$V_{\text{stress }DZ_1,DZ_2\,(\text{CSL})} = \frac{\sqrt{2}D}{1-D}V_{\text{in}-(\text{rms})} \tag{29}$$

$$V_{\text{stress }DZ_3\,(\text{CSL})} = \sqrt{2}\,V_{\text{in}-(\text{rms})} \tag{30}$$

$$V_{\text{stress }DZ_1,DZ_2\,(\text{MSCL})} = \frac{\sqrt{2}\left(1-n\right)}{1-D}V_{\text{in}-(\text{rms})}. \tag{31}$$

IV. EXPERIMENTAL RESULTS

Both proposed converters with the parameters summarized in Table I are implemented in the laboratory. A microcontroller, STM32F407VG from STMicroelectronics, generates the gating signals. The converters sense the input voltage for zero crossing detection. The modulated switching signals of both negative and positive half-cycles are shown in Fig. 10. As already stated, the switching strategy is very simple: S_1, S_3 in the positive half-cycle and S_2, S_4 in the negative half-cycle are controlled in the form of complementary. Figs. 11 and 12 show the operation of the CSL in the buck and boost modes, respectively. Input and output voltages and currents in the buck mode are plotted in Fig. 11(a) in which the input voltage is 110 V(rms) and by choosing $D = 0.24$, then the output voltage is decreased to 63 V(rms). The theoretical output voltage is calculated from (3) to be 69.3 V(rms), which well supports the experimental results. The winding current (I_{N1}) and the voltages across the CSL cell diodes (D_{z1}, D_{z2}, D_{z3}) are plotted in Fig. 11(b) from top to bottom. The voltage stresses on the positive cell diodes are determined by the operation of the negative cell and vice versa. In other words, during the nonoperation period of each cell, a blocking voltage appears across its diodes due to the coupling between the negative and the positive cells, which is shown in Fig. 11(b). The magnetizing current and the voltages across the negative and the positive charging switches (S_1 and S_4) are presented in Fig. 11(c). The magnetizing current is a rectified sinusoidal wave and its ripple frequency is as twice as each winding current. The same results for the boost mode of the CSL are shown in Fig. 12, where $D = 0.444$ and V_{out} is calculated from (3) to be 176 V(rms), which in practice is 161 V(rms) that is in close agreement with the theoretical results. The winding current ($I_{L1} = I_{N1}$) and voltage stresses of the CSL cell diodes (D_{z1}, D_{z2}, D_{z3}) in the boost mode can be observed in Fig. 12(b). The magnetizing current and the voltage stresses of each cycle (negative and positive) charging switches (S_1 and S_4) are shown in Fig. 12(c). As mentioned in Section II, the voltage gain of the MSCL from (10) depends on the turn ratio (n). In the experimental implementation, each cell windings are fabricated on the half of the middle leg of the EE ferrite core using the copper foils (refer to Fig. 8). In order to minimize the leakage inductance, the three windings are wound together (trifilar). The required turn number to achieve 100 μH for the magnetizing inductance is then 15 for the first and the second windings (N_1 and N_2), also the turn number of the third winding (N_3) is 5, resulting in the turn ratio being $n = 1/3$.

The waveforms in the buck and boost modes of the MSCL operation are shown in Figs. 13 and 14. The input voltage is

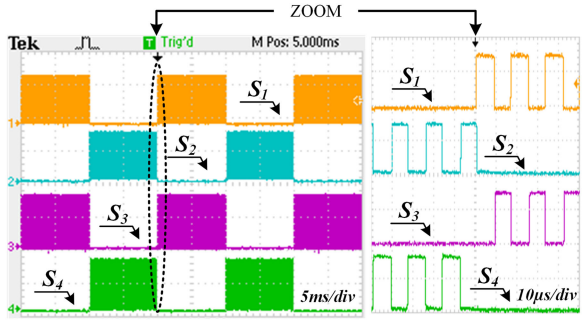

Fig. 10. Gating signals for the proposed structures.

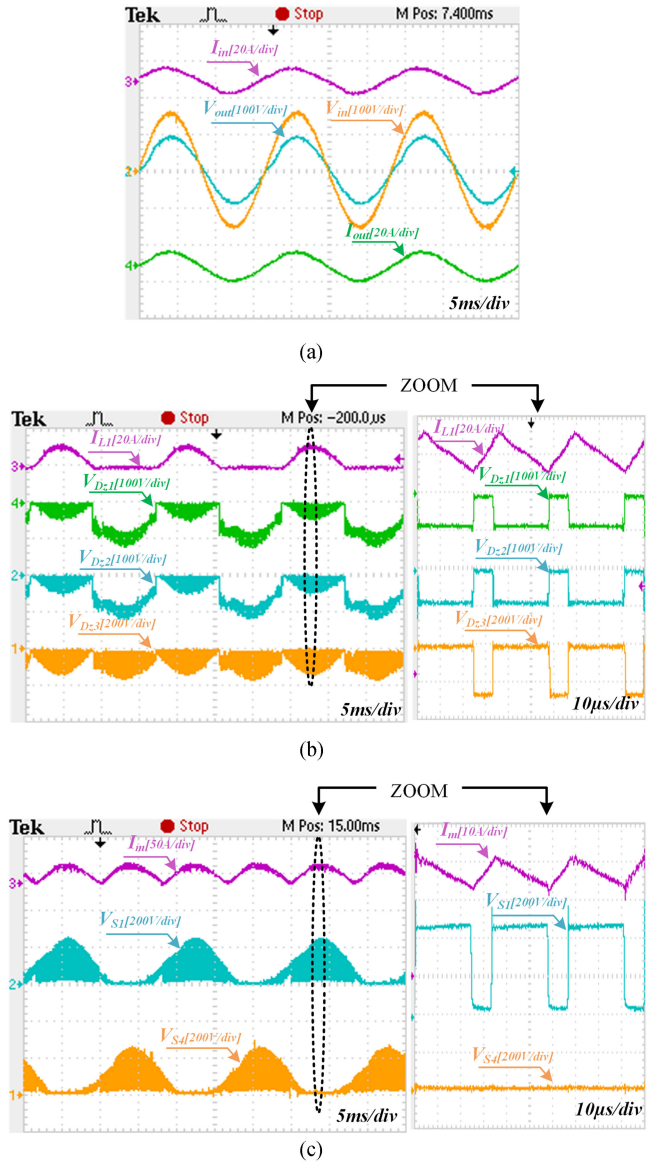

Fig. 11. Buck mode of the CSL ($D = 0.24$). (a) Voltages and currents at input and output. (b) Winding current and blocked voltages by positive cell diodes. (c) Magnetizing current and blocked voltages by charging switches (S_1 and S_4).

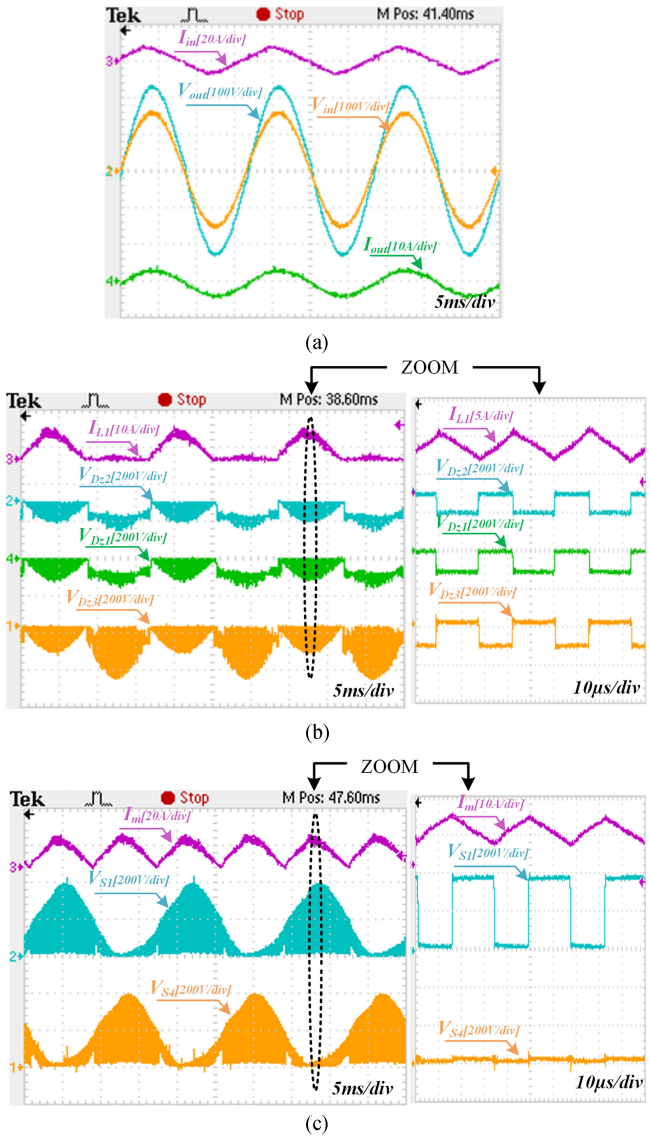

Fig. 12. Boost mode of the CSL ($D = 0.444$). (a) Voltages and currents at input and output. (b) Winding current and blocked voltages by positive cell diodes. (c) Magnetizing current and blocked voltages by charging switches (S_1 and S_4).

again fixed to 110 V(rms), while the output voltages are calculated as 93.5 and 198 V(rms) based on (10) and measured as 84 and 191 V(rms) in the buck and the boost modes, respectively. The transition between positive and negative half-cycles at the zero crossings of the input voltage causes abrupt changes in voltages and currents of the circuit. These transients generate zero crossing distortions (ZCDs), especially with the MSCL-based ac–ac converter, which can be seen in Figs. 13 and 14. The ZCD is mostly apparent in the output voltage of the MSCL-based ac–ac converter in which the capacitor of the MSCL cell becomes charged before its corresponding half-cycle begins again. Forcing this initial voltage value to change in a very short duration results in distortions at the zero crossings of the output voltage. The experimental results are in a good agreement with the calculations, which confirms the theoretical analysis. The winding currents ($I_{L1} = I_{N1}$ and $I_{L3} = I_{N3}$) and the voltages across the diodes in the positive half-cycle are shown in Figs. 13(b) and 14(b) in the buck and the boost modes, respectively. The winding currents during the charge mode [refer to Fig. 5(c)] are sinusoidal due to the resonance of the LC circuit. However, for the CSL, the winding currents are triangular waveforms with constant ramps.

The peak magnetizing current mainly determines the required magnetic core size. According to the electrical connection of the MSCL windings, the peak magnetizing current in this structure has almost the same value as the CSL. This is why the windings of the CSL and the MSCL structures are wound on the same core size without any concern about the saturation (refer to Fig. 8). The magnetizing current and the voltages across the charging

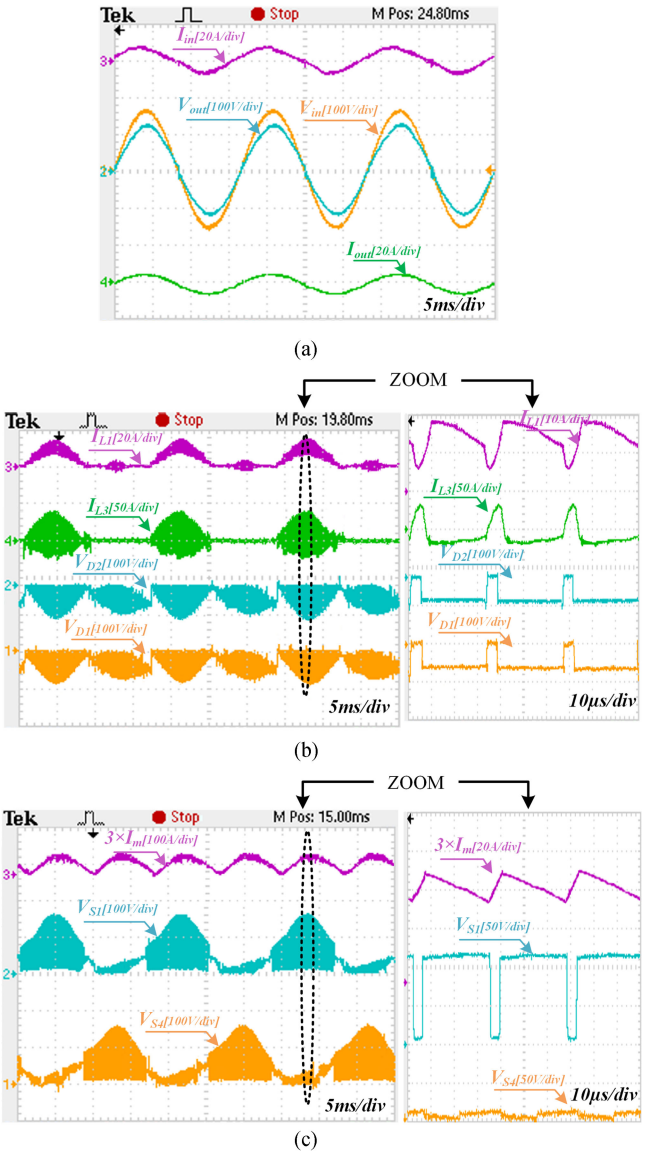

Fig. 13. Buck mode of the MSCL ($D = 0.1$). (a) Voltages and currents at input and output. (b) Windings currents and blocked voltages by positive cell diodes. (c) Magnetizing current and blocked voltages by charging switches (S_1 and S_4).

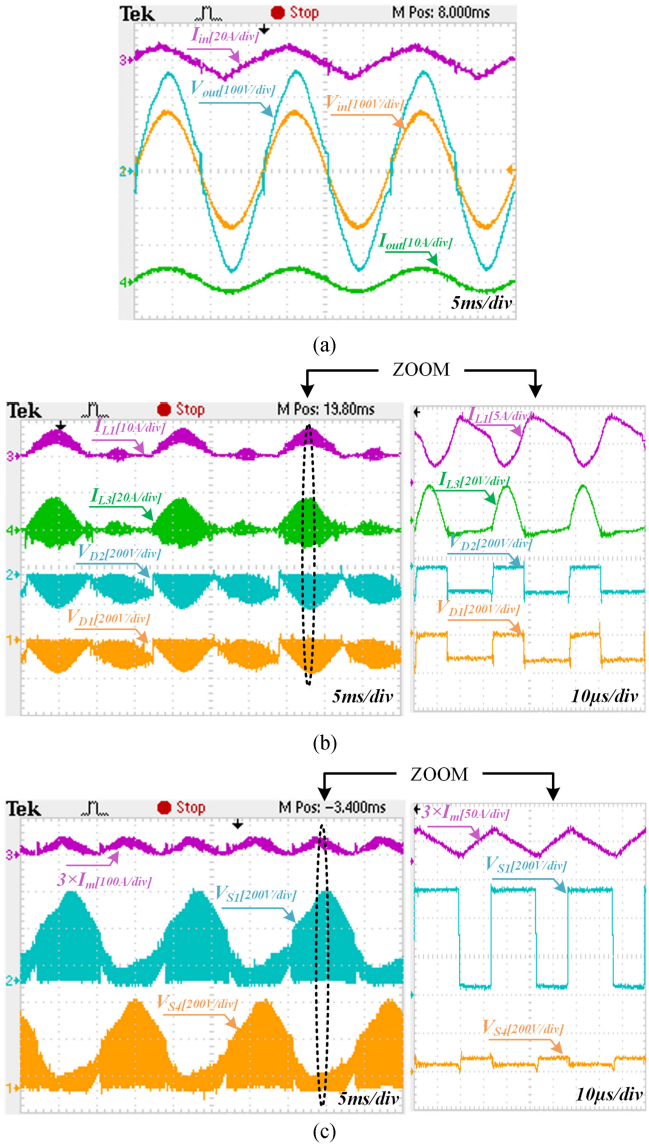

Fig. 14. Boost mode of the MSCL ($D = 0.4$). (a) Voltages and currents at input and output. (b) Windings currents and blocked voltages by positive cell diodes. (c) Magnetizing current and blocked voltages by charging switches (S_1 and S_4).

switches (S_1 and S_4) are shown in Figs. 13(c) and 14(c) in the buck and the boost modes, respectively. It must be clarified that for the MSCL structure, the magnetizing current is calculated from the measured winding currents multiplied by the turn numbers, i.e., $N_1 I_m = N_1 I_{L1} + N_2 I_{L2} + N_3 I_{L3}$. According to the turn numbers, it is more convenient to calculate $3I_m = 3I_{L1} + 3I_{L2} + I_{L3}$, which is then shown in Figs. 13(c) and 14(c).

The experimentally measured efficiency and waveforms quality (expressed with total harmonic distortion (THD)) are compared in Fig. 15. Clearly, the CSL offers a higher efficiency than the MSCL at all working conditions that is more distinct in the buck mode of operation. Also, the peak efficiency is 92.37% and 87.46% for the CSL and the MSCL, respectively. The measured THD of the output voltage and the input current is plotted in Fig. 15(b) and (c), measured by a FLUKE-435 power analyzer. Again, the CSL shows a better performance in producing the source currents and the load voltages with lower THDs compared to the MSCL.

The high peak resonance currents of the MSCL windings during the charging state can be recognized as a cause of increase in the switches losses and harmonic components in both input current and output voltage.

V. Comparative Analysis

The proposed converters and the recent topologies presented in [30], [31], and [33] are compared from different technical and practical aspects and the results are summarized in Table II.

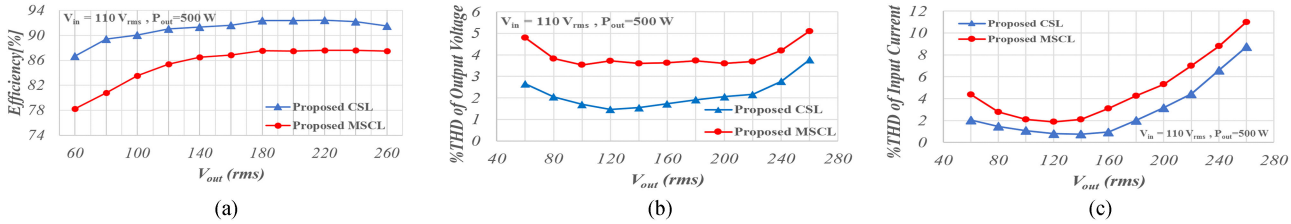

Fig. 15. Comparative performance analysis. (a) Efficiency. (b) THD of the output voltage. (c) THD of the input current.

TABLE II
COMPARISON AMONG THE PROPOSED CONVERTERS AND SOME COMPETITORS

	Proposed AC-AC Converters		Converter in [31]	Converter in [30]	Converter in [33]
	CSL	MSCL			
No. of switches	4 (S_1-S_4)	4 (S_1-S_4)	4 (S_1-S_4)	4 (S_1-S_4)	6 (S_1-S_4)
No. of diodes	4 (D_1-D_4) 6 (D_{z1}-D_{z6})	4 (S_1-S_4) 4 (D_{z1}-D_{z4})	4 (D_1-D_4)	--	--
No. of inductors	4 coupled-inductors (N_1-N_4)	6 coupled-inductors (N_1-N_6)	2 inductors (L_1 , L_2)	2 coupled-inductors (w_1 , w_2)	1 inductor & 2 coupled-inductors
No. of magnetic cores and size*	1 Low	1 Low	2 Medium	1 Low	2 Low
No. of capacitors (including filters)	2 (C_1 , C_2) 2 (C_{fin} , C_{fout})	2 (C_1 , C_2) 2 (C_{z1} , C_{z2}) 2 (C_{fin} , C_{fout})	2 (C_1 , C_2) 2 (C_{fin} , C_{fout})	2 (C , C_f)	3 (C_1 , C_2 , C)
No. of semiconductors conducting simultaneously	2	2	4	6	8
Switch/diode voltage stress*	High	High	Low	Medium	Low
Switch/diode current stress*	Low	Low	Medium	Medium	Very Low
Voltage gain	$\frac{2D}{1-D}$	$\frac{1-n+D}{1-D}$	$\frac{D}{1-D}$	$\frac{1-D}{1-\left(1+\frac{1}{\gamma_\Gamma-1}\right)D}$	$\frac{1}{1-(N+2)D}$
Turn ratio flexibility	--	$n>0$	--	$1<\gamma_\Gamma<2$	$N>0$
Operation modes	In-phase buck-boost	buck, boost and buck-boost (all either in- or out-of-phase)	In-phase buck-boost	Out-of-phase buck-boost, in-phase boost	Out-of-phase buck-boost, in-phase boost
Continuity of input and output current	Quasi continuous	Quasi continuous	Quasi continuous	Discontinuous	Continuous
Commutation problem	no	no	no	yes	yes
Current flow through body diodes	no	no	no	yes	yes
Common ground between V_{in} & V_{out}	no	no	no	yes	Yes
Peak efficiency	92.37%	87.46%	93.8%	88%	85%
Feeding inductive loads	limited, switching must be modified	limited, switching must be modified	possible	possible	possible

* the qualitative comparison is presented considering numerical calculations for buck and boost operations.

Clearly, the number of magnetic cores and the number of semiconductors conducting simultaneously are reduced with the proposed switching strategy for the proposed converters. Another considerable advantage of the proposed converters in comparison to other converters is the capability of the proposed converters to operate in-phase or out-of-phase in buck, boost, and buck–boost modes.

VI. CONCLUSION

Two single-phase ac–ac circuits with two series Z-source impedance networks in their structures are introduced. Besides having the conventional ac–ac choppers advantages, the proposed converters offer many unique features such as a much wider range of voltage gains than the conventional choppers,

reduced number and size of the magnetic elements by using the proposed switching strategy, high conversion efficiency, and high quality waveforms. Despite these advantages, the main shortcoming of this topology may be the separate ground of the input and the output.

This paper also describes the converter design for a 500 W prototype. Experimental results provided confirm the proper operation of the proposed ac–ac converter.

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