Development of a Converter-Based Transmission Line Emulator With Three-Phase Short-Circuit Fault Emulation Capability

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***Abstract*—A transmission line emulator has been developed to flexibly represent interconnected ac lines under normal operating conditions in a voltage-source-converter-based power system emulation platform. As the most serious short-circuit fault condition, the three-phase short-circuit fault emulation is essential for power system studies. This paper proposes a model to realize a three-phase short-circuit fault emulation at different locations along a single transmission line or one of several parallel-connected transmission lines. At the same time, a combination method is proposed to eliminate the undesired transients caused by the current reference step changes while switching between the fault state and the normal state. Experiment results verify the developed transmission line three-phase short-circuit fault emulation capability.**

***Index Terms*—Hardware test-bed (HTB), short-circuit fault emulation, transmission line emulator, transmission line fault.**

I. Introduction

BEFORE digital simulations, power system simulations, such as power flow, system oscillation, relay protection, and transient stability, mainly relied on analog emulation platforms [1], [2]. With the development of digital computing technology, digital simulation platforms have been widely adopted for power system studies because of several advantages over analog emulation platforms [3]–[5]. First, a digital simulation platform is relatively cheaper and smaller than an analog emulation platform. Second, the power grid simulated in a digital simulation environment can be modified easily, while an analog emulation platform needs significant effort to be reconfigured. Third, compared with an analog emulation platform, a digital simulation platform can simulate a power system with more buses. Despite these advantages, digital simulation platforms have not totally replaced analog emulation platforms. Many analog emulation facilities are still utilized for power system studies, real equipment testing, and laboratory education [6]–[8]. Instead of digital simulation results, which are acquired by neglecting several practical factors such as communication bandwidth, time delay, measurement errors, and electromagnetic interference, hardware testing results are still preferred and are more convincing for most power engineers. In addition, an analog emulation platform can be utilized for testing newly developed devices, whose mathematical models are either not accurate or not available.

Since the 1990s, with the development of real-time digital simulators (RTDS), such as Opal-RT and the Typhoon HIL, the hybrid simulation environment, which combines digital simulation and the hardware testing together with the hardware-in-the-loop (HIL) technology, has become a new trend for power system studies [9], [10]. With this technology, the simulation capability and flexibility can be improved by using RTDSs, and also physical devices can get involved in the testing at the same time. Except for testing controllers, such as protection relays, generator excitation control systems, and power electronic converter controllers, by using the control HIL technology, the power-level facilities can also be tested by using power amplifiers as the interfaces, which is named as power HIL [11]. Power HIL has been used to test different devices for a variety of purposes, such as photovoltaic inverters, wind generators, and microgrids [12], [13]. Instead of power-system-level testing and study, these platforms focus on testing only one device or a small system of no more than a microgrid with a few buses and lines. In [14], a hybrid emulation platform based on the RTDS and an analog emulation system has been established for power system study. Compared with using only the analog emulation system, it improves the testing capability and flexibility by putting a part of the simulated system into the RTDS. Nevertheless, the traditional analog emulation system is still based on scaled generators, transmission lines, motors, and loads, which are relatively massy, expensive, and inflexible.

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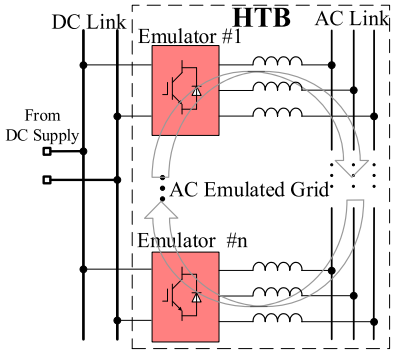

Fig. 1. System configuration of the HTB.

According to the power HIL concept, a hardware test-bed (HTB) platform has been developed by the Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks, The University of Tennessee, to emulate power systems by programming interconnected three-phase voltage-source converters (VSCs) to behave like the intended power system components, as shown in Fig. 1 [15]–[18]. The dc sides of the emulators share a common dc power supply. The ac side of each emulator is controlled to function as a power system component, such as a generator, a load, an energy storage unit, etc. Specifically, two converters connected back-to-back are cooperatively controlled to function as a transmission line. The ac-link connection forms the emulated ac grid by connecting each emulated component the same as it is in the original ac grid. Since the emulator VSCs share a common link, the active power circulates among the VSCs as indicated by the circulating arrows in Fig. 1, and the dc power supply only makes up for the system power loss.

Compared with traditional analog emulation platforms, the HTB is more cost effective and flexible, yet still enables realistic testing and demonstration of power system operation and control with actual measurement, communication, and control stations [19]. Different from the power HIL platform, which tests the hardware with the original ratings, the HTB is mainly utilized for power system studies, such as system operation, oscillation damping, system protection studies, and transient stability, with a scaled version of the original power grid.

As a common disturbance in power systems, transmission line short-circuit faults are employed for many studies. Specifically, as the most serious short-circuit fault condition, the three-phase short-circuit fault is widely adopted for power system transient studies [20]–[23]. As a power system emulation platform, it is essential for the HTB to have the transmission line three-phase short-circuit fault emulation capability. For example, the HTB has been applied to demonstrate the simplified Western Electricity Coordinating Council (WECC) system with a hypothetical three-terminal HVDC overlay, as shown in Fig. 2 [24].

Fig. 2(a) shows the one-line diagram of the WECC system with the corresponding map, and Fig. 2(b) shows the one-line diagram of the WECC system with scaled generators, loads, and transmission line parameters. A realistic and interesting case study would be to apply a three-phase short-circuit fault in the transmission line between Buses 3 and 4, which is a major power transmission path between the northeast and southeast portions

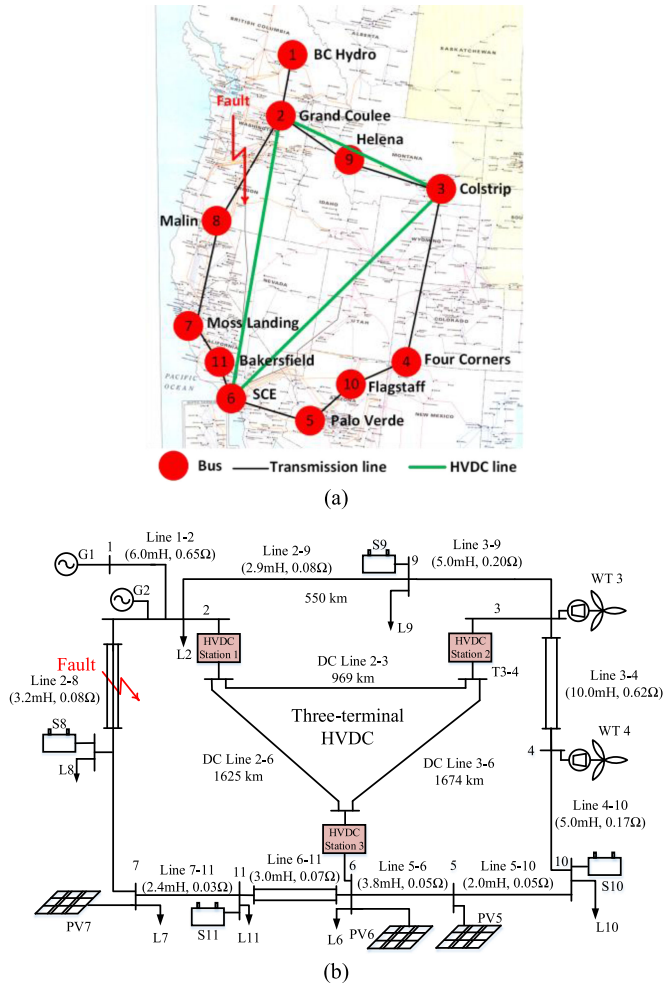

Fig. 2. WECC system with a hypothetical three-terminal HVDC overlay. (a) One-line diagram with the corresponding map. (b) One-line diagram with generators, loads, and transmission line parameters shown.

of the WECC. The California Oregon Intertie, identified as Path 66, is a critical power transmission path within the WECC [25]. Path 66, corresponding to the transmission lines among Buses 2, 8 and 7 in Fig. 2, is composed of several parallel-connected 500-kV power transmission lines [25]. Applying a three-phase short-circuit fault in a part of the parallel-connected transmission lines would be an essential and realistic scenario to study the transient stability of the WECC system.

In traditional analog emulation platforms, several sections of inductors, capacitors, and resistors can be employed to emulate transmission lines, and circuit breakers can be implemented at the common point between two sections to emulate a short-circuit fault [26], [27]. However, similar to the other elements in a traditional analog emulation platform, the disadvantages of high cost and less flexibility still exist, and the fault can only happen at several discrete locations, depending on the number of sections. In the HTB, a short-circuit fault emulator based on a shunt-connected VSC has previously been developed, but only the short-circuit fault at a voltage bus could be emulated [28]. Previously, a transmission line emulator based on two three-phase VSCs has been developed to improve the flexibility

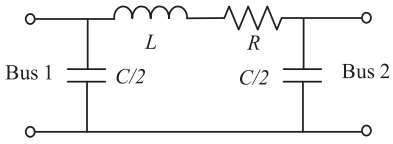

Fig. 3. Electrical single-line diagram of a transmission line Π model.

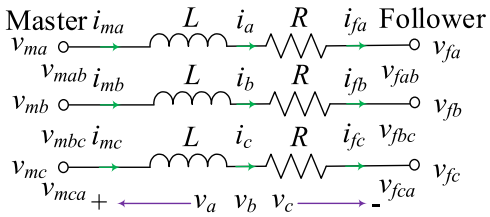

Fig. 4. Simplified three-phase transmission line under normal conditions.

of changing the emulated line impedance [29]. However, only the normal operation and manual line trip open functions are implemented [30]. The primary goal of this paper is to develop a transmission line emulator with the three-phase short-circuit fault emulation capability based on VSCs, where a fault at different locations along the line can be studied.

Different from previous work, this paper implements the three-phase short-circuit fault function in the converter-based transmission line emulator to represent a fault at different locations along the emulated transmission line. In addition to a three-phase short-circuit fault within a single transmission line, it can emulate a three-phase short-circuit fault within one of several parallel-connected transmission lines. This concept is first proposed and addressed in this paper. Except for the application in the HTB, it can also be utilized in the traditional analog emulation platform. The transmission line three-phase short-circuit fault emulation developed in this paper is based on the balanced three-phase three-wire system.

The structure of this paper is organized as follows. Section II presents the transmission line emulation model with both normal state and three-phase short-circuit fault state functions. Section III analyzes the transmission line emulation stability. Section IV presents the transmission line emulator implementation in the HTB. Section V presents the experimental verification. Finally, we will conclude this paper in Section VI.

II. Transmission Line Emulation Model

A. Single-Transmission-Line Model

A transmission line can be simplified as a Π model for many power system studies, as shown in Fig. 3 [31]–[36]. Usually, the transmission line is connected with buses on both sides, where generators or loads exist [37]–[40]. Thus, the parallel capacitors in the Π model can be integrated into the generator or load emulator connected on the same bus [41]–[44]. The parallel capacitance is also negligible for many short transmission lines. In this paper, the emulated three-phase transmission line is further simplified as an inductor in series with a resistor in each phase, as shown in Fig. 4 [29]–[30].

The two terminals of the transmission line are named as "Master" and "Follower," respectively, in this paper. The transmission

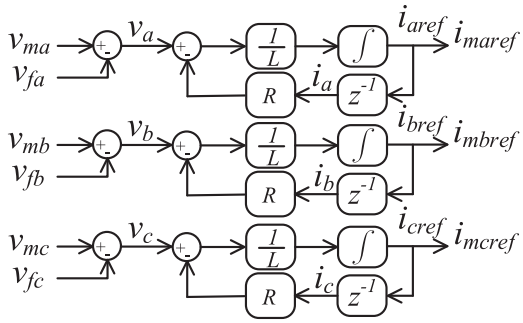

Fig. 5. Transmission line model under normal conditions.

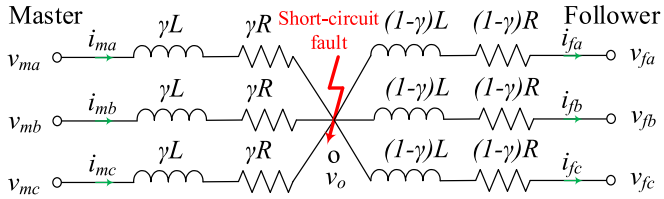

Fig. 6. Transmission line under three-phase short-circuit faults.

line inductance and resistance are L and R, respectively. The Master-side phase A, B, and C to neutral voltages are named as v_{ma}, v_{mb}, and v_{mc}, respectively. The Follower-side phase A, B, and C to neutral voltages are named as v_{fa}, v_{fb}, and v_{fc}, respectively.

The Master-side phase A to B, phase B to C, and phase C to A voltages are named as v_{mab}, v_{mbc}, and v_{mca}, respectively. The Follower-side phase A to B, phase B to C, and phase C to A voltages are named as v_{fab}, v_{fbc}, and v_{fca}, respectively.

The Master-side phase A, B, and C currents are named as i_{ma}, i_{mb}, and i_{mc}, respectively, with the corresponding current references $i_{ma\text{ref}}$, $i_{mb\text{ref}}$, and $i_{mc\text{ref}}$ from the transmission line model. The Follower-side phase A, B, and C currents are named as i_{fa}, i_{fb}, and i_{fc}, respectively, with the corresponding current references $i_{fa\text{ref}}$, $i_{fb\text{ref}}$, and $i_{fc\text{ref}}$ from the transmission line model. The phase A, B, and C voltages across the transmission line are named as v_a, v_b, and v_c, respectively. The phase A, B, and C currents flowing through the transmission line under normal conditions are named as i_a, i_b, and i_c, respectively. The voltage and current positive directions are defined in Fig. 4.

In the time domain, the transmission line is expressed as

$$v_x = v_{mx} - v_{fx} = L\frac{di_x}{dt} + Ri_x \quad (x = a, b, c). \tag{1}$$

By measuring the terminal voltages, the current references can be derived as

$$i_{mx\text{ref}} = i_{fx\text{ref}} = i_{x\text{ref}} = \int \frac{v_{mx} - v_{fx} - Ri_x}{L}\, dt. \tag{2}$$

Thus, the transmission line model under normal operating conditions is derived as shown in Fig. 5.

Considering that a three-phase short-circuit fault happens at the location "o," the transmission line during the fault is shown in Fig. 6. The parameter γ $(0 < \gamma < 1)$ is the percentage of the distance from the location "o" to the Master-side terminal with regard to the total line length.

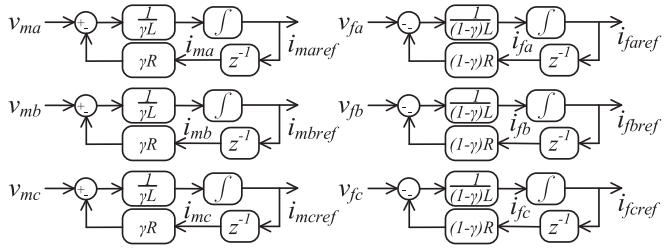

Fig. 7. Transmission line model under three-phase short-circuit faults.

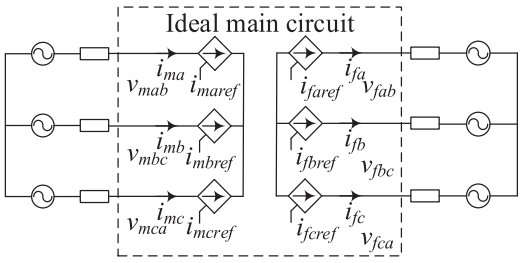

Fig. 8. Transmission line emulator ideal main circuit model.

Since the voltage at the three-phase short-circuit fault location, referring to the imaginary neutral point, is zero in the balanced three-phase system, the phase to neutral voltage equals to the phase to fault location voltage. Thus, the transmission line model can be expressed as

$$\begin{cases} v_{mx} = \gamma L \frac{di_{mx}}{dt} + \gamma R i_{mx} \\ v_{fx} = -(1-\gamma) L \frac{di_{fx}}{dt} - (1-\gamma) R i_{fx} \end{cases} (x = a, b, c). \tag{3}$$

By measuring the terminal voltages, the current references can be derived as

$$\begin{cases} i_{mx\mathrm{ref}} = \int \frac{v_{mx} - \gamma R i_{mx}}{\gamma L}\, dt \\ i_{fx\mathrm{ref}} = \int \frac{-v_{fx} - (1-\gamma) R i_{fx}}{(1-\gamma) L}\, dt. \end{cases} \tag{4}$$

Thus, the transmission line model under three-phase short-circuit fault conditions is shown in Fig. 7.

According to the derived transmission line models for the balanced three-phase three-wire system, the transmission line performance under both normal and three-phase short-circuit fault conditions can be emulated by injecting currents on both sides of the transmission line, which track the current references calculated based on the measured voltages.

B. Smooth Switching Between Normal and Fault States

Considering the ideal current tracking performance, the transmission line emulator main circuit can be simplified and represented as controlled current sources, as shown in Fig. 8.

By switching the controlled current-source input references between the model under the normal state and the model under the fault state, the transmission line emulator can realize the emulations of both the normal state and the fault state. However, at the switching moment, there can be current reference errors between the normal state and the fault state if the two models are calculated separately. The error introduces undesired transients, especially when the transmission line is in series with inductors, which cannot tolerate current step changes.

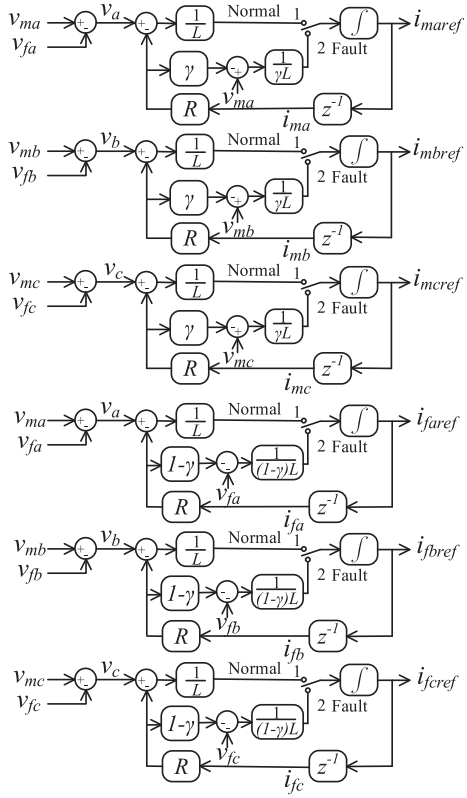

Fig. 9. Combined transmission line model.

In this paper, a combined model is proposed to avoid the switching transients between the normal state and the fault state. Instead of switching the controlled current-source input references, the inputs of the integral units for the current reference calculations are switched, as shown in Fig. 9, which combines the normal and fault states in one model. The single-pole double-throw switches are implemented to switch between the normal state and the short-circuit fault state. The emulated transmission line operates at the normal state when the switches are at position "1"; otherwise, it operates at the short-circuit fault state if the switches are at position "2".

C. Parallel-Connected Transmission Line Model

Parallel-connected transmission lines are commonly utilized in the electric grid for power delivery over long distances and for high power corridors. Fig. 10 shows a diagram with *k* parallel-connected lines.

When a three-phase short-circuit fault happens within one of the parallel-connected transmission lines, the parallel-connected transmission lines can be separated into two parts, which are the normal lines and the faulted line, as shown in Fig. 11. The normal lines can be integrated into a single transmission line with equivalent inductance L_n and resistance R_n of all normal lines in parallel. The faulted line inductance and resistance are named as L_s and R_s, respectively.

In this paper, the Master and Follower terminal voltage and current definitions of the parallel-connected transmission lines

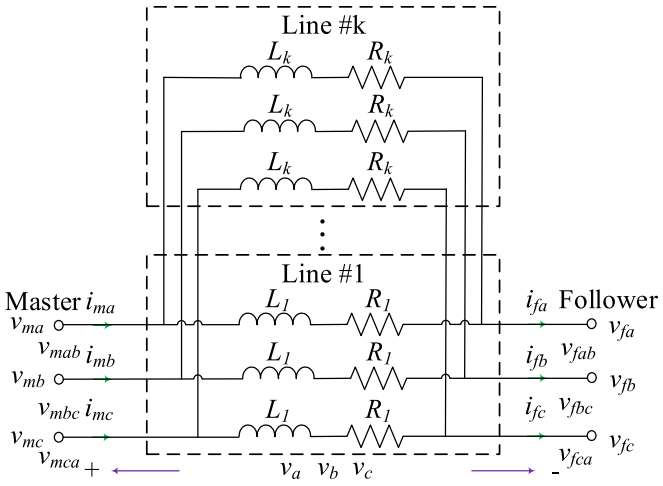

Fig. 10. Diagram of parallel-connected transmission lines.

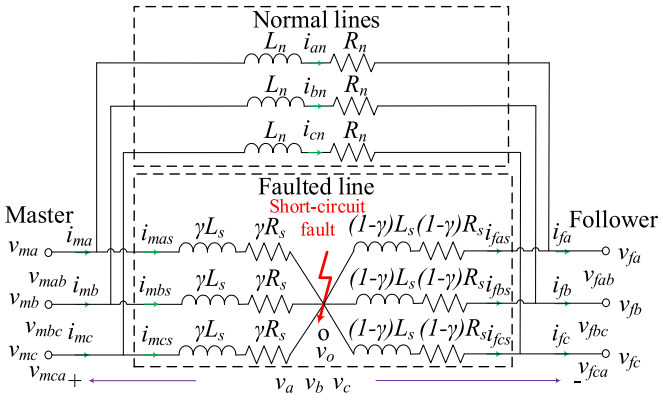

Fig. 11. Parallel-connected lines with a three-phase short-circuit fault.

are the same as the single transmission line. In addition to that, the phase A, B, and C currents of the normal lines are named as i_{an}, i_{bn}, and i_{cn}, respectively, with the corresponding current references $i_{an\text{ref}}$, $i_{bn\text{ref}}$, and $i_{cn\text{ref}}$ from the transmission line model. The Master-side phase A, B, and C currents of the short-circuit faulted line are named as i_{mas}, i_{mbs}, and i_{mcs}, respectively, with the corresponding current references $i_{mas\text{ref}}$, $i_{mbs\text{ref}}$, and $i_{mcs\text{ref}}$ from the transmission line model. The Follower-side phase A, B, and C currents of the short-circuit faulted line are named as i_{fas}, i_{fbs}, and i_{fcs}, respectively, with the corresponding current references $i_{fas\text{ref}}$, $i_{fbs\text{ref}}$, and $i_{fcs\text{ref}}$ from the line model.

Fig. 12 shows the combined model of parallel-connected transmission lines with a three-phase short-circuit fault that happens within one of the transmission lines.

The normal line model and the line model with a three-phase short-circuit fault are solved separately. The total current reference of the parallel-connected transmission lines is derived by adding up the current references of the normal line model and the line model with a three-phase short-circuit fault. The single-pole double-throw switches are implemented to switch between the normal state and the short-circuit fault state of the predetermined transmission line with a three-phase short-circuit fault emulation. The predetermined transmission line operates at the normal state when the switches are at position "1"; otherwise,

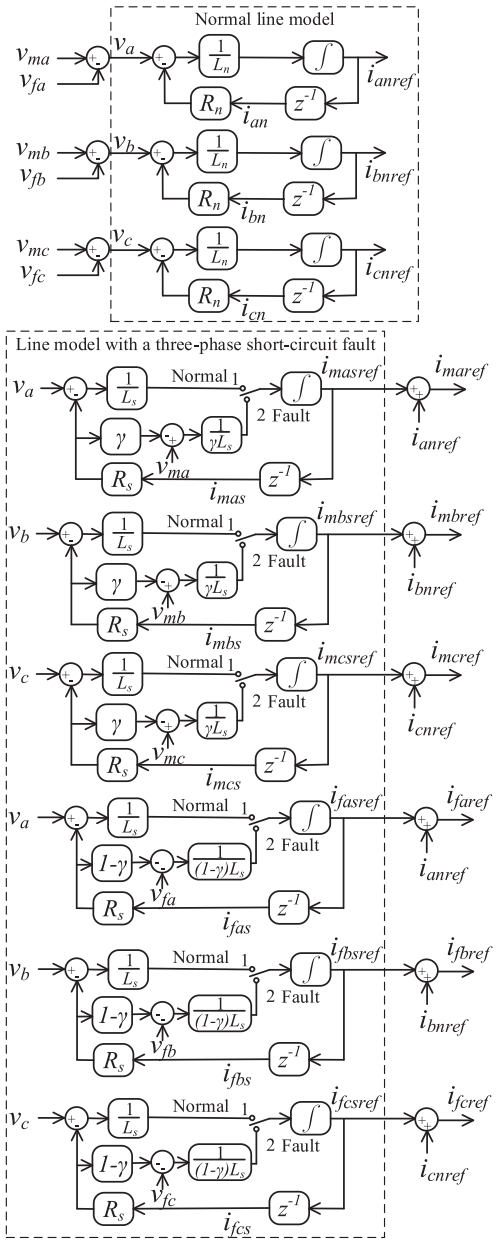

Fig. 12. Combined model of parallel-connected transmission lines.

it operates at the short-circuit fault state if the switches are at position "2".

III. Transmission Line Emulation Stability Analysis

Similar to the power HIL interface algorithms, there is a potential emulation stability issue induced by the time delay within the transmission line emulator. It is essential to locate the boundary conditions of emulating the transmission line stably [45]. A balanced three-phase circuit can be separated into three identical single-phase circuits for analysis.

Assume that the single-phase diagram of a power system with the transmission line can be simplified as in Fig. 13(a). E_1 and Z_1 are the equivalent voltage source and impedance at the Master side. E_2 and Z_2 are the equivalent voltage source and impedance at the Follower side. Theoretically, the models of the two VSCs,

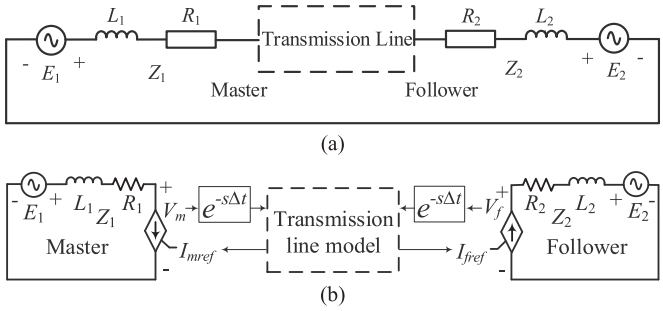

Fig. 13. Simplified single-phase diagram. (a) Original system. (b) System with a transmission line emulator.

which are programmed to emulate the transmission line, should also be considered in the stability analysis. In this paper, in order to focus on the stability analysis of the transmission line emulation algorithm itself and derive a more generalized stability condition guidance, the VSC current tracking performance is assumed to be ideal. Fig. 13(b) shows the single-phase diagram with the transmission line emulator considering ideal current tracking performance. Similar to the power HIL interface algorithm analysis in [14] and [46]–[48], assuming that the total time delay within the transmission line emulator is Δt, and the time delay is applied on the voltage measurements to simplify the analysis.

In the *s*-domain, the circuit at the Master side and the circuit at the Follower side can be expressed in (5) and (6), respectively:

$$E_1(s) = Z_1(s)I_{m\mathrm{ref}}(s) + V_m(s) \tag{5}$$

$$E_2(s) = -Z_2(s)I_{f\mathrm{ref}}(s) + V_f(s). \tag{6}$$

A. Single-Transmission-Line Emulation Stability

Under the normal condition, the transmission line model can be expressed as in (7), where Z_L is the transmission line impedance:

$$I_{m\mathrm{ref}}(s) = I_{f\mathrm{ref}}(s) = \left(V_m(s) - V_f(s)\right)e^{-s\Delta t}/Z_L(s). \tag{7}$$

Substituting (7) into (5) and (6), the current references can be solved as

$$I_{m\mathrm{ref}}(s) = I_{f\mathrm{ref}}(s) = \frac{\left(E_1(s) - E_2(s)\right)/Z_L(s)e^{-s\Delta t}}{\left(\left(Z_1(s) + Z_2(s)\right)/Z_L(s)e^{-s\Delta t}\right) + 1}. \tag{8}$$

According to (8), taking E_1 or E_2 as the input and $I_{m\mathrm{ref}}$ or $I_{f\mathrm{ref}}$ as the output, the denominator of the closed-loop transfer function is the denominator in (8). Thus, the open-loop transfer function can be obtained as the expression inside of the absolute value sign in (9). If the magnitude of the open-loop transfer function is smaller than 1, there is no 0-dB crossing point in the amplitude–frequency curve, which means that the phase margin is infinite. Thus, the system is assured to be stable when the following equation is satisfied:

$$\left|\left(Z_1(s) + Z_2(s)\right)/Z_L(s)e^{-s\Delta t}\right| < 1. \tag{9}$$

The stability requirement is expressed based on (9) as follows:

$$|Z_1 + Z_2| < |Z_L|. \tag{10}$$

According to (10), under normal conditions, the transmission line emulation is assured to be stable if the line impedance is larger than the sum of the equivalent source impedances at both sides of the transmission line.

Under a short-circuit fault condition, the transmission line model can be expressed as in (11), where Z_L is the transmission line impedance and γ is the percentage of the distance from the fault location to the Master-side terminal with regard to the total line length

$$\begin{cases} I_{m\mathrm{ref}}(s) = V_m(s)e^{-s\Delta t}/\left(\gamma Z_L(s)\right) \\ I_{f\mathrm{ref}}(s) = V_f(s)e^{-s\Delta t}/\left(\left(1-\gamma\right)Z_L(s)\right). \end{cases} \tag{11}$$

Substituting (11) into (5) and (6), the current references can be solved as

$$\begin{cases} I_{m\mathrm{ref}}(s) = \frac{E_1(s)/(\gamma Z_L(s))e^{-s\Delta t}}{(Z_1(s)/(\gamma Z_L(s))e^{-s\Delta t})+1} \\ I_{f\mathrm{ref}}(s) = \frac{E_2(s)/((1-\gamma)Z_L(s))e^{-s\Delta t}}{(Z_2(s)/((1-\gamma)Z_L(s))e^{-s\Delta t})+1}. \end{cases} \tag{12}$$

Similarly, the system is assured to be stable when the following equation is satisfied:

$$\begin{cases} \left|Z_1(s)/\left(\gamma Z_L(s)\right)e^{-s\Delta t}\right| < 1 \\ \left|Z_2(s)/\left(\left(1-\gamma\right)Z_L(s)\right)e^{-s\Delta t}\right| < 1. \end{cases} \tag{13}$$

The stability requirement is expressed in (14) based on (13), and the line model is more likely to be unstable if the fault is at one end of the transmission line (γ is close to 0 or 1).

$$\begin{cases} |Z_1| < |\gamma Z_L| \\ |Z_2| < |(1-\gamma)Z_L|. \end{cases} \tag{14}$$

B. Parallel-Connected Transmission Line Emulation Stability

Under normal conditions, the parallel-connected transmission line model is the same as the single transmission line; thus, the transmission line emulation is stable if the equivalent impedance of the parallel-connected transmission lines is larger than the sum of the equivalent source impedances at both sides of the transmission line.

Under a short-circuit fault condition, the transmission line can be separated into the normal lines and the faulted line. The emulation stability of normal lines can be evaluated by assuming the short-circuited line operates stably, as shown in Fig. 14(a). According to the Thevenin–Norton theorem, the Master-side and Follower-side equivalent impedances are $Z_1||(\gamma Z_s)$ and $Z_2||((1-\gamma)Z_s)$, respectively, where Z_s is the faulted transmission line impedance. Similar to the single-transmission-line analysis, the stability requirement is expressed in (15), where Z_n is the normal transmission line impedance:

$$\left|\left(Z_1||\left(\gamma Z_s\right)\right) + \left(Z_2||\left(\left(1-\gamma\right)Z_s\right)\right)\right| < |Z_n|. \tag{15}$$

The Master-side emulation stability of the faulted line can be evaluated by assuming that the normal lines and the faulted line

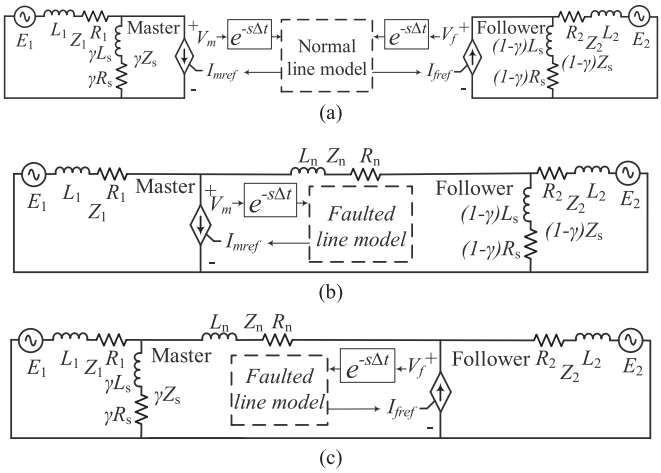

Fig. 14. Stability analysis diagram of the parallel-connected transmission line with a three-phase short-circuit fault at one of the transmission lines. (a) Normal line stability analysis model. (b) Faulted line Master-side stability analysis model. (c) Faulted line Follower-side stability analysis model.

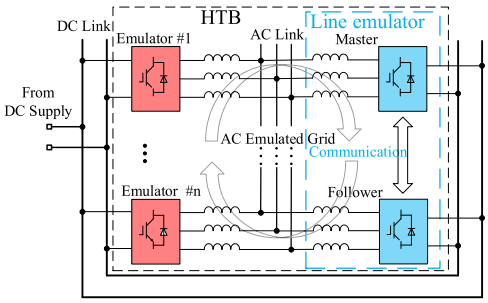

Fig. 15. System configuration of HTB with a transmission line emulator.

at the Follower side operate stably, as shown in Fig. 14(b). According to the Thevenin–Norton theorem, the equivalent impedance at the Master terminal is $((Z_2 \,||\, ((1-\gamma)Z_s)) + Z_n)||Z_1$. The stability requirement is expressed as

$$|((Z_2||\,((1-\gamma)\,Z_s)) + Z_n)\,||Z_1| < |\gamma Z_s|\,. \tag{16}$$

Similarly, the Follower-side emulation stability of the faulted line can be evaluated by assuming that the normal lines and the faulted line at the Master side operate stably, as shown in Fig. 14(c), and the Follower-side stability requirement is expressed as

$$|((Z_1||\,(\gamma Z_s)) + Z_n)\,||Z_2| < |(1-\gamma)\,Z_s|\,. \tag{17}$$

Thus, the emulation of parallel-connected transmission lines with a three-phase short-circuit fault within one transmission line is assured to be stable when (15)–(17) are satisfied.

IV. Transmission Line Emulator Implementation in the HTB

By highlighting a transmission line emulator in Fig. 1, the system configuration of the HTB grid emulator is shown in Fig. 15. The transmission line emulator is composed of two VSCs, which are named as Master and Follower, respectively, in this paper. The Master and Follower VSCs also share the same dc link with the other HTB emulator VSCs so that the power loss of Master and Follower VSCs does not affect the power loss

Fig. 16. HTB grid emulation platform.

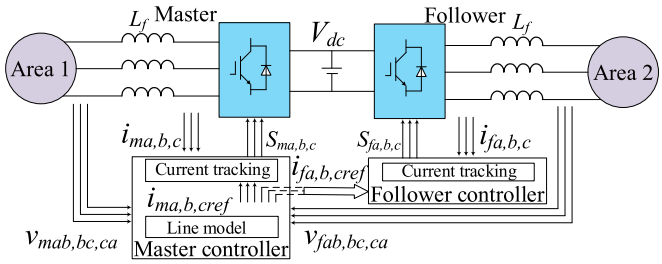

Fig. 17. Transmission line emulator structure.

TABLE I
Parameters of the VSC

Common parameters		Values
Filter inductance	L_f	0.575 mH
DC-link voltage	V_{dc}	200 V
Switching frequency	f_s	10 kHz

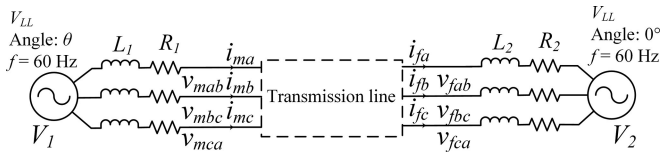

Fig. 18. System topology for experimental verification.

performance of the emulated transmission line. Fig. 16 shows the HTB grid emulation platform.

Both Master and Follower VSCs have their own controllers for current tracking control, as shown in Fig. 17. Area 1 and Area 2 represent two power system networks, which are connected by the emulated transmission line. The transmission line model, which calculates the current references according to the terminal voltages, locates in the Master controller. The Follower-side current references are calculated in the Master controller and sent to the Follower controller through dedicated serial communication. The VSC parameters are listed in Table I.

V. Experimental Results

In order to simplify the comparison, a system diagram of a transmission line connected between two voltage sources is set up to verify the transmission line fault emulation, as shown in Fig. 18.

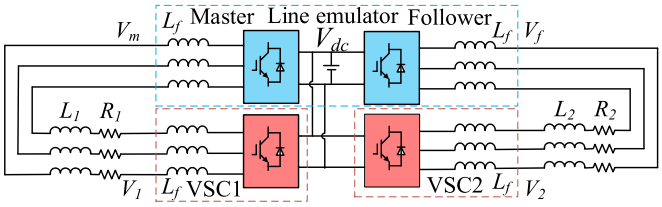

Fig. 19. Experimental line emulator platform setup.

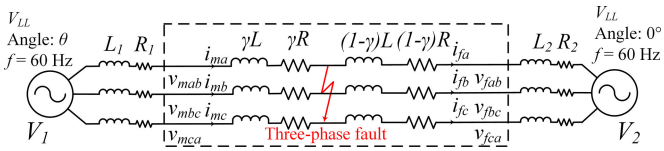

Fig. 20. System topology for single-line experimental verification.

In the HTB, the ideal voltage sources V_1 and V_2 are realized by VSCs through maintaining the voltage magnitude with closed-loop control. The ideal voltage-source frequency is kept at 60 Hz, but the angle can be modified manually through the human-machine interface to change the power flow between the two sources. The voltage-source internal impedances are realized by physical inductors, which are L_1, R_1 and L_2, R_2, respectively. The transmission line can be set to connect between two ideal voltage sources by using zero internal impedances (Set L_1, R_1, L_2, and R_2 to zero) for the voltage sources.

Fig. 19 shows the experimental line emulator platform setup based on HTB converters and the system topology in Fig. 18. The Master and Follower converters emulate the transmission line, and the VSC1 and VSC2 perform as the ideal voltage sources V_1 and V_2, respectively.

A. Fault Emulation of a Single Transmission Line

The system diagram of the single-transmission-line experiment verification is shown in Fig. 20. The transmission line inductance and resistance are *L* and *R*, respectively. The three-phase short-circuit fault happens at the location γ ($0 < \gamma < 1$), which is the ratio of the distance from the fault location to the Master-side terminal with regard to the total line length.

1) Single Transmission Line Connected With Two Ideal Voltage Sources Scenario: In order to verify the transmission line emulation performance by connecting to two ideal voltage sources, the voltage-source impedances are set to zero (L_1, R_1, L_2, and R_2 equal to zero). The transmission line inductance and resistance are selected as 12 mH and 0.3 Ω, respectively. Three fault scenarios with γ equals to 1/3, 1/2, and 2/3, respectively, are conducted to verify the three-phase short-circuit fault emulation capability at different locations within the emulated transmission line.

a) Three-phase short-circuit fault with $\gamma = 1/3$: A three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 1/3$ when the phase angle of V_{mab} is 170°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -26°$. The fault is cleared at 0.3 s. Fig. 21(a) and (b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

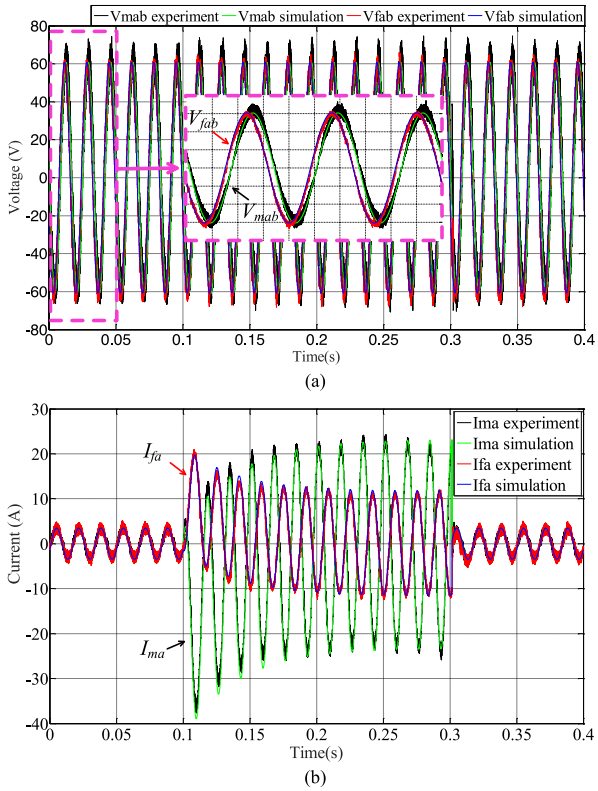

Fig. 21. Single-transmission-line experiment and simulation comparison with $\gamma = 1/3$. (a) V_{ab}. (b) I_a.

b) Three-phase short-circuit fault with $\gamma = 1/2$: A three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 1/2$ when the phase angle of V_{mab} is 130°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -30°$. The fault is cleared at 0.3 s. Fig. 22(a) and (b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

c) Three-phase short-circuit fault with $\gamma = 2/3$: A three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 2/3$ when the phase angle of V_{mab} is 150°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = -22°$. The fault is cleared at 0.3 s. Fig. 23(a) and (b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

According to the above comparisons, the experiment waveforms match with the simulation waveforms when a three-phase short-circuit fault happens at the locations of γ equals to 1/3, 1/2, or 2/3, which verifies the three-phase short-circuit fault emulation capability of the developed transmission line emulator to represent a fault at different locations along the emulated single transmission line.

2) Single Transmission Line Connected With Two Nonideal Voltage Sources Scenario: In order to verify the single-transmission-line emulation stability, two nonideal voltage sources are connected with the transmission line by setting the voltage-source impedances L_1 to 5.97 mH, R_1 to 0.65 Ω, L_2 to 2.4 mH, and R_2 to 0.07 Ω. Similar to the power HIL

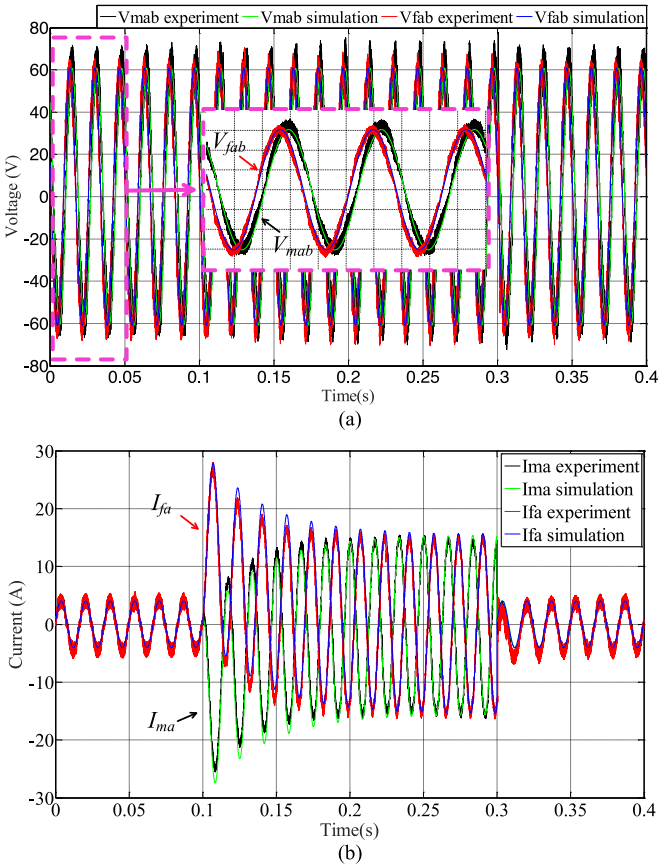

Fig. 22. Single-transmission-line experiment and simulation comparison with $\gamma = 1/2$. (a) V_{ab}. (b) I_a.

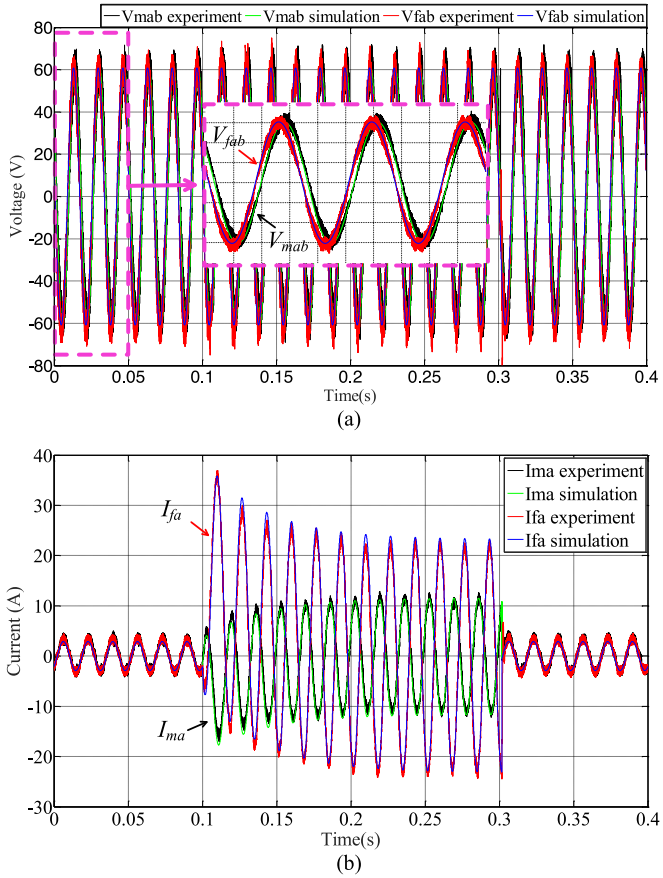

Fig. 23. Single-transmission-line experiment and simulation comparison with $\gamma = 2/3$. (a) V_{ab}. (b) I_a.

interface algorithm, the transmission line emulation instability usually happens at the frequency range higher than the fundamental frequency. In order to simplify the analysis, the inductance is employed to judge the transmission line emulation stability, since the resistance is negligible compared to the reactance in the high-frequency range. According to (10), the transmission line emulation is assured to be stable under normal conditions if the transmission line inductance L is larger than 5.97 mH + 2.4 mH = 8.37 mH. According to (14), the transmission line emulation is assured to be stable under fault conditions if the inductance between the fault location and the Master terminal γL is larger than 5.97 mH and the inductance between the fault location and the Follower terminal ((1-γ) L) is larger than 2.4 mH.

Fig. 24(a) shows the experiment and simulation result comparison of I_a when the transmission line inductance and resistance are $L = 8.5$ mH (> 8.37 mH) and $R = 0.25\,\Omega$, respectively. The three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 0.71$ (0.71×8.5 mH $= 6.035$ mH > 5.97 mH and 8.5 mH – 6.035 mH $= 2.465$ mH > 2.4 mH) when the phase angle of V_{mab} is 73°. Fig. 24(b) and (c) shows the experiment and simulation result comparisons of I_a when the transmission line inductance and resistance are $L = 10$ mH (> 8.37 mH) and $R = 0.3\,\Omega$, respectively. Fig. 24(b) shows the case when a three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 0.6$ (0.6×10 mH $= 6$ mH > 5.97 mH and 10 mH – 6 mH $= 4$ mH > 2.4 mH) when the phase angle of V_{mab} is 197°. Fig. 24(c) shows the case when a three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 0.75$ (0.75×10 mH $= 7.5$ mH > 5.97 mH and 10 mH – 7.5 mH $= 2.5$ mH > 2.4 mH) when the phase angle of V_{mab} is 177°. The transmission line emulation is stable when (10) and (14) are satisfied.

B. Fault Emulation of Parallel-Connected Transmission Lines

The system diagram for the parallel-connected transmission line experiment verification is shown in Fig. 25. The equivalent inductance and resistance of all parallel-connected transmission lines are L and R, respectively. The equivalent inductance and resistance of the normal transmission lines are L_n and R_n, respectively, and the equivalent inductance and resistance of the faulted transmission lines are L_s and R_s, respectively, as shown in Fig. 25. The three-phase short-circuit fault happens at the location γ ($0<\gamma<1$), which is the ratio of the distance from the fault location to the Master-side terminal with regard to the total line length.

1) Parallel-Connected Transmission Lines Connected With Two Ideal Voltage Sources Scenario: In order to verify the transmission line emulation performance by connecting to two ideal voltage sources, the voltage-source impedances are set to zero (L_1, R_1, L_2, and R_2 equal to zero). A transmission line diagram with three parallel-connected transmission lines is selected to verify the fault emulation of parallel-connected transmission lines. The total inductance and resistance of three

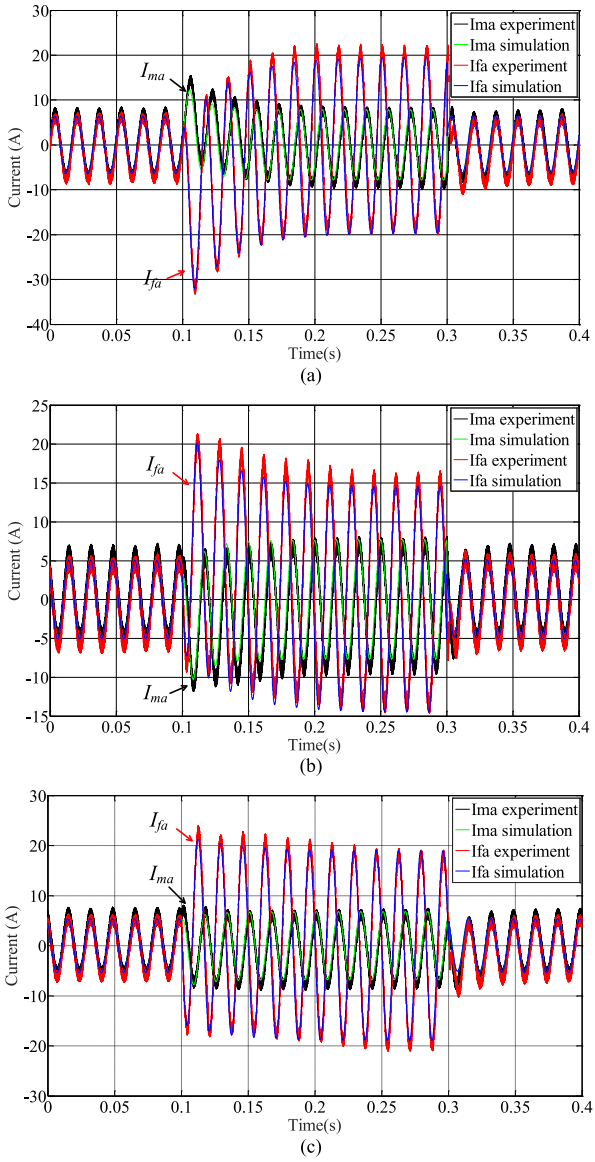

Fig. 24. Single-transmission-line experiment and simulation comparison under the nonideal voltage-source condition. (a) $L = 8.5\,\text{mH}$ and $\gamma = 0.71$. (b) $L = 10\,\text{mH}$ and $\gamma = 0.6$. (c) $L = 10\,\text{mH}$ and $\gamma = 0.75$.

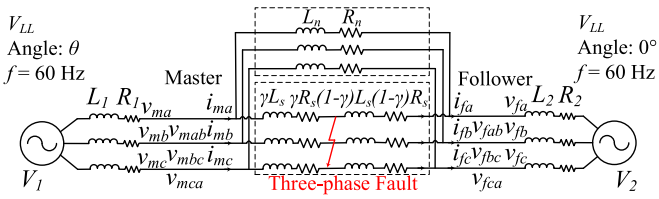

Fig. 25. System topology for parallel-connected transmission line experimental verification.

parallel–connected transmission lines are $L = 12\,\text{mH}$ and $R = 0.3\,\Omega$, respectively. The inductance and resistance of each transmission line are 36 mH and 0.9 Ω, respectively. Two of the transmission lines are normal and the three-phase short-circuit fault happens within one of the transmission lines. Thus, the normal line inductance and resistance are $L_n = 18\,\text{mH}$ and $R_n = 0.45\,\Omega$, respectively. Three fault scenarios with γ equals

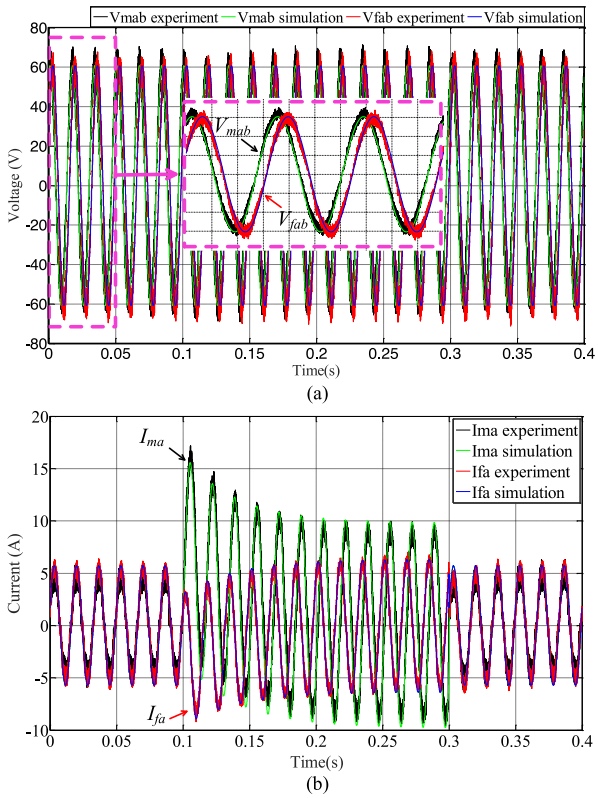

Fig. 26. Parallel-connected transmission line experiment and simulation comparison with $\gamma = 1/3$. (a) V_{ab}. (b) I_a.

to 1/3, 1/2, and 2/3, respectively, are tested to verify the three-phase short-circuit fault emulation capability at different locations within the emulated transmission line.

a) Three-phase short-circuit fault with $\gamma = 1/3$: A three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 1/3$ when the phase angle of V_{mab} is 65°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 43°$. The fault is cleared at 0.3 s. Fig. 26(a) and (b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

b) Three-phase short-circuit fault with $\gamma = 1/2$: A three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 1/2$ when the phase angle of V_{mab} is 350°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 41°$. The fault is cleared at 0.3 s. Fig. 27(a) and (b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

c) Three-phase short-circuit fault with $\gamma = 2/3$: A three-phase short-circuit fault happens at 0.1 s at the location $\gamma = 2/3$ when the phase angle of V_{mab} is 350°. The angle difference between the two voltage sources is $\theta = \theta_{V1} - \theta_{V2} = 33°$. The fault is cleared at 0.3 s. Fig. 28(a) and (b) show the experiment and simulation result comparisons of V_{ab} and I_a, respectively, which indicate that the experimental waveforms match well with the simulation results.

According to the above comparisons, the experiment waveforms match with the simulation waveforms when a three-phase

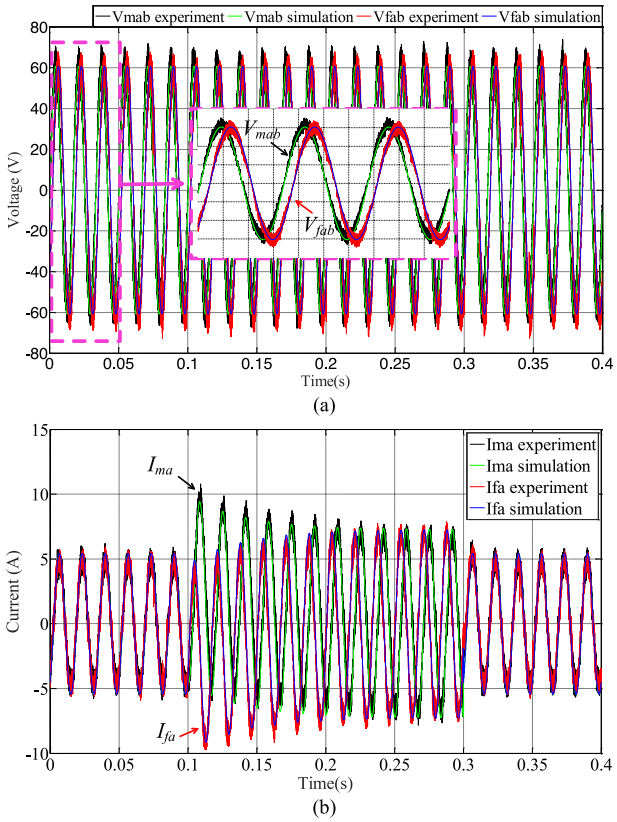

Fig. 27. Parallel-connected transmission line experiment and simulation comparison with $\gamma = 1/2$. (a) V_{ab}. (b) I_a.

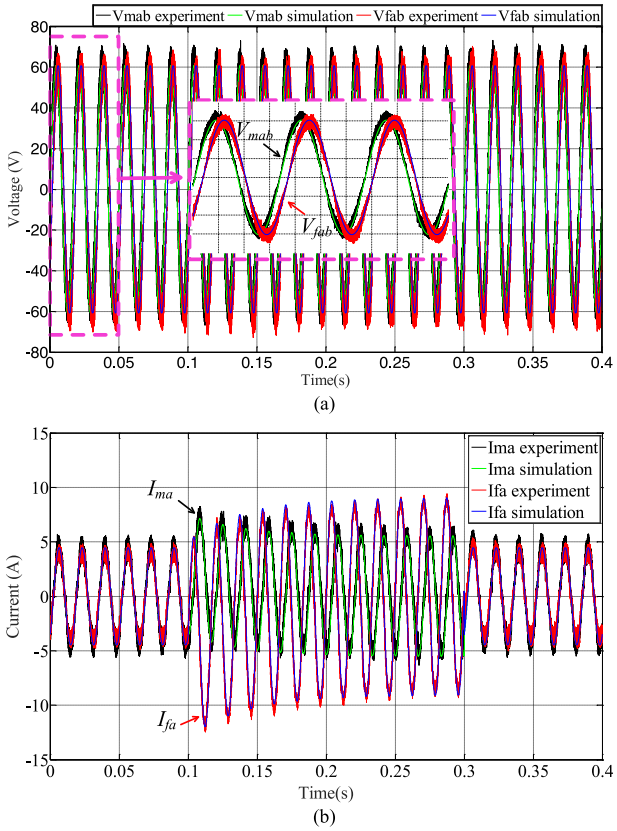

Fig. 28. Parallel-connected transmission line experiment and simulation comparison with $\gamma = 2/3$. (a) V_{ab}. (b) I_a.

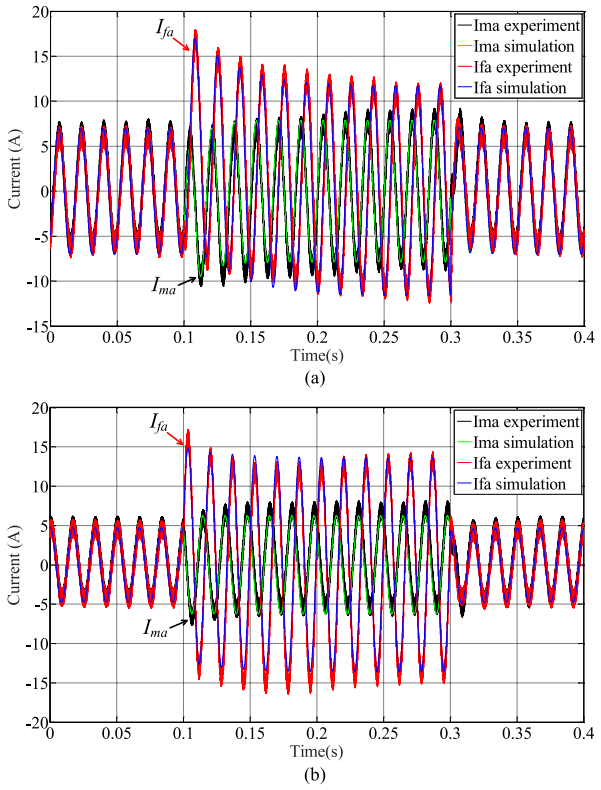

Fig. 29. Parallel-connected transmission line experiment and simulation comparison under the nonideal voltage-source condition. (a) $L = 8.5$ mH and $\gamma = 0.5$. (b) $L = 8.5$ mH and $\gamma = 0.7$.

short-circuit fault happens at the locations of γ equals to 1/3, 1/2, or 2/3, which verifies the three-phase short-circuit fault emulation capability of the developed transmission line emulator to represent a fault at different locations along one of the emulated parallel-connected transmission lines.

2) Parallel-Connected Transmission Lines Connected With Two Nonideal Voltage Sources Scenario: In order to verify the parallel-connected transmission line emulation stability, two nonideal voltage sources are connected with the transmission line by setting the voltage-source impedances L_1 to 5.97 mH, R_1 to 0.65 Ω, L_2 to 2.4 mH, and R_2 to 0.07 Ω. The whole transmission line equivalent inductance and resistance are $L = 8.5$ mH and $R = 0.25\,\Omega$, respectively. The normal transmission line equivalent inductance and resistance are $L_n = 17$ mH and $R_n = 0.5\,\Omega$, respectively. The faulted transmission line equivalent inductance and resistance are $L_n = 17$ mH and $R_n = 0.5\,\Omega$, respectively.

Fig. 29(a) and (b) show the experiment and simulation result comparisons of I_a when a three-phase short-circuit fault happens at 0.1 s with the fault location γ equals to 0.5 and 0.7, respectively. Similarly, the inductance is employed to judge the transmission line emulation stability. When γ equals 0.5, $(L_1||\gamma L_s) + (L_2||(1-\gamma)L_s) = 5.38\,\text{mH} < L_n = 17\,\text{mH}$ satisfies (15), $((L_2||(1-\gamma)L_s + L_n))||L_1 = 4.54\,\text{mH} < \gamma L_s = 8.5\,\text{mH}$ satisfies (16), and $((L_1||\gamma L_s) + L_n)||L_2 = 2.15\,\text{mH} < (1-\gamma)L_s = 8.5\,\text{mH}$ satisfies (17). When γ equals 0.7, $(L_1||\gamma L_s) + (L_2||(1-\gamma)L_s) = 5.61\,\text{mH} < L_n = 17\,\text{mH}$ satisfies (15), $((L_2||(1-\gamma)L_s + L_n))||L_1 = 4.52\,\text{mH} <$

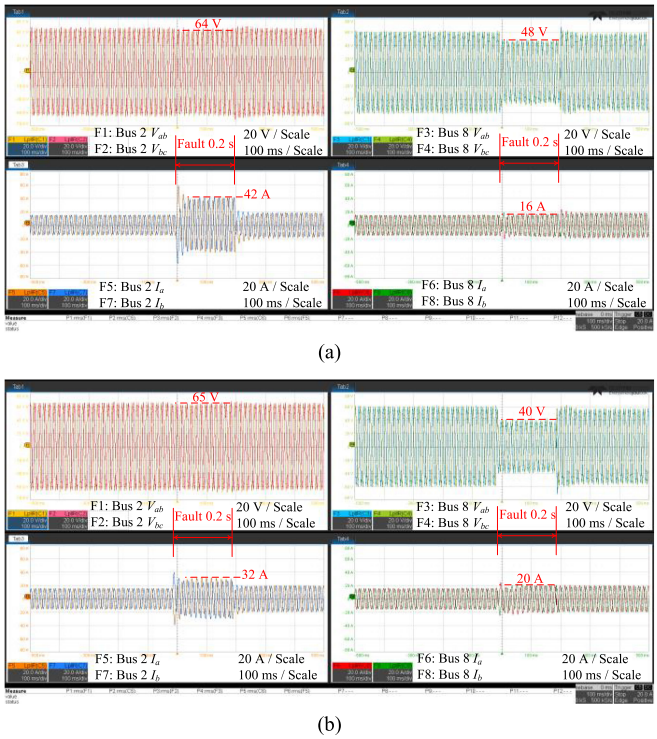

Fig. 30. Transmission line terminal voltage and current waveforms under a three-phase short-circuit fault at different locations within one of the three parallel-connected transmission lines. (a) $\gamma = 0.33$. (b) $\gamma = 0.67$.

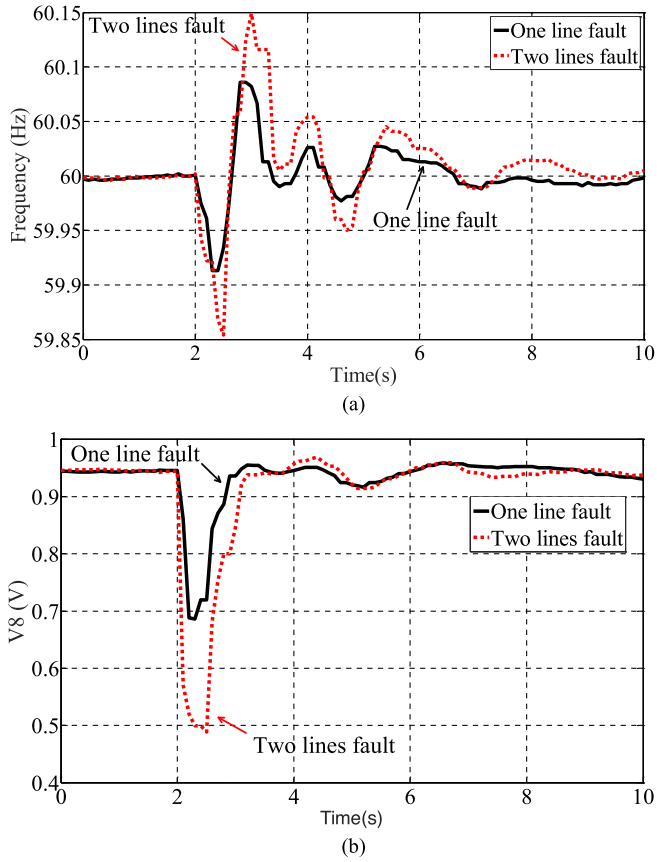

Fig. 31. System performance comparisons between the one-line fault and the two-line fault of the three parallel-connected transmission lines. (a) System frequency comparison. (b) Bus-8 voltage comparison.

$\gamma L_s = 11.90\,\text{mH}$ satisfies (16), and $((L_1||\gamma L_s) + L_n)||L_2 = 2.15\,\text{mH} < (1-\gamma)L_s = 5.1\,\text{mH}$ satisfies (17). The transmission line emulation is stable when (15)–(17) are satisfied.

C. Transmission Line Fault Emulation Application in a Real System Scenario

The simplified future WECC system with a hypothetical three-terminal HVDC overlay in Fig. 2 is scaled and emulated in the HTB for system studies. The transmission line between Buses 2 and 8, named as Line 2-8, is emulated by the transmission line emulator. The Line 2-8 is composed of three parallel-connected transmission lines, and the scaled total equivalent inductance and resistance are 3.2 mH and 0.08 Ω, respectively. The transmission line emulators Master side and Follower side are connected to Buses 2 and 8, respectively. The fault location γ represents the ratio of the distance from the fault location to Bus 2 with regard to the total line length. The transmission line emulator is employed to study the impacts of the fault location and the number of faulted lines on the system behaviors.

1) Fault Location Impact Study: A three-phase short-circuit fault happens at the location γ in one of the three parallel-connected transmission lines. Fig. 30 shows the transmission line terminal voltages and currents. Channels "F1" and "F2" are V_{ab} and V_{bc} at the terminal of Bus 2. Channels "F3" and "F4" are V_{ab} and V_{bc} at the terminal of Bus 8. Channels "F5" and "F7" are I_a and I_b at the terminal of Bus 2. Channels "F6" and "F8" are I_a and I_b at the terminal of Bus 8. Fig. 30(a) and (b) show the waveforms with the fault location $\gamma = 0.33$ and $\gamma = 0.67$, respectively. According to the waveforms, the fault currents at the terminal of Bus 2 decrease as the fault location γ increases, and the fault currents at the terminal of Bus 8 increase as the fault location γ increases. The Bus-8 voltage decreases as the fault location γ increases. The Bus-2 voltage does not change much during the fault with the increase of the fault location γ. This is because Bus 2 is supported by a synchronous generator G_2, which maintains the terminal voltage by the excitation control.

2) System Impact Study With a Different Number of Faulted Lines: Two cases are conducted where a three-phase short-circuit fault happens at the middle ($\gamma = 0.5$) of the transmission line for 0.4-s fault duration.

Case 1 (One-line fault): The fault happens in one of the three parallel-connected transmission lines.

Case 2 (two-line fault): The fault happens in two of the three parallel-connected transmission lines.

Fig. 31(a) and (b) show system frequency comparison and the Bus-8 voltage comparison between the one-line fault and two-line fault cases, and the fault happens at 2 s. The two-line fault creates a larger impact on the system, since the frequency and voltage deviations during the fault transient are large.

VI. Conclusion

In this paper, the fault model of a single transmission line has been proposed to realize three-phase short-circuit fault emulation at different locations along the emulated transmission line. By switching the input of the integrator for current reference

calculation, a combined transmission line model is proposed to avoid the switching transient between the normal and fault conditions. Furthermore, the fault model of parallel-connected transmission lines has also been proposed and implemented in the transmission line emulator to emulate a three-phase short-circuit fault within one of the parallel-connected transmission lines. Experiment results verified the proposed transmission line model and the effectiveness of the developed transmission line emulator with three-phase short-circuit fault emulation capability. This fault emulator will assist electric grid planners in the design and control of future transmission grids that have high penetration levels of renewable energy (wind and solar).

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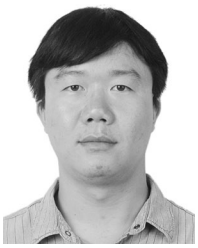

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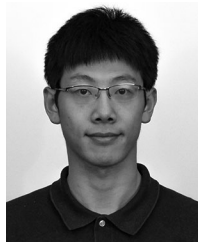

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