Design and Evaluation of a Reconfigurable Stacked Active Bridge DC–DC Converter for Efficient Wide Load Range Operation

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***Abstract*—This paper presents the design and implementation of a large-step-down soft-switched dc–dc converter based on the active bridge technique, which overcomes some of the limitations of the conventional dual active bridge converter. The topology comprises a double-stacked bridge inverter coupled to a reconfigurable rectifier through a special three-winding leakage transformer. This particular combination of stages enables the converter to run in an additional low-power mode that greatly increases light-load efficiency by reducing core loss and extending the zero-voltage switching range. The converter is implemented with a single compact magnetic component, providing power combining, isolation, voltage transformation, and energy transfer inductance. A 175 kHz, 300 W, 380–12 V GaN-based prototype converter achieves 95.9% efficiency at full load, a peak efficiency of 97.0%, an efficiency above 92.7% down to 10% load, and an efficiency above 79.8% down to 3.3% load.**

***Index Terms*—DC–DC power conversion, magnetic cores, phase control, transformer windings.**

I. Introduction

THERE is a growing need for high-efficiency, large-step-down dc–dc converters as dc loads and distribution systems become more prevalent. DC–DC converters allow for easier integration with dc systems such as solar panels, microgrid interfaces, LED lighting, and electric vehicle battery systems [1]–[3]. In addition, they are also used in dc distribution systems for data centers, where a high voltage (e.g., 380 V) must be converted down to a much lower voltage (e.g., 12 V) to provide power to server racks. These converters must maintain high efficiency across a wide load range, as servers can often remain in low current or idle states depending on computational demand.

High-voltage (here, hundreds of volts), large conversion ratio converters required by these applications face several challenges, such as large device switching loss and magnetic core loss. Soft-switching techniques such as zero-voltage switching (ZVS) or zero-current switching (ZCS) are often used to minimize switching losses. However, for many such converters, soft-switching can only be achieved under specific operating conditions, and the converters will lose soft-switching when operating outside of these conditions.

One popular topology for these applications is the dual active bridge (DAB) converter, which consists of two phase-shifted full bridges connected across a transformer and energy transfer inductance. The DAB is popular due to its ability to operate bidirectionally, its high power density, low component count, soft-switching capability for both input and output bridges, isolation, and high efficiency [4], [5]. In addition, it can be operated at a fixed frequency under a simple phase-shift control scheme [4]. The DAB converter achieves very high efficiencies at high power where the converter achieves ZVS. However, core loss stays constant (for a given voltage conversion ratio) as power decreases, and therefore can represent a significant portion of total loss at light-load conditions. In addition, the DAB can lose ZVS at low currents, or when the operating voltage ratio deviates substantially from the ideal transformation ratio, as described in [5]. However, many of the above-mentioned applications experience large input voltage or load variation, making it difficult to achieve ZVS over all desired operating conditions using the traditional DAB topology.

There has been a significant amount of work done to extend the soft-switching range of the DAB in order to increase efficiency at light loads, including more complex control schemes, dead time optimization, variable inductance or frequency techniques, and burst-mode control; these are reviewed below.

A. Alternative Control Schemes

Standard phase-shift control can result in high conduction and switching losses when operating away from nominal conditions

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[6]. There are various waveform shaping control methods (e.g., [6]–[8]) that involve generating three-level transformer voltages with arbitrary duty cycles to reduce reactive power in the transformer and decrease switching loss. These control schemes can also introduce switching states where the inductor current is zero in order to achieve ZCS. However, while ZCS eliminates overlap losses, it does not necessarily eliminate the CV^2 losses associated with the charging and discharging of device output capacitances as the switch and its parasitic capacitance swing from 0 V to its OFF-state drain-to-source voltage, and vice versa. Furthermore, these control schemes may not apply to the entire operating range, and many are designed for full-bridge topologies, precluding the use of stacked bridge architectures, which can offer several performance benefits as described in Section II.

B. Dead Time Control

As described in [9] and [10], the actual value of the switching dead times can have a large impact on efficiency, especially at low loads or where the voltage transfer ratio is far from the nominal transformer turns ratio. This is because the dead time can influence the actual value of the phase shift applied across the energy transfer inductance, and—at low powers—can dramatically affect the actual output power delivered. Additionally, if the dead time is longer than the amount of time required to charge or discharge the device output capacitances given the inductor current, the converter can experience additional losses due to body diode conduction or partial hard-switching due to resonant ring down on the switch drain-to-source voltage. There are several methods to adaptively control the dead time as a function of output power, (e.g., [9]–[11]), but these increase control and sensing circuitry complexity. Although not a subject of this paper, the authors note that the effect of dead time can also be significant at any power level in converters operated at frequencies where the dead time could be on the same order of magnitude as the time shift between the primary-side waveforms and the secondary-side waveforms.

C. Variable Inductance and Frequency Control

The leakage inductance value also heavily influences the DAB's ZVS capability, as achieving ZVS requires that the stored energy in the leakage inductance at the switching transition be equal to or higher than the stored energy in the output parasitic capacitances of the devices being switched [5], [12]. However, a high leakage inductance can result in a high rms-to-average current ratio for the converter, resulting in higher conduction losses and lower efficiency at full load. Therefore, work has been done to try to vary the leakage inductance and current as a function of the load to allow the DAB converter to be optimized for high efficiency at both full- and light-load conditions [12].

Some methods involve physically reconfiguring the leakage inductance, which requires additional control and physical components [12], [13], while other methods involve varying the frequency as a function of the desired output power. In variable frequency methods, lower frequencies are used at higher powers to reduce the required phase shift, and therefore rms currents, while higher frequencies are used at lower powers to increase the required phase shift and allow the inductor current to ramp up to a high enough value to achieve ZVS [12]. However, this class of approaches makes it harder to optimize the magnetics and filter design [14].

D. Burst-Mode Control

Another method to increase the current at the switch transition in low-power operation is burst-mode control. Here, the converter is turned ON and OFF at a burst frequency that is much lower than the converter's switching frequency. Burst-mode control for the DAB converter is explored in [12] and [15]. Using burst-mode control, the converter is operated under its full-load condition during the ON-time, so that the leakage inductor current is high enough to achieve ZVS, increasing the efficiency of the converter at light loads. However, transient events when the converter turns ON and OFF can deviate substantially from the ideal operating waveforms. Additionally, at very low powers where the converter is only on for a small percentage of the burst period, these transients can represent a significant portion of the converter ON-time, resulting in decreased efficiency.

E. Proposed Approach

This paper refines and expands upon an earlier conference publication [16], proposing a new converter topology that is optimized for high efficiency at high power as well as under light-load conditions, and as such is especially attractive for the 380–12 V conversion required for data center applications. The topology presented here provides a number of benefits resulting from its stacked inverter design, reconfigurable rectifier, and compact single-core three-winding leakage transformer. These components also allow for operation in a low-power operating mode designed to further increase light-load efficiency. Furthermore, the converter prototypes presented here all operate at a fixed dead time and fixed frequency, greatly simplifying the control (though more complex control techniques such as adaptive dead time, variable-frequency operation, and burst-mode control could be additionally applied to both operating modes if desired, further extending the high-performance operating range).

Section II describes the architecture and proposed control scheme, Section III provides simulated comparisons of the proposed topology and more traditional DAB architectures, and Section IV describes the implementation of several prototype converters and presents experimental results. Finally, Section V summarizes the paper. Analysis of the core loss in the low-power mode is provided in Appendix A, while simulation results for transitions between the full-power and low-power modes are provided in Appendix B.

II. Theory of the Proposed Architecture

Fig. 1 shows a conventional single-phase DAB topology [4], which consists of two full bridges that are phase shifted from each other across a transformer with some leakage inductance L_{lk}. The phase shift ϕ is used to control the output power, which

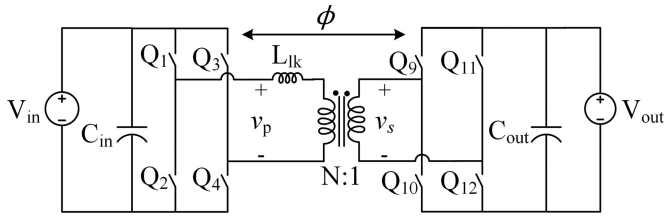


Fig. 1. DAB converter with a full-bridge input and output. The two bridges are phase shifted from each other across a transformer and an inductance $L_{\rm lk}$.

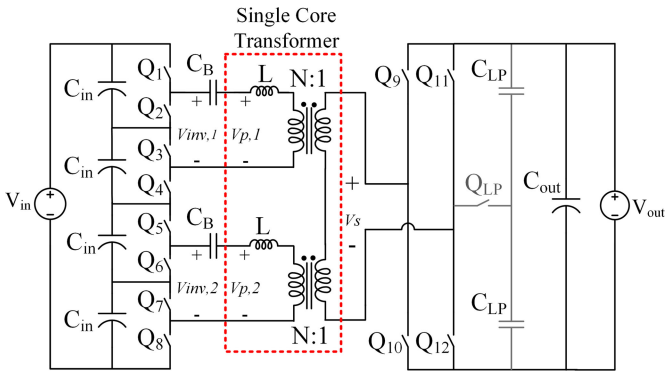


Fig. 2. Double-stacked active bridge (DSAB) topology. The dashed red box contains an equivalent circuit model for the single magnetic component. Each of the stacked bridges feeds a primary winding of a single-core, three-winding transformer. A blocking cap C_B is used to remove the dc component in the square-wave output of each stacked bridge. The total primary-referred leakage inductance is modeled as being split between the two primaries (with L on each primary, for a total primary-referred leakage inductance of $L_{\rm lk} = 2L$). An auxiliary switch $Q_{\rm LP}$ in the rectifier allows for a mode switch into a low-power mode.

can be expressed as

$$P_{\rm out} = \frac{V_p V_s N}{2\pi f_s L_{\rm lk}} \phi \left(1 - \frac{\phi}{\pi}\right) \tag{1}$$

where V_p is the effective primary voltage, V_s is the effective secondary voltage, N is the transformer turns ratio, f_s is the switching frequency in Hz, $L_{\rm lk}$ is the primary-referred leakage inductance, and ϕ is the phase shift in radians.

A limitation of the traditional DAB is that it can lose ZVS under light-load conditions when the current is insufficient to provide the required voltage transitions given the device output capacitance [5]. The proposed topology, referred to here as the double-stacked active bridge (DSAB) converter, addresses this limitation, and can achieve high efficiency over a wide power range because 1) its stacked inverter design reduces the voltage across each switch, decreasing the energy stored in the device capacitance and allowing for the use of lower voltage rated devices with lower device capacitance, both of which allow the converter to achieve ZVS at lower currents, and 2) the converter can operate in a low-power mode, which both reduces core loss and gating loss, and further extends the ZVS range.

The DSAB topology is shown in Fig. 2. It comprises a double-stacked bridge inverter coupled to a reconfigurable rectifier via a special three-winding leakage transformer, represented here by the model given in the dashed red box. Each stacked

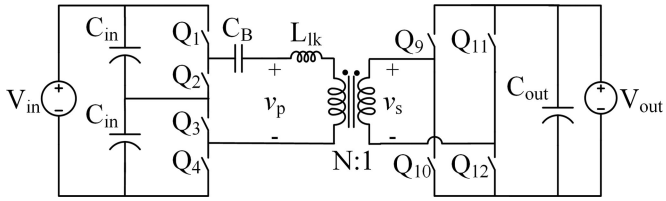


Fig. 3. DAB converter with a stacked full bridge on the input and a full bridge on the output. A blocking cap C_B is used to remove the dc component in the square-wave output of the stacked bridge.

full-bridge inverter feeds into a primary winding. The stacked full bridge can be viewed as a conventional full bridge with the two half-bridges stacked on top of each other, so that the top and bottom devices (Q_1 and Q_4 in the top stacked full bridge in Fig. 2) are switched complementarily to the middle devices (Q_2 and Q_3) to generate a square-wave output that swings from zero to half the applied dc voltage (e.g., as in [17]). For circuit analysis purposes, the three-winding transformer can be modeled as two transformers whose secondaries are connected in series. However, this model can be physically implemented by a single two-primary, single-secondary magnetic structure, as described later in the paper. The secondary winding then feeds into a reconfigurable rectifier, also described in a later section.

A. *Double-Stacked Bridge Inverter*

The converter uses "double stacking" of two stacked full-bridge inverters to achieve efficient high-voltage conversion. A double-stacked inverter has multiple benefits:

1) it decreases the individual inverter device voltage ratings, improving overall device performance;
2) it decreases the CV^2 energy stored in the device capacitance, making ZVS easier to achieve for lower inductor currents and reducing the switching loss in the case where ZVS cannot be achieved; and
3) the two stacked inverters enable additional switching patterns that allow for a low-power mode designed to increase light-load efficiency.

The reader will appreciate that one can use different converter topologies that can generate a multilevel waveform, such as stacked multilevel inverters, to implement the inverter stage. The stacked full-bridge inverter was deemed the most appropriate for this application due to the simplicity and symmetric nature of its drive signals and waveforms.

The decrease in inverter device rating can be seen by comparing Figs. 1–3. The devices $Q_1 - Q_4$ in Fig. 1 must be rated for the full input voltage $V_{\rm in}$. By comparison, switches $Q_1 - Q_4$ for an active bridge converter with a single-stacked bridge inverter, as shown in Fig. 3, are rated for $V_{\rm in}/2$, while switches $Q_1 - Q_8$ for the proposed double-stacked topology in Fig. 2 are only rated for $V_{\rm in}/4$.

Lower voltage rated devices can demonstrate much better switching performance due to lower parasitic ON-state resistance, device output capacitance, or both. This can be seen by the general increase in the device figure-of-merit of ON-state resistance multiplied by device output capacitance $R_{\rm ds,on}C_{\rm oss}$,

which is proportional to BV_{DSS}^{k} where BV_{DSS} is the breakdown voltage of the device and k is some exponent, $k > 2$ [18]. As this relationship grows superlinearly, stacking more devices can have lower loss associated with the switches due to the lower (and more favorable) figures-of-merit. Stacked topologies are especially attractive at higher input voltages, such as the 380 V application for which this converter is designed.

The figure-of-merit $R_{\text{ds,on}}C_{\text{oss}}$ was chosen to characterize the switching performance of the devices in this topology. This figure-of-merit precisely relates to the conduction loss in some high-frequency inverters, such as the classical Class E inverter [19], and represents two main loss mechanisms in the proposed topology's switches: 1) a higher $R_{\text{ds,on}}$ results in higher conduction loss, and 2) higher C_{oss} results in more energy stored in the parasitic device output capacitances. For hard-switched conditions, this means more power dissipated to charge and discharge C_{oss} during switch transitions. This loss (or a portion of it) will be present in a ZVS converter if the converter ever loses soft-switching.

In soft-switched applications such as the proposed topology, C_{oss} is charged and discharged inductively (i.e., with some inductance resonating with the output capacitance), so this energy does not contribute to power loss in the switch. However, a higher C_{oss} will require a greater amount of current to complete the necessary voltage transitions on the output capacitance in the given transition time (i.e., dead time) in order to achieve ZVS, as described in [5]. The minimum leakage inductor current $i_{l,\min}$ required to ensure that the voltage transitions are fully completed within the given dead time for the DSAB converter can be written as follows:

$$i_{l,\min} = 2C_{\text{oss}}\left(\frac{dV_c}{dt}\right) = 2C_{\text{oss}}\left(\frac{\frac{V_{\text{in}}}{4}}{dt_{\text{sw}}}\right) \tag{2}$$

where dV_c is the change in voltage on the switch capacitance and dt_{sw} is the dead time, which is the time in which the voltage transition must occur into order to achieve ZVS. The minimum leakage current can also be expressed in terms of the leakage inductance and device capacitance by balancing the energy stored in the leakage inductance and that required to charge and discharge the device capacitance, as shown in [5]. The result is

$$i_{l,\min} = 2 \cdot (dV_c) \cdot \sqrt{\frac{C_{\text{oss}}}{L_{\text{lk}}}} \tag{3}$$

where L_{lk} is the primary-referred leakage inductance of the transformer. For the DSAB converter, this leakage inductance is half that for either the single-stacked DAB or the full-bridge DAB for a given total primary-referred inductance (i.e., $L_{\text{lk}} = 2L$, when comparing Figs. 1 and 3 to Fig. 2). ZVS requires that $dV_c = V_{\text{in}}/4$ for the DSAB converter, as V_{ds} of each switch swings from 0 to $V_{\text{in}}/4$. In comparison, dV_c is two times higher for the single-stacked DAB and four times higher for the full-bridge DAB. This analysis neglects the device turn-OFF time and assumes that the switch capacitance voltage changes very little during this turn-OFF time, but illustrates how larger values of dV_c and C_{oss} require higher minimum currents for a given dead time to achieve ZVS.

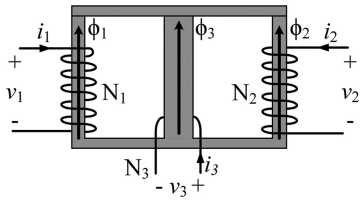


Fig. 4. Winding diagram of the three-winding transformer. The primary windings are wound around the outer legs (windings 1 and 2), while the secondary is wound around the middle leg (winding 3) of an E-I core. In standard operation, let $v_1 = v_2 = v_p$, $v_3 = -v_s$, $N_1 = N_2 = N$, and $N_3 = 1$.

While the dead time can be lengthened to allow the inductor current a longer time to ramp up to a higher peak value, this increases conduction losses. Also, as given in (3), there is a current level below which no amount of dead time is sufficient to provide ZVS, as there is not enough energy in the leakage inductance to fully transition the device voltages.

As devices that have very low values of $R_{\text{ds,on}}$ typically have higher values of C_{oss} due to the semiconductor construction, minimizing the product of $R_{\text{ds,on}}C_{\text{oss}}$ is a reasonable metric to use to minimize the overall losses associated with the switches. Because one of the main goals of this work is to demonstrate a topology with high efficiency even at light loads, devices with low $R_{\text{ds,on}}C_{\text{oss}}$ and C_{oss} values were preferentially chosen. More detail on the device selection process can be found in a later section as well as in [20].

B. Single Magnetic Component

The transformer structure in the DSAB converter is a special three-winding transformer that provides power combining, voltage transformation, isolation, and energy transfer leakage inductance all in a single compact planar printed circuit board (PCB) magnetic structure. Because the transformer structure and the energy transfer inductance can be implemented by the same core structure, this can reduce losses associated with additional discrete inductors, such as winding and interconnect losses and inductor core loss. Additionally, this combined planar structure can provide space or weight savings for the overall converter.

The three-winding, three-core-leg transformer has two primary windings, both of which are coupled to a single secondary winding. This can be physically realized in a single magnetic structure by winding each primary around the outer leg of an E-I core, and winding the secondary around the middle leg, as shown in Fig. 4. The transformer windings have a turns ratio of $N_1 : N_2 : N_3 = N : N : 1$, where N_1 and N_2 are the number of turns in the primary windings and N_3 is the number of turns in the secondary winding.

A simplified magnetic circuit model neglecting reluctance paths outside the core is shown in Fig. 5. $N_1 i_1$ through $N_3 i_3$ represent the magnetomotive forces of each winding, while $\mathcal{R}_1$ through $\mathcal{R}_3$ represent the reluctances of the core for each leg (where the horizontal sections of the core have been lumped into the reluctance terms for each leg for simplification). In the limit where the core reluctances are very small, and given $N_1 = N_2 = N$ and $N_3 = 1$, we can write $Ni_1 = Ni_2 = i_3$. Further analysis of this simple magnetic circuit then yields the

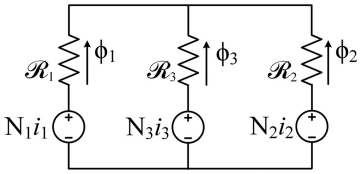


Fig. 5. Magnetic circuit model for the three-winding transformer. $N_1 i_1$, $N_2 i_2$, and $N_3 i_3$ represent the magnetomotive forces of each winding, while $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$ represent the reluctances of the core for each leg.

following idealized voltage relations:

$$\frac{v_1}{N_1} + \frac{v_2}{N_2} + \frac{v_3}{N_3} = \frac{v_p}{N} + \frac{v_p}{N} - \frac{v_s}{1} = 0 \tag{4}$$

where v_1 through v_3 and N_1 through N_3 are defined as in Fig. 5, v_p is the voltage on each primary winding, v_s is the voltage on the secondary winding, and N is the primary-to-secondary turns ratio, as shown in Fig. 2. Equation (4) can be rearranged to arrive at the following relationship, which states that the secondary voltage is the sum of the two primary voltages, transformed by the primary-to-secondary turns ratio, $N:1$

$$\frac{2v_p}{N} = v_s \rightarrow \frac{2v_p}{v_s} = N. \tag{5}$$

The leakage inductance is realized by the same physical structure, yielding an equivalent circuit model as shown in the dashed red box in Fig. 2. In this model, each primary winding is assigned an identical leakage inductance L. A more complicated model for multiwinding transformers could be used (e.g., see the cantilever model in [21]), but the symmetric topological structure and drive of this transformer make this model adequate for this analysis. The leakage inductance arises from the fact that a substantial portion of each primary winding lies outside the core, resulting in substantial fringing fields in that region. More details about the physical implementation of this leakage inductance are provided in Section IV.

C. Operating Modes

The DSAB converter can be operated in both a full-power mode (normal operation) and a low-power mode designed to decrease switching and core losses. The mode can be changed by adjusting the inverter and rectifier switching patterns and closing or opening an auxiliary switch Q_{LP}, shown in Fig. 2.

1) Full-Power Mode: From (4), it is apparent that the effective primary voltage is the sum of the voltages applied to each primary winding. The effective secondary voltage is that applied by the rectifier. For an input V_{in}, the voltage on each primary v_p will be a square wave of amplitude $V_{\mathrm{in}}/4$, assuming the two bridges have evenly balanced input voltages. For a full-bridge rectifier, the secondary winding voltage v_s is a square wave of amplitude V_{out}. Therefore, under full-power mode operation with both stacked bridge inverters operating in a square-wave mode and the rectifier operating as a full-bridge rectifier, the output power characteristic is given by

$$P_{\mathrm{out,FP}} = \frac{\left(\frac{V_{\mathrm{in}}}{4} + \frac{V_{\mathrm{in}}}{4}\right) V_{\mathrm{out}} N}{2\pi f_s (2L)} \phi \left(1 - \frac{\phi}{\pi}\right) \tag{6}$$

where $2L$ is the total primary-referred leakage inductance of the transformer, as shown in Fig. 2, V_{in} is the dc input voltage, V_{out} is the dc output voltage, f_s is the switching frequency in Hz, and ϕ is the phase shift between the inverter and rectifier in radians.

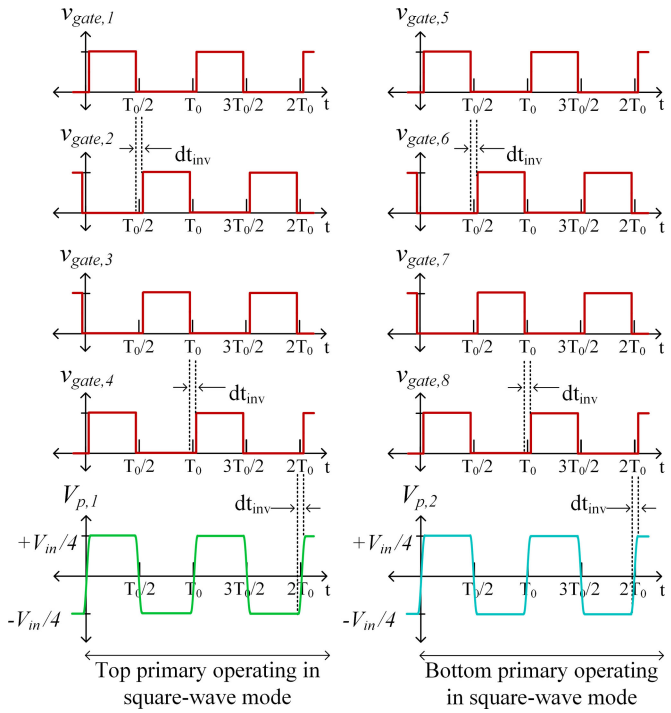


Fig. 6. Switching diagram for the inverter and primary winding voltages, while the converter is operating in the full-power mode.

Fig. 6 shows the switching waveforms for the inverter gate drive signals $v_{\mathrm{gate},1}$ through $v_{\mathrm{gate},8}$ for inverter devices Q_1 through Q_8, and the resulting primary waveforms $V_{p,1}$ and $V_{p,2}$. Both primaries are energized with in-phase square waves of the same amplitude, and these individual primary waveforms are summed to produce an effective primary voltage of amplitude $V_{\mathrm{in}}/2$. The dead time between inverter switches, labeled dt_{inv}, is required to prevent shoot-through and allow time for ZVS transitions (i.e., for the voltage on the device capacitances to fully transition).

Fig. 7 shows the full-power mode switching waveforms for the rectifier gate drive signals $v_{\mathrm{gate},9}$ through $v_{\mathrm{gate},12}$ for rectifier devices Q_9 through Q_{12}. The rectifier is driven as a full bridge, and the auxiliary switch Q_{LP} is held open during full-power mode operation (not shown in Fig. 7). The rectifier waveforms are shifted from the inverter waveforms by a time t_{shift}, which is related to the phase shift by the expression $\phi = 2\pi f_s t_{\mathrm{shift}}$. The dead time between rectifier switches, labeled dt_{rect}, prevents shoot-through and allows for ZVS transitions.

2) Low-Power Mode: A challenge of the traditional DAB converter is that as the power decreases, so does the current available to ensure ZVS transitions. The proposed converter can

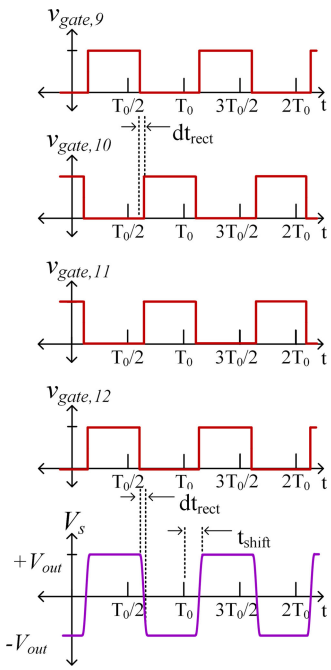


Fig. 7. Switching diagram for the rectifier secondary voltage, while the converter is operating in the full-power mode.

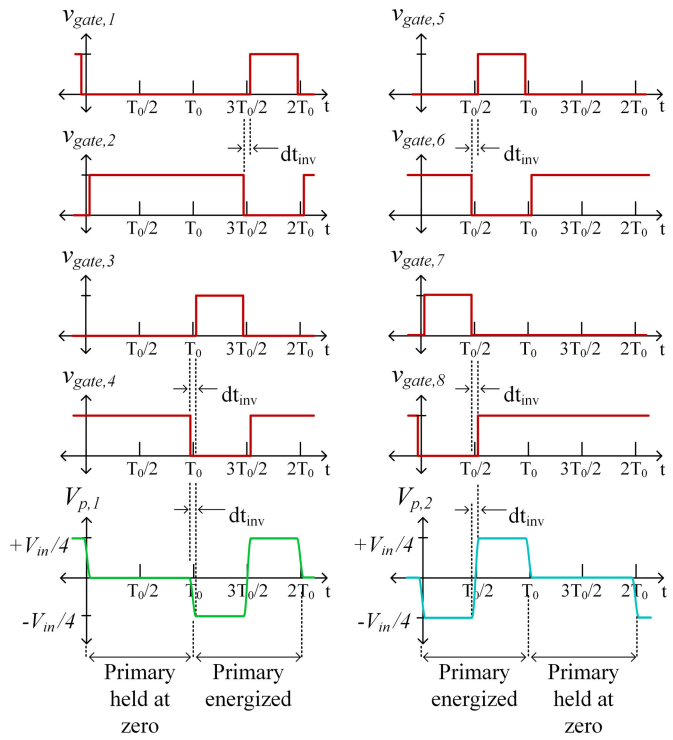


Fig. 8. Switching diagram for the inverter and primary winding voltages, while the converter is operating in the low-power mode.

be configured in a low-power mode that increases the current at the switch transitions, by taking advantage of the two-primary magnetic structure in order to energize the primaries in an alternating manner. This operation mode could not be achieved with a single inverter with one primary winding.

The low-power mode is designed to operate naturally at a lower power. Power reduction is achieved by effectively halving the net voltages at the transformer primary and secondary. The inverter is configured to only energize one primary at a time while holding zero voltage on the other primary. To maintain charge balance on the input capacitors as well as to fully utilize the transformer core, the proposed control scheme alternates which primary is energized or shorted (held at zero voltage) every other switching period. However, this alternation could be done on a longer time basis. Because the primary-side voltage of the transformer is effectively halved, it is necessary to reconfigure the rectifier to operate as a half-bridge rectifier by leaving Q_{11} and Q_{12} open and closing Q_{LP} so that the voltage seen across the secondary of the transformer is also halved (i.e., the amplitude is now only $V_{\mathrm{out}}/2$). In this way, the ratio of the primary-side voltage to the secondary-side voltage is still well-matched to the turns ratio of the transformer, a necessary condition for high performance in an active bridge converter.

Fig. 8 shows the low-power mode switching waveforms for the inverter gate drive signals $v_{\mathrm{gate},1}$ through $v_{\mathrm{gate},8}$ for inverter devices Q_1 through Q_8. Primary voltage $V_{p,1}$ is shown held at zero voltage for the first switching period. This is achieved by holding Q_2 and Q_4 closed, while Q_5 through Q_8 are switched in a normal stacked full-bridge fashion—that is, Q_5 and Q_8 are switched complementary to Q_6 and Q_7. (Note, Q_1 and Q_3 could be held closed instead, which would simply result in a change in polarity of the primary voltage waveforms.) To hold zero voltage

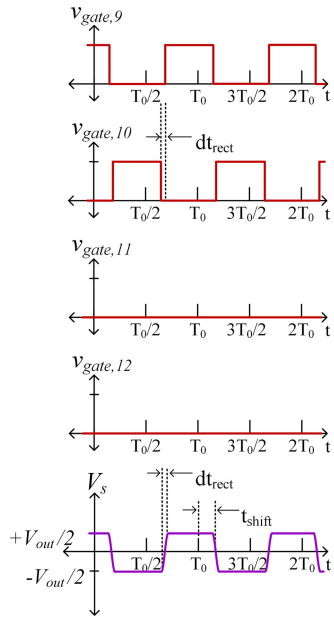


Fig. 9. Switching diagram for the rectifier secondary voltage, while the converter is operating in the low-power mode.

on the primary voltage $V_{p,2}$ during the second switching period, Q_6 and Q_8 are held closed, while Q_1 through Q_4 are switched. Since one primary is always held at zero, the total effective primary voltage is now half that of the full-power mode.

Fig. 9 shows the low-power switching waveforms for the rectifier gate drive signals $v_{\mathrm{gate},9}$ through $v_{\mathrm{gate},12}$ for rectifier devices Q_9 through Q_{12}. The rectifier is configured as a

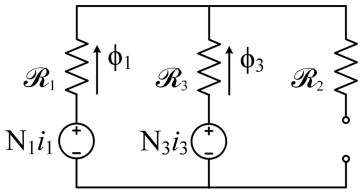


Fig. 10. Simplified magnetic circuit model for the three-winding transformer operating in the low-power mode, for the case when primary winding 2 is held at zero voltage, by connecting an ac short across it. Let $N_1 = N$ and $N_3 = 1$.

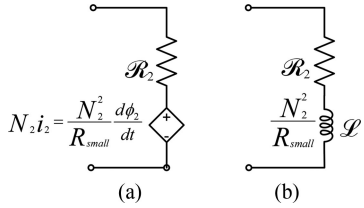


Fig. 11. (a) A model of the shorted winding (here, shown as winding 2), represented as a dependent source that produces a current i_2 to effectively cancel all flux in that leg. Nonidealities such as path resistance are represented by some small resistance R_{small}. (b) Equivalent transference model for the shorted winding, modeling it with some transference $\mathcal{L} = (N_2)^2/R_{\text{small}}$.

half-bridge rectifier by leaving Q_{11} and Q_{12} open and closing Q_{LP} so that the bottom terminal of the secondary winding is now connected to the midpoint of two series-connected capacitors, which are connected across the output such that each holds $V_{\text{out}}/2$ across it. The rectifier ac voltage now has an amplitude of $V_{\text{out}}/2$. The inverter and rectifier voltages are, therefore, both halved compared to the full-power mode, thereby maintaining the correct voltage transformation ratio across the transformer.

The output power characteristic for the low-power mode can be found by substituting the new values for the effective primary and secondary voltages into (1), and is given by

$$P_{\text{out,LP}} = \frac{\left(\frac{V_{\text{in}}}{4} + 0\right)\left(\frac{V_{\text{out}}}{2}\right) N}{2\pi f_s (2L)} \phi \left(1 - \frac{\phi}{\pi}\right). \tag{7}$$

As can be seen from (6) and (7), $P_{\text{out,LP}} = 1/4 P_{\text{out,FP}}$. For a given phase shift ϕ, the converter operating in the low-power mode, therefore, naturally delivers a quarter of the power compared to the full-power mode. Alternatively, this can be viewed as the low-power mode operating at a higher phase shift compared to the full-power mode for a given output power. This view highlights the ability of the low-power mode to extend the ZVS range by increasing the current available to charge and discharge the device output capacitances during the switch transition, as the inductor current is now given a longer time to ramp up.

a) Core loss in the low-power mode: In the traditional DAB converter topology, core loss remains constant over the entire load range for a given voltage transformation ratio, and therefore accounts for a substantial portion of total loss at low loads. The low-power mode proposed here decreases core loss by only energizing one primary (and exciting only one core leg) at a time. This also results in reduced flux density in the center leg of the core, due to the single-primary drive of the low-power mode.

A magnetic circuit model for the transformer operating in the low-power mode is shown in Fig. 10. For simplicity, the leakage flux outside the core is ignored. This circuit model represents the case where primary winding 2 is held at zero voltage. The total flux through this winding will, therefore, be zero. The winding will carry whatever current is necessary to keep net flux from flowing through it, which can be modeled in the ideal case by an open circuit in the flux path. The current flowing through the shorted primary is the same current flowing through the energized primary, minus the magnetizing current in the energized primary.

Fig. 11 shows a more detailed model of the open-circuited flux path in Fig. 10. The shorted winding can be modeled as a dependent source that generates the necessary current to cancel the flux flowing through its corresponding core leg, as shown in Fig. 11(a). The current generated is the observed $N_2 i_2$, such that

$$N_2 i_2 = \frac{N_2^2}{R_{\text{small}}} \left(\frac{d\phi_2}{dt}\right) \tag{8}$$

where R_{small} is some small resistance in the flux path. The dependent source can also be modeled by an equivalent transference model [22], as shown in Fig. 11(b), where winding 2 has some transference, given by

$$\mathcal{L} = \frac{N_2^2}{R_{\text{small}}}. \tag{9}$$

For our purposes here, the shorted winding can simply be treated as providing an open-circuit to the flux path. As shown in Appendix A, the low-power mode substantially reduces core loss, owing to the elimination of flux in one of the core legs and reduction of flux in the center post leg.

b) Switching loss in the low-power mode: The low-power mode naturally increases the converter currents for a given output power, thereby meeting the condition required for ZVS in (3) and extending the range of powers for which ZVS is achieved and increasing efficiency at light loads. Additionally, as can be seen by comparing Figs. 6 and 8, the low-power mode has fewer switching transitions on the inverter, which can further reduce CV^2 switching losses at ultralow powers where ZVS has been lost. Furthermore, gating losses are reduced because only one inverter stacked full bridge and one rectifier half-bridge are operated at a time. Because relatively low power is delivered in this mode relative to the conductor area available, conduction losses are also not severe.

D. Transitioning Between Modes

The converter can be started in either the full-power or low-power mode, which allows coarse-level matching of the operating mode to the load conditions. However, it is often desirable to be able to switch modes while the converter is running to account for dynamically changing load conditions. This is especially of importance for data center applications, where the load may change rapidly based on computational demand.

A simple hysteretic control method can be used, so that below a certain power level (ideally, the quarter-power point), the converter will operate in the low-power mode, and above a certain power level the converter will operate in the full-power mode. Ideally, the control will include some hysteresis to prevent the converter from repeatedly switching between modes if the demanded output power oscillates around the threshold power level for the mode switch, i.e., the quarter-power point.

In both modes, the phase shift between the input and output bridges is decreased to decrease the output power. As the phase shift decreases, the amplitude of the current through the leakage inductance will correspondingly decrease.

Let us denote the phase shift for the converter operating in the full-power mode in radians as

$$\phi_{\mathrm{FP}} = \frac{\pi - \sqrt{\pi^2 - \frac{4\pi P_{\mathrm{out}}}{x}}}{2} \tag{10}$$

where

$$x = \frac{\left(\frac{V_{\mathrm{in}}}{4} + \frac{V_{\mathrm{in}}}{4}\right)(V_{\mathrm{out}})\,N}{2\pi f_s\,(2L)}. \tag{11}$$

For a duration equal to $t_{\mathrm{shift}} = \phi_{\mathrm{FP}}/(2\pi f_s)$, the inductor current will ramp due to the applied voltage across it, with a slope given by

$$\frac{\Delta i_{L,\mathrm{FP}}}{\Delta t} = \frac{V_{\mathrm{in}}}{4L} + \frac{NV_{\mathrm{out}}}{2L}. \tag{12}$$

In practice, at very low powers where losses become more substantial, the actual phase shift required to achieve the desired output power can be higher than the theoretical phase shift due to dead time effects and other nonidealities. This can result in a difference between the predicted and actual phase shifts required for a given power at light-load conditions. For a given power level, an empirical value of the phase shift that includes the effects of dead time or other nonidealities can be used to determine both the transitional phase shift, as well as the phase shifts for steady-state operation.

During the low-power mode, the operating phase shift required for a given power is increased compared to that of the converter operating in the full-power mode, and the amplitude of the current, therefore, increases as well. The low-power phase shift in radians can then be expressed as

$$\phi_{\mathrm{LP}} = \frac{\pi - \sqrt{\pi^2 - \frac{4\pi P_{\mathrm{out}}}{y}}}{2} \tag{13}$$

where

$$y = \frac{\left(\frac{V_{\mathrm{in}}}{4} + 0\right)\left(\frac{V_{\mathrm{out}}}{2}\right)N}{2\pi f_s\,(2L)}. \tag{14}$$

During this phase shift, the inductor current will ramp with a slope of

$$\frac{\Delta i_{L,\mathrm{LP}}}{\Delta t} = \frac{V_{\mathrm{in}}}{8L} + \frac{NV_{\mathrm{out}}}{4L}. \tag{15}$$

We now present a method to use a transitional phase shift when switching operating modes to provide a smooth transition between the different phase shifts required for the full-power and low-power modes.

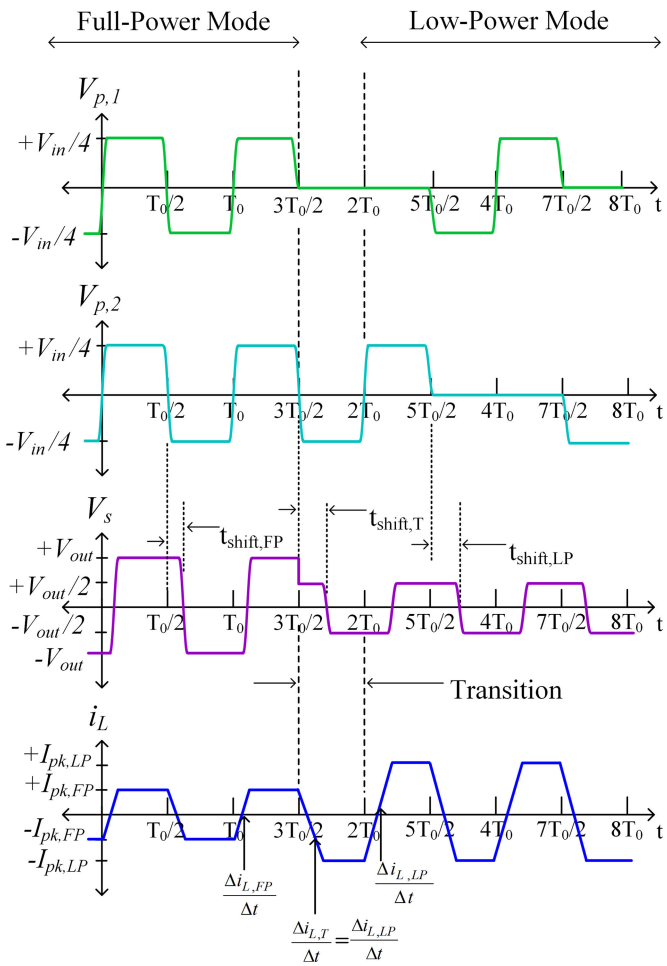


Fig. 12. Converter primary and secondary winding voltages and leakage inductor current, during a mode switch from the full-power mode to the low-power mode. The slopes of the inductor current waveform are labeled.

1) Transition from Full-Power to Low-Power Mode: Fig. 12 illustrates what the transformer primary and secondary voltages look like during the transition from full-power mode to low-power mode. The converter is shown initially operating in the full-power mode, with a phase shift between the primary and secondary voltages calculated according to the full-power mode power characteristic given in (6), and labeled as the time $t_{\mathrm{shift,FP}} = \phi_{\mathrm{FP}}/(2\pi f_s)$ in Fig. 12.

The transition from full-power mode to low-power mode is shown starting at $3T_0/2$, where T_0 is equal to the switching period $1/f_s$. At this point, the primary waveforms immediately switch into the low-power mode configuration, where each primary is alternately energized every other switching cycle. The rectifier also immediately switches from the full-power mode full-bridge rectifier to the low-power mode half-bridge rectifier by closing the auxiliary switch Q_{LP} and opening Q_{11} and Q_{12}. During the transition, the secondary waveforms are phase shifted by a transitionary time $t_{\mathrm{shift},T}$, which allows the primary inductor current to ramp down from $+I_{\mathrm{pk,FP}}$, its full-power mode amplitude, to $-I_{\mathrm{pk,LP}}$, its low-power mode amplitude. Af-

ter this transition time, the secondary waveform operates at the standard low-power phase shift, corresponding to the time $t_{\text{shift,LP}} = \phi_{\text{LP}}/(2\pi f_s)$ shown in Fig. 12.

Since the primary and secondary voltage waveforms switch to those of the low-power mode (at time $t = 3T_0/2$), the voltage across the inductor during the phase shift is dependent on the low-power mode primary and secondary voltages. Therefore, the time needed to ramp the inductor current from the full-power amplitude to the low-power amplitude is calculated using the low-power current slope given in (15).

In the full-power mode, the current would require the full phase-shift time $t_{\text{shift,FP}}$ to transition from $+I_{\text{pk,FP}}$ to $-I_{\text{pk,FP}}$, and only half that to go from $+I_{\text{pk,FP}}$ to 0. Because the slope of the inductor current in the low-power mode is half that of the slope of the inductor current in the full-power mode, it will take twice as long for the current to ramp a given amount in the low-power mode. Therefore, when transitioning from the full-power amplitude to the low-power amplitude, the current would require a time $t_{\text{shift,FP}}$ to transition from $+I_{\text{pk,FP}}$ to 0.

Since the low-power mode requires a time $t_{\text{shift,LP}}$ to transition from $+I_{\text{pk,LP}}$ to $-I_{\text{pk,LP}}$, when transitioning from full power to low power, an additional time of $1/2t_{\text{shift,LP}}$ is required to complete the transition from 0 to $-I_{\text{pk,LP}}$. Combining these, we can denote the total time for the transition from full power to low power mode as

$$t_{\text{shift},T} = t_{\text{shift,FP}} + \frac{1}{2}t_{\text{shift,LP}}. \tag{16}$$

This can be expressed as a transitional phase shift in radians, given by

$$\phi_T = \phi_{\text{FP}} + \frac{1}{2}\phi_{\text{LP}}. \tag{17}$$

2) Transition From Low-Power to Full-Power Mode: Fig. 13 illustrates what the transformer primary and secondary voltages look like during the transition from low-power mode to full-power mode. The converter is shown initially operating in the low-power mode, with a phase shift corresponding to a time $t_{\text{shift,LP}} = \phi_{\text{LP}}/(2\pi f_s)$ between the primary and secondary voltages. The transition from full-power mode to low-power mode is shown starting at $2T_0$ in Fig. 13. At this point, the primary waveforms immediately switch into the full-power mode pattern, where both primaries are simultaneously energized. As before, the rectifier also immediately switches modes, now from the low-power mode half-bridge rectifier to the full-bridge rectifier. This is achieved by opening the auxiliary switch Q_{LP} and switching Q_{11} and Q_{12} as in a full-bridge rectifier, along with Q_9 and Q_{10}.

During the transition, the secondary waveforms are phase shifted by a transitionary time $t_{\text{shift},T}$, which allows the primary inductor current to ramp down from $+I_{\text{pk,LP}}$, its low-power mode amplitude, to $-I_{\text{pk,FP}}$, its full-power mode amplitude. After this transition time, the secondary waveform then operates at the standard full-power phase shift, corresponding to the time $t_{\text{shift,FP}} = \phi_{\text{FP}}/(2\pi f_s)$, as shown in Fig. 13.

Because the primary and secondary voltage waveforms immediately switch to those of the full-power mode at the transition time (time $t = 2T_0$ in Fig. 13), the voltage across the inductor

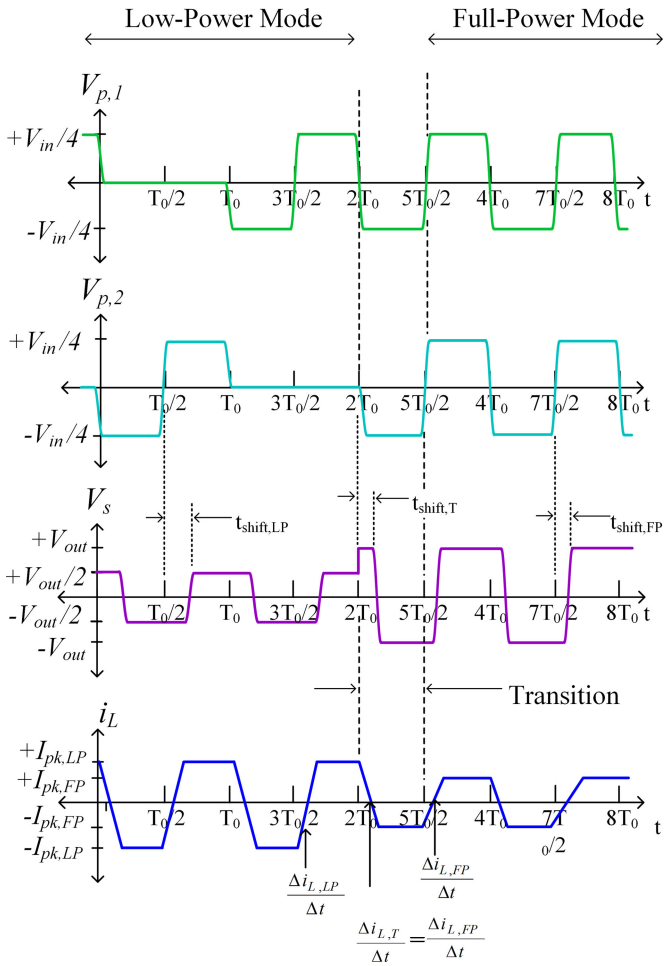


Fig. 13. Converter primary and secondary winding voltages and inductor current, during a mode switch from the low-power mode to the full-power mode. The slopes of the inductor current waveform are labeled.

for the phase shift is dependent on the full-power mode primary and secondary voltages (which are each double that of the low-power mode voltages). Therefore, the time needed to ramp the inductor from the full-power amplitude to the low-power amplitude is calculated using the full-power current slope given in (12).

In the full-power mode, the current would require the full phase-shift time $t_{\text{shift,FP}}$ to transition from $+I_{\text{pk,FP}}$ to $-I_{\text{pk,FP}}$. Since the slope of the full-power mode current is twice that of the low-power mode, it will only take $1/4t_{\text{shift,LP}}$ to transition from $+I_{\text{pk,LP}}$ to 0, and will then take a further $1/2t_{\text{shift,FP}}$ to transition from 0 to $-I_{\text{pk,FP}}$. Combining these terms, we can denote the total time for the transition between low-power and full-power mode as

$$t_{\text{shift},T} = \frac{1}{2}t_{\text{shift,FP}} + \frac{1}{4}t_{\text{shift,LP}}. \tag{18}$$

This can be expressed as a phase shift in radians, given by

$$\phi_T = \frac{1}{2}\phi_{\text{FP}} + \frac{1}{4}\phi_{\text{LP}}. \tag{19}$$

Both mode transitions were simulated using LTSpice, and the results are shown in Appendix B. The mode transitions

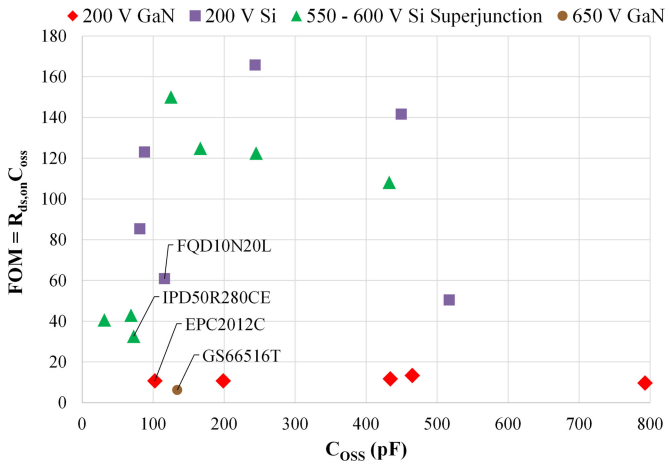


Fig. 14. Graph showing the figure-of-merit $R_{\text{ds,on}}C_{\text{oss}}$ versus C_{oss} for 200 V GaN devices, 200 V Si devices, 550 and 600 V Si superjunction devices, and 650 V GaN devices for the inverter.

demonstrate rapid settling in each direction across the transition boundary for both continuously adjusted power and for sudden load steps.

III. Simulation Comparison

Simulations of the DSAB topology, a single-stacked full-bridge DAB topology, and a traditional full-bridge DAB topology were performed using LTSpice, to validate the DSAB's operation and compare its performance to more traditional topologies. The three topologies were simulated with both GaN and Si inverter devices, and the DSAB was simulated in both the full-power and low-power modes. All three topologies were simulated over a wide load range, to assess the ZVS performance and efficiency at light-load conditions.

Fig. 14 shows a graph of the figure-of-merit $R_{\text{ds,on}}C_{\text{oss}}$ versus C_{oss} for several possible inverter devices, which was used to select the devices with the lowest combination of figure-of-merit and device capacitance for each topology and device technology combination.

In order to keep the inverter driver circuitry the same across prototypes, only devices that could be driven with the 6 V drive signals required by the GaN FETs were included in the analysis. From Fig. 14, it can be seen that the 200 V GaN EPC2012C device has a much lower figure-of-merit than the 200 V Si FQD10N20L device, although the 550 V Si superjunction IPD50R280CE has a figure-of-merit between the two, and a lower capacitance than either. This is because of its superjunction process, which uses a different device structure and doping method to achieve a much lower resistance and capacitance than in a traditional MOSFET structure; however, this technology is mostly applicable at high voltage, which limits the device voltage ratings offered. Table I also lists the values of $R_{\text{ds,on}}$ and C_{oss} for the selected inverter and rectifier devices used in each simulation to assess efficiency and ZVS performance across output power. The IPD50R280CE device has a much higher resistance than the EPC2012C device, so in the case that the application could support a higher cost or more exotic device, it would be more beneficial to use the GaN technology in the DSAB converter.

The asterisks in Table I denote that the device was only used in simulation and not in an experimental prototype for that particular topology. Of these simulations, the GaN and Si DSAB and the Si single-stacked DAB converters were experimentally implemented, and results are given in Section IV. All topologies were simulated at an input voltage of 380 V, an output voltage of 12 V, and a switching frequency of 175 kHz, which was selected as the finalized experimental switching frequency. The total primary-side inductance was simulated as 32 μH for all topologies; it is modeled as being evenly split into two 16 μH inductances for the double primary transformer. The converters were each simulated from the full-power value of 300 W down to 10 W, except for when simulating the low-power modes, where they were swept from 125 to 10 W. For the stacked full-bridge and DSAB topologies, the dead time was chosen to be large enough to allow for ZVS at low powers, but less than the maximum dead time, which if exceeded would result in losses due to body-diode conduction or resonant ring down. Efficiency values over a wide range of output powers were calculated by stepping the phase shift for each converter and device combination. Switch dead times were kept constant over the entire load range for each device type to simplify the simulation process. [20] provides greater detail about the general simulation setup and parameter settings, and also includes examples of LTSpice netlists and schematics in its Appendices.

A. Simulated Efficiency Results

Table II lists parameters associated with the ZVS performance of each converter, including the voltage across the device capacitance in the OFF-state V_c, which relates to switching loss, and the value of the primary-side leakage inductance L_{lk}, which determines the minimum inductor current required to ensure ZVS. In order to establish a benchmark for the switching losses of each topology independent of device voltage rating or technology, the energy stored and released each cycle by one switch can be expressed in terms of a constant effective switch capacitance $C_{\text{oss,eff}}$.

The energy for charging and discharging one switch is then given by $E_{C\text{oss,eff}} = C_{\text{oss,eff}}V_c^2$. Table II presents the total energy loss for the whole inverter for each topology, by multiplying $E_{C\text{oss,eff}}$ by the corresponding number of inverter devices. A portion of this loss would be present if the converter could not achieve full ZVS, and would be present in its entirety if the switches were completely hard-switched. The overall inverter CV^2 loss of the full-bridge converter is four times higher than that of the single-stacked DAB and eight times higher than that of the DSAB converter, even given the greater number of inverter switches in the DSAB converter; this reduction is so dramatic due to the energy loss being proportional to the voltage squared.

Table II also illustrates how the full-bridge DAB converter requires a higher minimum leakage inductor current $i_{l,\min}$ at the switching transition, where $i_{l,\min}$ is calculated using (3). Because the total primary-referred leakage inductance is divided between each primary for the DSAB converter, the inductance

TABLE I
DEVICE PARAMETERS FOR A SPICE MODEL

	Topology	Technology	Device	$R_{\text{ds,on}}$ (mΩ)	C_{oss} (pF)
Inverter	DSAB	GaN	EPC2012C	105	102.5
		Si	FQD10N20L	525	116
	Single-stacked DAB	GaN*	EPC2025	141.75	108.125
		Si superjunction	IPD50R280CE	450	72.5
Rectifier	Full-bridge DAB	GaN*	GS66516T	46.875	134
		Si superjunction*	IPD50R280CE	450	72.5
	All topologies	GaN	EPC2023	1.5	1854

The asterisk (*) denotes that the corresponding device technology and topology combination was only simulated, not experimentally tested. Only the GaN and Si DSAB and the Si superjunction single-stacked DAB were experimentally tested.

TABLE II
COMPARISON OF LOSS PARAMETERS BETWEEN TOPOLOGIES

	V_c	L_{lk}	$E_{C\,\text{oss,eff}}$ (Inverter)	$i_{l,\min}$
DSAB	$\frac{V_{\text{in}}}{4}$	L	$8\text{ devices}\cdot C_{\text{oss,eff}}(\frac{V_{\text{in}}}{4})^2 = \frac{1}{2}C_{\text{oss,eff}}V_{\text{in}}^2$	$2\cdot(\frac{V_{\text{in}}}{4})\cdot\sqrt{\frac{C_{\text{oss,eff}}}{L}} = \frac{1}{2}V_{\text{in}}\cdot\sqrt{\frac{C_{\text{oss,eff}}}{L}}$
Single-stacked DAB	$\frac{V_{\text{in}}}{2}$	$2L$	$4\text{ devices}\cdot C_{\text{oss,eff}}(\frac{V_{\text{in}}}{2})^2 = C_{\text{oss,eff}}V_{\text{in}}^2$	$2\cdot(\frac{V_{\text{in}}}{2})\cdot\sqrt{\frac{C_{\text{oss,eff}}}{2L}} = \frac{\sqrt{2}}{2}V_{\text{in}}\cdot\sqrt{\frac{C_{\text{oss,eff}}}{L}}$
Full-bridge DAB	V_{in}	$2L$	$4\text{ devices}\cdot C_{\text{oss,eff}}V_{\text{in}}^2 = 4C_{\text{oss,eff}}V_{\text{in}}^2$	$2\cdot V_{\text{in}}\cdot\sqrt{\frac{C_{\text{oss,eff}}}{2L}} = \sqrt{2}V_{\text{in}}\cdot\sqrt{\frac{C_{\text{oss,eff}}}{L}}$

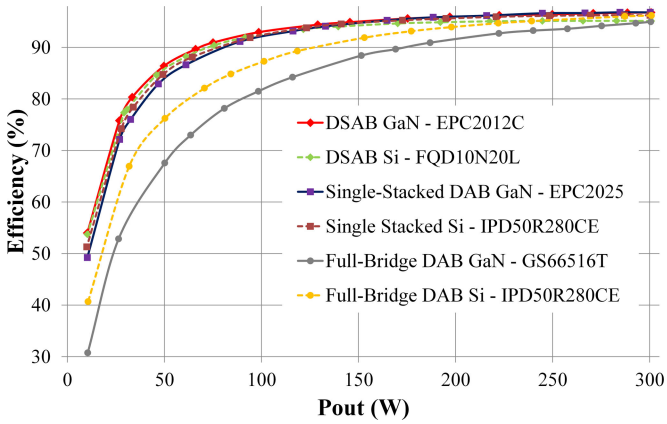


Fig. 15. Simulated efficiency curves for all topologies with all device combinations. The full-bridge DAB converter (shown in orange and gray) has much lower efficiency across the entire power range compared to the stacked topologies. While the single-stacked DAB has similar efficiencies to that of the DSAB at full power, it becomes much less efficient with decreasing output power, due to losing ZVS earlier than the DSAB converter.

that resonantly charges and discharges the device output capacitance of each stacked full bridge is only half that of the single-stacked and full-bridge DAB converters. However, because of the much smaller voltage across the device capacitance, the DSAB converter ends up having the smallest minimum inductor current, and therefore can achieve ZVS down to the lowest output power, assuming the same $C_{\text{oss,eff}}$ across all topologies and devices as before. Note, these relationships could be even more extreme in reality, as C_{oss} could decrease with voltage rating.

Fig. 15 shows efficiency curves for the three different topologies, with each topology simulated with both Si and GaN devices. The full-bridge topology shows significantly lower efficiency compared to both the single-stacked DAB and the DSAB topologies across the entire load range, but especially below 200 W. While both the DSAB and the single-stacked DAB converter can operate under ZVS over a large power range, the full-bridge converter does not achieve a high enough inductor current for ZVS even at full power and the maximum dead time. Additionally, the full bridge has larger CV^2 energy loss once hard-switching, due to the higher voltage across the device capacitance C_{oss}.

The effect of the device switching performance on efficiency can be seen in Table III, which compares some of the simulated losses in the inverter and transformer at 300 W for each topology and device combination. P_{loss} is the total loss at 300 W, P_{core} is the transformer core loss, P_{cond} is the inverter conduction loss, given for both a single FET and the entire inverter (also expressed as a percentage of P_{loss}), and $P_{C\,\text{oss}}$ is the inverter switching loss related to the charging and discharging of C_{oss}, given for a single FET and the inverter overall (also expressed as a percentage of P_{loss}). Table III also lists the minimum required inductor current $i_{l,\min,\text{ZVS}}$ and $P_{C\,\text{oss,hard-sw}}$ the total inverter switching loss if the inverter devices were entirely hard-switched (which would happen if ZVS were completely lost). These last two parameters do not represent the operating condition at 300 W, but rather worst case or limiting values for the switching performance of the converter.

The single-stacked and DSAB converters are zero-voltage switched and have no CV^2 switching loss. However, both the GaN and Si full-bridge converters cannot fully achieve ZVS even at 300 W, and partially hard-switch the voltage transition across the device capacitance. The GaN GS66516T has the worse switching loss of the two full-bridge converters, due to its

TABLE III
LOAD ANALYSIS AT FULL LOAD (300 W)

	Device	P_{loss} (W)	P_{core}		P_{cond}			P_{Coss}			ZVS PERFORMANCE PARAMETERS	
					FET	Inverter		FET	Inverter		$i_{l,min,ZVS}$ (A)	$P_{Coss,hard\text{-}sw}$ for Inverter (W)
			(W)	(% of P_{loss})	(W)	(W)	(% of P_{loss})	(W)	(W)	(% of P_{loss})		
DSAB	EPC2012C	10.0	6.9	**69.0**	0.16	1.27	**12.6**	0	0	**0**	0.48	1.30
	FQD10N20L	15.5	6.9	**44.7**	0.82	6.54	**42.2**	0	0	**0**	0.51	1.47
Single-Stacked DAB	EPC2025	9.9	6.9	**69.7**	0.21	0.85	**8.6**	0	0	**0**	0.70	2.73
	IPD50R280CE	11.5	6.9	**59.9**	0.68	2.73	**23.6**	0	0	**0**	0.57	1.83
Full-Bridge DAB	GS66516T	15.9	7.0	**43.8**	0.76	3.04	**19.1**	1.17	4.70	**29.5**	1.56	13.54
	IPD50R280CE	11.9	7.0	**58.3**	0.47	1.87	**15.6**	0.45	1.81	**15.1**	1.14	7.33

higher C_{oss} (134 pF compared to the IPD50R280CE's 72.5 pF), and therefore higher minimum required inductor current. The efficiency of the GS66516T full-bridge converter is significantly worse than the IPD50R80CE full-bridge converter (even given the latter's much lower $R_{ds,on}$), in part due to this much higher switching loss; additionally, the rms inverter switch current in the GS66516T was higher due to the presence of high current pulses at the switch transition, further increasing the overall loss compared to the IPD50R280CE converter. This illustrates that even though the overall figure-of-merit was very favorable for the GS66516T converter, it still had significant loss due to the higher switch voltages associated with a full-bridge topology.

At high powers, the GaN single-stacked DAB and the GaN DSAB topologies have similar efficiencies, as both have similar $R_{ds,on}$ and C_{oss} values (though the Si DSAB converter has the lowest overall efficiency at high load where resistive losses are largest, due to having the highest $R_{ds,on}$). However, as output power decreases, the GaN and Si single-stacked DAB converters start to lose ZVS, and therefore drop in efficiency compared to the GaN and Si DSAB converters. Although the devices used in both the Si and GaN single-stacked DAB converters have very low C_{oss} values, the minimum required leakage inductance current is larger than that of either the GaN or Si DSAB converters, due to the larger voltage that must be transitioned across the switches. The improved switching performance of the stacked topologies can also be seen by examining $P_{Coss,hard\text{-}sw}$ in Table III, which gives the switching loss if all inverter devices were completely hard-switched. Even though the DSAB converter has eight devices compared to the four devices of the single-stacked and full-bridge converters, it still has the lowest overall hard-switched energy loss. However, both the DSAB and the single-stacked converters have significantly lower $P_{Coss,hard\text{-}sw}$ than the full-bridge converters. The DSAB converter will, therefore, lose ZVS at a lower output power compared to the other two topologies, and once hard-switching, will have lower overall switching loss.

The resistive losses are also presented in Table III. These losses increase with switch current, and are, therefore, the highest at full load. However, they are mostly low in comparison with the total converter loss (with the exception of the high-$R_{ds,on}$ FQD10N20L device), as the inverter switches carry low currents (<2 A). For the stacked topologies (the DSAB and the single-stacked DAB), the GaN-based design had lower conduction loss than the Si-based design due to the lower $R_{ds,on}$.

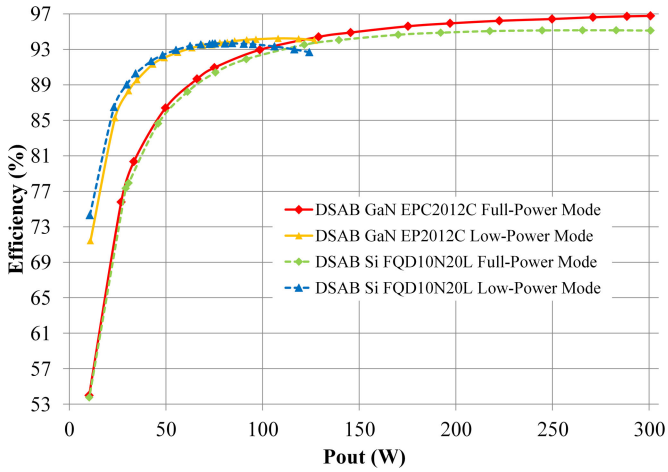


Fig. 16. Simulated efficiency curves for the Si and GaN DSAB converters operating in the full-power and low-power modes.

However, the GaN-based design for the full-bridge converter had higher total resistive losses, due to the presence of high current pulses in the inverter devices at the switching transitions that were much higher than those in the Si-based full-bridge converter, despite both experiencing hard-switching. The conduction losses greatly depend on the particular device technology; for example, even though the IPD50R280CE device is rated for 550 V, it has low overall figure-of-merit due to the superjunction construction. As conduction loss is not a huge portion of the overall loss, increased resistive losses can be traded for higher primary-side current, which increases the ZVS range of the stacked topologies.

The core loss P_{core} of all three topologies is the same when the DSAB is operating in the full-power mode, as the volt–seconds across the transformer is constant for the three converters (this can be seen more easily by recognizing that the secondary has the same voltage across all three topologies). However, as described in previous sections and Appendix A, the core loss is approximately halved for the DSAB converter when operating in the low-power mode, due to the reduced flux density in the core as a result of the alternating primary drive and reconfigured rectifier.

The low-power mode was simulated for both the GaN and Si DSAB converters. Fig. 16 shows simulated efficiency curves for the both the Si and GaN DSAB converters operating in the

full-power and low-power modes. The low-power mode has a simulated efficiency that is 7–10 percentage points higher than the full-power mode for output powers around 30 W, and 17–20 percentage points higher for output powers around 10 W, due to a reduction in core loss and hard-switching loss. Simulations also show that at the quarter-power point (75 W), the core loss represents approximately 90% of the overall loss in the full-power mode DSAB converter, while it is reduced to approximately 70% of the overall loss in the low-power mode. Additionally, the inverter devices are partially hard-switched in the full-power mode, while they still achieve ZVS in the low-power mode. As seen in Table III, the C_{oss} values for the Si and GaN devices were very close, so their ZVS behavior is very similar.

Based on the simulation results, the DSAB converter with GaN EPC2012C inverter devices was predicted to be the most efficient topology overall, and the DSAB's low-power mode showed significant improvement in efficiency at low output powers for both the Si and GaN versions.

IV. Experimental Validation

To illustrate the value of the proposed approach, we present results from multiple converters, all using the same core and PCB windings and designed for a nominal operating point of 380 V input, 12 V output at 300 W, and operating at 175 kHz. The three prototypes each have a different inverter stage, to allow for comparisons between device technologies as well as between a single-stacked inverter design and a double-stacked inverter design. These variations are

1) the proposed double-stacked topology with 200 V EPC GaN devices;
2) the proposed double-stacked topology with 200 V Fairchild Si MOSFETs; and
3) a DAB with a stacked inverter (see Fig. 3), using the same transformer design but with the two primaries connected in series to form one primary winding, and with 550 V Infineon superjunction Si MOSFETs.

The inverter devices were selected on the basis of minimizing the product $R_{\text{ds,on}}C_{\text{oss}}$ while preferentially selecting devices with low C_{oss} to allow the converter to achieve ZVS at lower powers. 200 V devices were chosen for the double-stacked converter to allow for some headroom on the blocking voltage. 550 V Si superjunction devices were chosen for the single-stacked topology even though the single-stacked full bridge inverter devices only needed to block (380 V)/2 = 190 V. This was because the superjunction devices offered a better $R_{\text{ds,on}}C_{\text{oss}}$ product than the available 250–300 V MOSFETs, and their standard DPAK package allowed the same Si-based DSAB converter PCB to be used, reducing prototyping costs. The design of each prototype is summarized in Table IV, and the top side of the GaN DSAB converter is shown in Fig. 17.

A. Transformer Design

A single core magnetic component was used to implement the three-winding transformer as well as the leakage inductance used to realize the energy transfer inductors; the design realizes the function modeled in the dashed red box in Fig. 2. The nominal operating point of the DSAB converter was chosen to satisfy the requirements for a 380 V dc bus in data centers with dc distribution, with a 380 V nominal input voltage (with 350–410 V input voltage range) and a constant 12 V output voltage [23]. Using (5) and the values of 380 and 12 V for the system input and output voltages, the transformer turns ratio was designed for the nominal condition so that

$$N = \frac{2v_p}{v_s} = \frac{190\text{ V}}{12\text{ V}} = 15.833 \approx 16 \tag{20}$$

TABLE IV
Components for Prototype Converters

Component	Description	Value / Device	
Q_1-Q_8	Inverter switch	DSAB GaN	EPC2012C
		DSAB Si	FQD10N20L
		Single-Stacked DAB Si[a]	IPD50R280CE
Q_9-Q_{12}	Rectifier switch	3x EPC2023 30 V/60 A eGaN FETs connected in parallel	
Q_{LP}	Low-power switch	2x EPC2023 30 V/60 A eGaN FET, source connected 2 sets in parallel	
N	Transformer turns ratio	16:1, primary-to-secondary	
L	Leakage inductance	32 µH total primary-referred[b] EPCOS EILP43-N49 core 8-layer PCB, 4 oz copper internal layers, 2oz copper external layers	
C_{in}	Input capacitors	DSAB	3x 3.3 µF 250 V ceramic
		Single-Stacked DAB	4x 2.2 µF 450 V ceramic
C_{out}	Output capacitors	12x 100 µF 16 V ceramic	
C_{LP}	Low-power capacitors	2x 100 µF 16 V ceramic 1x 1000 µF 16 V electrolytic	
C_B	Blocking capacitors	DSAB	2x 3.3 µF 250 V ceramic
		Single-Stacked DAB	2x 2.2 µF 450 V ceramic
C_{bal}	Balancer capacitors	1 µF 250 V ceramic	
D	Balancer diodes	Diode Array 300 V 225 mA 2 pair series connection	

[a] Single-stacked DAB only requires inverter switches Q_1-Q_4
[b] Value from experimental data, based on both impedance analyzer measurements across one primary with the other windings shorted and experimental power transfer data

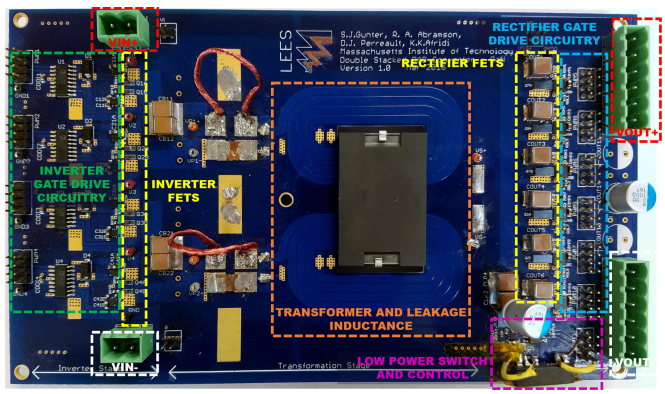


Fig. 17. Top side of the GaN-based DSAB prototype. The inverter and rectifier devices and control circuitry are labeled, as is the single-core magnetic component.

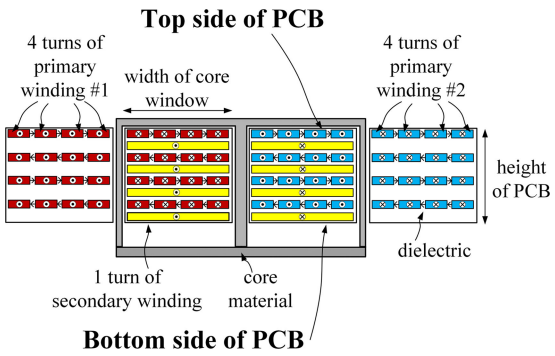


Fig. 18. Cross section of the magnetic core and PCB layer stack-up for the three-winding transformer. The red and blue primary windings are interleaved inside the core window with the yellow secondary windings.

where 16 was chosen as the closest integer value. The primary-to-secondary turns ratio is then 16:1.

For the reasons summarized in [24], a planar winding design was chosen to implement the three-winding leakage transformer. An 8-layer PCB stack-up was used to allow for interleaving between the primary and secondary windings to reduce ac resistance, as well as to allow for paralleled secondary windings to increase current carrying capability and decrease dc resistance. A simplified representation of the PCB stack-up is shown in Fig. 18. The primary windings are shown in red (primary winding #1) and blue (primary winding #2) and wrap around the outer legs; the secondary winding is shown in yellow and wraps around the center leg. The primary and secondary windings are interleaved inside the core window, but the primary windings on the outside of the core are not interleaved as there is no secondary winding in that section of PCB. Each primary winding has 16 turns, while the secondary only has one turn. Each primary has four dedicated PCB layers, and each layer contains four turns.

The four layers are then connected in series to form a total of 16 turns, as required. The secondary winding is also split over four layers. However, because it carries high current and only requires one turn, each trace is made almost as wide as the core window and the four secondary layers are then paralleled to further decrease dc resistance by increasing trace cross-sectional area. To reduce proximity effect and decrease ac resistance, the secondary and primary layers are fully interleaved. 4 oz. copper was used on the six internal PCB layers to mitigate skin effects, while 2 oz. copper was used on the external layers to allow for the required trace spacing and footprint width of the fine-pitch GaN devices. Further details can be found in [20] and [25].

The leakage inductance is also realized by this structure. A significant portion of the leakage arises due to the sections of primary winding that are outside the core window. These outside sections of winding generate magnetic field lines, which do not link to the secondary, increasing leakage inductance. The resultant leakage inductance depends on the area of primary windings that lie outside the core, which themselves depend on the core window width, as the width of the primary windings must not exceed this dimension in order to fit around the center post. Fig. 19(a) shows the main flux paths for the transformer, including these leakage paths. Fig. 19(b) shows the corresponding magnetic circuit model.

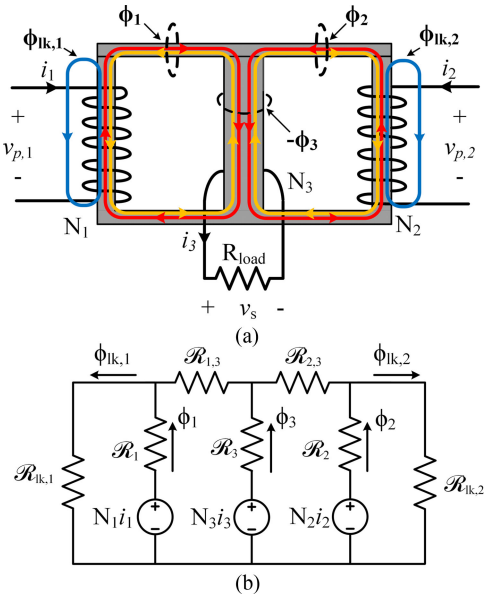


Fig. 19. (a) Diagram of the flux paths of the three-winding transformer. Fluxes ϕ_1 and ϕ_2 in the outer legs link the secondary, and $-\phi_3$ is the flux through the center leg. Fluxes $\phi_{lk,1}$ and $\phi_{lk,2}$ are the primary winding leakage fluxes that do not link to the secondary. (b) The equivalent magnetic circuit model that includes the primary-side leakage paths, as well as the main flux paths through the core legs.

The resulting leakage of this structure was measured on an impedance analyzer to be approximately 32 μH when referred to the primary side, so that $L = 16$ μH in Fig. 2. To verify this, the value of the total leakage was also found experimentally by operating the DSAB converter and using the power characteristic of (5) to back solve for L, given all other parameters. The switching frequency was chosen based on the measured leakage inductance in order to maximize efficiency for a given power level by balancing the effects of core loss—which decreased with frequency in the range of interest—and conduction and switching losses—which increased with frequency. A higher frequency would result in current waveforms that are more triangular than trapezoidal or square in nature, and therefore would have a higher rms value for a given mean value, resulting in a higher conduction loss.

B. Prototype Performance

Waveforms of the GaN-based DSAB converter running in the full-power mode and operating at the nominal operating point of 380 V input and 12 V output at 300 W are shown in Fig. 20. The top and bottom primary voltages can be seen to be right on top of each other, showing good voltage balancing between the inverters without the need for active balancing circuits. Small passive balancing circuits are used within each individual stacked full-bridge inverter (but not between the two inverters), as illustrated in Fig. 21; these circuits process negligible power. The current waveform is the desired flat-topped trapezoid.

Operating waveforms are also shown for the converter at one quarter of the rated output power. Fig. 22 shows a comparison of the waveforms for the GaN DSAB converter operating at 75 W (the quarter-power point) in (a) the full-power mode and (b) the low-power mode. As can be seen, the low-power mode

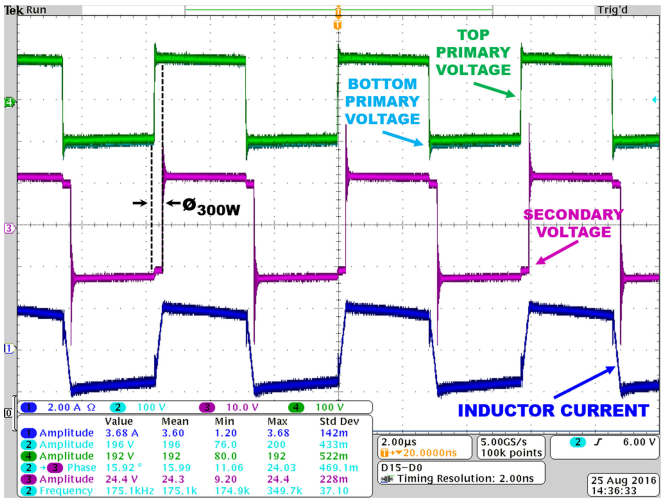


Fig. 20. Operating waveforms for the GaN DSAB converter operating in the full-power mode with an input voltage of 380 V, an output voltage of 12 V, and a phase shift of 17.2° to deliver 300 W (100% load).

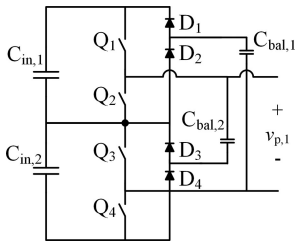


Fig. 21. Balancer circuit used to balance the input capacitors within one stacked full-bridge inverter. $C_{\text{in},1}$ and $C_{\text{in},2}$ are balanced with respect to each other using $C_{\text{bal},1}$ and $C_{\text{bal},2}$. Only the top inverter, connected to $V_{\text{inv},1}$ (as labeled in Fig. 2), is shown here; the same circuit is used on the bottom inverter. Values for the balancer components are presented in Table IV.

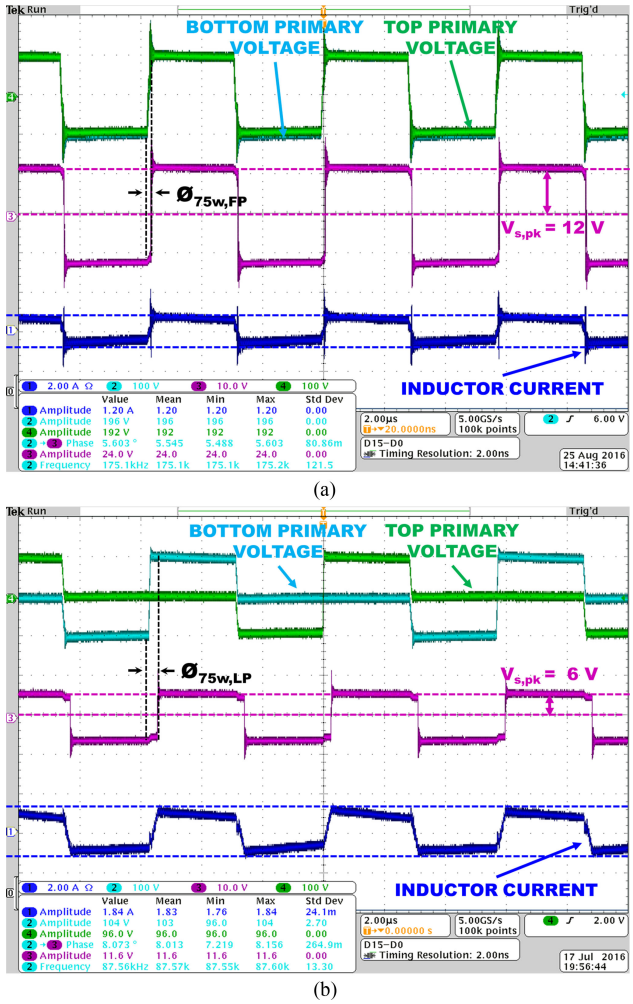


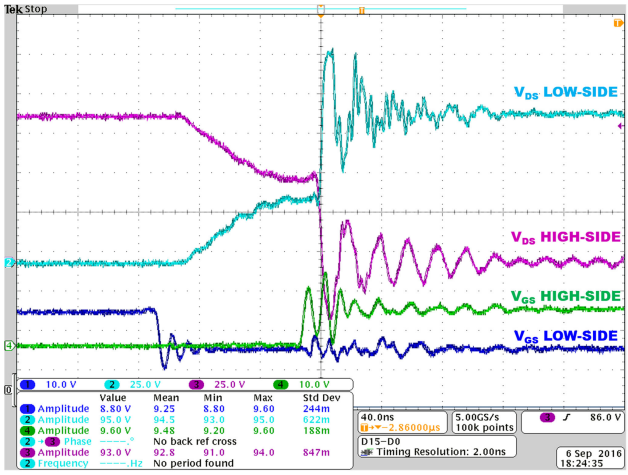
Fig. 22. Operating waveforms for the GaN DSAB converter with an input voltage of 380 V, an output voltage of 12 V, and an output power of 75 W in (a) full-power mode at a phase shift of 8.1° (0.141 rad), and (b) low-power mode at a phase shift of 18.0° (0.314 rad).

results in an increase in the peak inductor current relative to the full-power mode. The low-power phase shift $\phi_{75\ W,LP} = 18.0°$ (0.314 rad) is larger than the full-power phase shift $\phi_{75\ W,FP} = 8.1°$ (0.141 rad), so the inductor current is allowed to ramp longer, and therefore reaches a higher peak value. This results in the converter achieving ZVS down to a lower output power.

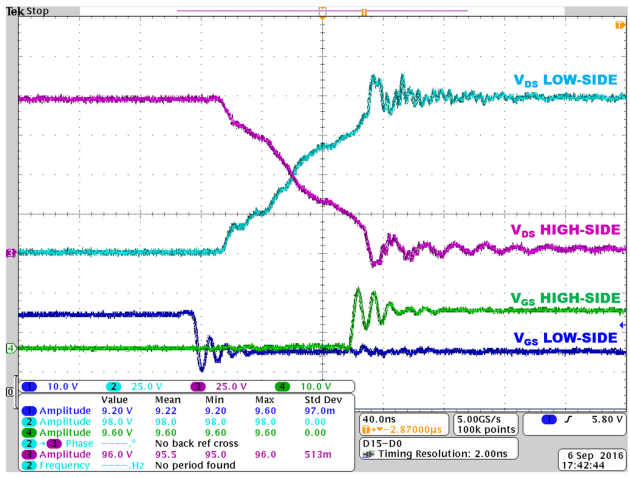
Fig. 23 shows a comparison of the switch transitions for the GaN DSAB converter in both full-power and low-power mode, by showing the V_{ds} and V_{gs} waveforms for the high-side and low-side devices in one inverter half-bridge. Fig. 23(a) shows the switch transition for the converter operating in the full-power mode at an output power of 75 W. The switches are hard-switched (with only a fraction of device capacitive energy saved), as evidenced by the large ringing on the V_{ds} waveform, and the fact that the V_{ds} voltage does not rise or fall all the way to its final value by the end of the dead time (where the dead time is the time when both top- and bottom-side V_{gs} signals are zero). Fig. 23(b) shows the converter operating in the low-power mode, also at 75 W. In the low-power mode, it was observed that the rise and fall transitions on the inverter devices had slightly different ZVS capability, possibly due to the asymmetry in the primary drive signals. The transition that achieved the least amount of soft-switching is shown here. As can be seen, however, most of the transition is still soft-switched, with only slight ringing on the V_{ds} waveform. The low-power mode was able to maintain ZVS on at least one of the rise and/or fall transitions down to 52 W, while the full-power mode started to lose ZVS around 150 W, demonstrating that the low-power mode was successful at maintaining ZVS down to a much lower power compared to the full-power mode.

The single-stacked DAB converter's ZVS performance was also investigated and performed worse than either the full-power or low-power modes of the GaN DSAB. While the single-stacked DAB was able to achieve ZVS at full power, by 50% load (150 W), the converter switch transitions were hard-switched for most of the transition, as shown in Fig. 24.

The Si DSAB converter's efficiency was further tested over a wide input range of 350–410 V to match the standard input voltage variation expected in a data center application. Fig. 25 shows the experimental efficiency of the Si DSAB converter from 350 to 410 V at an output power of 300 W. The efficiency stays above 94% over the entire voltage range, and increases



(a)



(b)

Fig. 23. V_{ds} and V_{gs} waveforms for an inverter half-bridge in the GaN DSAB converter operating at 75 W in (a) the full-power mode and (b) the low power mode. The low-power mode is able to mostly achieve soft-switching, while the full-power mode experiences substantial hard-switching.

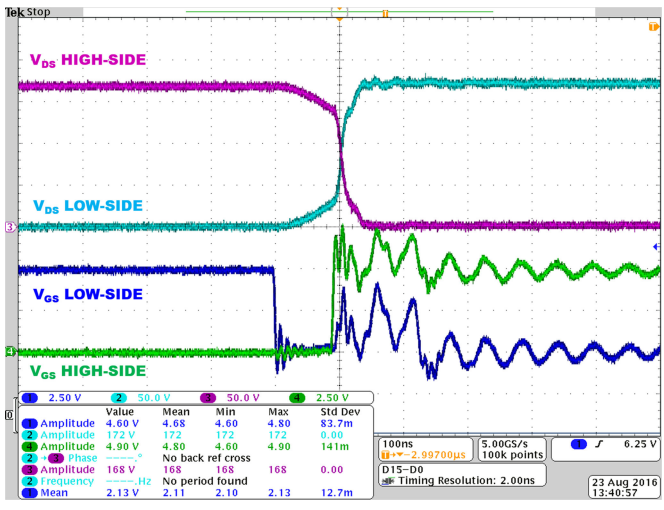


Fig. 24. V_{ds} and V_{gs} waveforms for an inverter half-bridge in the Si single-stacked DAB converter operating with an input voltage of 380 V, an output voltage of 12 V, and a phase shift of 14.7° (0.257 rad) to deliver 150 W. The switches are hard-switched for most of the switch transition.

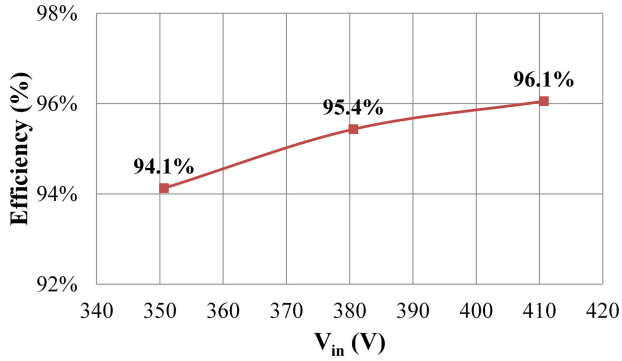
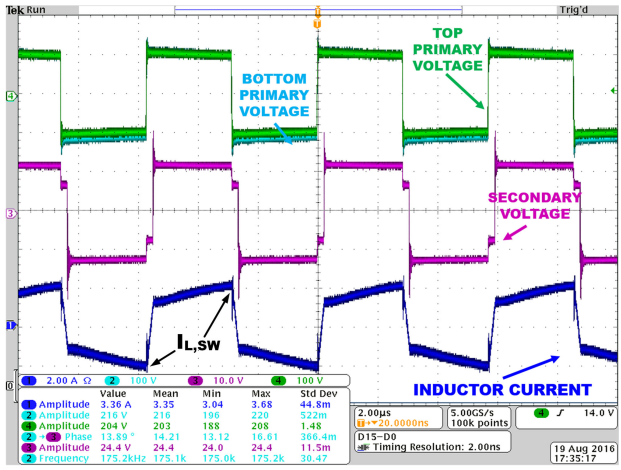
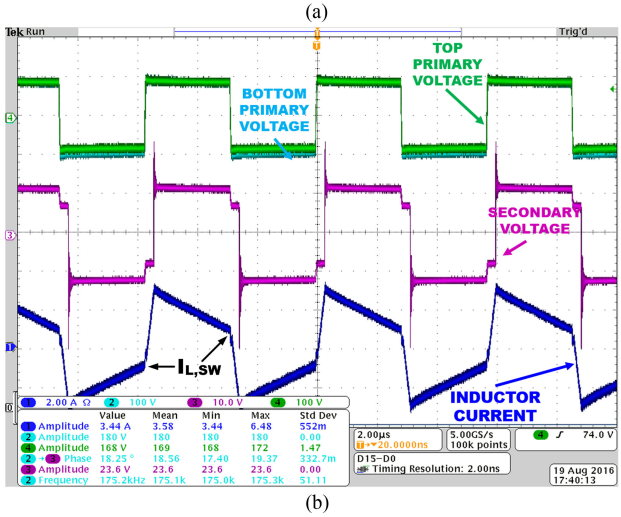


Fig. 25. Experimental efficiency of the Si DSAB converter delivering 300 W over an input voltage range of 350–410 V.



(a)



(b)

Fig. 26. Si DSAB converter operating waveforms at an input voltage of (a) 410 V and (b) 350 V, both at an output voltage of 12 V and an output power of 300 W. The inductor current at the switch transitions $I_{L,SW}$ is shown with an arrow.

with increasing voltage, due to the lower rms currents at the high end of the input voltage range.

Fig. 26 shows the operating waveforms for the Si DSAB converter at (a) 410 V input and (b) 350 V input at an output power of 300 W. At 410 V, the inductor current slopes up as the input

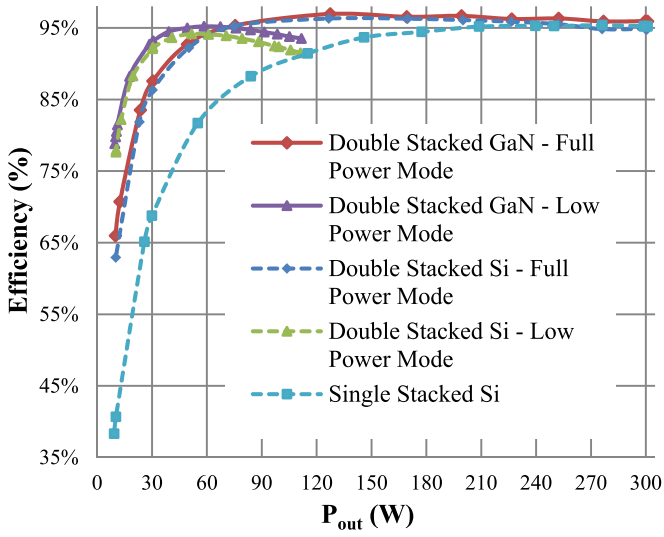


Fig. 27. Experimental efficiency curves across output power for the DSAB converters populated with GaN and Si switches, operating in full-power and low-power modes, as well as a curve for the single-stacked DAB converter populated with superjunction Si switches.

TABLE V
EFFICIENCY AT 300 W (100% LOAD)

Topology	P_{out} (W)	Efficiency (%)
DSAB GaN—full-power mode	299.6	95.9%
DSAB Si—full-power mode	299.7	94.9%
Single-stacked DAB Si	299.1	95.2%

voltage is higher than the nominal voltage, so there is a voltage transformation ratio mismatch. At 350 V, the inductor current slopes downward, as the input voltage is lower than nominal. As can be seen in Fig. 26, the amplitude of the inductor current at the inverter switch transitions $I_{L,\text{SW}}$ is lower at 350 V than at 410 V. As the input voltage is further decreased, the converter will lose ZVS due to the shape of the current waveform, a well-known limitation of the traditional DAB converter. While this converter can still be operated across a reasonably wide input voltage range with high efficiency, the true benefit of the proposed topology and control scheme is seen across a very wide output power range.

Efficiency curves for operation across a wide output power range were obtained for all three topologies mentioned above, as well as for the low-power modes for the double-stacked converters (the single-stacked converter is not capable of low-power mode operation). As shown in Fig. 27 and Table V, the three converters' efficiencies are close above 250 W (but favoring the DSAB GaN design); however, below this, the efficiencies of the single-stacked DAB designs drop dramatically compared to the DSAB designs. As shown in Section III and [20], [25], simulations indicated that a traditional full-bridge DAB converter would have even worse efficiency performance. The DSAB converter, thus, provides significant efficiency benefit across output power compared to a single-stacked design, even when only used in the full-power mode.

TABLE VI
EFFICIENCY AT 10 W (3.3% LOAD)

Topology	P_{out} (W)	Efficiency (%)
DSAB GaN—full-power mode	9.97	66.0%
DSAB GaN—low-power mode	10.01	79.8%
DSAB Si—full-power mode	10.07	62.9%
DSAB Si—low-power mode	10.19	77.6%
Single-stacked DAB Si	10.20	41.4%

Below 20% load, the DSAB's low-power mode significantly improves the efficiency of the converter as compared to the full-power mode, increasing the efficiency from 66.0% to 79.8% for the GaN DSAB converter, which represents a roughly 40% reduction in loss; see Table VI. The GaN-based DSAB topology has an efficiency of greater than 92.7% down to 10% load. In comparison, the single-stacked DAB topology drops to 69.5% across this range. The DSAB GaN design in the low-power mode is 79.8% efficient at 3.3% load, while the single-stacked DAB is only 41.4% efficient, highlighting the proposed topology's ability to achieve high-efficiency operation across a wide power range.

Additionally, the GaN DSAB converter showed better performance compared to the Si DSAB converter at high powers due to its lower $R_{\text{ds,on}}$, achieving 0.8–1.2% improvement in the efficiency (or equivalently a roughly 20% reduction in loss). Using Si devices, the DSAB converter was able to achieve an efficiency of 94.9% at full load, a peak efficiency of 96.3% at an output power of 126.5 W, an efficiency above 92.3% down to 10% load, and an efficiency above 77.6% down to 3.3% load. By comparison, the GaN-based DSAB converter was able to achieve an efficiency of 95.9% at full load, a peak efficiency of 97.0% at an output power of 127.4 W, an efficiency above 92.7% at 10% load, and an efficiency above 79.8% at 3.3% load.

V. CONCLUSION

This paper has presented the design and implementation of a new converter topology designed to achieve high efficiency under both full-load and light-load conditions. This was done through

1) the use of a double-stacked bridge inverter, which reduces the voltage that must be charged and discharged across the switch output capacitance and allows for the use of lower voltage rated devices which can exhibit better performance characteristics, thereby improving ZVS performance and overall efficiency;
2) a compact single-core three-winding leakage transformer; and
3) a reconfigurable rectifier and alternative switching patterns providing a low-power mode that reduces core loss and further extends the ZVS range of the converter. The low-power mode is implemented with an auxiliary switch and a change in inverter and rectifier drive signals, which can be preprogrammed into a controller for easy configuration. The converter is operated with simple phase-shift control and with fixed dead times for both modes.

This paper also presented experimental results from three prototype converters: GaN and Si DSAB converters, as well as a Si superjunction single-stacked DAB converter. The GaN DSAB topology proved to be the most efficient over the entire load range, and was capable of achieving a peak efficiency of 97.0%, an efficiency greater than 92.7% down to 10% load, and an efficiency greater than 79.8% down to 3.3% load.

APPENDIX A
CORE LOSS IN THE LOW-POWER MODE

The low-power mode substantially reduces core loss, due to the reduction of flux in the core volume. Using the Steinmetz equation, the core loss for the three-winding transformer can be compared for the full-power and low-power modes. The peak magnetic flux density for each core leg wound with a primary winding can be expressed as

$$B_{\mathrm{pk1}} = \frac{V_{\mathrm{pk}}\left(\frac{T}{2}\right)}{N\left(\frac{A_e}{2}\right)} = \frac{\frac{V_{\mathrm{in}}}{4}}{N f_s A_e} = B_{\mathrm{pk2}} \tag{21}$$

where B_{pk1} and B_{pk2} are the peak magnetic flux densities in the core leg sections for primary windings 1 and 2, V_{pk} is the magnitude of the voltage excitation on the primary, T is the period of the voltage excitation on the primary, so that the voltage waveform peaks at $T/2$, N is the number of primary turns, A_e is the area of the core (specifically the core center post), and f_s is the frequency of the voltage excitation on the primary. The magnitude of the primary voltage waveform can be expressed in terms of the dc input voltage, which is $V_{\mathrm{in}}/4$ as described previously. The core area is divided by two in the above-mentioned expression since each primary is wound around the outer leg of the E-I core, which has half the area of the center-post for the chosen core.

The power loss in the core while operating in the full-power mode can then be expressed as

$$P_{\mathrm{core,FP}} = K p_{v,\mathrm{sin}} \left(\frac{f_s}{f_0}\right)^{\alpha} \left(\left(\frac{B_{\mathrm{pk1}}}{B_0}\right)^{\beta} + \left(\frac{B_{\mathrm{pk2}}}{B_0}\right)^{\beta}\right) \left(\frac{V_{\mathrm{core}}}{2}\right) \tag{22}$$

where K is a multiplication factor for the specific core shape used; $p_{v,\mathrm{sin}}$ is the loss density at a specified temperature, base frequency f_0, and peak sinusoidal flux density B_0; α is the Steinmetz exponent for frequency; β is the Steinmetz exponent for flux density for the core material, and V_{core} is the volume of the core. Core volume is divided by two here for each primary contributing flux, as each primary's individual flux can be imagined as only traveling through half the volume of the core. It is also noted that to use typical Steinmetz loss data, the loss for a triangular flux waveform (as in the double-stacked bridge converter) is being modeled the same as for a sinusoid of the same peak flux value. This is only a rough approximation, but is sufficient for illustrating how loss scales between the full-power and low-power modes.

For the low-power mode, the peak magnetic flux density remains the same, but now only one primary is energized at a time. The amplitude of the primary voltage waveform is the same as that of the full-power mode, but there is also a period where the voltage is zero. If we assume no flux in the outer leg that corresponds to the shorted winding, the center leg will have reduced flux density due to the one-primary drive. An overestimation of the core loss can then be found by letting one of the B_{pk} terms go to zero, as follows:

$$P_{\mathrm{core,LP}} = K p_{v,\mathrm{sin}} \left(\frac{f_s}{f_0}\right)^{\alpha} \left(\frac{B_{\mathrm{pk1}}}{B_0}\right)^{\beta} \left(\frac{V_{\mathrm{core}}}{2}\right). \tag{23}$$

$P_{\mathrm{core,LP}}$ is, therefore, much lower than the core loss in the full-power mode. Note that because the center leg flux is reduced due to only one primary driving flux into it at a time during the low-power mode, the actual core loss will be a little bit lower.

APPENDIX B
SIMULATED MODE TRANSITIONS

The DSAB converter was simulated during mode switches from 1) the full-power mode to the low-power mode and from 2) the low-power mode to the full-power mode. For simplicity, the simulations were performed only for the GaN DSAB converter. All simulations of the mode transitions used the same dead times and output capacitance parameters as for the steady-state simulations that evaluated efficiency. This was done to try to get as realistic results as possible.

A. Transition From Full-Power to Low-Power Mode

The converter was simulated switching from the full-power mode to the low-power mode under two conditions:

1) While remaining at 75 W in both modes, to demonstrate the ability of the transitional phase shift to deliver constant power across the mode shift at the quarter-power point.
2) While stepping from 100 W in the full-power mode to 50 W in the low-power to show an exaggerated transient load step, in order to examine the stability of the operating waveforms.

Fig. 28 shows the operating waveforms for the converter (a) switching from full power to low power while maintaining a constant 75 W output, and (b) switching from full power to low power while stepping from 100 to 50 W output. The top and bottom primary voltages ($V_{p,1}$ and $V_{p,2}$ in Fig. 2) are shown in the top pane, followed by the secondary voltage (V_s in Fig. 2), and the top and bottom primary currents (the currents through the leakage inductors of value L in Fig. 2). The transition point is marked by the dotted black line and can also be seen by a change from the in-phase primary waveforms of the full-power mode to the alternately energized primary waveforms of the low-power mode, and by the halving of the transformer secondary voltage. The blue and red horizontal limit lines plotted with the primary currents show the steady-state amplitude after the converter has been operating in the low-power mode after about 1 ms. As can be seen in the figure, the current amplitude only slightly exceeds these limits right after the transition and quickly settles to the steady-state value in both Fig. 28(a) and (b). The primary and secondary voltages show no transients, other than the explicitly defined transitionary step in the secondary voltage.

Of note, Fig. 28(a) and (b) shows that the inductor current has different slopes during the flat-topped portion of the trapezoidal

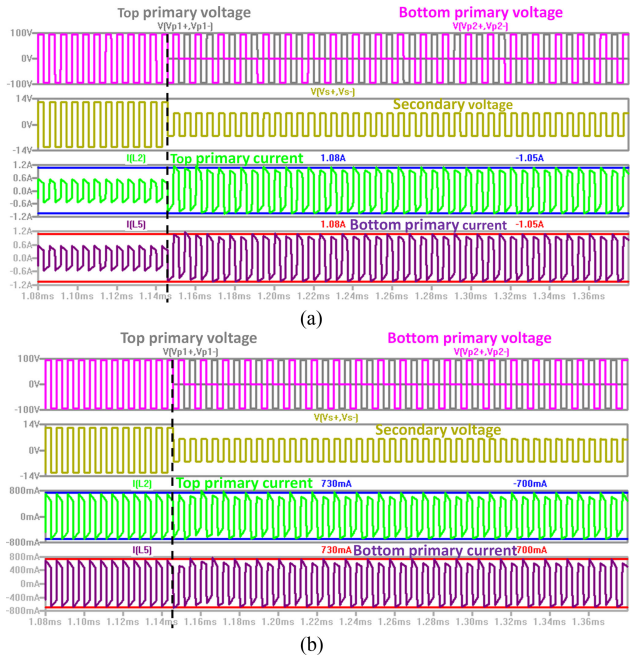


Fig. 28. Simulated operating waveforms for the GaN DSAB converter for (a) a transition from the full-power mode to low-power mode at a constant 75 W, and (b) a transition from the full-power mode to low-power mode for a step in output power from 100 to 50 . The blue and red sets of horizontal lines show the steady-state amplitude of the current.

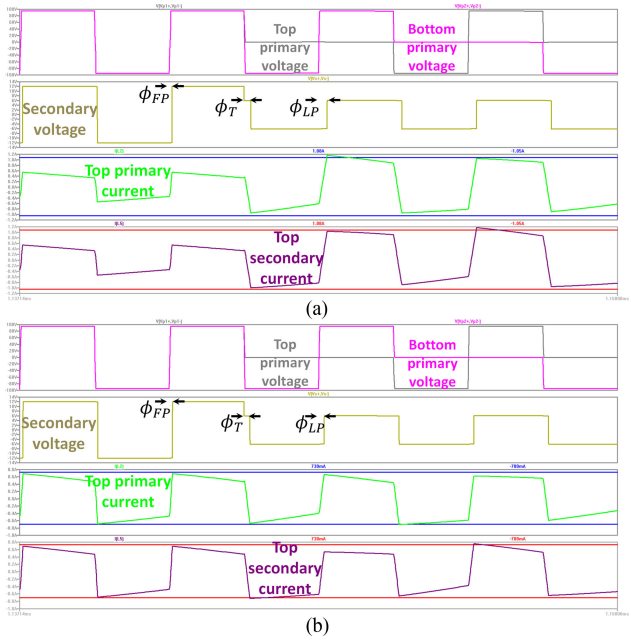


Fig. 29. Zoomed in simulated operating waveforms for the GaN DSAB converter for (a) a transition from full-power to low-power mode, while remaining at 75 W, and (b) a transition from full-power to low-power mode for a step in output power from 100 to 50 W. The full-power phase shift ϕ_{FP}, low-power phase shift ϕ_{LP}, and transition phase shift ϕ_T are labeled.

current waveform, with these slopes alternating every switching period. This is due to the fact that during the low-power mode, the same current flows through the top and bottom leakage inductances due to the shorted winding configuration, with the exception that the primary branch that is currently being energized will have an additional current component due to the voltage applied across its magnetizing inductance. Comparing the top and bottom inductor currents, it is evident that the currents have alternating slopes for each switching period, as each primary is alternately energized.

Fig. 29 shows zoomed-in waveforms for the same operating conditions shown in Fig. 28, and more clearly shows the transitionary step down in the secondary voltage due to the change from the full-power full-bridge rectifier mode to the low-power half-bridge rectifier mode at the transition time. The full-power phase shift ϕ_{FP}, low-power phase shift ϕ_{LP}, and transition phase shift ϕ_T are also labeled.

B. Transition From Low-Power to Full-Power Mode

The converter was also simulated for a mode switch in the opposite direction, from low-power to full-power mode. This was again done under two conditions:

1) While remaining at 75 W in both modes.
2) While stepping from 50 W in the low-power mode to 100 W in the full-power mode to show an exaggerated transient load step, now with a transition in the opposite direction.

Fig. 30 shows the operating waveforms for the converter switching from low power to full power while maintaining a constant 75 W output, and (b) switching from low power to full

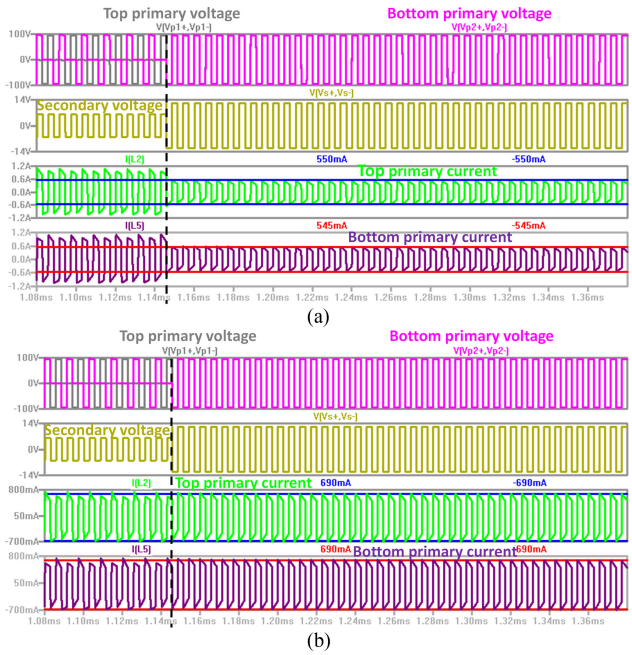


Fig. 30. Simulated operating waveforms for the GaN DSAB converter for (a) a transition from the low-power mode to full-power mode at a constant 75 W, and (b) a transition from the low-power mode to full-power mode for a step in output power from 50 to 100 W. The blue and red sets of horizontal lines show the steady-state amplitude of the current.

power while stepping from 50 to 100 W. The transition point is again marked with a dotted black line, and can also be seen by the change in the primary waveforms and by the doubling of the transformer secondary voltage.

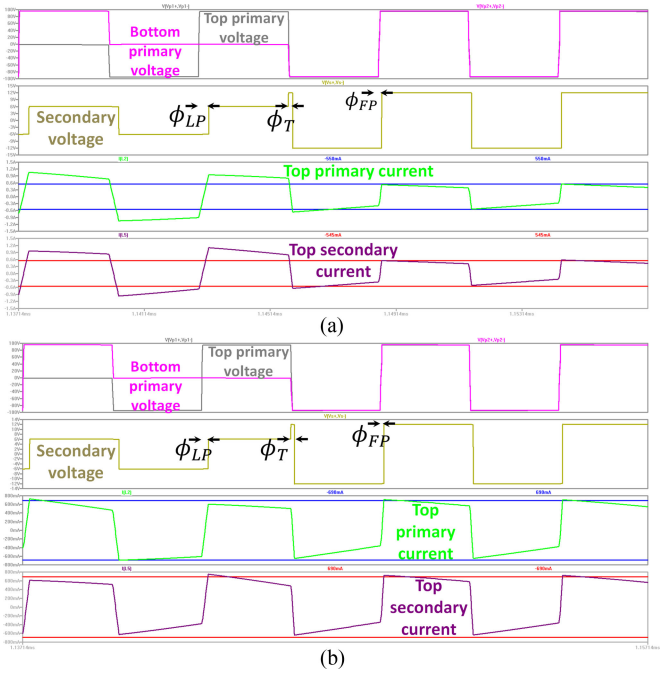


Fig. 31. Zoomed in simulated operating waveforms for the GaN DSAB converter for (a) a transition from the low-power mode to full-power mode while maintaining the output power at 75 W across the mode switch, and (b) a transition from the low-power mode to full-power mode for a step in output power from 50 to 100 W. The full-power phase shift ϕ_{FP}, low-power phase shift ϕ_{LP}, and transition phase shift ϕ_T are labeled.

Fig. 30(a) shows the output power held constant at 75 W while the converter is switched from low power to full power. The current decreases as a result of switching to the lower full-power phase shift, the opposite of the case shown in Fig. 28(a). The blue and red limit lines again show the steady-state amplitude after the converter has been operating in the full-power mode after about 1 ms. As can be seen in the figure, the current amplitude during the transition very quickly settles to the steady-state value. Fig. 30(b) shows a load step from 50 to 100 W. Here, the primary currents exceed the limits by a small amount right after the mode switch, but again display a very nice step in operating waveforms without significant transients.

Fig. 31 shows zoomed-in waveforms for the same operating conditions as in Fig. 30, and shows the transitionary step up in the secondary voltage due to the switch from the half-bridge rectifier configuration to the full-bridge rectifier configuration. The full-power phase shift ϕ_{FP}, low-power phase shift ϕ_{LP}, and transition phase shift ϕ_T are again labeled.

Table VII presents the measured values for output power before and after the mode switch for both the full-power to low-power and low-power to full-power mode transitions. $P_{\mathrm{out},T}$ is the rms output power over four switching periods, centered around the transition point. For the case where the output power remains constant between the full-power and low-power modes, the transition power also remains constant. This demonstrates that the converter can switch modes while delivering constant output power. In the case where the output power is stepped down, the transition power is about half-way between the start and end output power, as the rms operation essentially averages the full-power and low-power operating powers.

TABLE VII
OUTPUT POWER DURING MODE TRANSITIONS

Full-power to low-power	$P_{\mathrm{out,FP}}$ (W)	$P_{\mathrm{out,LP}}$ (W)	$P_{\mathrm{out},T}$ (W)
Case 1	75.2	75.1	74.0
Case 2	100.4	49.9	70.1
Low-power to full-power	$P_{\mathrm{out,LP}}$ (W)	$P_{\mathrm{out,FP}}$ (W)	$P_{\mathrm{out},T}$ (W)
Case 1	75.1	75.1	77.5
Case 2	49.9	100.4	77.5

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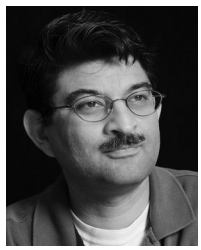

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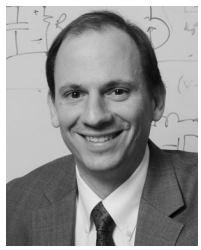

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