Letters

Control and Operating Range Analysis of an AC-Stacked PV Inverter Architecture Integrated With a Battery

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***Abstract*—This letter presents a control scheme to operate a battery-integrated ac-stacked photovoltaic (PV) inverter architecture and its operating range analysis. The main operation strategy is the combination of decentralized controls of individual inverter members; PV and battery. In ac-series integration, battery charging and discharging operations affect operating margins of the PV inverter members. The interactive operation needs to be analyzed to identify the system operating range under different conditions. A ramp-rate control, which mitigates PV output variations and improves grid stability, is a suitable application for the PV-battery ac-stacked inverter architecture utilizing a panel-level modular inverter design. In this letter, decentralized ramp-rate control is proposed and demonstrated to analyze the system operating range. The detailed system control and analysis are performed through controller hardware-in-the-loop testing.**

***Index Terms*—AC-stacked PV inverter, battery integration, decentralized ramp-rate control, operating range analysis.**

I. Introduction

THE ac-stacked photovoltaic (PV) inverter architecture is a panel-level cascaded modular inverter topology suitable for single-phase grid-tied PV applications [1], [2]. High-frequency and low-voltage PV inverter members are stacked in series to satisfy the ac voltage for grid connection and extract maximum output power from individual PV panels. To maximize the architecture's effectiveness, each building block is controlled independently without communications among themselves and with minimum handshaking with the supervisory control center for grid synchronization [2]. Its tangible advantages and capabilities with smart inverter functions are verified through laboratory experiments, controller hardware-in-the-loop (CHIL) testing, and site demonstration in [2]–[7].

In PV applications, integration of a battery into a PV generation system has received significant attention because of the intermittent nature of solar energy sources [8]–[10]. In most

Manuscript received December 21, 2017; revised February 1, 2018 and April 5, 2018; accepted April 11, 2018. Date of publication April 23, 2018; date of current version September 28, 2018. *(Corresponding author: Namwon Kim.)*

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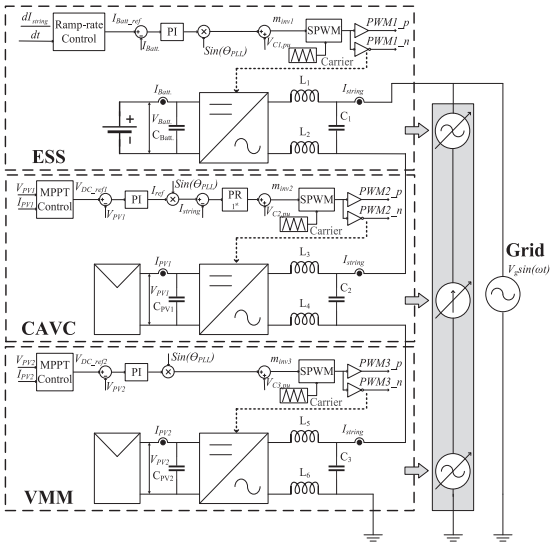


Fig. 1. PV-battery ac-stacked inverter architecture and control diagram.

proper amount of the battery current reference for the DRRC are presented. The control performance of the DRRC and the interactive operation among the inverter members with PV and battery output variations are demonstrated through CHIL testing.

II. PV-Battery AC-Stacked Inverter Architecture

A. Proposed PV-Battery AC-Stacked Inverter Architecture

The proposed PV-battery ac-stacked inverter architecture is composed of three different types of modular inverters: 1) current administrator voltage compensator (CAVC), 2) voltage mode members (VMM), and 3) energy storage system (ESS). By stacking or connecting a group of PV inverters in series, the architecture can support the ac grid voltage requirement for grid connection with low-voltage semiconductor devices. Fig. 1 presents the ac-series configuration and the control diagram of the three different types of modular inverters. A CAVC controls its dc input voltage V_{PV1} with a closed-loop PI controller. A maximum power point tracking (MPPT) control generates the dc input voltage reference to extract the maximum power from the PV panel. Also, the CAVC is responsible for controlling the ac string current I_{string} with a closed-loop PR controller. A VMM only controls its dc input voltage V_{PV2} for the MPPT control of its PV panel. Multiple VMMs work as voltage buffers to build up the architecture's ac output voltage. An ESS controls the battery charging and discharging current $I_{\mathrm{Batt.}}$ with a closed-loop PI controller. The proposed RRC generates the battery current reference to mitigating PV output variations. Individual closed-loop controls generate modulation indices m_{inv1}, m_{inv2}, and m_{inv3} to operate individual inverter members, and the feedforward terms $V_{C1,\mathrm{pu}}$, $V_{C2,\mathrm{pu}}$, and $V_{C3,\mathrm{pu}}$ are applied to improve the system control response and lower the impact of grid disturbances. Details of the RRC strategy are explained in Section III. Since the PV-battery ac-stacked inverter architecture provides the decentralized environment in terms of both physical topology and control, each modular inverter is controlled autonomously by using its local measurements except for grid-synchronization information.

B. Interactive Operation Between Inverter Members

The main operation principle of the proposed PV-battery ac-stacked inverter architecture is the combination of the decentralized control algorithm of the individual inverter members connected in series. In the ac string where the same ac current i_{string} is passing through all the inverter members, the inverters' output voltages vary based on the inverter output power. Since the inverters are cooperating to regulate their ac output power in grid connection, one inverter's output power variations may affect others' ac output voltages corresponding to the inverters' operating margin. Therefore, the interaction between the inverters limits the operating range of the architecture.

When asymmetrical irradiance drop is applied to the PV panels, the PV inverter with the low output power decreases its ac output voltage, and it makes other inverters increase their output voltage to compensate the ac voltage drop and track individual maximum power point (MPP), as presented in previous publications [2], [4]. Likewise, battery charging and discharging operations force PV inverters' ac output voltage changes [21]. When battery charging mode is applied to the ESS inverter, the ESS ac voltage appears to be inverted to have negative power flow through the ESS. The inverted ESS ac voltage makes the CAVC and the VMM increase their ac voltages resulting the PV inverters' higher modulation indices. Higher modulation index requests the use of more operating margin for the inverter. If the amount of the compensated ac voltage is higher than the PV inverters' remaining operating margins, the modulation indices reach the maximum amount (1.0), and abnormal operation such as ac current distortion or losing MPPT occurs because the inverters have no room to increase their output voltage more. Different control schemes in the CAVC and the VMM introduce the different abnormal operations, ac current distortion, and losing MPPT control, since the CAVC utilizes sinusoidal ac string current information as the feedback signal for the closed-loop control and the VMM utilizes dc input voltage information. This interaction is required to be considered to design the reliable PV-battery ac-stacked inverter architecture, which has a wide operating range and provides high-quality ac current.

III. Decentralized Ramp-Rate Control Strategy

In the proposed architecture utilizing a panel-level inverter design, a RRC, which smooths out PV output variations, is a suitable application of the battery integration due to the battery charging and discharging limitations caused by the interaction addressed in the previous section. In this architecture, the ESS determines its battery current reference without handshaking with PV inverters or supervisory control center to achieve decentralized control environment. In the proposed DRRC strategy, the ESS utilizes its local ac string current measurement $i_{\mathrm{string}}(t)$ for detection of PV output variations and battery current calculation. The overall mechanism of the DRRC is shown in Fig. 2(a). The first step is the detection of PV variations with the differentiation of ac string current, as follows:

$$\frac{di_{\mathrm{string\_avg}}\left(t_k\right)}{dt} = \frac{i_{\mathrm{string\_avg}}\left(t_k\right) - i_{\mathrm{string\_avg}}\left(t_{k-1}\right)}{t_k - t_{k-1}} \tag{1}$$

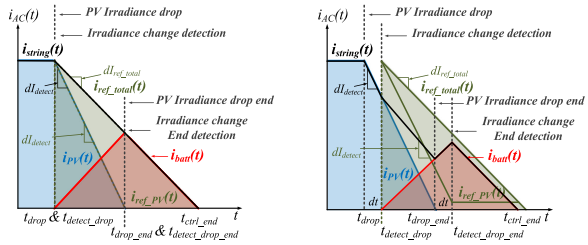


Fig. 2. Illustration of the DRRC algorithm. (a) Ideal case: without detection delay. (b) Practical case: with detection delay.

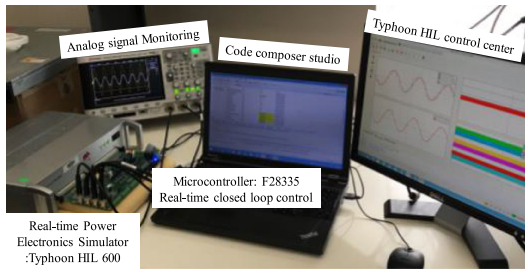


Fig. 3. CHIL set-up for testing a PV-battery ac-stacked inverter system.

where t_k is the time at the kth instant, t_{k-1} is the time at the $(k-1)$th instant, $i_{\text{string\_avg}}(t)$ is the rms average of $i_{\text{string}}(t)$, and $dI_{\text{string\_avg}}(t)$ is the ac current difference. To ignore small variations caused by the MPPT control, a dead band dI_{limit} is applied, as follows:

$$dI_{\text{detect}} = \begin{cases} dI_{\text{string\_avg}}\left(t_{\text{detect\_drop}}\right), & dI_{\text{string\_avg}}\left(t_{\text{detect\_drop}}\right) > dI_{\text{limit}} \\ 0, & dI_{\text{string\_avg}}\left(t_{\text{detect\_drop}}\right) \le dI_{\text{limit}} \end{cases} \tag{2}$$

where $t_{\text{detect\_drop}}$ is the moment when PV output variation is detected, $dI_{\text{string\_avg}}(t_{\text{detect\_drop}})$ is the ac string current difference at $t_{\text{detect\_drop}}$, and dI_{detect} is the PV output change detected.

The ESS will start to charge or discharge the battery to achieve the desired ramp-rate of the inverter architecture's output once the PV output variation is detected. In the proposed architecture, a criterion to distinguish the PV output changes from the total ac string output power is required for the decision of the ESS output current since the output of the ESS also affects the differentiation of the ac string current due to the series connection. As shown in Fig. 2(a), two current references $i_{\text{ref\_PV}}(t)$ and $i_{\text{ref\_total}}(t)$ are generated with two different ramp-rates; the detected PV output ramp-rate dI_{detect} and the desired architecture's output ramp-rate $dI_{\text{ref\_total}}$, respectively, as follows:

$$i_{\text{ref\_PV}}\left(t_k\right) = i_{\text{ref\_PV}}\left(t_{k-1}\right) + \frac{dI_{\text{detect}}}{dt} \times T_{\text{step}} \tag{3}$$

$$i_{\text{ref\_total}}\left(t_k\right) = i_{\text{ref\_total}}\left(t_{k-1}\right) + \frac{dI_{\text{ref\_total}}}{dt} \times T_{\text{step}} \tag{4}$$

$$dI_{\text{ref\_total}} = dI_{\text{detect}} \times k_{\text{ramp\_rate\_total}} \tag{5}$$

where T_{step} is the controller time step and $k_{\text{ramp\_rate\_total}}$ is the ramp-rate gain (0.1–1). By subtracting $i_{\text{ref\_PV}}(t)$ from $i_{\text{ref\_total}}(t)$, the battery current reference $i_{\text{batt}}(t)$ can be calculated, and its absolute value $|i_{\text{batt}}(t)|$ is increased until the moment of PV output variations stop denoted as $t_{\text{drop\_end}}$. After $t_{\text{drop\_end}}$, $i_{\text{ref\_PV}}(t)$ is set as constant by forcing dI_{detect} zero, and $|i_{\text{batt}}(t)|$ decreases constantly until it becomes zero $t_{\text{ctrl\_end}}$, as follows:

$$i_{\text{batt}}\left(t_k\right) = \begin{cases} \left(i_{\text{ref\_total}}\left(t_k\right) - i_{\text{ref\_PV}}\left(t_k\right)\right) \times k_{\text{ac to dc}}, \\ \qquad t_k \le t_{\text{detect\_drop\_end}} \\ \left(i_{\text{ref\_total}}\left(t_k\right) - i_{\text{ref\_PV}}\left(t_{\text{detect\_drop\_end}}\right)\right) \times k_{\text{ac to dc}}, \\ \qquad t_{\text{detect\_drop\_end}} < t_k \le t_{\text{ctrl\_end}} \end{cases} \tag{6}$$

TABLE I
DESIGN PROPERTIES OF THE PV-BATTERY AC-STACKED INVERTER

System specifications		
Grid		
Voltage	V_g (V_{RMS})	30
PV panel		
MPPT: Power (1000W/m^2)	P_{MPP} (W)	255.10
MPPT: Voltage (1000W/m^2)	V_{MPP} (V)	33.45
MPPT: Current (1000W/m^2)	I_{MPP} (V)	7.63
Battery		
Nominal voltage	$V_{Battery}$ (V)	42.2
Capacity	$C_{Battery}$ (Ah)	20

where $k_{\text{ac to dc}}$ is the ac-to-dc current gain and $t_{\text{detect\_drop\_end}}$ is the moment when the ESS detects PV output variation stop. The detection of PV output variation stop is achieved by monitoring the differentiation of the ac current, as follows:

$$|i_{\text{batt}}\left(t_k\right)| \text{ decreases,}$$
$$\text{if} \begin{cases} \frac{di_{\text{string\_avg}}(t_k)}{dt} \le 0, & \text{Charging mode} \\ \frac{di_{\text{string\_avg}}(t_k)}{dt} \ge 0, & \text{Discharging mode.} \end{cases} \tag{7}$$

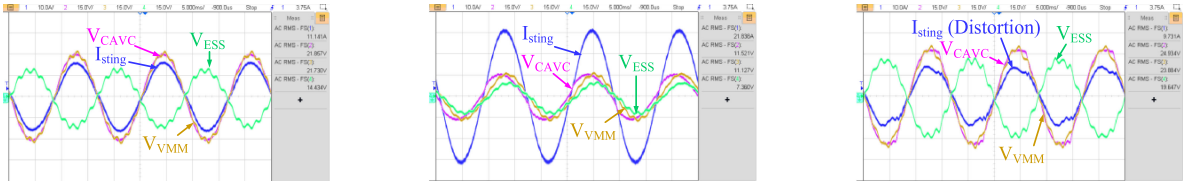
When PV output variations stop, $|i_{\text{batt}}(t)|$ continues to increase and the differentiation of the ac current is going to be zero. Moreover, the direction of the differentiation will be reversed unless $|i_{\text{batt}}(t)|$ starts to decrease. The reversed direction of the differentiation can be an indicator of $t_{\text{detect\_drop\_end}}$. After $t_{\text{detect\_drop\_end}}$, $|i_{\text{batt}}(t)|$ decreases to zero ($t_{\text{ctrl\_end}}$) and the proposed DRRC is completed. In Fig. 2(a) and (b), ideal and practical cases of the DRRC strategy are illustrated. In Fig. 2(b), each transition of detection sequences such as from t_{drop} to $t_{\text{detect\_drop}}$ and from $t_{\text{drop\_end}}$ to $t_{\text{detect\_drop\_end}}$ requires the differentiation calculation delay. This sequence delay will cause the mismatch between the final ramp-rate and the desired ramp-rate, and the small fluctuation of the ac power. The ramp-rate mismatch error can be reduced by optimizing the sequence delay.

IV. RESULTS AND DISCUSSIONS

To verify the effectiveness of the proposed architecture and its DRRC strategy, the CHIL test set-up is built, as shown in Fig. 3 [26]. In this set-up, two PV inverters, a CAVC and a VMM, and an ESS inverter are constructed. The detail system parameters are presented in Table I.

TABLE II
SUMMARY OF CHIL TEST RESULTS: PEAK MODULATION INDICES AND OPERATING MARGIN OF THE INVERTERS WITH DIFFERENT OPERATING CONDITIONS

Detail conditions			Peak modulation indices			Not in MPP	Current Distortion	Operating margin		
Irradiance level (W/m^2)		Battery current (A)	CAVC	VMM	ESS			CAVC	VMM	ESS
CAVC	VMM									
1000	1000	-	0.72	0.67	0.03	-	-	28%	33%	97%
500	1000	-	0.51	0.89	0.03	-	-	-	11% (-22%)	-
320	1000	-	0.39	1.0	0.03	-	-	-	0% (-33%)	-
100	1000	-	0.28	1.0	0.03	☑	-	-	0% (-33%)	-
1000	500	-	0.91	0.46	0.03	-	-	9% (-19%)	-	-
1000	250	-	1.00	0.29	0.03	-	-	0% (-28%)	-	-
1000	100	-	1.00	0.16	0.03	-	☑	0% (-28%)	-	-
500	500	-	0.72	0.68	0.03	-	-	18% (0%)	32% (-1%)	-
1000	1000	Charging: -4	0.99	0.97	0.46	-	-	1% (-27%)	3% (-30%)	54% (-43%)
1000	1000	Charging: -4.6	1.00	1.00	0.58	-	-	0% (-28%)	0% (-33%)	42% (-55%)
1000	1000	Charging: -4.8	1.00	1.00	0.64	-	☑	0% (-28%)	0% (-33%)	36% (-61%)
1000	1000	Discharging: 13.9	0.65	0.33	0.57	-	-	35% (+7%)	67% (+34%)	33% (-64%)



(a) (b) (c)

Fig. 4. Interactive operation of the inverters with battery operating conditions; I_{string}: ac string current, V_{CAVC}: CAVC ac voltage, V_{VMM}: VMM ac voltage, and V_{ESS}: ESS ac voltage. (a) Charging mode (–4 A). (b) Discharging mode (4 A). (c) Charging mode (–4.8 A).

A. *Interactive Operation Between PV and ESS Inverters*

The CHIL test results of the inverters' interaction under asymmetrical PV output variations and battery charging and discharging are presented in Table II. The minimum irradiance level on the CAVC where the architecture provides stable operation is 320 W/m^2. Under this condition, the peak modulation index of the VMM reaches 1.0 by using all operating margin to cover the CAVC ac voltage drop. Below the minimum irradiance level (100 W/m^2), the architecture cannot perform MPPT control because the VMM is required to move its operating point to the right side of the MPP to increase its output voltage. In case of asymmetrical irradiance drop on the VMM, the minimum irradiance level is 250 W/m^2. Below the minimum irradiance level (100 W/m^2), ac current distortion occurs. The PV inverters' interaction limits the architecture's operating range.

Battery charging mode limits the architecture's operating range, as shown in Fig. 4. When battery current is –4 A_{dc}, the ESS generates –14.37 V_{rms} ac voltage. The CAVC and the VMM consume their 96.4% $(27\%/28\% \times 100 = 96.4\%)$ and 90.9% $(30\%/33\% \times 100 = 90.9\%)$ of available operating margin, respectively, to compensate the inverted ESS ac voltage. The maximum battery charging current is –4.6 A_{dc} and the peak modulation indices of the PV inverters reach 1.0 by using all operating margin. With higher battery charging current than –4.6 A, the ac current distortion occurs, as shown in Fig. 4(c). Therefore, the operating range in the battery charging mode is related to the operating margin of the PV inverters ($\approx$28% of CAVC's and $\approx$33% of VMM's). If the architecture is extended for 120 V_{rms} electrical grid by adding identical PV inverters, the architecture can handle more asymmetrical irradiance drop and battery charging currents. However, the percentage of available operating margin is maintained. The PV inverters must be redesigned with a higher dc input voltage to increase the percentage of available operating margin.

B. *Decentralized Ramp-Rate Control*

Table III and Fig. 5 present the CHIL test results of the DRRC under different asymmetrical irradiance changes. In this test, the 0.5 ramp-rate gain $k_{\text{ref\_total}}$ is applied. When a CAVC irradiance drop (1000 W/m^2 $\rightarrow$ 500 W/m^2) is applied, the CAVC output power is decreased by 122.1 W for 2.72 s introducing the PV output ramp-rate –1.50 A_{rms}/s, as shown in Fig. 5(a). Adopting the DRRC strategy, the architecture achieves 47% of the PV output ramp-rate –0.70 A_{rms}/s by discharging the battery, as shown in Fig. 5(b). Detecting the ac power changes, the ESS increases the battery discharging current until the irradiance drop ends. Detecting the reversed sign of the differentiation of $i_{\text{string}}(t)$, the ESS decreases the battery discharging current from 1.11 to 0 A. The interaction between inverters is shown in Fig. 5(c). The CAVC ac voltage is decreased by the CAVC output power drop. The VMM compensates the CAVC ac voltage drop by increasing its ac voltage. Also, the ESS participates the compensation of the CAVC voltage drop and reduces a burden on the VMM slightly during battery discharging operation. When the CAVC irradiance rise (500 W/m^2 $\rightarrow$ 1000 W/m^2) is applied, the PV output ramp-rate 1.61 A_{rms}/ s is achieved, as shown in Fig. 5(d). With the DRRC, 49% of the PV output ramp-rate 0.79 A_{rms}/ s is achieved by charging the battery, as presented in Fig. 5(e). The maximum battery charging current is 1.51 A. In this case, the PV inverters increase their ac voltage to compensate the inverted ESS ac voltage, as shown in Fig. 5(f). Therefore, battery charging operation charges more operating margin of PV inverters. As illustrated in Fig. 2(b), the ramp-rate mis-

TABLE III
SUMMARY OF CHIL TEST RESULTS: THE DRRC WITH DIFFERENT OPERATING CONDITIONS

Detail conditions					Changes			Without DRRC		With DRRC			Ramp-rate ratio (%)	Inverter limitation
Modular inverter		Irradiance level (W/m^2)			P_{PV} (W)	I_{PV} (A)	I_{string} (A_{RMS})	Time (sec)	Ramp-rate (A_{RMS}/s)	Time (sec)	Ramp-rate (A_{RMS}/s)	MAX. $I_{batt.}$ (A)		
CAVC	VMM	Type	From	To										
☑	-	Drop	1000	500	-122. 1	-4.6	-4.07	2.72	-1.50	5.82	-0.70	1.11	47	-
☑	-	Rise	500	1000	127.2	4.6	4.24	2.64	1.61	5.34	0.79	1.51	49	-
-	☑	Drop	1000	500	-127.2	-4.8	-4.24	2.58	-1.64	5.86	-0.72	1.11	44	-
-	☑	Rise	500	1000	127.2	4.6	4.24	2.84	1.49	6.56	0.65	1.35	44	-
☑	☑	Drop	1000	500	-254.4	-9.2	-8.48	5.48	-1.55	11.34	-0.75	2.23	48	-
☑	☑	Rise	500	1000	254.4	9.2	8.48	5.62	1.51	11.74	0.72	2.3	48	-
☑	-	Rise	350	1000	164.4	5.3	5.48	2.88	1.90	8.16	0.67	1.6	35	☑
-	☑	Rise	350	1000	169.8	5.3	5.66	3.4	1.66	6.16	0.92	1.35	55	☑

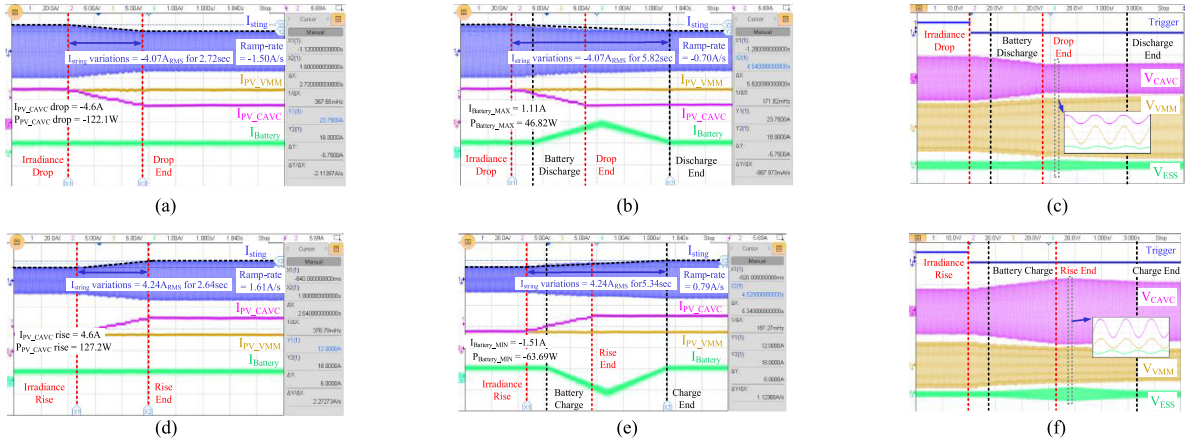


Fig. 5. DRRC: Asymmetrical irradiance changes on the CAVC (1000 W/m^2 $\leftrightarrow$ 500 W/m^2), ramp-rate factor: 50%. (a) Without DRRC: Irradiance drop, inverter currents. (b) With DRRC: Irradiance drop, inverter currents. (c) With DRRC: Irradiance drop, inverter voltages. (d) Without DRRC: Irradiance rise, inverter currents. (e) With DRRC: Irradiance rise, inverter currents. (f) With DRRC: Irradiance rise, inverter voltages.

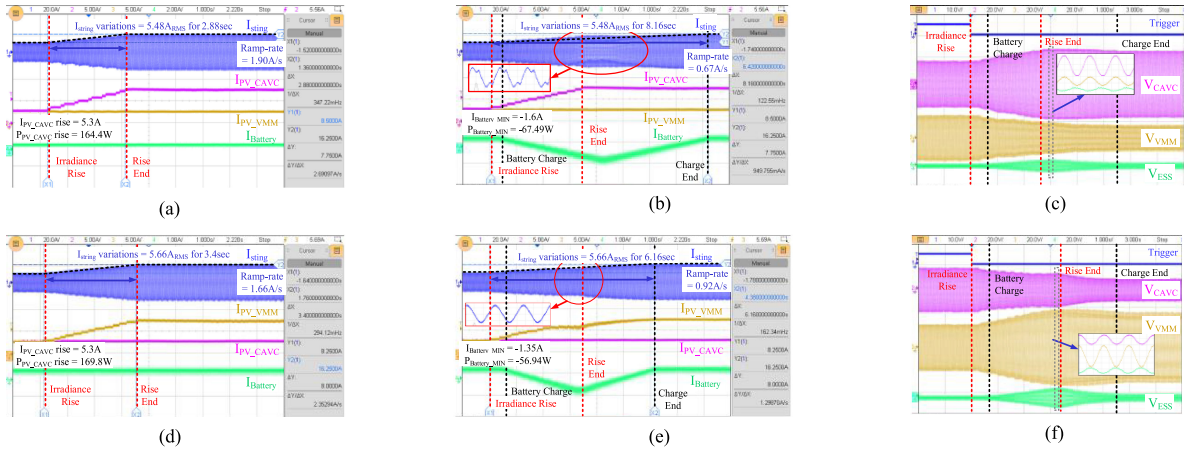


Fig. 6. DRRC: Severe asymmetrical irradiance changes (350 W/m^2 $\rightarrow$ 1000 W/m^2), ramp-rate factor: 50%. (a) Without DRRC: On the CAVC, inverter currents. (b) With DRRC: On the CAVC, inverter currents. (c) With DRRC: On the CAVC, inverter voltages. (d) Without DRRC: On VMM, inverter currents. (e) With DRRC: On VMM, inverter currents. (f) With DRRC: On VMM, inverter voltages.

match occurs due to the differentiation calculation delays. The mismatch errors are from 2% $(1 - 49\%/50\% \times 100 = 2\%)$ to 12% $(1 - 44\%/50\% \times 100 = 12\%)$. Also, small fluctuation of the ac current is observed.

C. Operating Range of the Decentralized Ramp-Rate Control

Severe asymmetrical irradiance rise (350 W/m^2 $\rightarrow$ 1000 W/m^2) is applied to the CAVC and the VMM to analyze the operating range of the DRRC in the proposed architecture, as shown in Fig. 6. In case of the CAVC irradiance rise, the ac current distortion occurs in the middle of the slope where two interactions caused by asymmetrical irradiance changes and battery charging mode are overlapped at the same time, as illustrated in Fig. 6(b). Since the detection of the PV output change stop is delayed due to the ac current distortion, the DRRC time is extended to 8.16 s resulting 35% of the PV output ramp-rate. Therefore, the ramp-rate mismatch error is increased to 30% $(1 - 35\%/50\% \times 100 = 30\%)$.

The interaction between inverters is shown in Fig. 6(c). The CAVC reaches its maximum ac voltage to cover the VMM ac voltage drop and the inverted ESS ac voltage. In case of the VMM irradiance rise, the limitation of the ac current occurs in the middle of the slope due to the overlapped interactions, as presented in Fig. 6(e). Therefore, the VMM moves its operating point from the MPP. This results in the PV current decrease. Since the ac current limitation allows for early detection of the PV output change stop, the DRRC time is shortened to 6.16 s resulting 55% of the PV output ramp-rate. Therefore, the negative ramp-rate mismatch error occurs as –10% $(1 - 55\%/50\% \times 100 = -10\%)$.

V. Conclusion

This letter presented a control scheme for the PV-battery ac-stacked inverter architecture and its analysis of the system operating range. The PV and ESS inverters' interactive operation and the feasibility of the DRRC were verified through the CHIL test results. Operation constraints on the constructed architecture were asymmetrical irradiance drop, 320 W/m^2 on the CAVC and 250 W/m^2 on VMM, and the –4.6 A battery charging current. Operating margins of inverters are critical in designing a reliable inverter architecture. A RRC mitigating PV output variations is a suitable application for the proposed architecture due to the battery charging and discharging limitations caused by the interaction. The DRRC can realize the decentralized control environment and minimize the communication requirements between the inverters. Applying the DRRC, the architecture achieved the desired total ac output ramp-rates during the irradiance changes on PV panels. The overlapped interactions (the asymmetrical irradiance level and battery charging mode) affected the performance of the DRRC. The ac current distortion and early detection of the PV output change stop were observed once the PV inverters use all of their operating margins. Further improvement can be made by implementing PV out curtailment control, which can reduce the required amount of the battery charging current.

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