Comparison Study of Common-Mode Noise and Thermal Performance for Lateral Wire-Bonded and Vertically Integrated High Power Diode Modules

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***Abstract*—This paper investigates the power module design for better common-mode (CM) noise and thermal performance. A high-frequency full-bridge diode rectifier is selected as a case study. The most influential factors in CM noise generation and mitigation are first identified with a simplified CM equivalent model and a comprehensive parametric study. Studies show proper parasitic value and parasitics symmetry can improve CM noise performance. The analysis of packaging structures indicates the vertical module has better CM noise and thermal performance than the traditional lateral wire-bonded module. To validate this, both modules are designed and prototyped for verification. The thermal simulation shows the vertical module exhibits a 25.5% lower thermal resistance from junction to case and a 51% increase of power density in a force-air-cooled condition. Experiments also reveal 15 dB of CM noise reduction from 150 kHz to 6 MHz and a 32% improvement of power density in a force-air-cooling condition. Finally, a case study demonstrates the vertical power module CM noise performance in a typical unsymmetrical topology. This results in a 30 dB CM noise reduction up to 6 MHz.**

***Index Terms*—Common-mode (CM) noise, power module, thermal performance, three-dimensional (3-D) packaging.**

I. Introduction

POWER modules are core components of high-performance power conversion systems. The most popular packaging structure for power modules is based on the wire-bond technology. In this structure, the semiconductor is attached to the substrate with solder and the top-side electrical connection is realized by wire bonds. Wire-bond technology is mature, flexible, and also cheap. However, its structure limits the further improvement of electrical and thermal performance of power modules. In the wire-bonded structure, the top-side interconnection using wire bonds usually leads to large stray inductances. Majority of the heat generated by the semiconductor device is dissipated through its bottom surface to the substrate. The top surface can only carry a limited amount of heat due to small diameters of wire bonds. Emerging wide bandgap (WBG) power devices can switch much faster and also have smaller die sizes. Therefore, it requires smaller module parasitic and also better heat dissipation to fully extract the benefits of WBG devices, which make new packaging approaches even more essential.

Recent developments in power module packaging techniques primarily focus on reducing the package parasitic inductances, enhancing module reliability and improving thermal performance and high-temperature operating capability [1]–[3]. Parasitic inductances have a strong impact on switching characteristics of power semiconductor devices. The traditional lateral wire-bonded module structure usually introduces a large stray inductance. Several proposed methods can decrease stray inductance by optimizing high-frequency current commutation loop [4], [5] and improving the symmetry of the layout in power modules [6]. To further reduce the stray inductance and enable double-sided cooling, solder-bump and direct-solder interconnections based flip-chip [7] and planar modules [8]–[12] are introduced, in which top side of the device are connected with solder. Planar modules can achieve very small stray inductances, and also small thermal impedances for heat dissipation. However, the fabrication process is quite involved compared with wire bond-based designs. In [13] and [14], a hybrid module is proposed to offer a less complex fabricating process but still achieves a modest reduction of stray inductances. However, none of above work discusses grounding capacitances in the module, which is a key factor of common-mode (CM) noise performance.

Electromagnetic interference (EMI) performance is also an important aspect of power converters. Typically, CM noise is caused by capacitive current, which is induced by switching nodes potential variation with respect to the ground. The noise current can potentially affect the normal operation of other interconnected devices. Within the converter, EMI problem could have an adverse impact on cost, loss, and reliability of the converter. With more noise generated, components with better noise immunity are needed, which usually come with higher costs. EMI noise oftentimes can induce voltage and current ringing, which also contribute to the loss. For some special case like motor drive systems, the ac-side CM current can lead to motor-side bearing currents, which are detrimental to the lifetime and reliability of a machine [15]. Therefore, there are standards specifying EMI noise emission allowances for different applications. To

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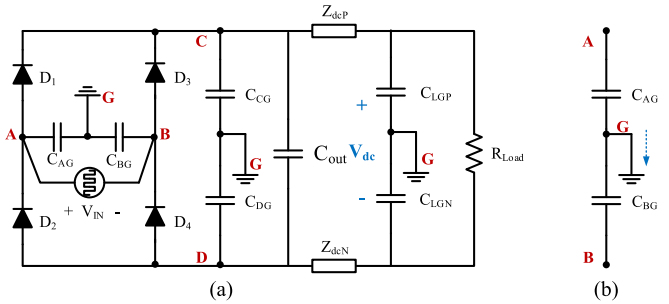


Fig. 1. (a) Schematic of a full-bridge diode rectifier. (b) CM current generation mechanism.

qualify for EMI standards, EMI filters are typically required to attenuate the noise. However, those filters can take a significant portion of the total system volume [16]. Recently, there is some efforts in reducing the EMI filter sizes and component counts, such as integrated EMI filters [17]–[22], active filters [23], [24], and integrated busbar EMI filters [25], [26]. However, a very few work considers optimizing the power module's parasitics for better EMI performance. It would be very beneficial if the CM noise current can be attenuated inside the power module, which is close to the noise source. A three-dimensional (3-D) module structure that stacks two devices together is proposed by the G2E lab in [26], **Error! Reference source not found**. This vertically integrated module structure offers a significantly reduced grounding capacitance, which is effective in suppressing CM noise.

This paper investigates the power module design for better CM noise and thermal performance. The traditional wire-bonded structure and the vertically integrated structure are compared in a full-bridge diode rectifier case study. The CM noise of the full-bridge rectifier is analyzed first. In Section II, the most important factors affecting the CM noise are identified through a simplified CM noise equivalent model and a comprehensive parametric study. In Section III, a comparison study is performed between the vertical structure and the wire-bonded structures. CM noise and thermal performance are compared in simulations. After that, both modules are fabricated and the CM noise performance is compared in experiments. Finally, a brief discussion is held on the CM noise of a vertical power module with an asymmetrical topology.

II. CM Noise Coupling Mechanisms of Full-Bridge Diode Rectifier

A high-frequency full-bridge diode rectifier is used as a case study. It works as the secondary side of an isolated dc/dc converter, shown in Fig. 1. The impact of module parasitics on CM noise is analyzed to provide guidelines for the module design. V_{IN} represents the secondary side of a high-frequency transformer in a dc/dc converter. Parasitic capacitances to the ground are then considered for node A, B, C, and D. $Z_{\mathrm{dcp}}/Z_{\mathrm{dcn}}$ represents the impedance of positive and negative lines between the C_{out} and the load, which consists of resistance and inductance. AC-side parasitic inductances are considered later in the comprehensive parametric study.

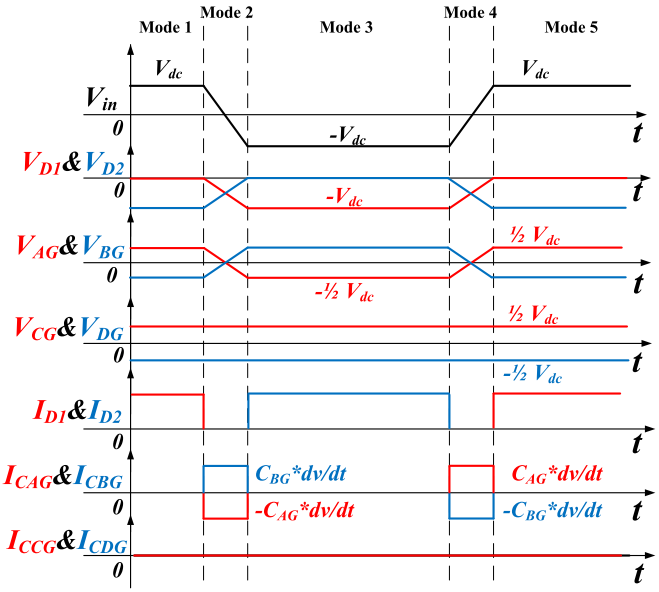


Fig. 2. Operation waveforms of a full-bridge diode rectifier.

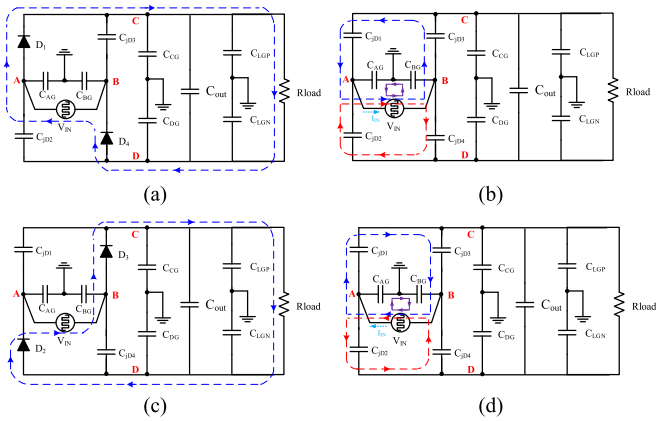


Fig. 3. Switching-mode diagrams of a full-bridge diode rectifier in a switching cycle. (a) Mode 1: positive current flow. (b) Mode 2: *–dv/dt* mode. (c) Mode 3: negative current flow. (d) Mode 4: *dv/dt* mode.

A. CM Noise Behavior

In the steady state, the rectifier has two switching modes and two transient modes within a switching cycle. The basic CM current generation mechanism can be explained with the circuit in Fig. 1(b). If voltage variation is presented on V_{AB}, any mismatch current of C_{AG} and C_{BG} goes to the ground, which is CM current. A similar principle applies to C_{CG} and C_{DG}. The operation waveforms and switching-mode diagrams are shown in Figs. 2 and 3(a) and (d). Due to the large output capacitor (C_{out}), node C and D have much less voltage fluctuation, compared with node A and B. Thus, less CM current is generated by the mismatch of C_{CG} and C_{DG}. CM currents generated by node A and node B dominate. Thus, it is reasonably accurate to ignore the mismatch effect of C_{CG} and C_{DG} in the simplified model. Among the four switching modes, mode 2 and mode 4 generate a significant amount of current going through grounding capacitance C_{AG} and C_{BG}. However, these two grounding currents (I_{CAG} and I_{CBG}) can cancel each other if (1) is satisfied.

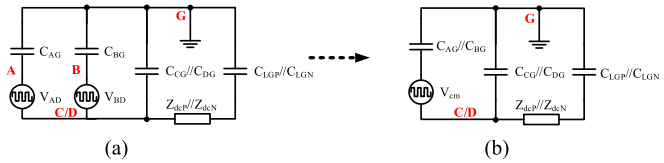


Fig. 4. Derivation of a simplified CM noise equivalent model. (a) Intermedia model. (b) Final model.

TABLE I
CIRCUIT PARAMETERS' IMPACT ON THE CM NOISE

Factors	Value	Symmetry
C_{AG} and C_{BG}	Smaller the better	Significant
Diode ESL and ac-side stray inductance	Smaller the better	Major impact (high frequency)
C_{CG} and C_{DG}	Larger the better	Minor impact
Diode junction capacitance	Minor impact	Major impact (high frequency)
DC-side inductance	Larger the better	Major
Diode reverse recovery	Minor impact	Minor impact
Diode forward voltage	Minor impact	Minor impact

In summary, the full-bridge diode rectifier does not generate noticeable CM current because the ac sides grounding capacitances and voltage slew rates are symmetrical

$$C_{\mathrm{AG}}\frac{d_{\mathrm{VA}}}{dt} = -C_{\mathrm{BG}}\frac{d_{\mathrm{VB}}}{dt}. \tag{1}$$

B. Preferred Module Parasitics Configuration Based on CM Noise Model

To quantify the impact of circuit parasitics and symmetry on CM noise, a simplified CM equivalent model is developed, as shown in Fig. 4(b). Node C and D can be seen as short for CM noise due to the large C_{out}. Node A and B referred to node C/D are modeled and are two voltage sources, as shown in Fig. 4(a). The C_{AG} and C_{BG} branches can be combined based on the Thevenin theorem to form the final model. The equivalent CM voltage source, V_{cm}, is expressed in (2). This model is simple yet effective enough to show main factors in CM noise generation. The CM noise model indicates that for less CM noise at the load side $(C_{\mathrm{LGP}}//C_{\mathrm{LGN}})$, it prefers a smaller C_{AG}, C_{BG} and larger C_{CG}, C_{DG}. Ideally, V_{AD} and V_{BD} are out of phase in a full-bridge rectifier. If $C_{\mathrm{AG}} = C_{\mathrm{BG}}$ also holds, then V_{cm} becomes zero. But if V_{AD} and V_{BD} are not exactly out of phase or $C_{\mathrm{AG}} \neq C_{\mathrm{BG}}$, CM noise appears at the load side

$$V_{\mathrm{cm}}(t) = \frac{C_{\mathrm{AG}}V_{\mathrm{AD}}(t) + C_{\mathrm{BG}}V_{\mathrm{BD}}(t)}{C_{\mathrm{AG}} + C_{\mathrm{BG}}}. \tag{2}$$

With the developed CM model, a comprehensive study investigates the impact of circuit parameters and parasitics on CM noise generation. The results are summarized in Table I.

C_{AG} and C_{BG}: These two ac-side grounding capacitances affect both CM noise generation and propagation. The mismatch between the two can generate CM noise, even if V_{AD} and V_{BD} are out of phase. The two capacitances also provide series attenuation for the CM noise. Matching C_{AG} and C_{BG} is quite challenging to realize at 100% during the design and fabrication process. However, for the same amount of mismatch ratio k ($C_{\mathrm{AG}} = k \times C_{\mathrm{BG}}$), the smaller the capacitances, the weaker the V_{cm} is. Moreover, smaller ac-side capacitances also provide a larger series CM impedance. As a result, it is better to decrease the ac-side grounding capacitance value and match them as much as possible.

C_{CG} and C_{DG}: The matching of these two capacitances has a minor impact on the CM voltage generation as the voltage V_{CD} is relatively stable. Moreover, these two dc-side grounding capacitances can help to filter out some CM noise, so it is preferred to have larger values.

DC-side inductance, L_{dcp} and L_{dcn}: The impedance of $Z_{dcN}//Z_{dcP}$ in high frequency are mainly decided by these two inductances. Together with the dc-side grounding capacitance, C_{CG} and C_{DG}, $L_{dcN}//L_{dcP}$ forms a CM *CL* filter. Without discrete CM choke, these impedances are usually in the order of mΩ and hundreds of nH. Thus, symmetrical dc-side inductances with larger values are usually preferred to achieve a higher series CM impedance.

Diode ESL, ac-side stray inductances, diode reverse recovery, and diode forward voltage: The four parasitics and parameters mainly affect the slew rates of V_{AD} and V_{BD}. The inductances are usually too small to bring any significant attenuation of CM noise, so it is better to match the four characteristics in two phase legs.

III. COMPARISON OF TWO POWER MODULE STRUCTURES

The CM noise analysis above shows, with fixed parasitics tolerances, smaller C_{AG}, C_{BG} and ac-side inductances are preferred. Larger C_{CG} and C_{DG} also help to bypass more CM current. Thermal performance is also critical for a high-power-density system. Therefore, the EMI and thermal performance are compared between two module structures: the traditional wire-bonded structure and the vertically integrated structure.

A. Lateral Wire-Bonded and Vertically Integrated Structures

Based on the two packaging structures, the schematics of a single diode phase-leg are shown in Fig. 5. Rather than placing two devices laterally, the vertically integrated structure stacks two devices together in a vertical way. Such an arrangement aligns the current flow direction in power modules with the vertical power device modules. The two devices are mounted on two substrates. The ac terminal is sandwiched between the two devices.

Due to the 3-D structure, the vertical power modules' parasitics are more favorable toward smaller CM noises. First, the ac-side CM capacitance, C_{AG}, is significantly smaller than the wire-bonded module. This is because the node A is far from the ground plane (G) in the vertical structure, and not used for heat dissipation. Furthermore, two dc busbars also work as shielding layers to further reduce C_{AG}. Second, the dc-side CM capacitances, C_{CG} and C_{DG}, are typically larger than the lateral structure as the copper pattern of node C and node D cover the entire substrates. Third, the elimination of wire bonds decreases

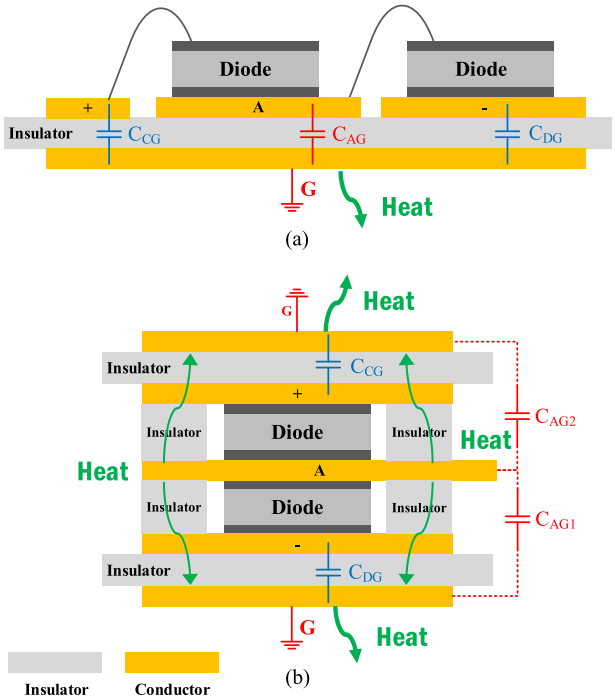


Fig. 5. Diode module packaging structures. (a) Lateral wire-bonded structure. (b) Vertically integrated structure.

the interconnection stray inductance. Fourth, by utilizing the vertical dimension, the module is made smaller, thus decreasing most of the parasitics. These combined properties help to achieve a smaller CM noise. In contrast, the traditional wire-bonded structure tends to have larger C_{AG}, smaller C_{CG} and C_{DG}, and larger stray inductance.

In the traditional wire-bonded structure, there is always a tradeoff between grounding capacitance and thermal impedance of high *dv/dt* nodes, such as A and B. The thermal impedance of the substrate is made smaller with a thinner insulation layer. However, a thinner insulation layer also leads to larger parasitic grounding capacitance. This conflict is not presented in the vertical structure because the heat is mainly dissipated through the two large substrates, dc+, and dc–. In this case, the substrate insulator can be made very thin, as large C_{CG} and C_{DG} are preferred. Furthermore, as each substrate only accommodates one device, the larger area dissipates heat more efficiently. Finally, the vertical module also has a quasi-double-sided cooling capability. The devices are able to dissipate some heat through the ac terminal to the heat sink with one more insulation layer, as shown in Fig. 5. However, this insulation layer is preferred to be thicker to minimize the parasitic grounding capacitance from high *dv/dt* nodes.

The main characteristics of the two module structures are summarized in Table II, concluding that the vertically integrated module inherently achieves both better CM and thermal performance, compared with the traditional later wire-bonded structure.

B. Module Design

To validate the analysis on CM noise and thermal performance, a comparative study is conducted on the lateral wire-bonded structure and vertically integrated structure. The topology is a full-bridge diode rectifier, which functions as the poststage circuit of a typical high-frequency isolated dc/dc converter.

In the comparative study, both modules are designed based on the same area of 20 by 20 mm. The 3-D models of this are depicted in Figs. 6 and 7. The same SiC diodes (CPW41200S020B) are used for both modules. Printed circuit boards (PCBs) are used for the substrate for simplification. Having the same amount of copper in both modules is desired. Thus, a 2 oz. PCB is utilized for the lateral module substrate, while two 1 oz. PCBs are applied for the vertical module. The ac lead frames in the vertical modules are implemented by small pieces of PCBs. Both devices are connected to the ac spacers in a phase leg, negating the need for accurate alignment. To obtain a fair comparison, several iterations on module layouts are conducted to achieve an optimal thermal performance for both modules.

TABLE II
MAIN CHARACTERISTICS OF THE TWO MODULE STRUCTURES

Power module structures	Lateral wire-bonded structure	Vertically integrated structure
Parasitic inductance	Large	Small
Parasitic grounding capacitance	Large	Small
Cooling capability	Single-sided cooling	Quasi-double-sided cooling

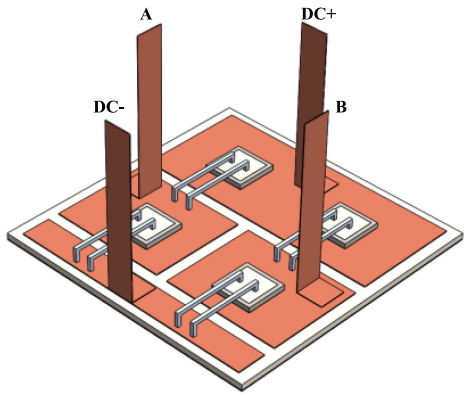


Fig. 6. Three-dimensional model of the wire-bonded module.

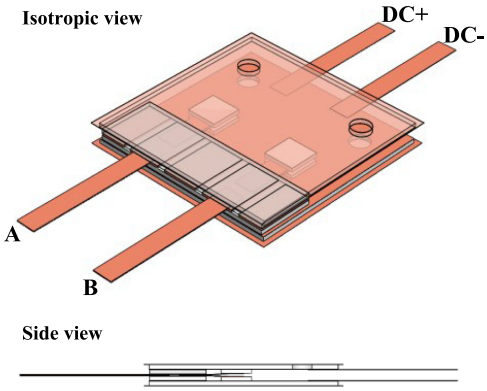


Fig. 7. Three-dimensional model of the vertically integrated module.

TABLE III
PARASITICS EXTRACTION RESULTS OF THE TWO MODULES

	Lateral module	Vertically integrated module	Reduction ratio
Inductance (per device)	3.181 nH	2.221 nH	3.120 dB
C_{AG}	6.836 pF	0.07140 pF	39.622 dB
C_{BG}	6.764 pF	0.07102 pF	39.576 dB
C_{CG}	15.108 pF	35.946 pF	−7.529 dB
C_{DG}	4.721 pF	35.958 pF	−17.635 dB

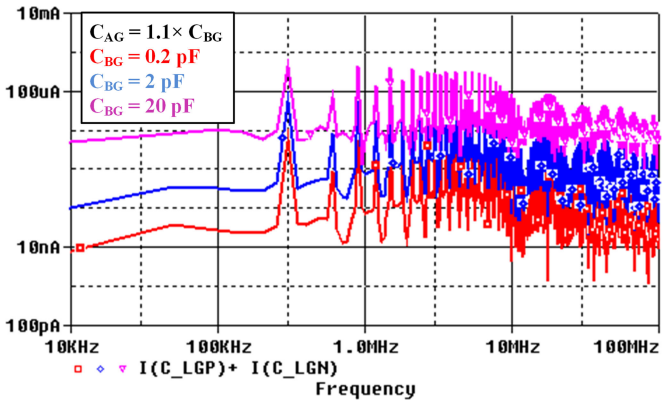


Fig. 8. C_{AG} and C_{BG}'s impact on CM noise at the load side.

The copper layout and bare die locations have been adjusted to ensure the same maximum junction temperature distribution and lower maximum junction temperature.

C. Parasitic Extraction

Parasitics of the two designed modules are extracted with Q3D. As shown in Table III, in the vertical module, C_{AG} and C_{BG} are reduced significantly. Diodes top-side interconnection inductances are also reduced as wire bonds are replaced by copper sheets. Meanwhile, C_{CG} and C_{DG} are increased to become more symmetrical. The results prove smaller C_{AG}, C_{BG}, larger C_{CG}, C_{DG}, and smaller ac-side stray inductance are possible in the vertical module, making parasitics symmetry easier to achieve as well.

D. Verification and Comparison of CM Noise

With the extracted parasitics in Table III and the diode model from CREE, a detailed circuit simulation model is developed in PSPICE to validate the CM noise model and also to compare the load-side CM noise of the two modules. Fig. 8 shows the results of a case study on the impact of C_{AG} and C_{BG}, illustrating a 20 dB reduction on the load-side CM noise current is achieved by realizing a 20 dB reduction on C_{AG} and C_{BG}. A similar case study is conducted on C_{CG} and C_{DG}. Fig. 9 shows when these capacitances become large enough, significant attenuation is also achieved. By increasing the two capacitances from 200 to 2000 pF, the CM current is reduced by 18 dB. Both simulation results agree with the trend indicated in the CM noise model of Fig. 4.

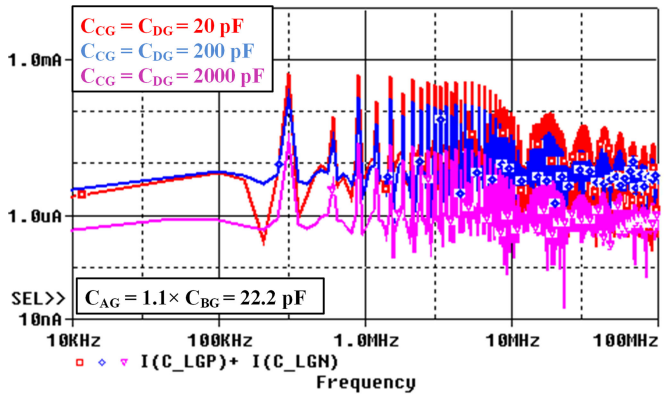


Fig. 9. C_{CG} and C_{DG}'s impact on CM noise at the load side.

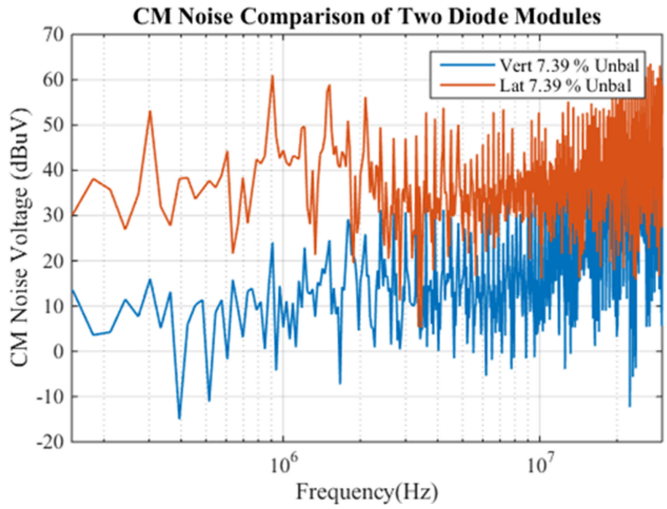


Fig. 10. Simulated CM noise voltage spectrum using FFT with $C_{AG} = 1.074 \times C_{BG}$.

To compare the CM noise performance of the two modules, a 7.4% mismatch between C_{AG} and C_{BG} is assumed, namely, $C_{AG} = 1.074 \times C_{BG}$. With line impedance stabilization networks (LISNs) added at the load side, the simulated CM noise voltage spectrums of two modules are shown in Fig. 10. The spectrums are obtained through fast Fourier transform (FFT) of the time domain signals. The CM noise envelope of the vertical module is reduced significantly between 150 kHz and 10 MHz. The noise reduction ratio in the high-frequency region is affected by the resonance between the dc-side inductance and grounding capacitances.

E. Comparison of Thermal Performance

As previously discussed, the vertically integrated module has inherently better performance due to a larger surface area and quasi-double-sided cooling capability. Steady-state FEM simulation is performed to verify the steady-state thermal performance analysis of two modules. In the simulation, each bare die body is assigned with the same heat generation. The substrate surfaces, where cold plates or heat sinks are attached to, are assigned as either a fixed case temperature (the first scenario) or an equivalent heat transfer coefficient (HTC; scenario scenario).

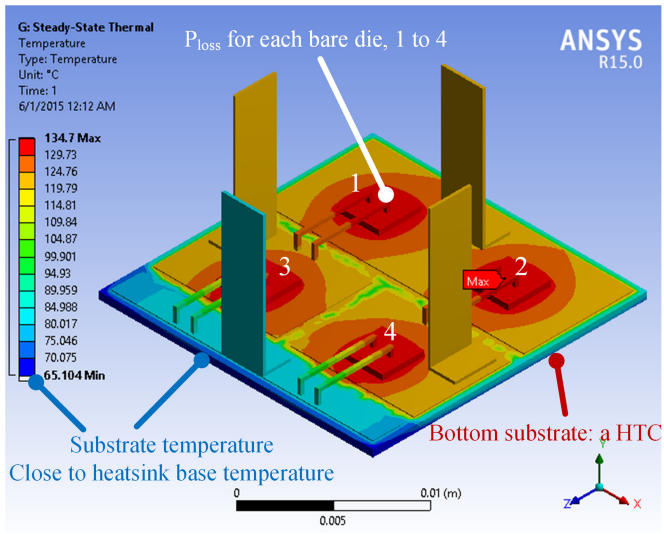
TABLE IV
COMPARISON ON THERMAL RESISTANCE OF THE TWO MODULES

	Lateral module	Vertically integrated module	Reduction ratio
Junction temperature	86.4 °C	71.1 °C	17.7%
Thermal Resistance	5.1 °C/W	3.8 °C/W	25.5%

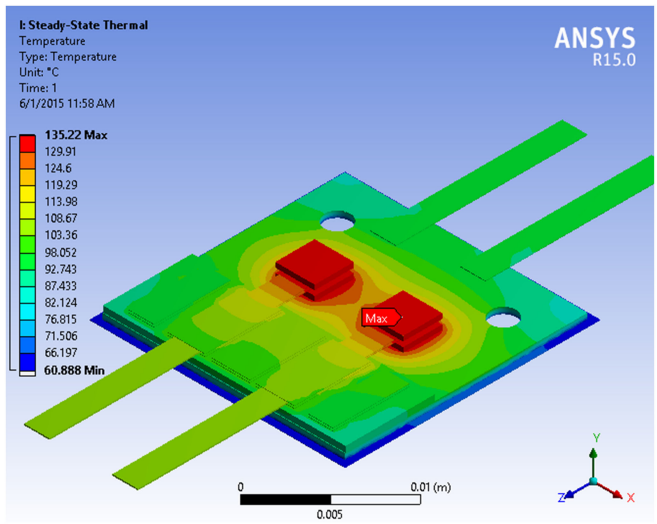
The first scenario compares the thermal performance of the modules and in a liquid cooled application, in which a fixed case temperature of 25 °C is set for the heat dissipation surfaces of both modules. Each diode dissipates 3 W. Results in Table IV show the vertical module exhibits 17.7% lower junction temperature and 25.5% lower thermal resistance from junction to case.

The second scenario involves both the module and actual heat sinks. This situation simulates a forced-air-cooled condition. The same series of heat sinks from Wakefield-Vette is used for both modules. One 902-21-1-28-2-B-0 with 28 mm height is selected for the lateral module and two 902-21-1-12-2-B-0 with 12 mm height are chosen for the vertical module, which results in similar volumes of heat sinks. In the thermal simulation, equivalent HTCs are assigned at the bottom surface of the module substrates. The HTCs are calculated based on heat sink thermal resistance and heat sink base area, which are 868.9 W/(m^{2}K) for 902-21-1-28-2-B-0 and 587.5 W/(m^{2}K) for 902-21-1-12-2-B-0. The power losses of the devices are adjusted to achieve a 135 °C maximum junction temperature. Each power loss corresponds to a power rating. The power loss versus output power curve is extracted from the detailed circuit simulation model. The simulated temperature distributions at steady-state conditions are shown in Fig. 11. The resulted power handling capability, power rating, and power density are shown in Table V. The power density difference of the modules are larger when heat sinks are considered, and the vertical diode module exhibits a 51% improvement in the power density. The improvement is even larger than the previous scenario because the thermal resistance of a typical forced-air-cooling heatsink does not decrease linearly with the increased fin height. In other words, two shorter heatsinks perform better than a taller one.

In summary, the two case studies demonstrate that the vertically integrated module inherently has better thermal performance. Furthermore, two sides cooling capability of the module can take advantage of the heat sink's thermal impedance characteristics to further improve the power density.



(a)



(b)

Fig. 11. Simulated module temperature distribution with heat sinks. (a) Lateral wire-bonded diode power module. (b) Vertically integrated diode power module (the top-side substrate is hidden).

TABLE V
THERMAL PERFORMANCE COMPARISON WITH HEAT SINKS

	Lateral module	Vertically integrated module
Heat sink size (mm^3)	20 × 20 × 28	20 × 20 × 12 × 2 (two heatsinks)
Total power loss (W)	11.80	16.08
Module Power Rating (W)	897	1223
Power Density (W/inch^3)	1225	1855

IV. MODULE FABRICATION AND TEST RESULTS

A. Module Fabrication

According to the design in Section III-B, the two fabricated modules are shown in Fig. 12. The fabrication process of the lateral wire-bonded module is following the traditional practicing. For substrates, 2 oz. PCBs are used. The copper pattern was realized by a Computer Numerical Control router. The four diodes in bare die form are then attached to the PCB with Sn96.5Ag3.0Cu0.5 solder preforms. Two 10 mils wire bonds are used to connect the diode top surface to the substrate. The power terminals are mounted with Sn63Pb37 solder preforms. Finally, the module is encapsulated with Nusil 2188.

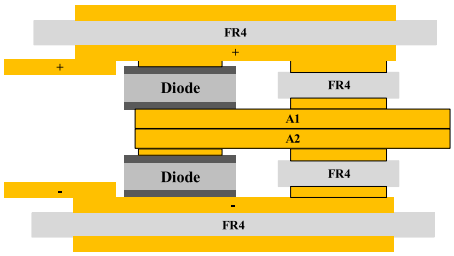


Fig. 12. Prototypes of the lateral and vertical modules.

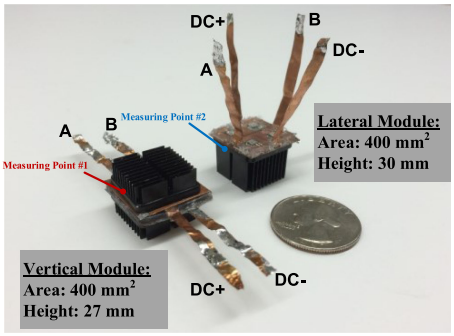
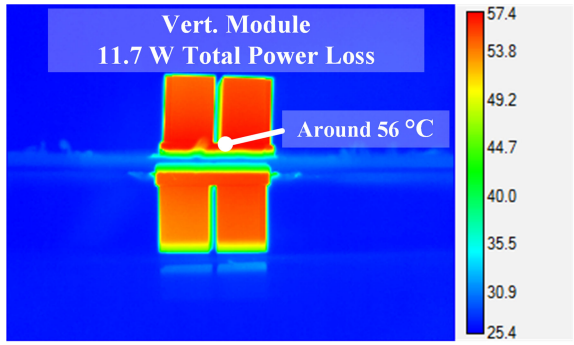


Fig. 13. Simplified prototype design of the vertically integrated module.

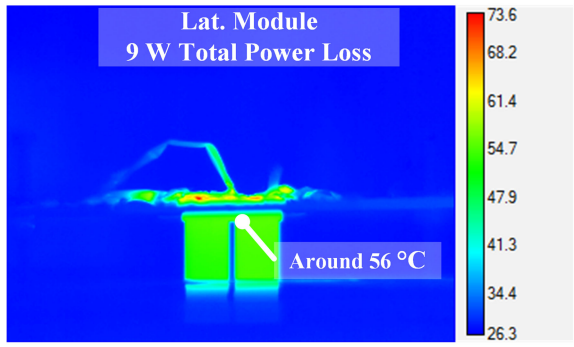
Fabrication of the vertically integrated module starts with the patterning of 1 oz. PCB substrates and ac terminal spacers. The ac terminal spacer is soldered to the substrate with Sn96.5Ag3.0Cu0.5 solder preforms, and a small copper spacer is attached to each anode pad on the diode with silver epoxy H20E to increase the distance from the guarding rings, as shown in Fig. 13. Nusil 2188 is then applied to protect the guarding rings and the edge of the chip. After the die preparation, four bare dies are attached to the substrates with silver epoxy. Copper foil is used to connect the switching nodes to the ac terminal spacer. After that, Nusil 2188 is used to encapsulate the module, and the two substrates are clamped together.

B. Thermal Performance Comparison in Forced-Air-Cooling Conditions

Experiments have been conducted to compare the thermal performance of two modules in forced-air-cooling condition. A dc voltage source is used to bias four diodes from node D to node C. The power supplied to the module is adjusted such that the measured point #1 and point #2 temperatures are close to the FEA simulated temperature. With forced air cooling of around 400 LFM flow rate, the temperature profiles measured by a thermal camera are shown in Fig. 14. Due to limited equipment, it is difficult to achieve the desired flow rate, which is higher than 400 LFM in the experiment. The measured heat sink temperatures are around 7 °C lower, as listed in Table VI. Overall, the measured thermal performance of both modules is worse than the ideal thermal simulations, which exhibit around 23%–27% less loss handling capability. The worse performance is mainly due to fabrication quality issues, which can lead to larger contact and thermal resistance of the bare die attachment and topside interconnections. However, vertical module's 32.2% more power loss handling capability could still prove a better thermal performance, which means 47% improvement of power density.



(a)



(b)

Fig. 14. Thermal image of two modules. (a) Vertically integrated module. (b) Lateral wire-bonded module.

TABLE VI
THERMAL PERFORMANCE COMPARISON OF SIMULATION AND EXPERIMENT

	Lateral module	Vertically integrated module	Improvement Vert. versus Lat.
Simulated power loss (W)	11.80	16.08	36.3%
Measured power loss (W)	9 (76% of 11.8)	11.7 (73% of 16.08)	32.2%
Simulated substrate temperature (°C)	65.1	62.5	N/A
Measured heatsink temperature (°C)	Around 56	Around 56	N/A

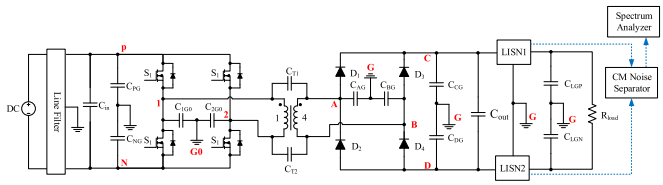


Fig. 15. Test schematic of the diode module CM noise with a front stage full-bridge inverter and a transformer.

C. CM Noise Test Setup of the Diode Rectifier

Experiments have been conducted to validate the CM noise model and compare the performance of the two modules. A schematic of the CM noise test setup is shown in Fig. 15.

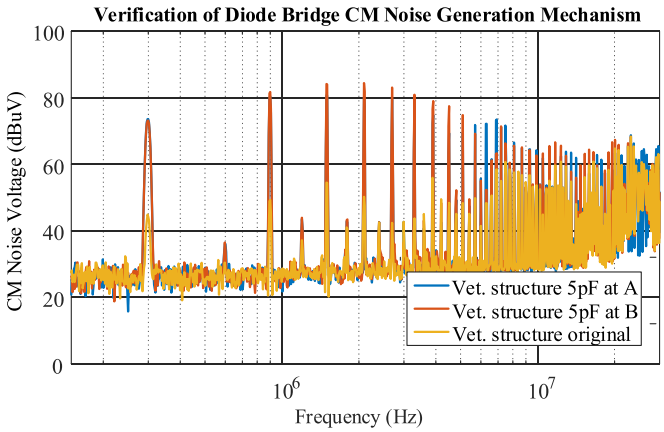


Fig. 16. Load-side CM noise spectrum (peak detection) of the vertically integrated module when 5 pF is added at either node A or B.

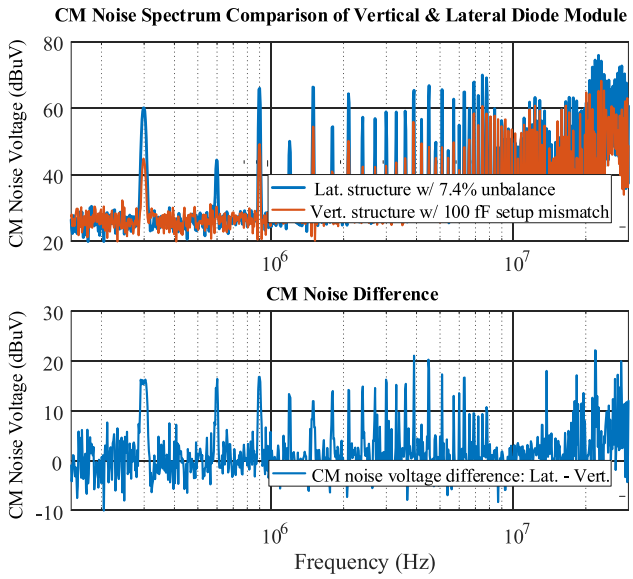


Fig. 17. Comparison of CM noise voltage spectrum (peak detection) between the lateral and vertical module with grounding capacitance mismatch.

The primary-side H-bridge inverter generates high-frequency floating square voltage waveform for the secondary-side diode bridge. The EMI noises at the output side are measured by two LISNs, inserted between the module output and the load. Two LISNs outputs are fed to a CM noise separator to pass the CM noise while rejecting the DM noise. The output CM voltage is sent to a spectrum analyzer. The high-frequency diode rectifier is fed by a full-bridge inverter and a 1:4 step-up transformer. The test configuration is specially designed to minimize the influence of CM noises generated by the primary-side circuit.

1) A step-up transformer allows a lower dc voltage at the primary-side circuit.
2) The transformer is also carefully designed to achieve a 10 pF ($C_{T1} + C_{T2}$) winding-to-winding coupling capacitance.
3) Grounds of two sides (G0 and G) are isolated from each other.
4) A line filter is added between the input dc power supply and the full-bridge inverter.

As a result, most of the CM currents generated by the input power supply and the inverter do not travel to the secondary-side circuit. A 1.74 pF grounding capacitor added to node B compensates the setup grounding capacitance mismatch. However, due to the accuracy of capacitance, there is still some grounding capacitance mismatch in the test setup preventing perfect compensation.

D. Verification of Diode Bridge CM Noise Generation Mechanism

As discussed in Section II, the majority of the load-side CM noise is generated by the mismatched ac-side grounding capacitances, $|C_{\mathrm{AG}} - C_{\mathrm{BG}}|$. This noise generation mechanism is verified by intentionally introducing mismatch between C_{AG} and C_{BG}. A 5 pF capacitor is added between node A to the ground and then node B to ground, respectively. The measured CM voltage spectrums with peak detection are shown in Fig. 16. Note that original vertical module has small CM noise, however, adding the 5 pF grounding capacitance to either node A or B yields similar CM noise spectrums. The peak noise amplitudes increase by about 30 dB for most frequencies.

E. CM Noise Comparison of Two Modules

To allow more flexibility in the validation process, the ac-side grounding capacitances in the lateral module are carefully designed the same, such as $C_{\mathrm{AG}} = C_{\mathrm{BG}}$. In the prototype, they are measured as $C_{\mathrm{AG}} = 8.773$ pF and $C_{\mathrm{BG}} = 8.755$ pF, with 0.21% mismatch. To match the previous EMI simulation, a 0.648 pF grounding capacitor (7.4% mismatch) is added at node A of the lateral module. However, in the vertical module, a 7.4% mismatch of grounding capacitance (5 fF) is very difficult to realize due to the accuracy issue. However, the residual mismatch grounding capacitance of the test setup (around 100 fF) is already much larger than 5 fF. Thus, no mismatch capacitance is added to the vertical module during the test. As shown in Fig. 17, the vertical module's CM noises (peak detection) have an around 15 dB noise reduction from 150 kHz to 6 MHz.

The measured CM peak noise difference between the lateral and vertical is smaller than the simulated results in Fig. 10. The possible reasons are as follows:

1) influence of the residual grounding capacitance mismatch in the test setup;
2) influence of the dc input power supply and the CM noise of the inverter;
3) the inherent topological symmetry of the diode rectifier, which alone generates very small CM noise.

In other words, the vertical power module only generates a very small amount of CM noise and is easily masked by CM noise occurring during the test setup.

V. Discussion

Being a symmetrical topology, a full-bridge diode rectifier may not fully demonstrate the benefit of reduced grounding

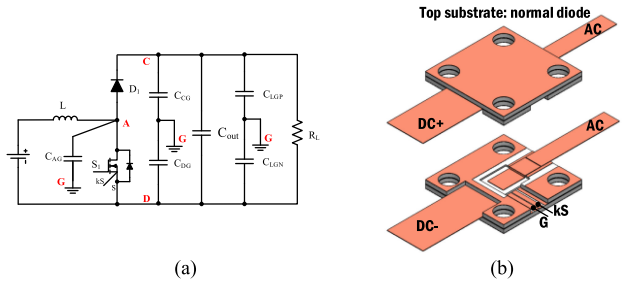


Fig. 18. Vertically integrated phase-leg module for boost converters. (a) Schematic. (b) 3D model.

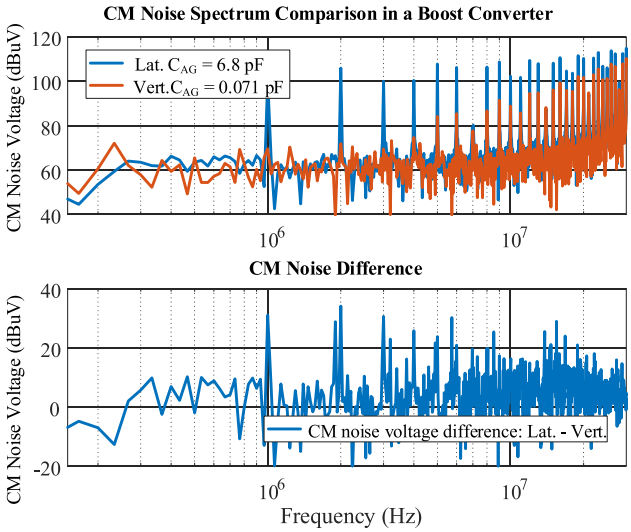


Fig. 19. Comparison of input CM noise voltage spectrum between the lateral and vertical module in a boost converter.

capacitance brought by the vertically integrated structure. This section aims to demonstrate a more significant advantage in CM noise reduction in an unsymmetrical topology. A boost converter is selected for the case study. The schematic and 3-D model of the vertically integrated boost module is shown in Fig. 18, in which the MOSFET is flip-chip packaged. In the vertically integrated module, the switching node grounding capacitance C_{AG} can be made very small compared with the lateral structure. Detailed circuit simulations are conducted at the condition of $V_{\mathrm{in}} = 150\,\mathrm{V}$, $V_{\mathrm{out}} = 380\,\mathrm{V}$, $f_{\mathrm{sw}} = 1\,\mathrm{MHz}$, and $P_{\mathrm{out}} = 660\,\mathrm{W}$. The same parasitic grounding capacitances from Section III are used, 6.8 pF for the lateral module and 0.071 pF for the vertical module. The simulated CM noise spectrum, with LISN added at the input side, is shown in Fig. 19. This reveals about 30 dB CM noise reduction is achieved, starting from 1 MHz (switching frequency) to 6 MHz. Compared with full-bridge diode modules, the noise reduction is larger. More importantly, the reduction is not easily affected by other CM noises due to its higher noise floor. Therefore, the CM reduction would be more helpful in shrinking the CM EMI filter size.

VI. Conclusion

This paper investigates the module design for better CM noise and thermal performance. A high-frequency full-bridge diode rectifier is used as a case study. Impacts of module parasitics and device parameters are analyzed with a CM equivalent model and a comprehensive parametric study. Studies show that both the value and symmetry of the module parasitics are critical for the CM noise performance. In particular, to suppress CM noise, it is preferred to have

1) smaller and balanced ac-side CM parasitic capacitances;
2) smaller and balanced ac-side diodes interconnection inductance;
3) larger and balanced dc-side CM parasitic capacitances.

The lateral wire-bonded structure and the vertically integrated structure are compared against the CM noise requirements. The vertical module does not only meet the CM noise requirements but also exhibits a better thermal performance. For verification, a comparative study is conducted between the two modules. Detailed switching circuit simulation results show the vertical module achieves significant CM noise reduction for most of the low-frequency range. The thermal simulation also shows the vertical module exhibits a 25.5% lower thermal resistance from junction to case and a 51% increase of power density in a force-air-cooled condition. To verify the simulation, the two modules are fabricated. Experimental results indicate a 15 dB of CM noise reduction is realized from 150 kHz to 6 MHz. And a 32% improvement of power density is achieved in a force-air-cooling condition. Finally, a case study is conducted to demonstrate vertical power module's CM noise permanence in unsymmetrical topologies, in which a 30 dB CM noise reduction is achieved up to 6 MHz.

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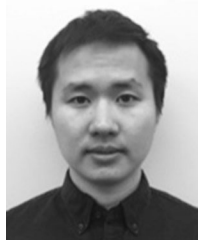

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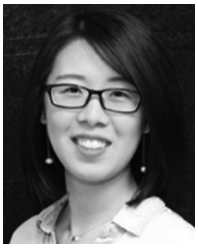

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