Analysis and Study of the Duty Ratio Effects on the Class-E_M Power Amplifier Including MOSFET Nonlinear Gate-to-Drain and Drain-to-Source Capacitances

Mohsen Hayati, Hamed Abbasi, Marian K. Kazimierczuk, *Fellow, IEEE*, and Hiroo Sekiya, *Senior Member, IEEE*

***Abstract*—In this paper, the effects of the duty ratio variation on the class-E_M power amplifier are studied and analyzed, including nonlinear gate-to-drain and drain-to-source parasitic capacitances. The duty ratio is one of the important parameters in class-E_M power amplifiers, which has high effects on the switch voltage and current waveforms, output power, efficiency, power loss, and output phase shift. To achieve a better agreement between theoretical and experimental results, the nonlinear gate-to-drain and drain-to-source parasitic capacitances are included in theoretical analysis. To demonstrate the validity of the presented analysis, five class-E_M power amplifiers are designed, simulated, fabricated, and tested using IRF510 MOSFET with the duty ratio equal to 0.5, 0.6, and 0.7 and IRFZ24N MOSFET with the duty ratio equal to 0.5 with and without considering MOSFET nonlinear capacitances. It is shown that the amplifier with IRFZ24N MOSFET has higher efficiency than that with IRF510 MOSFET. This is because of the lower drain-to-source on-state resistance of the IRFZ24N MOSFET. The obtained efficiency with IRFZ24N MOSFET considering nonlinear capacitances at the operating frequency of 3.5 MHz was 95.7%. The obtained output power for IRF510 and IRFZ24N MOSFETs at the duty ratio equal to 0.5 was 14.41 and 17.82 W, respectively. Simulation and theoretical results are performed using PSpice and MATLAB, respectively. The theoretical results and PSpice simulations agreed with experimental results.**

***Index Terms*—Class-E_M power amplifier (PA), efficiency, mixed mode, nonlinear gate-to-drain capacitance, nonlinear drain-to-source capacitance, soft switching, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

RADIO frequency (RF) power amplifiers (PAs) can be used to convert dc power into microwave signal. Higher power efficiency offers a higher output microwave signal and lower power loss [1]. To achieve a high efficiency, the PA transistor operates as an on/off switch at the RF-output frequency. The switch-mode PAs are classified into two categories, which are single mode and mixed mode. The single-mode switching PAs category consists of class-E, E^{-1}, F, and F^{-1} [1]. The famous mixed mode switching PAs category consists of class-EF, E/F, and E_M. Efficiency, switching peak voltage, power dissipation, gain, and complexity are the main challenges in the PAs design. The class-F PA operates at high frequency with low peak voltage, although it has lower efficiency and complex circuit in comparison with other switch-mode PAs [1]. The complexity of the class-F PA is caused by its many resonant circuits. Class-F^{-1} [2] is the dual tuning of class-F. In [3], the class-F and class-F^{-1} amplifiers are numerically compared in terms of the optimum load impedance, output power, and efficiency as functions of the conduction angle.

In [4] and [5], the efficiency of the class-F amplifier has been improved using an embedded harmonic control circuit in the structure. To increase the output power capability and efficiency, class-EF and class-E/F PAs have been presented in [6]–[9]. The analysis and design of the class E/F amplifier have been presented in [6] and [7]. High-efficiency class-EF amplifiers have been presented in [8] and [9]. Because the class-E amplifier has a simple structure and high efficiency, many studies of this class have been done [10]–[19]. In [20], the analysis of the class-E PA with the MOSFET linear gate-to-drain capacitance and nonlinear drain-to-source capacitance, which satisfies the class-E zero-voltage switching (ZVS) and zero-voltage derivative switching (ZVDS) conditions at any duty ratio, has been carried out. To achieve higher power conversion efficiency of the class-E amplifier when the transistor has a long turn-off switching time, a modified class-E amplifier, which is called class-E_M, is presented. Fig. 1 shows the circuit topology of the class-E_M PAs. The circuit of the class-E_M amplifier consists of the main circuit and the auxiliary circuit. The turn-off transition time is important at high frequencies. A limitation of the class-E amplifier is the turn-off switching time with increasing operating frequency. Also, the class-E transistor has a current jump at turn off. In the class-E_M, by injecting biharmonic current to the main circuit

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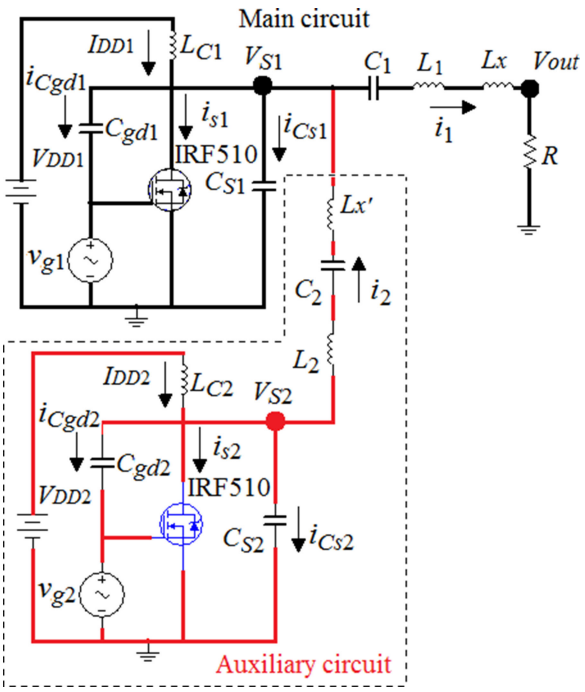

Fig. 1. Class-E_M power amplifier circuit.

using an auxiliary circuit, both nominal conditions for current and voltage, which are the ZVS and ZVDS conditions at turn-on instant and the zero-current switching (ZCS) and zero-current derivative switching (ZCDS) conditions at turn-off instant, can be achieved. So, continuous switch voltage and current waveforms can be realized in the main circuit. The turn-off transition time is approximately inversely proportional to the input power. The auxiliary circuit causes input power reduction and therefore achieves higher power-added efficiency. In [21], the analysis of the class-E_M switching-mode tuned PA with high efficiency and slow switching transistor has been presented. In its analysis, the MOSFET nonlinear gate-to-drain and drain-to-source capacitances were not considered. In [22], the effect of MOSFET body junction diode nonlinear capacitance has been considered in the design, but still the MOSFET nonlinear gate-to-drain capacitance was not considered. In [23], to achieve less total harmonic distortion and to have less critical impedance matching network, a symmetrical structure of the class-E_M has been presented. In [24], a class-E_M PA with a single input signal has been presented. In [25], a novel analytical procedure for the class-E_M amplifier has been presented. In its analysis, the harmonic components have been considered in the output currents of the main and auxiliary circuits. In [26], the class-D, E, E^{-1}, DE, and F switch-mode PAs have been introduced.

The focus of this paper is as follows:

1) analytical study of the duty ratio effects on the class-E_M PA performance;
2) design procedure of the class-E_M PA at any duty ratio; and
3) analytical study of the nonlinearity effects of the gate-to-drain and drain-to-source parasitic capacitances on the class-E_M PA performance.

This paper is organized as follows. Section II presents the circuit topology of the class-E_M PA and introduces its elements and voltage and current waveforms. Section III describes analytically the effects of the duty ratio and nonlinearity of the gate-to-drain and drain-to-source parasitic capacitances on the output phase shift, output current amplitude, power loss in main and auxiliary circuits, switch voltage and current waveforms, maximum switch voltage and current, efficiency, and maximum output power capability. In addition, expressions for all elements of the class-E_M PA are derived at any duty ratio based on the presented analysis. Section IV presents the validity of the presented analysis; five class-E_M PAs with IRF510 MOSFETs with the duty ratio equal to 0.5, 0.6, and 0.7 and IRFZ24N MOSFET with the duty ratio equal to 0.5 with and without considering nonlinear capacitances are designed, simulated, fabricated, and tested. Finally, conclusions are presented in Section V.

II. Class-E_M Power Amplifier

A. Circuit Topology

The inductances L_{C1} and L_{C2} shown in Fig. 1 are used to block the ac signals and supply a pure dc current for the circuits. The capacitances C_{S1} and C_{S2} are the sum of the internal drain-to-source nonlinear parasitic capacitances and external linear capacitances of the main and auxiliary transistors, respectively, which are as follows:

$$\begin{aligned} C_{S1} &= C_{\mathrm{ds1}} + C_{\mathrm{fix1}} \\ C_{S2} &= C_{\mathrm{ds2}} + C_{\mathrm{fix2}} \end{aligned} \tag{1}$$

where C_{fix1} and C_{fix2} are the external linear capacitances of the main and auxiliary transistors, respectively. The capacitances C_{ds1} and C_{ds2} are the nonlinear drain-to-source MOSFET parasitic capacitances in the main and auxiliary circuit, which are given as

$$C_{\mathrm{ds1}} = \frac{C_{j01}}{\left(1+\frac{V_{S1}}{V_{\mathrm{bi1}}}\right)^{m1}}, \quad C_{\mathrm{ds2}} = \frac{C_{j01}}{\left(1+\frac{V_{S2}}{V_{\mathrm{bi1}}}\right)^{m1}} \tag{2}$$

where V_{S1} and V_{S2} are the drain-to-source voltages of the main MOSFET and the auxiliary MOSFET, respectively, and V_{bi1} is the built-in voltage of the pn junction, C_{j01} is the drain-to-source capacitance at $V_{S1}=0$ or $V_{S2}=0$, and m_1 is the grading coefficient for the nonlinear drain-to-source capacitances. The capacitances C_{gd1} and C_{gd2} are the nonlinear gate-to-drain MOSFET parasitic capacitances in the main and auxiliary circuit, respectively. They are given as

$$C_{\mathrm{gd1}} = \frac{C_{j02}}{\left(1+\frac{V_{\mathrm{gd1}}}{V_{\mathrm{bi2}}}\right)^{m2}}, \quad C_{\mathrm{gd2}} = \frac{C_{j02}}{\left(1+\frac{V_{\mathrm{gd2}}}{V_{\mathrm{bi2}}}\right)^{m2}} \tag{3}$$

where V_{gd1} and V_{gd2} are the voltage across the gate-to-drain capacitance in the main and auxiliary circuit, C_{j02} is the initial gate-to-drain capacitance at $V_{\mathrm{gd1}}=0$ or $V_{\mathrm{gd2}}=0$ and C_{gd1} is the built-in potential corresponding to C_{gd1} and C_{gd2}, and m_2 is the grading coefficient for the nonlinear gate-to-drain capacitances. It should be noted that super-junction devices and GaN devices with different field-plate arrangements have the nonlinear capacitance that is not properly modeled by (2) and

TABLE I
PARAMETERS OF THE MOSFETS

MOS	C_{j01} (pF)	$V_{\rm bi1}$ (V)	m_1	C_{j02} (pF)	$V_{\rm bi2}$ (V)	m_2
IRF510	298	0.774	0.423	185	0.5	0.651
IRFZ24N	296	0.51	0.3	438	0.5	0.5787

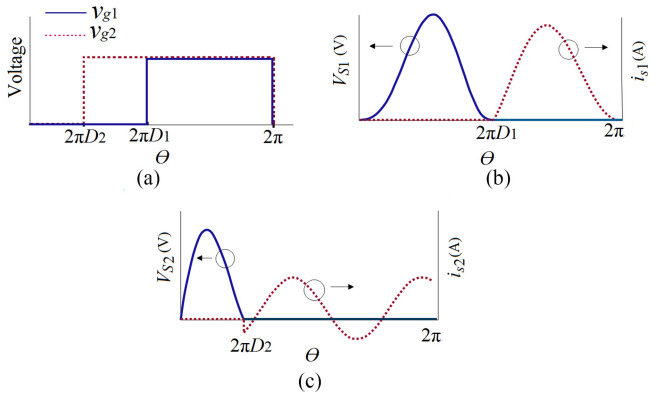

Fig. 2. (a) The waveforms of the input voltages v_{g1} and v_{g2}. (b) Nominal current and voltage waveforms of the class-E_M amplifier for the main MOSFET. (c) Current and voltage waveforms of the class-E_M amplifier for the auxiliary MOSFET.

(3). The parameters of the IRF510 and IRFZ24N MOSFETs are shown in Table I. These parameters are obtained from PSpice MOSFET models given by International Rectifier [27] and Vishay Intertechnology [28]. L_1 and C_1 are calculated so that they resonate at the operating frequency. L_2 and C_2 are calculated so that they resonate at the second harmonic of the operational frequency. The phase shift of i_1 in the main circuits is created by L_x and the phase shift of i_2 current in the auxiliary circuits is created by $L_{x'}$. In this paper, it is assumed that the transistors act as on/off switches with zero resistance at the turn-on instance and extremely high resistance at the turn-off instance.

B. Voltage and Current Waveforms

The waveforms of the input voltages v_{g1} and v_{g2} are shown in Fig. 2(a). D_1 and D_2 are the duty ratios of the main and auxiliary circuits. Nominal current and voltage waveforms of the class-E_M amplifier for the main MOSFET are shown in Fig. 2(b). Fig. 2(b) and (c) shows that the class-E_M amplifier satisfies the ZVS and ZVDS conditions for drain-to-source voltage and the ZCS and ZCDS conditions for MOSFET current in the main circuit and the ZVS condition for drain-to-source voltage in the auxiliary circuit. These conditions make the voltage and currents waveforms do not have overlap, which results in high efficiency.

III. PRESENTED ANALYSIS

By Kirchhoff's current laws (KCL) at the drain of the MOSFET in the main circuit in$0 \le \theta \le 2\pi D_1$, we get

$$i_{CS1} = i_2 - i_{\text{}} + I_{\rm DD1} - i_{C\rm gd1} \tag{4}$$

where i_{CS1} is the sum of current flowing in $C_{\rm ds1}$ and $C_{\rm fix1}$, and $i_{C\rm gd1}$ expresses the current flowing in $C_{\rm gd1}$. So (4) is rewritten as

$$\omega C_{S1}\frac{dV_{S1}}{d\theta} = I_{\rm DD1} + i_2 - i_1 - \omega C_{\rm gd1}\frac{dV_{C\rm gd1}}{d\theta}. \tag{5}$$

The loaded quality factor Q is expressed as follows:

$$Q = \frac{\omega L}{R} \tag{6}$$

where $L = L_1 + L_x$. Q is high enough to create a pure sinusoidal current at the output. In this design, only the fundamental component for the main circuit and the biharmonic component for the auxiliary circuit are considered and it is assumed that other harmonic components have negligible values. Currents i_1 and i_2 shown in Fig. 1 can be written as

$$i_1 = I_{m1}\sin(\theta+\varphi_1); \quad i_2 = I_{m2}\sin(2\theta+\varphi_2) \tag{7}$$

where φ_1 and φ_2 are the phase shift between the input and output voltage in the main and auxiliary circuit, respectively. I_{m1} and I_{m2} are currents amplitude. Considering $v_{g1} = 0$ in$0 \le \theta \le 2\pi D_1$, $V_{C\rm gd1}$ is equal to V_{S1}. Also, substituting (1) and (7) into (5), we obtain

$$\omega(C_{dS1} + C_{\rm fix1} + C_{\rm gd1})\frac{dV_{S1}}{d\theta} = I_{\rm DD1} + I_{m2}\sin(2\theta+\varphi_2) - I_{m1}\sin(\theta+\varphi_1). \tag{8}$$

Substituting (2) and (3) into (8)

$$\omega\left[\frac{C_{j01}}{\left(1+\frac{V_{S1}}{V_{\rm bi1}}\right)^{m1}} + C_{\rm fix1} + \frac{C_{j02}}{\left(1+\frac{V_{\rm gd1}}{V_{\rm bi2}}\right)^{m2}}\right]\frac{dV_{S1}}{d\theta} = I_{\rm DD1} + I_{m2}\sin(2\theta+\varphi_2) - I_{m1}\sin(\theta+\varphi_1). \tag{9}$$

By integrating (9), V_{S1} can be calculated as

$$\frac{\omega C_{j01}V_{\rm bi1}}{1-m_1}\left[\left(1+\frac{V_{S1}}{V_{\rm bi1}}\right)^{1-m_1} - 1\right] + \frac{\omega C_{j02}V_{\rm bi2}}{1-m_2} \times \left[\left(1+\frac{V_{S1}}{V_{\rm bi2}}\right)^{1-m2} - 1\right] + \omega C_{\rm fix1}V_{S1} = I_{\rm DD1}\theta + I_{m1}(\cos(\theta+\varphi_1) - \cos(\varphi_1)) - 0.5I_{m2}(\cos(2\theta+\varphi_2) - \cos(\varphi_2)). \tag{10}$$

At switch turn-on instant of the main circuit, the switch voltage V_{S1} satisfies the ZVS and ZVDS conditions, which are expressed as

$$V_{S1}(2\pi D_1) = 0 \tag{11}$$

$$\left.\frac{dV_{S1}}{d\theta}\right|_{\theta=2\pi D_1} = 0. \tag{12}$$

Using (9)–(12)

$$I_{\rm DD1} + I_{m2}\sin(4\pi D_1+\varphi_2) - I_{m1}\sin(2\pi D_1+\varphi_1) = 0 \tag{13}$$

$$I_{\rm DD1}2\pi D_1 + I_{m1}[\cos(2\pi D_1+\varphi_1) - \cos(\varphi_1)] - 0.5I_{m2}[\cos(4\pi D_1+\varphi_2) - \cos(\varphi_2)] = 0. \tag{14}$$

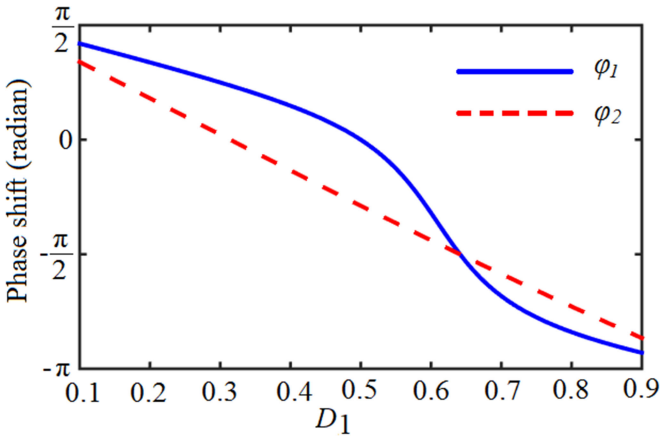

Fig. 3. φ_1 and φ_2 as a function of D_1.

In the class-E$_M$ amplifier, both the ZCS and ZCDS conditions are achieved at switch turn-off instant. These conditions are expressed as follows:

$$i_{s1}\left(2\pi\right) = 0 \tag{15}$$

$$\left.\frac{di_{s1}}{d\theta}\right|_{\theta=2\pi} = 0. \tag{16}$$

These switching conditions are obtained because the biharmonic current is injected from the auxiliary circuit. By KCL at the drain of the MOSFET in the main circuit for $2\pi D_1 \leq \theta \leq 2\pi$

$$i_{S1} = i_2 - i_{\text{}} + I_{\text{DD1}}, \quad 2\pi D_1 \leq \theta \leq 2\pi. \tag{17}$$

Substituting (7) into (17), the following equations are obtained:

$$i_{S1} = I_{\text{DD1}} + I_{m2}\sin\left(2\theta+\varphi_2\right) - I_{m1}\sin\left(\theta+\varphi_1\right) \tag{18}$$

$$\frac{di_{S1}}{d\theta} = 2I_{m2}\cos\left(2\theta+\varphi_2\right) - I_{m1}\cos\left(\theta+\varphi_1\right). \tag{19}$$

From (15) to (19), we get

$$I_{\text{DD1}} + I_{m2}\sin\left(\varphi_2\right) - I_{m1}\sin\left(\varphi_1\right) = 0 \tag{20}$$

$$2I_{m2}\cos\left(\varphi_2\right) - I_{m1}\cos\left(\varphi_1\right) = 0. \tag{21}$$

Solving numerically (13), (14), (20), and (21), φ_1 and φ_2 are computed according to D_1. Fig. 3 shows variations of φ_1 and φ_2 versus D_1. When D_1 increases, φ_1 and φ_2 decrease. In other words, when D_1 increases to create the required output phase shift, L_x and $L_{x'}$ should be increased.

Equation (10) does not have an analytical solution, but it can be solved numerically. Fig. 4(a), (b), and (c) shows variations of V_{S1} versus I_{DD1} and θ for IRF510 with $D_1 = 0.4$, 0.5, and 0.6, respectively. To obtain a high output power, the value of the dc input current must be increased. This increment leads to increase in peak switch voltage, as shown in Fig. 4. The average value of V_{S1} represents the dc input voltage. Fig. 4(a), (b) and (c) shows that when D_1 increases, more dc input voltage is needed to have the same input dc current, output current, and consequently output power.

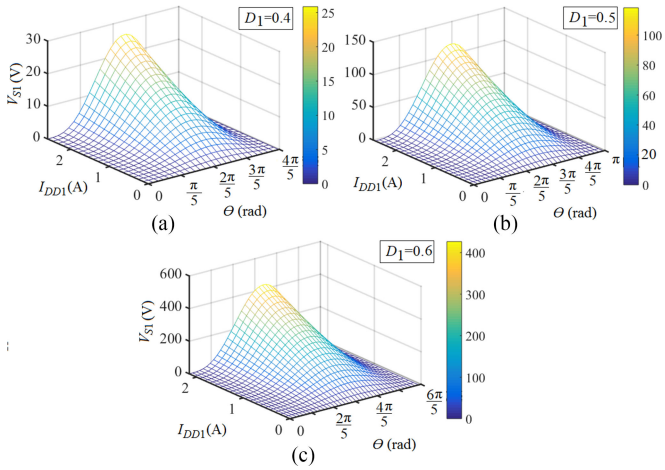

Fig. 4. Variations of V_{S1} versus I_{DD1} and θ for IRF510 for (a) $D_1 = 0.4$, (b) $D_1 = 0.5$, and (c) $D_1 = 0.6$.

Voltage V_{DD1} is the average value of V_{S1}

$$V_{\text{DD1}} = \frac{1}{2\pi}\int_0^{2\pi} V_{S1}(\theta)d\theta. \tag{22}$$

Since V_{S1} is equal to zero from $2\pi D_1$ to 2π, (22) is rewritten as

$$V_{\text{DD1}} = \frac{1}{2\pi}\int_0^{2\pi D_1} V_{S1}(\theta)d\theta. \tag{23}$$

By integrating (10)

$$\begin{aligned}&\frac{\omega C_{j01}V_{\text{bi1}}}{2\pi\left(1-m_1\right)}\int_0^{2\pi D_1}\left(1+\frac{V_{S1}}{V_{\text{bi1}}}\right)^{1-m_1}d\theta\\ &+\frac{\omega C_{j02}V_{\text{bi2}}}{2\pi\left(1-m_2\right)}\int_0^{2\pi D_1}\left(1+\frac{V_{S1}}{V_{\text{bi2}}}\right)^{1-m_2}d\theta\\ &+\omega C_{\text{fix1}}V_{\text{DD1}} - \frac{1}{2\pi}\int_0^{2\pi D_1} T(\theta) = 0\end{aligned} \tag{24}$$

where

$$\begin{aligned}T(\theta) = &\left[-\frac{I_{m1}\cos\left(\varphi_1\right)}{2\cos\left(\varphi_2\right)}\sin\left(\varphi_2\right) + I_{m1}\sin\left(\varphi_1\right)\right]\theta\\ &+ I_{m1}\left[\cos\left(\theta+\varphi_1\right) - \cos\left(\varphi_1\right)\right]\\ &- 0.5\frac{I_{m1}\cos\left(\varphi_1\right)}{2\cos\left(\varphi_2\right)}\left[\cos\left(2\theta+\varphi_2\right) - \cos\left(\varphi_2\right)\right]\\ &+ \frac{\omega C_{j01}V_{\text{bi1}}}{1-m_1} + \frac{\omega C_{j02}V_{\text{bi2}}}{1-m_2}.\end{aligned} \tag{25}$$

The integral in (24) does not have an analytical solution, but it can be solved numerically. Fig. 5(a) shows theoretical amplitude of I_{m1} versus V_{DD1} for IRFZ24N and IRF510 MOSFETs with linear and nonlinear capacitances at $D_1 = 0.5$. It is shown that if nonlinear capacitances are included in the design, the amplitude of the output current is decreased. This effect can change the class-E$_M$ PA performance; for instance, it can decrease the output power. Fig. 5(b) shows variations of I_{m1} versus V_{DD1} for IRFZ24N MOSFET with nonlinear capacitances and different values of D_1. When D_1 increases, I_{m1} decreases for a constant

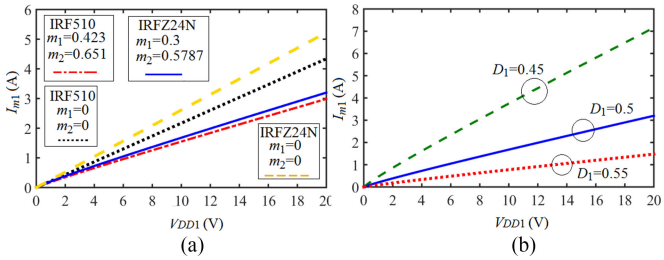

Fig. 5. (a) Theoretical amplitude of I_{m1} versus V_{DD1} for IRFZ24N and IRF510 MOSFETs with linear and nonlinear capacitances and $D_1 = 0.5$. (b) Variations of I_{m1} versus V_{DD1} for IRFZ24N MOSFET with nonlinear capacitances and different values of D_1.

V_{DD1}, as shown in Fig. 5(b). It reduces the conversion of dc to ac power. In addition, Fig. 5(b) shows that when D_1 increases, V_{DD1} should be increased to have constant I_{m1}.

The auxiliary circuit satisfies the ZVS condition at switch turn-on instant

$$V_{S2}(2\pi D_2) = 0. \tag{26}$$

For the auxiliary circuit in $0 \le \theta \le 2\pi D_2$

$$i_{CS2} = I_{\mathrm{DD2}} - i_2 - i_{C\mathrm{gd2}}. \tag{27}$$

Substituting (1) and (7) into (27)

$$\frac{dV_{S2}}{d\theta} = \frac{I_{\mathrm{DD2}} - I_{m2}\sin(2\theta+\varphi_2)}{\omega\left(C_{S2}+C_{\mathrm{gd2}}\right)}. \tag{28}$$

Substituting (2) and (3) into (28) and after integration, the obtained equation is

$$\frac{\omega C_{j01}V_{\mathrm{bi1}}}{1-m_1}\left[\left(1+\frac{V_{S2}}{V_{\mathrm{bi1}}}\right)^{1-m_1}-1\right] + \frac{\omega C_{j02}V_{\mathrm{bi2}}}{1-m_2}\left[\left(1+\frac{V_{S2}}{V_{\mathrm{bi2}}}\right)^{1-m_2}-1\right] + \omega C_{\mathrm{fix2}}V_{S2} = I_{\mathrm{DD2}}\theta + 0.5I_{m2}\left(\cos(2\theta+\varphi_2)-\cos(\varphi_2)\right). \tag{29}$$

From (26) and (29), the following equation is obtained:

$$I_{\mathrm{DD2}}2\pi D_2 + 0.5I_{m2}\left[\cos(4\pi D_2+\varphi_2)-\cos(\varphi_2)\right] = 0. \tag{30}$$

In this design, $V_{\mathrm{DD1}} = 11.5\,\mathrm{V}$ and $D_2 = D_1/2$ is selected. Solving (24) and (25), I_{m1} as a function of D_1 can be obtained. I_{m2} can be obtained from (21). From (20) and (21), I_{DD1} is obtained as follows:

$$I_{\mathrm{DD1}} = I_{m1}\left[\sin(\varphi_1) - 0.5\cos(\varphi_1)\tan(\varphi_2)\right]. \tag{31}$$

From (30) and (21), $I_{\mathrm{DD}}2$ is calculated as follows:

$$I_{\mathrm{DD2}} = -\frac{I_{m1}\cos(\varphi_1)}{8\pi D_2\cos(\varphi_2)}\left[\cos(4\pi D_2+\varphi_2)-\cos(\varphi_2)\right]. \tag{32}$$

Fig. 6(a), (b), (c), and (d) shows variations of I_{m1}, I_{m2}, I_{DD1}, and I_{DD2} as a function of D_1 for IRFZ24N and IRF510 MOSFETs with linear and nonlinear capacitances, respectively. It is shown that I_{m1}, I_{m2}, I_{DD1}, and I_{DD2} decrease when D_1 increases. The

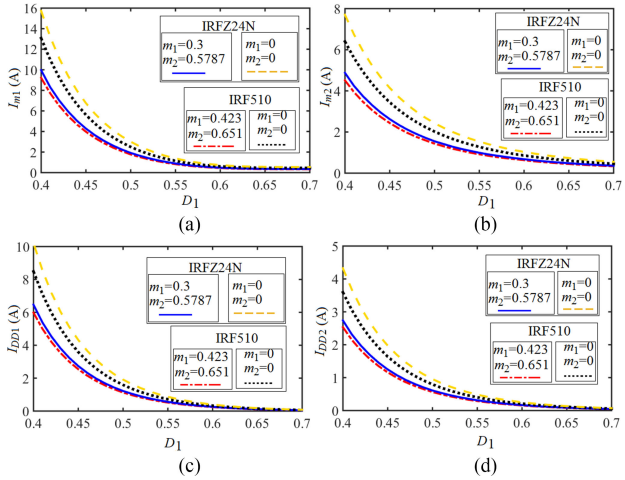

Fig. 6. Variations of (a) I_{m1}, (b) I_{m2}, (c) I_{DD1}, and (d) I_{DD2} versus D_1 for IRFZ24N and IRF510 MOSFETs with linear and nonlinear parasitic capacitances in V_{DD1} equal to 11.5 V.

nonlinear capacitances decrease I_{m1}, I_{m2}, I_{DD1}, and I_{DD2}, as shown in Fig. 6. They have a lower value with IRF510 MOSFET in comparison with IRFZ24N MOSFET. Fig. 6(c) and (d) shows that as D_1 increases, the input dc power in the main and auxiliary circuit decreases. This is because of on-state time of both main and auxiliary MOSFETs decrease when D_1 and D_2 increase.

From (10) and (18), the waveforms of the switch voltage and current of the main and auxiliary circuit for IRF510 with nonlinear capacitances and different values of D_1 are obtained, as shown in Fig. 7(a)–(d). It can be seen when D_1 decreases, the switch peak voltage and current are increased. In all of duty ratios, ZVS, ZVDS, ZCS, and ZCDS conditions are achieved, as shown in Fig. 7. The variations of V_{DD2} as a function of D_1 for IRF510 and IRFZ24N MOSFETs with linear and nonlinear capacitances are shown in Fig. 7(e). V_{DD2} decreases as D_1 increases. Fig. 7(e) shows, to achieve class-$\mathrm{E_M}$ switching nominal conditions, more V_{DD2} is needed for IRF510. If nonlinear capacitances are included in the design, more V_{DD2} should be applied to the auxiliary circuit, as shown in Fig. 7(e).

Fig. 8 shows the waveforms of V_{S1} and V_{S2} with constant I_{m1} and V_{DD1} for IRF510 and IRFZ24N MOSFET with linear and nonlinear capacitances. Fig. 8(a) shows to have the same output current V_{S1} and V_{S2} have more values in IRF510 in comparison with IRFZ24N. If nonlinear capacitances are not included in the design, V_{S1} and V_{S2} have lower values, so they should be included in the design process. Fig. 8(b) shows that the maximum switch voltage for IRFZ24N has more value in comparison with IRF510 at constant V_{DD1}. Similar to constant I_{m1} designs in constant V_{DD1}, V_{S1} and V_{S2} have lower values when nonlinear capacitances are not included.

Fig. 9(a) shows the equivalent circuit of the presented class-$\mathrm{E_M}$ PA in the first and second harmonics. The fundamental frequency of V_{S1} is as follows:

$$V_{S1f1}(\theta) = V_{1f1}\sin(\theta+\varphi_{V_{S1f1}}) \tag{33}$$

where V_{1f1} is the amplitude of the main circuit switch voltage fundamental component and $\varphi_{V_{S1f1}}$ is the phase shift of the

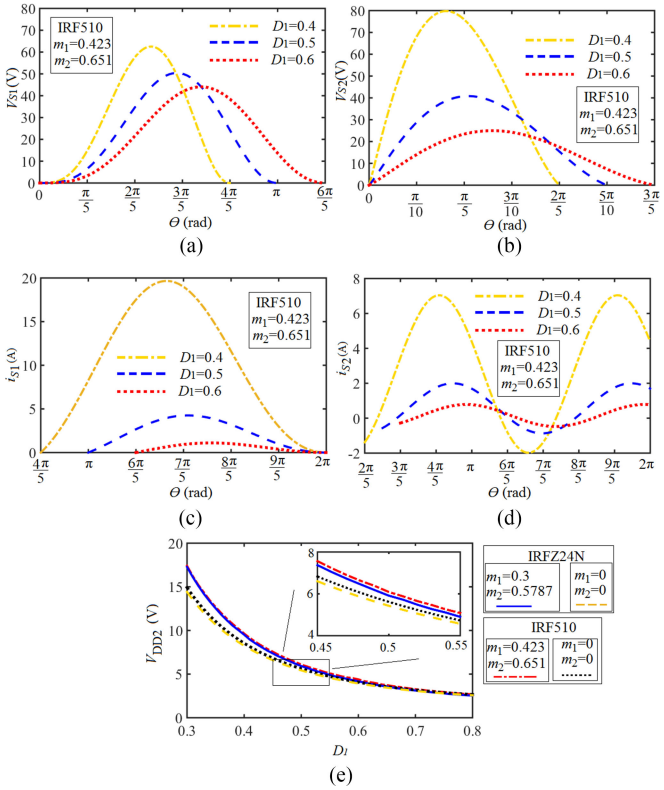

Fig. 7. Waveforms of (a) V_{S1}, (b) i_{S1}, (c) V_{S2}, (d) i_{S2} for IRF510 MOSFET with nonlinear capacitances and different values of D_1 in V_{DD1} equal to 11.5 V, and (e) variations of V_{DD2} as a function of D_1 for IRF510 and IRFZ24N MOSFETs with linear and nonlinear capacitances.

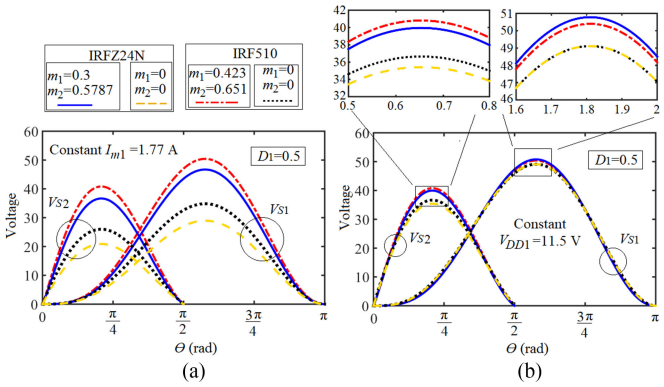

Fig. 8. Waveforms of V_{S1} and V_{S2} with (a) constant I_{m1} and (b) constant V_{DD1} for IRF510 and IRFZ24N MOSFET with linear and nonlinear capacitances.

fundamental component of the main circuit switch voltage with respect to the input voltage. At the fundamental frequency, the impedance of the series resonant circuit in the main circuit is equal to zero, so the switch voltage at this state V_{1f1} is the sum of the voltage across L_x and the output voltage, as shown in Fig. 9(a). Therefore

$$V_{S1f1}(\theta) = RL_{m1}\sin(\theta+\varphi_1) + V_{Lx}(\theta) = V_{1f1}\sin(\theta+\varphi_{V_{S1f1}}) \tag{34}$$

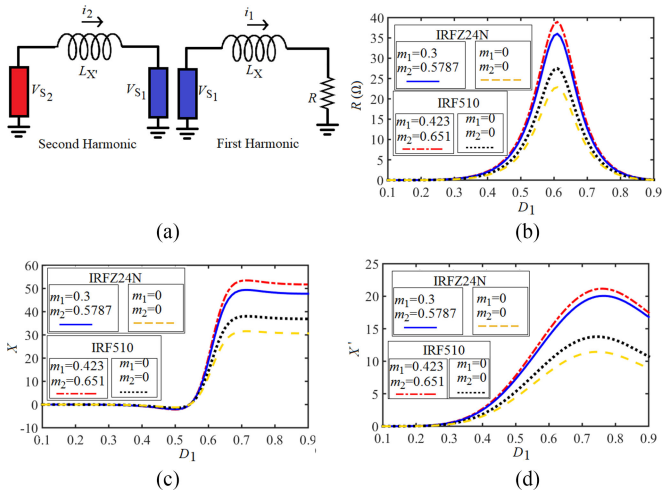

Fig. 9. (a) Equivalent circuit of the presented class-E$_M$ PA in the first and second harmonics. (b) R. (c) X. (d) X' as a function of D_1 for linear and nonlinear capacitances.

where V_{Lx} is the fundamental component of the voltage across L_x, which is as follows:

$$V_{Lx}(\theta) = X\frac{di_1}{dt} = XI_{m1}\cos(\theta+\varphi_1) \tag{35}$$

where X is the inductive reactance of L_x. V_1 and φ_{Vs} can be determined as

$$V_{1f1} = I_{m1}\sqrt{X^2+R^2}, \tag{36}$$

$$\varphi_{V_{S1f1}} = \varphi_1 + \tan^{-1}\left(\frac{X}{R}\right). \tag{37}$$

R and X are obtained from (36) and (37) as follows:

$$R = \sqrt{\frac{{V_{1f1}}^2}{I_{m1}^2(1+\tan^2(\varphi_{V_{S1f1}}-\varphi_1))}} \tag{38}$$

$$X = \sqrt{\frac{{V_{1f1}}^2\tan^2(\varphi_{V_{S1f1}}-\varphi_1)}{I_{m1}^2(1+\tan^2(\varphi_{V_{S1f1}}-\varphi_1))}}. \tag{39}$$

Fig. 9(b) and (c) shows R and X as functions of D_1 for IRFZ24N and IRF510 MOSFETs with linear and nonlinear capacitances. It is seen that R increases from D_1 equal to 0.1–0.61 and decreases from D_1 equal to 0.61–0.9. In addition, X increases as D_1 increases.

By KVL in a second harmonic equivalent circuit

$$-V_{S2f2} + V_{Lx'} + V_{S1f2} = 0 \tag{40}$$

where V_{S2f2} and V_{S1f2} are the second harmonic component of V_{S1} and V_{S2}, respectively. $V_{Lx'}$ is the second harmonic component of the voltage across $L_{x'}$, which is given as follows:

$$V_{S1f2}(\theta) = V_{1f2}\sin(2\theta+\varphi_{V_{S1f2}}) \tag{41}$$

$$V_{S2f2}(\theta) = V_{2f2}\sin(2\theta+\varphi_{V_{S2f2}}) \tag{42}$$

$$V_{Lx'}(\theta) = X'\frac{di_2}{dt} = 2X'I_{m2}\cos(2\theta+\varphi_2) \tag{43}$$

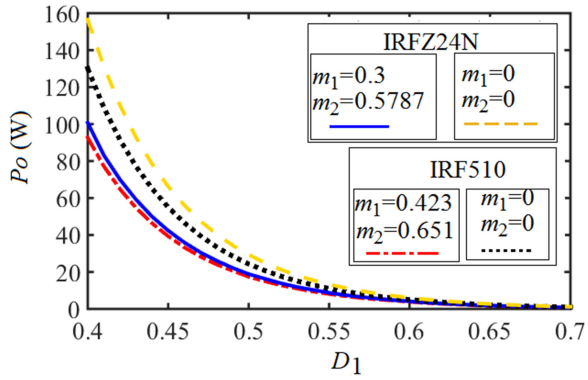

Fig. 10. Output power as a function of D_1 at $V_{\mathrm{DD1}} = 11.5$ V for IRFZ24N and IRF510 MOSFETs with nonlinear and linear parasitic capacitances.

where V_{1f2} and V_{2f2} are the amplitude and $\varphi_{V_{S1f2}}$ and $\varphi_{V_{S2f2}}$ are the phase shift of the second harmonic component of the main and auxiliary circuit switch voltage, respectively. By substituting (41)–(43) into (40)

$$V_{2f2}\sin\left(2\theta+\varphi_{V_{S2f2}}\right)=V_{1f2}\sin\left(2\theta+\varphi_{V_{S1f2}}\right)+2X'I_{m2}\cos\left(2\theta+\varphi_2\right). \quad (44)$$

By solving (44)

$$\varphi_{V_{S2f2}}=\tan^{-1}\left(\frac{\alpha}{\beta}\right) \quad (45)$$

where

$$\alpha=2X'I_{m2}\cos\left(\varphi_2\right)+V_{1f2}\sin\left(\varphi_{V_{S1f2}}\right) \quad (46)$$

$$\beta=-2X'I_{m2}\sin\left(\varphi_2\right)+V_{1f2}\cos\left(\varphi_{V_{S1f2}}\right). \quad (47)$$

By solving (45), X' can be obtained. Fig. 9(d) shows X' as functions of D_1 for IRFZ24N and IRF510 MOSFETs with linear and nonlinear capacitances. It is seen that X' increases from D_1 equal to 0.1–0.75 and decreases from D_1 equal to 0.75–0.9.

Fig. 10 shows output power as a function of D_1 at $V_{\mathrm{DD1}} = 11.5$ V for IRFZ24N and IRF510 with nonlinear and linear C_{gd1} and C_{ds1} capacitances, respectively. It is seen that the output power decreases as the duty ratio increases. Fig. 10 shows that if nonlinear capacitances are included in the design, the output power is decreased. So to design a class-$\mathrm{E_M}$ PA, considering MOSFET nonlinear gate-to-drain and drain-to-source capacitances is very important.

The output power capability is

$$C_p=\frac{P}{V_{S1\max}i_{S1\max}+V_{S2\max}i_{S2\max}} \quad (48)$$

where P is the output power with nominal switching conditions. $V_{S1\max}$, $i_{S1\max}$, $V_{S2\max}$, and $i_{S2\max}$ are the maximum switch voltage and current of the main and auxiliary circuits. From (48)

$$C_p=\frac{V_{\mathrm{DD1}}I_{\mathrm{DD1}}+V_{\mathrm{DD2}}I_{\mathrm{DD2}}}{V_{S1\max}i_{S1\max}+V_{S2\max}i_{S2\max}}. \quad (49)$$

$V_{S1\max}$, $V_{S2\max}$, $i_{S1\max}$, and $i_{S2\max}$ as a function of D_1 at constant $V_{\mathrm{DD1}} = 11.5$ V are shown in Fig. 11(a), (b), (c), and (d). It is seen, they are reduced as D_1 increases. To use MOSFETs

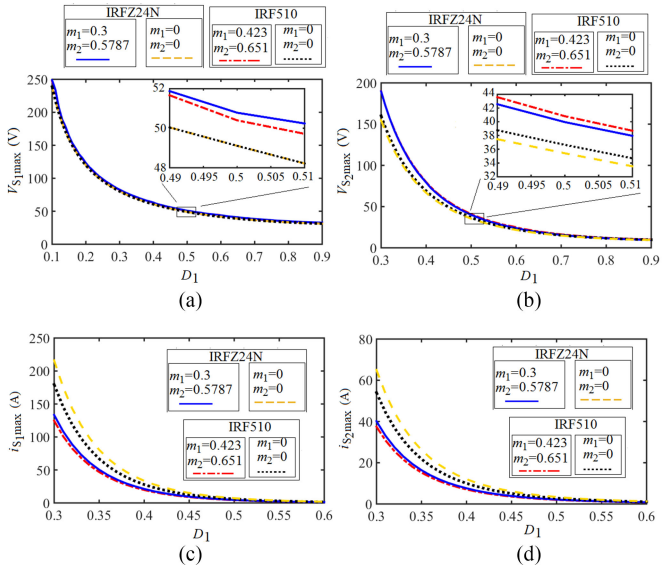

Fig. 11. (a) $V_{S1\max}$, (b) $V_{S2\max}$, (c) $i_{S1\max}$, and (d) $i_{S2\max}$ as a function of D_1 at constant $V_{\mathrm{DD1}} = 11.5$ V.

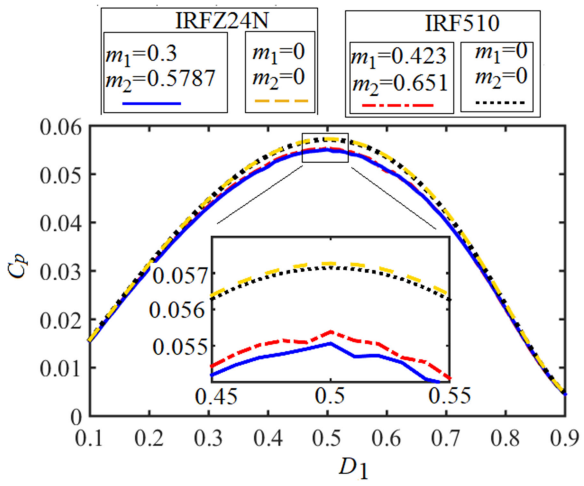

Fig. 12. C_P as a function of D_1 at constant $V_{\mathrm{DD1}} = 11.5$ V.

with lower drain voltage tolerances, it is best to choose a larger duty ratio. If nonlinear capacitances are not included in the design process, lower $V_{S1\max}$ and $V_{S2\max}$ and higher $i_{S1\max}$ and $i_{S2\max}$ are obtained.

Fig. 12 shows C_P as a function of D_1. It is seen that C_P has the highest value at $D_1 = 0.5$ for both IRF510 and IRFZ24N MOSFETs. It can be understood from Fig. 12 that the class-$\mathrm{E_M}$ PA with IRF510 has higher output power capability with constant V_{DD1} in comparison with the class-$\mathrm{E_M}$ PA with IRFZ24N MOSFET.

The power efficiency can be written as (50) which is shown at the bottom of the next page, where $P_{L_{C1}}$ and $P_{L_{C2}}$ are power losses of dc feed inductances L_{C1} and L_{C2}, respectively. $P_{r_{\mathrm{DS1}}}$ and $P_{r_{\mathrm{DS2}}}$ are power losses in on-resistance of main and auxiliary MOSFETs, respectively. $P_{\mathrm{resonance1}}$ and $P_{\mathrm{resonance2}}$ are power losses in main and auxiliary series resonant circuits. They

are calculated as follows:

$$P_{L_{C1}} = \frac{1}{2\pi}\int_0^{2\pi} r_{L_{C1}} I_{\mathrm{DD1}}^2 d\theta = r_{L_{C1}} I_{\mathrm{DD1}}^2 = r_{L_{C1}} I_{m1}^2 [\sin(\varphi_1) - 0.5\cos(\varphi_1)\tan(\varphi_2)]^2 \quad (51)$$

$$P_{L_{C2}} = \frac{1}{2\pi}\int_0^{2\pi} r_{L_{C2}} I_{\mathrm{DD2}}^2 d\theta = r_{L_{C2}} I_{\mathrm{DD2}}^2 = r_{L_{C2}} I_{m1}^2 \times \left[\frac{0.5\cos(\varphi_1)(\cos(4\pi D_2 + \varphi_2) - \cos(\varphi_2))}{4\pi D_2 \cos(\varphi_2)}\right]^2 \quad (52)$$

$$P_{r_{\mathrm{DS1}}} = \frac{1}{2\pi}\int_0^{2\pi} r_{\mathrm{DS1}} i_{S1}^2 d\theta = \frac{1}{2\pi}\int_{2\pi D1}^{2\pi} r_{\mathrm{DS1}} [I_{\mathrm{DD1}} + I_{m2}\sin(2\theta + \varphi_2) - I_{m1}\sin(\theta + \varphi_1)]^2 d\theta \quad (53)$$

$$P_{r_{\mathrm{DS2}}} = \frac{1}{2\pi}\int_0^{2\pi} r_{\mathrm{DS2}} i_{S2}^2 d\theta = \frac{1}{2\pi}\int_{2\pi D2}^{2\pi} \times r_{\mathrm{DS2}} [I_{\mathrm{DD2}} - I_{m2}\sin(2\theta + \varphi_2)]^2 d\theta \quad (54)$$

$$P_{\mathrm{resonance1}} = \frac{1}{2\pi}\int_0^{2\pi} r_{\mathrm{resonance1}} i_1^2 d\theta = 0.5 r_{\mathrm{resonance1}} I_{m1}^2 \quad (55)$$

$$P_{\mathrm{resonance2}} = \frac{1}{2\pi}\int_0^{2\pi} r_{\mathrm{resonance2}} i_2^2 d\theta = 0.5 r_{\mathrm{resonance2}}$$

$$I_{m2}^2 = 0.5 r_{\mathrm{resonance2}} I_{m1}^2 \left(\frac{\cos(\varphi_1)}{2\cos(\varphi_2)}\right)^2 \quad (56)$$

where the position of $r_{\mathrm{resonance\ 1}}$, $r_{\mathrm{resonance\ 2}}$, r_{Lc1}, r_{Lc2}, r_{DS1}, and r_{DS2} is shown in Fig. 13. In (50), the MOSFETs' OFF-state conduction and gate losses are ignored.

In the presented analysis, it is assumed that MOSFETs work as a switch, which means they have zero resistance in the on state. Fig. 14 shows the power efficiency as a function of D_1 for IRF510 and IRFZ24N MOSFETs with linear and nonlinear C_{gd1} and C_{gd2} capacitances, which are calculated with MATLAB. It is seen that the efficiency with nonlinear capacitances has higher value in both MOSFETs. Class-E$_M$ PA with IRF510 has higher efficiency in comparison with IRFZ24N at constant V_{DD1}, as shown in Fig. 14. The output power decreases as D_1 increases, as shown in Fig. 9. Fig. 14 shows that the efficiency increases when D_1 increases from 0.1 to 0.7 and decreases when D_1 increases from 0.7 to 0.9.

When the current ripple ratio is less than 0.1, the dc feed inductances L_{C1} and L_{C2} are given as [1]

$$L_{C1} = 2\left(\frac{\pi^2}{4} + 1\right)\frac{R}{f} \quad (57)$$

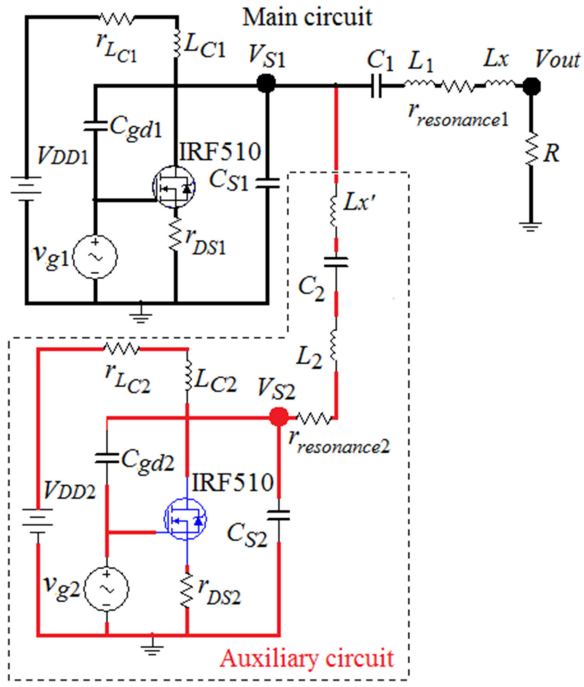

Fig. 13. Position of $r_{\mathrm{resonance\ 1}}$, $r_{\mathrm{resonance\ 2}}$, r_{Lc1}, r_{Lc2}, r_{DS1}, and r_{DS2} in the class-E$_M$ power amplifier.

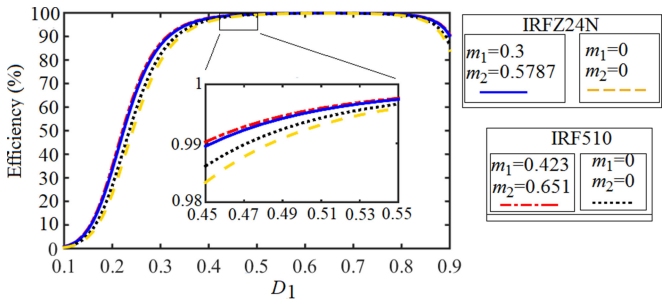

Fig. 14. Efficiency as a function of D_1 for IRF510 and IRFZ24N MOSFETs with linear and nonlinear parasitic capacitances.

$$L_{C2} = \left(\frac{\pi^2}{4} + 1\right)\frac{r_{\mathrm{DS1}}}{f}. \quad (58)$$

where r_{DS1} is the drain-to-source on-state resistance of the MOSFET. L_1 and C_1 of the series filter in the main circuit and L_2 and C_2 in the auxiliary circuit are calculated as follows:

$$f = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (59)$$

$$2f = \frac{1}{2\pi\sqrt{L_2 C_2}}. \quad (60)$$

Therefore, all elements of the class-E$_M$ amplifier can be obtained when D_1, D_2, f, and V_{DD1} are specified and the MOSFET is selected.

$$\eta = \frac{0.5RI_{m1}^2}{0.5RI_{m1}^2 + P_{L_{C1}} + P_{L_{C2}} + P_{r_{\mathrm{DS1}}} + P_{r_{\mathrm{DS2}}} + P_{\mathrm{resonance1}} + P_{\mathrm{resonance2}}} \quad (50)$$

TABLE II
SPECIFICATIONS OF THE PROPOSED DESIGNS

MOSFET	IRF510			IRFZ24N		
Duty ratio	$D_1 = 0.5$			$D_1 = 0.5$		
	Theoretical	Simulated	Measured	Theoretical	Simulated	Measured
D_2	0.25	0.25	0.25	0.25	0.25	0.25
I_{DD1} (A)	1.13	1.13	1.12	1.22	1.29	1.3
I_{DD2} (A)	0.56	0.62	0.6	0.61	0.62	0.63
I_{m1} (A)	1.77	1.63	1.61	1.91	1.86	1.86
I_{m2} (A)	1.43	1.26	1.25	1.55	1.41	1.48
P_{out} (W)	17.42	14.8	14.41	18.8	17.82	17.82
P_{DC1} (W)	13	13	12.88	14	14.83	14.9
P_{DC2} (W)	3.4	3.78	3.66	3.66	3.66	3.72
η from (50)	99.6%	–	–	99.6%	–	–
η	100%	88.2%	87.1%	100%	96.4%	95.7%

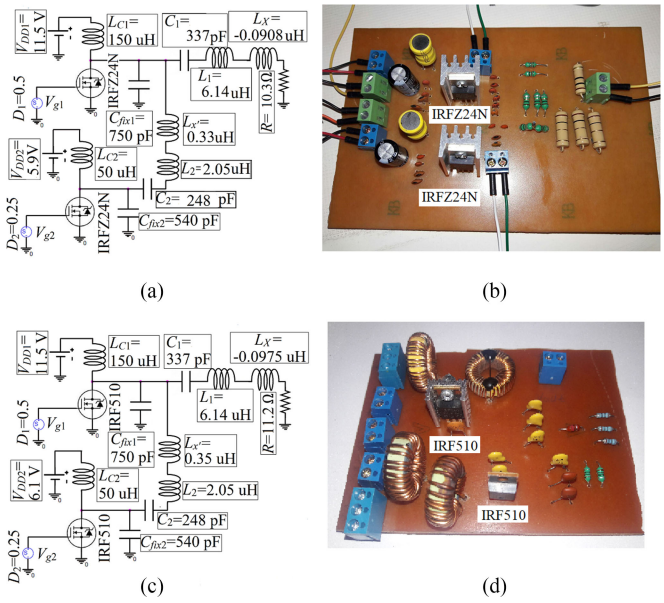

Fig. 15. (a) Circuit and (b) photograph of the class-E_M PA with IRFZ24N at $D_1 = 0.5$. (c) Circuit and (d) photograph of the class-E_M PA with IRF510 at $D_1 = 0.5$.

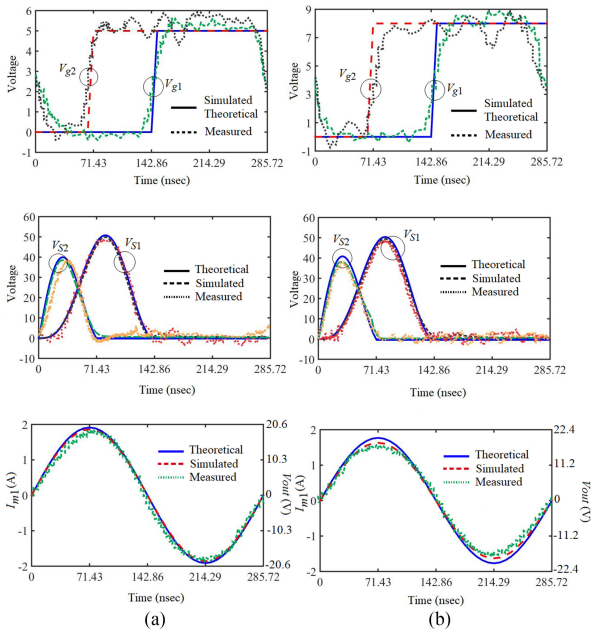

Fig. 16. Waveforms of the design examples, considering nonlinear drain-to-source and nonlinear gate-to-drain capacitances. (a) The theoretical expressions, PSpice simulations, and experimental results for IRFZ24N at $D_1 = 0.5$. (b) The theoretical expressions, PSpice simulations, and experimental results for IRF510 MOSFET at $D_1 = 0.5$.

IV. SIMULATION AND MEASUREMENT RESULTS

To validate the presented analysis, simulation and experimental results are presented in this section.

1) Since theoretical analysis shows that the power output capability has the maximum value at $D_1 = 0.5$, two class-E_M PAs with IRF510 and IRFZ24N at $D_1 = 0.5$ are designed, simulated, and fabricated and their specifications are compared.
2) To confirm the analysis of the class-E_M PA design at any duty ratio and the duty ratio effects on the amplifier performance, three class-E_M PAs with IRF510 at $D_1 = 0.5$, 0.6, and 0.7 are fabricated and measured. The results are compared with simulated and theoretical results.
3) To show the effects of the MOSFET nonlinear capacitances, two class-E_M PAs with IRFZ24N at $D_1 = 0.5$ with and without considering MOSFET nonlinear capacitances are designed, simulated, and fabricated. Then simulated and measured responses are compared with theoretical results.

A. Designing Class-E_M PAs With IRF510 and IRFZ24N at $D_1 = 0.5$ and Comparison Their Specifications

To validate the presented analysis and compare specifications of class-E_M PAs with IRF510 and IRFZ24N, two class-E_M PAs with IRF510 and IRFZ24N at $D_1 = 0.5$ were designed, simulated, and fabricated. The fundamental frequency of the proposed class-E_M PAs was 3.5 MHz. The circuit and photograph of the fabricated class-E_M amplifiers are shown in Fig. 15. The parameters for the proposed circuits are listed in Table II.

DC voltage for the main circuit was 11.5 V for both presented circuits. The loaded resistance was calculated using (38), which was equal to 10.3 and 11.2 Ω for IRFZ24N and IRF510, respectively. L_x and $L_{x'}$ for IRFZ24N were calculated from (39) and (45), respectively, which are equal to –0.0908 and 0.33 μH. They are equal to –0.0975 and 0.35 μH for IRF510. Negative value

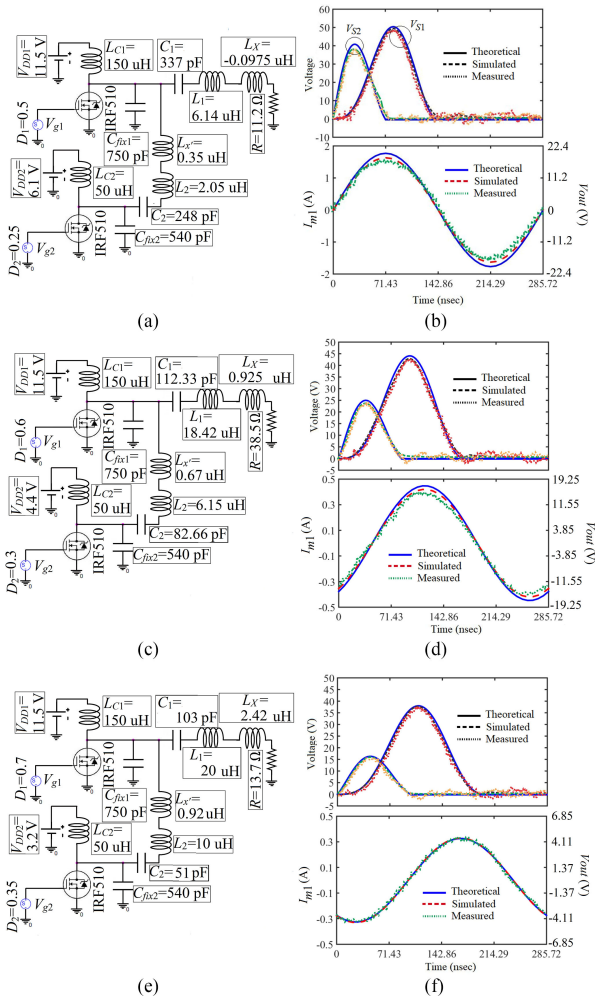

Fig. 17. (a) Circuit and (b) theoretical expressions, PSpice simulations, and experimental results for IRF510 at $D_1 = 0.5$. (c) Circuit and (d) theoretical expressions, PSpice simulations, and experimental results for IRF510 at $D_1 = 0.6$. (e) Circuit and (f) theoretical expressions, PSpice simulations, and experimental results for IRF510 at $D_1 = 0.7$.

for L_x means that the series inductive L_1 should be reduced by L_x in order to obtain ZVS and ZVDS nominal conditions. The series resonance elements for the main circuit and the auxiliary circuit were obtained using (6), (59), and (60). The dc feed inductances L_{C1} and L_{C2} were calculated using (57) and (58), respectively. The values of MOSFET on-resistance were obtained from the PSpice models, which are 0.54 Ω for IRF510 MOSFET and 0.07 Ω for IRFZ24N MOSFET. The applied gate-to-source voltage is a square wave with the amplitude of 8 and 5 V for IRF510 and IRFZ24N MOSFETs, respectively.

The theoretical, simulated, and measured efficiencies of the designed class-E_M amplifier with IRF510 MOSFET at $D_1 = 0.5$ were 99.6%, 88.2%, and 87.1%, respectively. Also, their output powers were 17.42, 14.8, and 14.41 W, respectively, whereas these values for the designed class-E_M amplifier with IRFZ24N MOSFET at $D_1 = 0.5$ were 99.6%, 96.4%, and 95.7%, respectively. Their output powers were 18.8, 17.82, and 17.82 W. The theoretical results were in good agreement with measured and simulated results, as shown in Table II. Fig. 16(a) shows

TABLE III
SPECIFICATIONS OF THE PRESENTED CLASS-E_M PAS WITH IRF510 AT $D_1 = 0.5$, 0.6, AND 0.7

Parameters	Duty ratio	Theoretical	Simulated	Measured
D_2	$D_1 = 0.5$	0.25	0.25	0.25
	$D_1 = 0.6$	0.3	0.3	0.3
	$D_1 = 0.7$	0.35	0.35	0.35
I_{DD1} (A)	$D_1 = 0.5$	1.13	1.13	1.12
	$D_1 = 0.6$	0.24	0.25	0.24
	$D_1 = 0.7$	0.05	0.053	0.054
I_{DD2} (A)	$D_1 = 0.5$	0.56	0.62	0.6
	$D_1 = 0.6$	0.15	0.16	0.16
	$D_1 = 0.7$	0.04	0.041	0.042
I_{m1} (A)	$D_1 = 0.5$	1.77	1.63	1.61
	$D_1 = 0.6$	0.45	0.43	0.42
	$D_1 = 0.7$	0.326	0.33	0.33
I_{m2} (A)	$D_1 = 0.5$	1.43	1.26	1.25
	$D_1 = 0.6$	0.63	0.6	0.58
	$D_1 = 0.7$	0.332	0.36	0.33
P_{out} (W)	$D_1 = 0.5$	17.42	14.8	14.41
	$D_1 = 0.6$	3.9	3.56	3.4
	$D_1 = 0.7$	0.73	0.746	0.746
P_{DC1} (W)	$D_1 = 0.5$	13	13	12.88
	$D_1 = 0.6$	2.7	2.9	2.8
	$D_1 = 0.7$	0.57	0.61	0.621
P_{DC2} (W)	$D_1 = 0.5$	3.4	3.78	3.66
	$D_1 = 0.6$	0.66	0.7	0.7
	$D_1 = 0.7$	0.13	0.13	0.13
η from (50)	$D_1 = 0.5$	99.6%	–	–
	$D_1 = 0.6$	100%	–	–
	$D_1 = 0.7$	100%	–	–
η	$D_1 = 0.5$	100%	88.2%	87.1%
	$D_1 = 0.6$	100%	98.8%	97.1%
	$D_1 = 0.7$	100%	100%	99.3%

TABLE IV
COMPARISON BETWEEN THE PRESENTED CIRCUITS WITH THE REFERENCES

Ref.	Class	MOSFET	r_{DS} (Ω)	D_1	P_O (W)	η (%)
[25]	Class-E_M	IRFZ24N	0.07	0.5	14	95.6
				0.5	14.2	95
[22]	Class-E_M	IRFZ24N	0.07	0.5	14.1	94.4
[21]	Class-E_M	IRFZ24N	0.07	0.5	13.23	89.6
The proposed circuits	Class-E_M	IRF510	0.54	0.5	14.41	87.1
				0.6	3.4	97.1
				0.7	0.746	99.3
		IRFZ24N	0.07	0.5	17.82	95.7

the obtained waveforms from theoretical expressions, PSpice simulations, and circuit experiments for the designed class-E_M amplifier with IRFZ24N MOSFET and $D_1 = 0.5$. The switch-voltage waveforms of the both PSpice simulations and circuit experiments satisfied the class-E ZVS/ZVDS conditions and agreed with the theoretical waveforms.

Fig. 16(b) shows the obtained waveforms from theoretical expressions, PSpice simulations, and circuit experiments for the designed class-E_M amplifier with IRF510 MOSFET at $D_1 = 0.5$. Simulation and theoretical results were done using PSpice and MATLAB, respectively. The theoretical results and

TABLE V
SPECIFICATIONS OF THE PRESENTED CIRCUITS WITH IRFZ24N AND WITH AND WITHOUT CONSIDERING NONLINEAR MOSFET CAPACITANCES

MOSFET	IRFZ24N			IRFZ24N		
Duty ratio	$D_1 = 0.5$			$D_1 = 0.5$		
MOSFET Capacitances	Assume capacitances are linear			Assume capacitances are nonlinear		
	Theoretical	Simulated	Measured	Theoretical	Simulated	Measured
D_2	0.25	0.25	0.25	0.25	0.25	0.25
I_{DD1} (A)	1.91	1.76	1.8	1.22	1.29	1.3
I_{DD2} (A)	0.95	0.64	0.7	0.61	0.62	0.63
I_{m1} (A)	3	2.5	2.4	1.91	1.86	1.86
I_{m2} (A)	2.43	1.11	0.9	1.55	1.41	1.48
P_{out} (W)	29.2	20.3	18.72	18.8	17.82	17.82
P_{DC1} (W)	21.96	20.24	20.7	14	14.83	14.9
P_{DC2} (W)	5.13	3.45	3.78	3.66	3.66	3.72
η from (50)	99.5%	–	–	99.6%	–	–
η	100%	85%	76.5%	100%	96.4%	95.7%

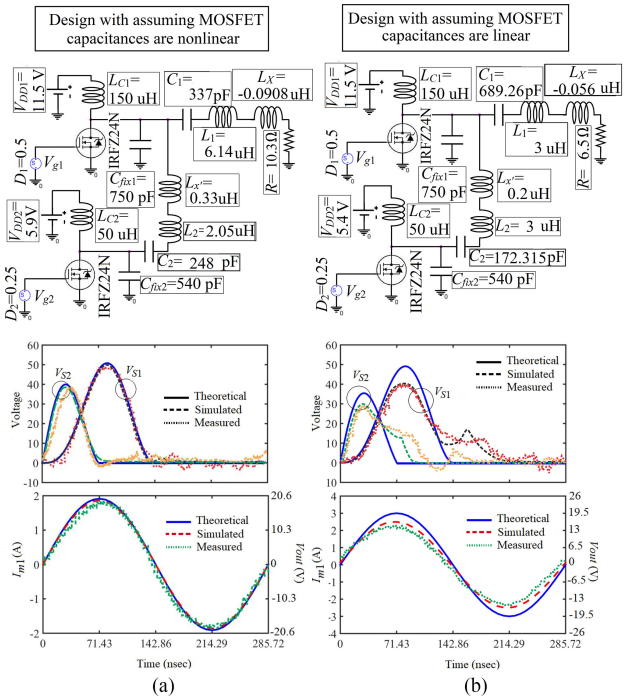

Fig. 18. (a) Circuit and theoretical expressions, PSpice simulations, and experimental results for IRFZ24N at $D_1 = 0.5$ considering nonlinear drain-to-source and nonlinear gate-to-drain capacitances. (b) Circuit and theoretical expressions, PSpice simulations, and experimental results for IRFZ24N at $D_1 = 0.5$ considering linear drain-to-source and linear gate-to-drain capacitances.

PSpice simulations agreed with experimental results. The efficiency for the presented class-E_M PA with IRFZ24N MOSFET was higher than the class-E_M PA with IRF510 MOSFET. This is because of lower on-resistance of IRFZ24N MOSFET, which is 0.07 Ω in comparison with on-resistance of IRF510 MOSFET, which is 0.54 Ω. The accuracy of the theoretical results for IRFZ24N was better because in the theoretical analysis it was assumed that MOSFETs operate like a switch. It means that they have zero resistance in the on-state, since the on-state resistance of IRFZ24N is closer to zero so the theoretical results are more accurate for the class-E_M PA with IRFZ24N. The output power for the class-E_M PA with IRFZ24N MOSFET was more than IRF510 MOSFET.

B. Class-E_M PA Design at Any Duty Ratio and Duty Ratio Effects

To validate the analysis, three class-E_M PAs with IRF510 at $D_1 = 0.5, 0.6$, and 0.7 were designed, simulated, and fabricated as examples. Fig. 17 shows their circuits with elements value and theoretical expressions, PSpice simulations, and experimental results of the design examples, considering nonlinear drain-to-source and nonlinear gate-to-drain capacitances. DC voltage for the main circuit was 11.5 V for all three presented circuits. The loaded resistances were calculated using (38), which were equal to 11.2, 38.5 Ω, and 13.7 Ω, respectively. L_x and $L_{x'}$ were calculated from (39) and (45), which were equal to –0.0975 and 0.35 μH for $D_1 = 0.5$, they were equal to 0.925 and 0.67 μH for $D_1 = 0.6$, and they were equal to 2.42 and 0.92 μH for $D_1 = 0.7$. The series resonance elements for the main circuit and the auxiliary circuit were obtained using (6), (59), and (60). The dc feed inductances L_{C1} and L_{C2} were calculated using (57) and (58), respectively. The applied gate-to-source voltage was a square wave with the amplitude of 8 V. Table III shows specifications for the design examples. The theoretical, simulated, and measured efficiencies, and output power of the designed class-E_M amplifiers with IRF510 MOSFET at $D_1 = 0.52$ were 99.6% with 17.42 W, 88.2% with 14.8 W, and 87.1% with 14.41 W, respectively, whereas these values were 100% with 3.9 W, 98.8% with 3.56 W, and 97.1% with 3.4 W for the designed class-E_M amplifier at $D_1 = 0.6$ and were 100% with 0.73 W, 100% with 0.748 W, and 99.3% with 0.746 W for the designed class-E_M amplifier at $D_1 = 0.7$. The theoretical results show that the efficiency is increased when D_1 increases from 0.1 to 0.7 and decreased when D_1 increases from 0.7 to 0.9, as shown in Fig. 14. The simulated and measured results confirm the theoretical results.

Table IV shows the comparison between the presented circuits with those given in references. The efficiency for the presented class-E_M PA with IRFZ24N MOSFET is higher than the class-E_M PA with IRF510 MOSFET. In overall, it is seen that the proposed

circuit has better efficiency and output power with respect to those in the references.

C. Effect of the Nonlinear Capacitances

To show the nonlinearity effects, two class-E_M PAs with IRFZ24N at the duty ratio equal to 0.5 with and without considering the MOSFET nonlinear capacitances were designed, as shown in Fig. 18. Also, theoretical, simulated, and measured results for the presented circuits are shown in Fig. 18. Their specifications are shown in Table V. It is seen in the theoretical results that both ZVS and ZVDS conditions were satisfied in both circuits, but in the simulated and measured results the switching conditions are achieved just in the design with considered nonlinear MOSFET capacitances. The switches voltage of the design with assumed linear MOSFET capacitances has jump that creates overlap between the voltage and current waveforms, which results in a power conversion efficiency decrement. This shows the impact of considering nonlinearity.

V. Conclusion

In this paper, the analysis of the class-E_M PA considering the drain-to-source and gate-to-drain capacitances as nonlinear capacitances at any duty ratio has been presented. It has been shown that the nonlinear capacitances increase the switch peak voltage and efficiency, but decrease output power. Also, the duty ratio increment decreases the switch peak voltage, current, and output power, but it increases efficiency in 0.1–0.7 duty ratio range. The output power capability has been calculated versus of the duty ratio. The highest value of the output power capability has been obtained at the duty ratio equal to 0.5. It has been shown that the presented theoretical analysis is more accurate for MOSFETs with lower on-state resistance. Eventually, to validate the presented analysis, five sample designs with IRF510 and IRFZ24N MOSFETs at 3.5 MHz fundamental frequency have been presented. The agreement between theoretical, simulation, and experimental results was very good. It is seen that the proposed work has better efficiency and output power with respect to those in references.

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