Analysis and Implementation of a New SEPIC-Based Single-Switch Buck–Boost DC–DC Converter With Continuous Input Current

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***Abstract*—In this paper, a novel buck–boost dc–dc converter with continuous input current is proposed. The voltage gain of the presented converter is higher than conventional converters, such as buck–boost, single-ended primary-inductance converter, Cuk, and Zeta converters. This converter works only by one switch and voltage stress across the switch is low. Input current of the proposed converter is continuous so a large filter at the input is not needed. Furthermore, continuous input current has made this converter suitable for renewable energy and fuel cell applications. In this converter, noninverting output voltage is obtained and high gain of voltage is achieved as well. So it can operate at wide output voltage range only by changing the duty cycle of the power switch pulse. The presented converter can easily controlled in continuous conduction mode operation, because of using only one power switch. In the following, the principle of operation and the mathematical analyses of the proposed converter are explained, finally, validity of the proposed dc–dc converter is verified by the experimental results.**

***Index Terms*—Buck–boost dc–dc converter, high-gain dc–dc, nonisolated converter, single-ended primary-inductance converter (SEPIC).**

I. Introduction

NOWADAYS global energy consumption tends to grow endlessly. In order to fulfill the demand for electric power against a background of the reduction of conventional fossil resources, the renewable energy sources are becoming more prevalent [1], [2]. Fuel cells represent one of the most efficient and effective alternative renewable energy sources for many applications, such as hybrid electric vehicles, uninterruptible power supplies, telecom back-up facilities, and portable electronics. A number of energy sources, such as solar panel and fuel cell, exhibit low terminal voltage, which calls for high-gain step-up converter to interface with inverter for grid connection. Also, photovoltaic (PV) and wind require an auxiliary converter to have a maximum power extraction. For this reason we will require some tools for using the output energy of this resource. Owing to instabilities in the output voltage of this energy resource, an additional dc–dc buck–boost converter is needed to regulate the output voltage [3]–[7]. But, the traditional buck–boost converter is not suitable for fuel cells sources, because of discontinuous input current. Even though, efficiency of the traditional buck–boost converter is expected high, however, it is limited by the effects of diodes, switches, and equivalent series resistance (ESR) of capacitors and inductors [8]. Therefore, in order to achieve the high efficiency and high-voltage gain, numerous high step-up dc–dc converters have been proposed [9]. Several converter types are capable of providing both step-up and step-down voltage conversion containing the conventional converters, such as inverting buck–boost converter [10], the flyback converter, the Cuk converter, and the single-ended primary-inductance converter (SEPIC) [11]. However, these converters have a great stress across the switches and also, the efficiency of the flyback converter is low because of its high-leakage inductance [12]. In [13], a single-switch isolated step-up converter is presented, which is derived from the traditional flyback converter and charge pump concept. In this converter the output current is nonpulsating. In this converter, because of the use of flyback structure, the output power is limited and the efficiency all over the load is low. In [14], a configuration of switched-capacitor converters connected in parallel with their inputs and outputs interleaved with low EMI is proposed, but the high number of switches and discontinuous input current are some of the disadvantages of this converter. A new scheme of a step-up converter with very high voltage gain based on a natural combination of the switched-coupled-inductor boost converter and the diode-capacitor multiplier is proposed in [15]. Also, this paper analyzes both steady-state and dynamic operation of the converter. In [16], a high efficiency bidirectional dc–dc converter with zero-voltage transition is realized. So, the switching losses of this converter is very low but the use of high number of switches that need more driver and also reduced range of output power controlling can be the restrictions of this converter.

Some dc–dc buck–boost converters are recently presented by using the i.e., 2D converters (KY) [17]. But, four power switches have been used in these converters. In [18], transformerless dc–dc converters to achieve high step-up voltage gain without an extremely high duty ratio are presented. In [19], a noninverting buck–boost converter for fuel-cell system using three power switches and with a voltage gain $2D/1-D$ is proposed. However, the number of switches seems to be high. A

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hybrid nonisolated dc–dc commutation cell, which is generated by the integration between conventional commutation cell and ladder-type passive switched-capacitor cell, is presented in [20]. A buck–boost converter based on the KY converter is proposed in [21]. However, the voltage gain of this converter is $2D$ and two power switches are used. Also, in [22], a transformerless buck–boost dc–dc converter with voltage gain $2D/1-D$ is proposed, which has a suitable voltage gain, but the input current of this converter and the converter in [21] is discontinuous. In [23], a transformerless high-gain buck–boost is proposed, the gain of that converter is $3D/1-D$, but the discontinuous input current and negative voltage polarity are obtained. A single-switch quadratic buck–boost dc–dc converter is presented in [24], which can obtain a wider range of the voltage conversion ratio. A two-stage inverting buck–boost converter is proposed in [25]. However, using two switches and discontinuous input current are some of disadvantages of this converter. The presented converter is constructed of two parallel conventional buck–boost converters. Quality of input current is an important issue in renewable energy applications and also, if the input current of a converter is not continuous, a large filter at its input should be considered.

In this paper, a novel single-switch nonisolated buck–boost dc–dc converter with high step-up voltage gain is proposed. This proposed converter is a single-input single-output converter. It is derived from conventional SEPIC converter at input to have a continuous input current and to obtain both buck and boost capabilities, and also a combination of inductors, capacitors, and diodes are used to have a higher gain rather than an SEPIC and obtain a high-gain buck–boost dc–dc converter. For the proposed converter, the voltage stress on the power switch is low. The voltage transfer gain of the proposed converter is $3D/1-D$, which is higher than the typical buck–boost converter, CUK, SEPIC, and ZETA converters. This converter contains only a power switch, therefore the control of the converter will be easy. The voltage stress across the diodes and power switch is less than the output voltage. The input current of proposed converter is continuous; hence, it can be used in renewable energy applications and also can be utilized in many applications, such as fuel-cell systems, PV maximum power point tracking (mppt), and LED drivers.

The contents of the paper are divided to five sections as follows: introduction in Section I, operating principles of converter in Section II, steady-state analysis in Section III, experimental results in Section IV, and conclusion in Section V.

II. Operating Principle of the Proposed Converter

The proposed single-switch nonisolated converter is shown in Fig. 1(a). This converter consists of a power switch S; three diodes D_1, D_2, and D_3; four inductors L_1, L_2, L_3, and L_4; six capacitors C_1, C_2, C_3, C_{o1}, C_{o2}, C_o; and the load R. The following assumptions are considered for the simplicity of the analysis of the operating principles:

1) The capacitors of the presented converter are large enough, therefore the voltage across the capacitors is assumed to be constant.

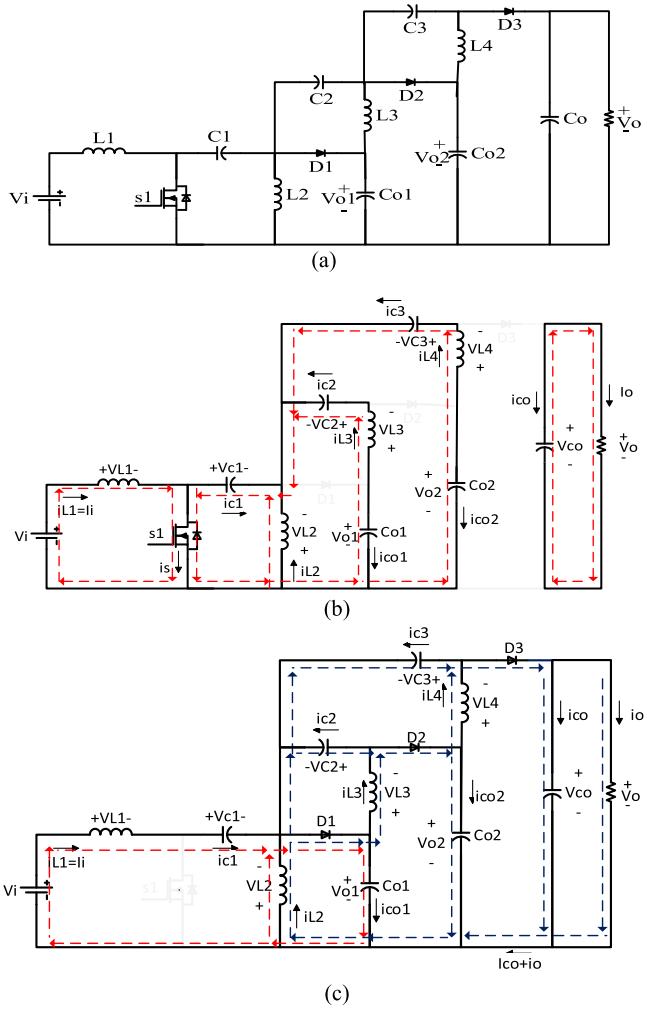

Fig. 1. (a) Equivalent circuit of the proposed converter, (b) Mode 1, and (c) Mode 2.

2) The main switch is treated as ideal and so the parasitic capacitor of the main switch can be neglected.

The proposed converter can be operated in two main conditions, continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). Operation principles and analyses of the converter in CCM contain two main modes that are explained as follows.

1) First mode [$0 \le T \le DT_s$]: During this mode, as shown in Fig. 1(b), switch S is turned ON and the diodes D_1, D_2, D_3 are turned OFF. The inductors L_1, L_2, L_3, and L_4 are magnetized linearly. The capacitor C_1 is discharged, and C_2 and C_3 are, respectively, charged by the capacitors C_{o1} and C_{o2}. Thus, the related equations can be written as follows:

$$V_{L1} = V_i \tag{1}$$

$$V_{L2} = -V_{c1} = -V_i = -V_{c2} - V_{L3} + V_{o1} = -V_{c3} - V_{L4} + V_{o2} \tag{2}$$

$$V_{L3} = V_{c1} - V_{c2} + V_{o1} = V_i \tag{3}$$

$$V_{L4} = V_{c1} - V_{c3} + V_{o2} = V_i. \tag{4}$$

2) Second mode [$DT_s \le T \le T_s$]: The corresponding circuit is shown in Fig. 1(c). During this mode, the power switch S is turned OFF and the diodes D_1, D_2, D_3 are turned ON. The inductors L_1, L_2, L_3, and L_4 are demagnetized linearly. The capacitor C_1 is charged by the inductor L_1, capacitors C_{o1} and C_{o2} are charged by L_2, L_3, respectively, and capacitors C_2, C_3 are discharged. The corresponding equations can be written as follows:

$$V_{L1} = V_g - V_{c1} - V_{L2} = \frac{-D}{1-D}V_i \tag{5}$$

$$V_{L2} = -V_{c2} + V_{o2} = -V_{c3} + V_o = V_{o1} = \frac{D}{1-D}V_i \tag{6}$$

$$V_{L3} = -V_{c2} = \frac{-D}{1-D}V_i \tag{7}$$

$$V_{L4} = V_{c2} - V_{c3} = \frac{-D}{1-D}V_i. \tag{8}$$

III. Steady-State Analysis of the Proposed Converter

A. Voltage Gain

By applying the voltage-second balance principle on the inductors L_1, L_2, L_3, and L_4 and using (1)–(8), it gives

$$\frac{1}{T_s}\left(\int_0^{DT_s} V_i dt + \int_0^{DT_s} (V_i - V_{c1} - V_{L2})dt\right) = 0 \tag{9}$$

$$\frac{1}{T_s}\left(\int_0^{DT_s} -V_{c1} dt + \int_{DT_s}^{T_s} V_{o1} dt\right) = 0 \tag{10}$$

$$\frac{1}{T_s}\left(\int_0^{DT_s} (V_{c1} - V_{c2} + V_{o1})dt + \int_{DT_s}^{T_s} -V_{c2} dt\right) = 0 \tag{11}$$

$$\frac{1}{T_s}\left(\int_0^{DT_s} (V_{c1} - V_{c3} + V_{o2})dt + \int_{DT_s}^{T_s} (V_{c2} - V_{c3})dt\right) = 0. \tag{12}$$

By using (6) in (9) and solving (9)–(10), we have

$$V_{c1} = V_i = \frac{1-D}{D}V_{o1}. \tag{13}$$

And by using (13) in (11), one obtains

$$V_{c2} = V_{o1}. \tag{14}$$

By using $V_{o2} - V_{c2}$ instead of V_{o1} in (10), V_{o2} can be achieved as follows:

$$V_{o2} = 2V_{o1}. \tag{15}$$

By using the results of V_{c1} and V_{c2} in (12), we have

$$V_{c3} = 2V_{o1}. \tag{16}$$

By using $V_{o2} - V_o$ instead of $V_{c2} - V_{c3}$ in (12) and using (13), V_o can be achieved as follows:

$$V_o = 3V_{o1} = \frac{3D}{1-D}. \tag{17}$$

Hence, the voltage transfer gain (M_{CCM}) can be found as follows:

$$M_{\mathrm{CCM}} = \frac{V_o}{V_i} = \frac{3D}{1-D}. \tag{18}$$

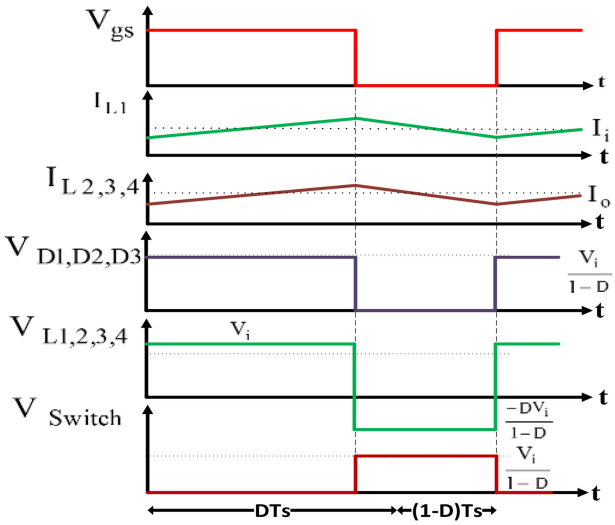

Fig. 2. Some typical waveforms of the proposed converter.

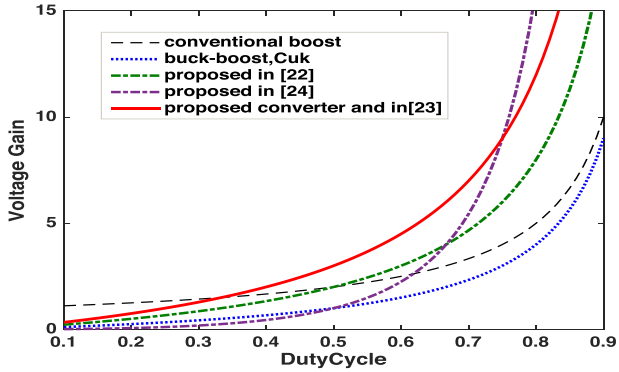

Fig. 3. Curves of voltage gain comparison of the proposed converter and other converters at CCM operation.

Some of the key waveforms of the proposed converter in CCM mode are shown in Fig. 2.

A comparison between voltage transfer gains of the proposed converter with conventional boost, buck–boost dc–dc converter, SEPIC, and converter proposed in [22], [23], and [24] is shown in Fig. 3. It shows that the voltage transfer gain of the proposed converter is higher than that of these converters. And it is shown that the gain of the buck–boost dc–dc converter is the lowest in a range of duty cycle from 0.1 to 0.9.

B. Calculation of Currents

During the on state of a switch, average current equations for capacitors can be written as follows:

$$i_{c1} = -i_{L2} - i_{c2} - i_{c3} = -3i_o \tag{19}$$

$$i_{c2} = -i_{co1} = i_{L3} = i_o \tag{20}$$

$$i_{c3} = -i_{co2} = i_{L4} = i_o \tag{21}$$

$$i_{co} = -i_o. \tag{22}$$

And during the off state of a switch, we have

$$i_{c1} = I_i = i_{L1} = -i_{L2} + i_{L3} + i_{co1} - i_{c2} - i_{c3} = \frac{3D}{1-D} i_o \tag{23}$$

$$i_{c2} = i_{L3} - i_{L4} - i_{co2} = \frac{-1}{1-D} i_o \tag{24}$$

$$i_{c3} = i_{L4} - i_{co} - i_o = \frac{-D}{1-D} i_o. \tag{25}$$

By applying the current-second balance principle on capacitors $C_{1,2,3}$ and $C_{o1,o2,o}$ the following equation is derived as follows:

$$\frac{1}{T_s}\left(\int_0^{DT_s} I_{C1,2,3,o1,o2,o,\text{on}}\, dt + \int_{DT_s}^{T_s} I_{C1,2,3,o1,o2,o,\text{off}}\, dt\right) = 0. \tag{26}$$

By substituting (19)–(25) into (26), and considering $i_{L1} = I_i$, the average current through the inductors and capacitors can be described as follows:

$$i_{L1} = i_{\text{in}} = \frac{3D}{1-D} i_o \tag{27}$$

$$i_{L2} = i_{L3} = i_{L4} = \frac{-1}{3} i_{c1,\text{on}} = i_{c2,\text{on}} = i_{c3,\text{on}} = i_{co,\text{on}} = i_o$$

$$i_{co1,\text{on}} = i_{co2,\text{on}} = -i_o. \tag{28}$$

According to Fig. 1(b), for the average current that flows through the switch S (i_s), it can be written

$$i_{\text{S,on}} = i_{L1} - i_{c1} = i_{L1} + i_{L2} + i_{L3} + i_{L4} = \frac{3}{1-D} i_o. \tag{29}$$

For average currents of diodes, from (23) to (25) and Fig. 1(c) it can be obtained that

$$i_{D1} = I_i + i_{L2} + i_{c2,off} + i_{c3,off} = \frac{I_o}{1-D} \tag{30}$$

$$i_{D2} = i_{L3} - i_{c2,off} = \frac{I_o}{1-D} \tag{31}$$

$$i_{D3} = i_{L4} - i_{c3,off} = \frac{I_o}{1-D}. \tag{32}$$

The current ripple of inductor $L1$ and current ripple of inductors $L2$, $L3$, and $L4$ can be calculated as follows:

$$\Delta I_{L1} = \frac{DV_i}{L_1 f_s} = \frac{(1-D)V_o}{3L_1 f_s} \tag{33}$$

$$\Delta I_{L2,3,4} = \frac{DV_i}{L_{2,3,4} f_s} = \frac{(1-D)V_o}{3L_{2,3,4} f_s}. \tag{34}$$

C. Discontinuous Conduction Mode

In this mode, the proposed converter operation can be divided into three modes. Mode 1 and mode 2 are same as that of CCM, and in mode 3, the current of the main switch and currents of diodes D_1, D_2, D_3 are zero. Also, the currents of inductors L_1, L_2, L_3, and L_4 are zero. Hence the voltage across the inductors are zero. The equivalent circuit and typical waveforms of the converter are shown in Figs. 4 and 5.

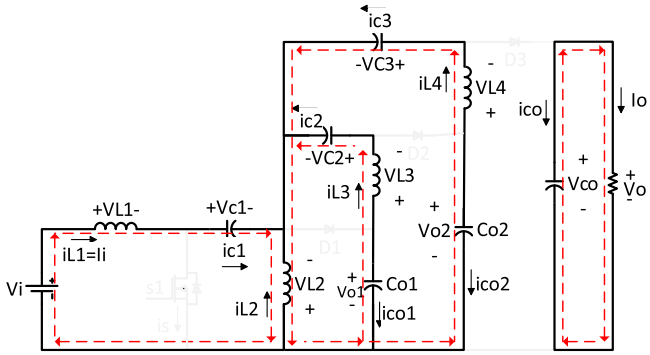

Fig. 4. Equivalent circuits of the proposed converter in third mode at DCM operation.

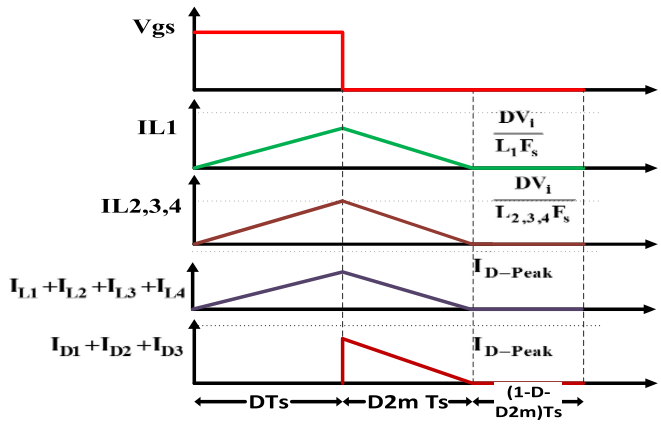

Fig. 5. Some demonstrated key waveforms of the presented converter at DCM operation.

According to (30)–(32) and considering $i_{L1} = i_g$, sum of the diodes D_1, D_2, D_3 currents and the average currents of diodes $(I_{D1,\text{avg}}, I_{D2,\text{avg}}, I_{D3,\text{avg}})$, can be written as follows:

$$i_{D1} + i_{D2} + i_{D3} = i_{L1} + i_{L2} + i_{L3} + i_{L4} \tag{35}$$

$$I_{D1,\text{avg}} = I_{D2,\text{avg}} = I_{D3,\text{avg}} = I_o = \frac{V_o}{R}. \tag{36}$$

By observing Fig. 4 it can be defined that sum of the diodes D_1, D_2, D_3 currents during a period of switching can be obtained as follows:

$$\sum_{i=1}^{3} I_{Di,\text{avg}} = \frac{1}{2} \times D_{2m} \times I_{D-\text{peak}} \tag{37}$$

where D_{2m} is the duty cycle of the second mode in DCM and $I_{D-\text{Peak}}$ is sum of the peak currents for inductors L_1, L_2, L_3, and L_4. In Fig. 5, $I_{D-\text{Peak}}$ can be calculated as follows:

$$I_{D-\text{peak}} = I_{L1,\text{Peak}} + I_{L2,\text{Peak}} + I_{L3,\text{Peak}} + I_{L4,\text{Peak}}$$

$$= \sum_{n=1}^{4} \frac{DT_s V_i}{L_n} = \frac{DT_s V_i}{L_{\text{eq}}} \tag{38}$$

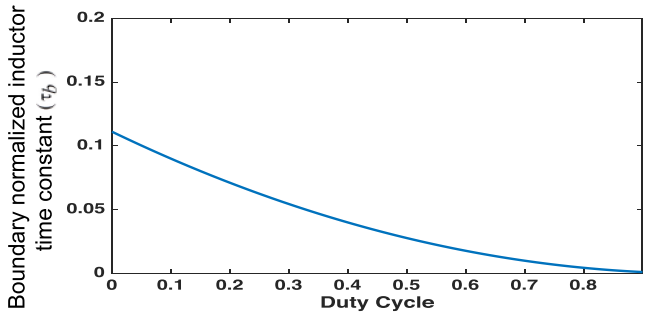

Fig. 6. Normalized inductor time constant versus duty cycle.

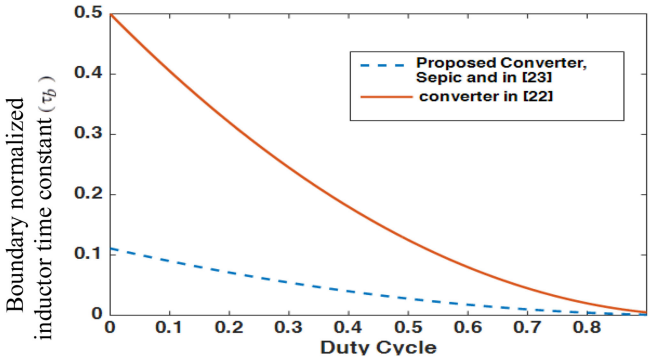

Fig. 7. Curves of boundary inductor time constant comparison of proposed converter and other converters.

where

$$L_{\rm eq} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4}. \tag{39}$$

For calculating DCM voltage transfer gain, voltage-second balance principle should apply on the inductors L_1, L_2, L_3, and L_4 in the second mode of DCM operation. Hence, duty cycle (D_{2m}) in second mode can be earned as follows:

$$D_{2m} = \frac{3DV_i}{V_o}. \tag{40}$$

Now, voltage transfer gain can be calculated using (35)–(40) as follows:

$$M_{\rm DCM} = \frac{D}{\sqrt{\tau_L}} \tag{41}$$

where τ_L is expressed as follows:

$$\tau_L = \frac{2L_{\rm eq}}{RT_s}. \tag{42}$$

D. Boundary Conduction Mode (BCM)

In this mode, normalized inductor time constant (τ_b) is obtained. In BCM, the voltage transfer gain of the CCM is equal to the voltage transfer gain of the DCM. Hence, from (18)–(41), τ_b can be obtained as

$$\tau_b = \frac{(1-D)^2}{9}. \tag{43}$$

For the proposed converter in operating point, if τ_L is larger than τ_b, the converter operates in CCM and if τ_b is larger than τ_L, the converter operates in DCM. The curves for τ_b is shown in Fig. 6. It shows that the proposed converter works in CCM for a large range of operation.

The curves of normalized inductor time constant of the proposed converter, converter in [22] and [23], and conventional SEPIC are shown in Fig. 7.

From Fig. 7, one obtains that the boundary normalized inductor time constant for the proposed converter is same as that of the conventional SEPIC.

E. Averaged Switch Modeling

The averaged switch model of the proposed converter, by using and replacing the general switch and diode model in [26], is obtained. So, in order to show the dynamic characteristics of the proposed converter in CCM, the averaged switch model of the converter is provided and is shown in Fig. 8. In this model, the symbol ($\wedge$) shows the dynamic changes of the parameter. So, in a period of switching (T_s), the duty cycle is $\langle d(t)\rangle = D + \hat{d}(t)$, input voltage $\langle V_i(t)\rangle = V_i + \hat{V}_i(t)$, capacitors voltage $\langle V_C(t)\rangle = V_C + \hat{V}_C(t)$, and inductors current is $\langle I_L(t)\rangle = I_L + \hat{I}_L(t)$. In Fig. 8, *vs*1, *i*1, *i*2, and *i*3 are, respectively, $\hat{d}(t)V_i/DD'$, $\hat{d}(t)I_{D1}/DD'$, $\hat{d}(t)I_{D2}/DD'$, and $\hat{d}(t)I_{D3}/DD'$.

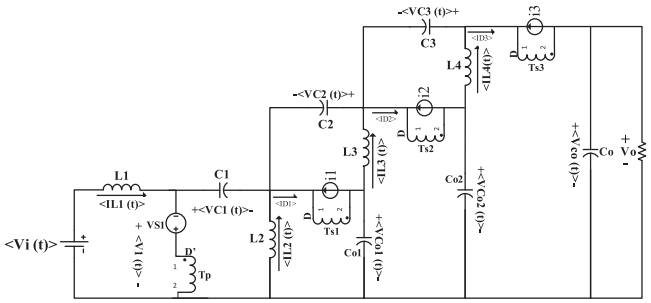

Fig. 8. Averaged switch model of the proposed converter.

In this model, T_p is transformer primary and also, T_{s1}, T_{s2}, and T_{s3} are transformer secondary windings.

F. Efficiency Analysis

The efficiency of the proposed converter is analyzed by the following assumptions. The parasitic resistances are defined as follows: r_{ds} is switch on-state resistances, R_{F1}, R_{F2}, R_{F3} are forward resistances of diodes D_1, D_2, D_3, respectively. Forward voltages V_{F1}, V_{F2}, and V_{F3}, are the forward bias voltages of diodes D_1, D_2, and D_3, respectively.

r_{L1}, r_{L2}, r_{L3}, and r_{L4} are the ESR of inductors *L*1, *L*2, and *L*3, respectively. r_{c1}, r_{c2}, r_{c3}, r_{co1}, r_{co2}, and r_{co} are the ESR of capacitors *C1*, *C2*, *C3*, *Co1*, *Co2*, and *Co*, respectively, and the voltage ripple across the capacitors and the inductors is ignored.

The conduction power loss through the main switch S (P_{rds}) can be earned as follows:

$$P_{rds} = r_{ds} I_{s,\rm rms}^2 = r_{ds} \frac{9D}{(1-D)^2} I_o^2. \tag{44}$$

Switching loss of the switch S ($P_{\rm sw}$) can be achieved as follows:

$$P_{\rm sw} = f_s C_s V_s^2 = f_s C_s \frac{V_i^2}{(1-D)^2}. \tag{45}$$

The total losses of the switch S ($P_{\rm switch,tot}$) can be earned as follows:

$$P_{\rm switch,tot} = P_{rds} + P_{\rm sw}. \tag{46}$$

The diodes D_1, D_2, and D_3 forward resistance losses ($P_{{\rm RF}_{D1,D2,D3}}$) and forward voltage losses ($P_{{\rm VF}_{D1,D2,D3}}$) can be achieved as follows:

$$P_{{\rm RF}_{D1,D2,D3}} = R \times I_{D\rm rms}^2 = R_{F1,2,3} \frac{I_o^2}{(1-D)} \tag{47}$$

$$P_{{\rm VF}_{D1,D2,D3}} = V_{F_{D1,D2,D3}} \times I_{D{\rm rms}_{D1,D2,D3}}^2 = V_{F1,2,3} I_o. \tag{48}$$

The power losses of capacitors, *C1*, *C2*, *C3*, *Co1*, *Co2*, and *Co*, (P_{rC1}) and ($P_{rC2,3,o1,o2,o}$) due to the ESR, respectively, can be obtained as follows:

$$P_{rc1} = r_{c1} \times I_{c1,\rm rms}^2 = R_{c1} \frac{9D}{1-D} I_o^2 \tag{49}$$

$$P_{rc2,3,o1,o2,o} = r_{c2,3,o1,o2,o} \times I_{c2,3,o1,o2,o,\rm rms}^2 = r_{c2,3,o1,o2,o} \frac{D}{1-D} I_o^2. \tag{50}$$

The conduction losses of inductors, *L1, L2, L3,* and *L4*, P_{rL1} and $P_{rL2,3,4}$ can be calculated as follows:

$$P_{rL1} = r_{L1} \times I_{L1,\rm rms}^2 = r_{L1} \left(\frac{3D}{1-D}\right) I_o^2 \tag{51}$$

$$P_{rL2,3,4} = r_{L1} \times I_{L1,\rm rms}^2 = r_{L1} I_o^2. \tag{52}$$

The total power dissipation of the converter is the sum of (44)–(52) and can be obtained as follows:

$$P_{\rm Loss} = P_{\rm Switch} + \sum_{i=1}^{3} (P_{Di} + P_{rci}) + \sum_{i=1}^{4} (P_{rLi}) + P_{rco} + \sum_{i=1}^{2} (P_{rcoi}). \tag{53}$$

The efficiency (η) of the converter can be obtained as follows:

$$\eta = \frac{P_o}{P_{\rm Loss} + P_o} = \frac{1}{1 + \frac{P_{\rm Loss}}{RI_o^2}}. \tag{54}$$

G. Voltage Stress and Number of Elements Comparison

In the proposed converter, the voltage stress of switch and diodes D_1, D_2, and D_3 during switch off state and diodes off state ($V_{\rm S,rev}, V_{D,\rm rev}$), respectively, can be expressed as follows:

$$V_{S,\rm rev} = V_{D,\rm rev} = \frac{V_i}{1-D}. \tag{55}$$

A comparison of normalized stress of switch $V_{S,\rm rev}/V_i$ between the proposed converter and the conventional boost, buck–boost dc–dc converter, SEPIC, and converter proposed in [22]–[24] is shown in Fig. 9. Table I shows an elements number comparison between the proposed converter and some other converters. According to Table I, the voltage stress across switch, in comparison with the converters in [22]–[24], and the traditional SEPIC is less and suitable. Also, the continuous input current of the proposed converter with positive output voltage, is the advantage of this converter rather than the converter in [23] and the conventional buck–boost dc–dc converter. Even though the number of elements in the proposed converter is higher than other converters, but small voltage stress of elements, continuous input current, high gain of voltage, positive output, and the use of a single switch are the advantages of the proposed converter.

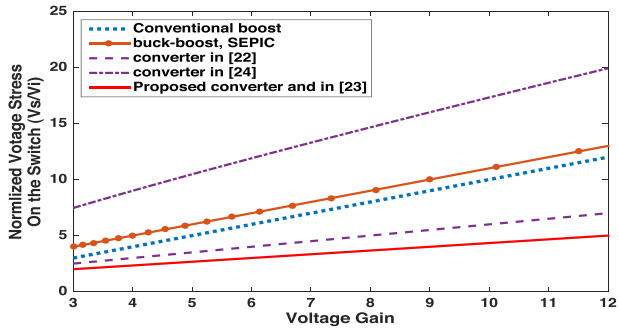

Fig. 9. Normalized switch voltage stress versus voltage gain.

TABLE I
COMPARISON BETWEEN PROPOSED CONVERTER AND OTHER STRUCTURES

Case	Proposed	Converter in [23]	Converter in [22]	SEPIC	Converter in [24]
Numbers of switches	1	1	1	1	1
Numbers of diodes	3	3	2	1	5
Numbers of capacitors	6	5	3	2	3
Numbers of inductors	4	3	2	2	3
Total device count	14	12	8	6	12
Voltage gain	$\frac{3DV_i}{1-D}$	$\frac{-3DV_i}{1-D}$	$\frac{2DV_i}{1-D}$	$\frac{DV_i}{1-D}$	$\frac{D^2V_i}{(1-D)^2}$
Switch Voltage Stress	$\frac{V_o}{3D}$	$\frac{V_o}{3D}$	$\frac{V_o}{2D}$	$\frac{V_o}{D}$	$\frac{V_o}{D^2}$
Continuous Input current	YES	NO	NO	YES	Yes

1) Calculation of the Voltage Ripple of the Capacitors: During the operation of the proposed converter, capacitors voltage has a dc and an ac component. The ac component determines the ripple of capacitor voltage and is not suitable for the converter. The ripple of each capacitor is the sum of the capacitor and it's ESR resistance. The amount of the ripple of the capacitors *C1, C2, C3, Co1, Co2,* and *Co* ($\Delta V_{C1,\rm cap}$, $\Delta V_{C2,\rm cap}$, $\Delta V_{C3,\rm cap}$, $\Delta V_{Co1,\rm cap}$, $\Delta V_{Co2,\rm cap}$, $\Delta V_{Co,\rm cap}$) with their ESR ripple ($\Delta V_{C1,ESR}$, $\Delta V_{C2,ESR}$, $\Delta V_{C3,ESR}$, $\Delta V_{Co1,ESR}$, $\Delta V_{Co2,ESR}$, $\Delta V_{Co,ESR}$) are expressed as follows:

$$\Delta V_{c1,\rm cap} = \frac{3DI_o}{C_1 f_s} = \frac{3DT_s V_o}{C_1 R} \tag{56}$$

$$\Delta V_{c1,ESR} = {\rm ESR}_{C1} \Delta I_{C1} \simeq {\rm ESR}_{C1}(I_{C1,\rm on} - I_{C1,\rm off}) = \frac{3{\rm ESR}_c I_o}{1-D}. \tag{57}$$

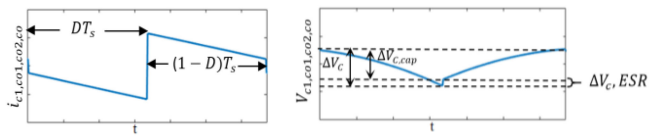

Fig. 10. Current and voltage of the capacitors C_1, C_{o1}, C_{o2}, and C_O.

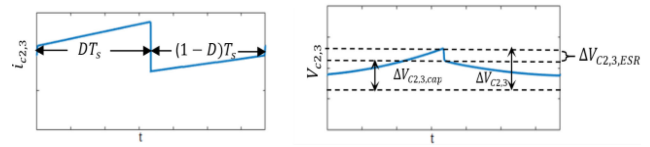

Fig. 11. Current and voltage of the capacitors C_2 and C_3.

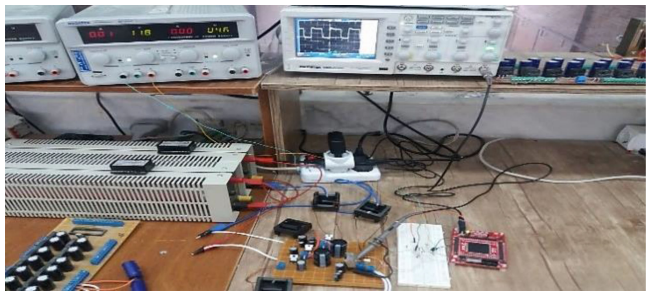

Fig. 12. Prototype of the proposed converter.

For other capacitors, we have

$$\Delta V_{c2,3,o1,o2,o,\text{cap}} = \frac{DI_o}{C_{2,3,o1,o2,o} f_s} = \frac{DT_s V_o}{RC_{2,3,o1,o2,o}} \tag{58}$$

$$\Delta V_{c2,3,o1,o2,o} = \frac{I_o \times \text{ESR}_{(c2,3,o1,o2,o)}}{1-D}. \tag{59}$$

Now, the total voltage ripples of capacitors can be written as follows:

$$\Delta V_{c1} = \frac{3DI_o}{C_1 f_s} + \frac{I_o \text{ESR}_{c1}}{1-D} \tag{60}$$

$$\Delta V_{c(2,3,o1,o2,o)} = \frac{DT_s I_o}{C_{(2,3,o1,o2,o)}} + \frac{I_o \times \text{ESR}_{(c2,3,o1,o2,o)}}{1-D}. \tag{61}$$

The current and voltage of the capacitors *C1, C2, C3, Co1, Co2, Co* are shown in Figs. 10 and 11. The dimension of waveforms can varies by changing capacitor or ESR amounts and waveforms only shows how currents and voltage varies.

IV. Experimental Results

In order to validate theoretical calculations of the proposed converter, a prototype of the converter is built as shown in Fig. 12. A Xilinx sprtan3 FPGA is used to generate pulses for the converter. In Table II, the proposed converter's components specifications, input voltages, and output loads of buck and boost states, under the test condition are presented.

The experimental results are presented at 33 kHz switching frequency with 22% duty cycle in buck state and with 60% in boost state operation.

TABLE II
Proposed Converter Components Specifications and Input Voltages at Test Condition

Input voltage-buck	22 V
Output voltage-buck	18 V
Output power-buck	33.48 W
Input voltage-boost	25 V
Output voltage-boost	110 V
Output power-boost	110 W
Switch	IRFP260 n
Diodes D_1, D_2, D_3	MUR860
Inductor L_1	260 μH
Inductor L_2, L_3, L_4	510 μH
Capacitors C_1, C_2, C_3, Co_1	100 μF
Capacitors Co_2, C_o	470 μF

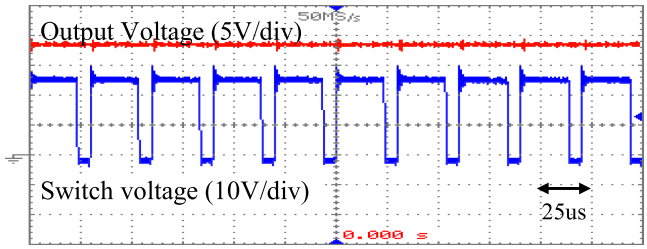

Fig. 13. Output voltage and switch S voltage.

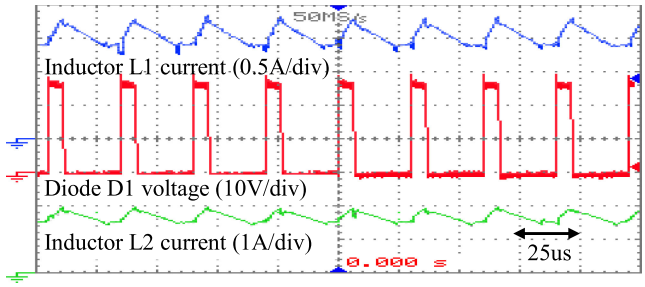

Fig. 14. Inductor *L*1 current, diode D1 voltage, and inductor *L*2 current.

The waveforms of the converter while operating in CCM and step-down state operation are shown in Figs. 13 and 14. According to (18), with the input voltage $V_i = 22$, the output voltage at ideal condition can be obtained as follows:

$$V_o = \frac{3 \times D}{1-D} V_i = \frac{3 \times 0.22}{1-0.22} \times 22 = 18.61 \tag{62}$$

which closely agrees with the output voltage in Fig. 13. It shows that the output voltage in step-down state is 18 V. Also, according to (27), the average current values of L_1, L_2, L_3, and L_4 are about 1.57, 1.86, 1.86, 1.86 A, respectively, and the current ripple of inductors *L*1 and *L*2, *L*3, and *L*4 by using (33) and (34) can be calculated as follows:

$$\Delta I_{L1} = \frac{DV_i}{L_1 f_s} = \frac{0.22 \times 22}{260 \times 10^{-6} \times 33000} \approx 0.56\,\text{A} \tag{63}$$

$$\Delta I_{L2,3,4} = \frac{DV_i}{L2,3,4 f_s} = \frac{0.22 * 22}{510 \times 10^{-6} \times 33000} \approx 0.28\,\text{A} \tag{64}$$

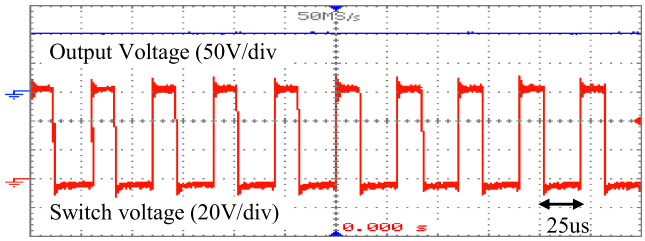

Fig. 15. Output voltage and switch S voltage.

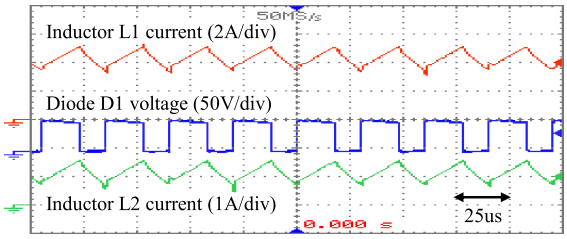

Fig. 16. Inductor $L1$ current, diode $D1$ voltage, and inductor $L2$ current.

which closely agree with the experimental results in Fig. 14. Also, the theoretical voltage stress of power switch (S) and diode ($D1$, $D2$, $D3$) by using (55) can be obtained as

$$V_{s,\text{rev}} = V_{D1,D2,D3,\text{rev}} = \frac{V_i}{1-D} = \frac{22}{1-0.22} = 28.2\,\text{V} \tag{65}$$

which closely approves with the experimental results Figs. 13 and 14.

The key waveforms of the proposed converter while operating in CCM and step-up state operation, is shown in Figs. 15 and 16. According to (18) the output voltage in step-up state at 60% duty cycle and input voltage 25 V, is 112.5 V. Also, the output voltage at Fig. 15 is 110 V and by using a 110 Ω output load, the output power is obtained 110 W. The average current values of L_1, L_2, L_3, and L_4 according to (27) are about 4.6, 1, 1, and 1 A, respectively, which closely agree with the experimental results. Also, by using (33) and (34) and using parameters listed in Table II, the current ripple of the inductors $L1$ and inductors $L2$, $L3$, and $L4$ can be calculated as follows:

$$\Delta I_{L1} = \frac{DV_i}{L_1 f_s} = \frac{0.6 \times 25}{260 \times 10^{-6} \times 33000} \approx 1.74\,\text{A} \tag{66}$$

$$\Delta I_{L2,3,4} = \frac{DV_i}{L2,3,4 f_s} = \frac{0.6 * 25}{510 \times 10^{-6} \times 33000} \approx 0.89\,\text{A}. \tag{67}$$

So, calculated current ripples closely agree with the experimental results shown in Fig. 16. However, by using (55) the theoretical voltage stress of power switch (S) and diode ($D1$, $D2$, $D3$) in CCM condition and in step-up mode of operation, can be obtained as:

$$V_{s,\text{rev}} = V_{D1,D2,D3,\text{rev}} = \frac{V_i}{1-D} = \frac{25}{1-0.6} = 62.5\,\text{V} \tag{68}$$

which closely approves with the experimental results shown in Figs. 15 and 16.

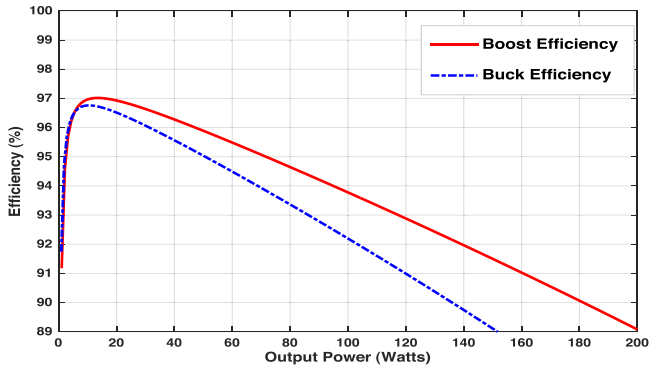

Fig. 17. Proposed converter efficiency versus output power.

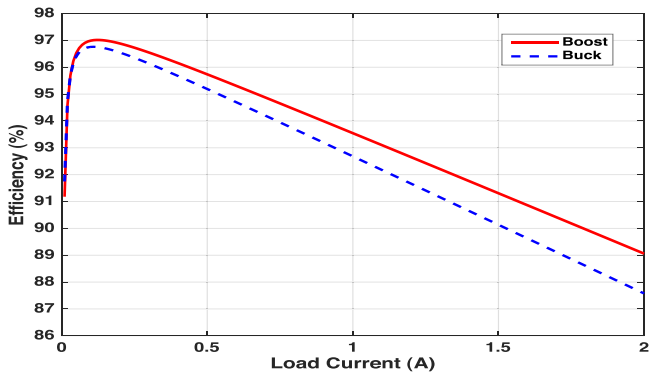

Fig. 18. Proposed converter efficiency versus load current.

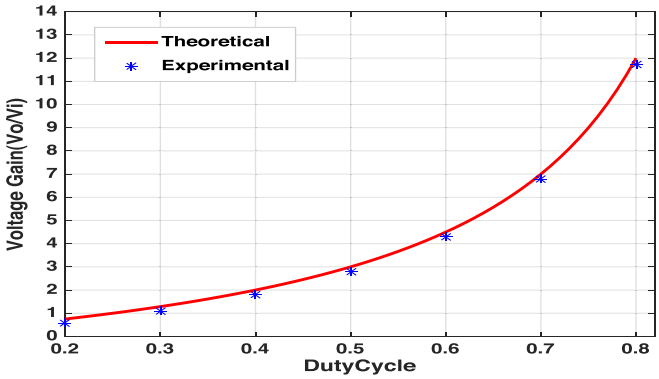

Fig. 19. Proposed converter theoretical voltage gain versus experimental.

For the proposed converter, Figs. 17 and 18 show the curve of efficiency versus output power and the curve of efficiency versus load current, respectively. The efficiency curves are obtained at fixed duty cycle and in CCM state operation with $d = 60\%$, $V_{\text{in}} = 25$ V for boost and with $d = 22\%$ and $V_{\text{in}} = 22$ V for buck state and CCM state operation. Also, at both buck and boost conditions, because of CCM state of operation, the output voltage has been maintained constant and output voltage is not varied by changing output load. However, by using the results of Fig. 17, it can be understood that the maximum efficiency of the converter is in boost state and it is 97%. However, the efficiency of the converter in 110 W is 93.3%.

In order to show the effect of varying duty cycle from 0.2 to 0.8 on the voltage gain of the converter at CCM state of

operation and showing the variations of the experimental voltage gain versus theoretical voltage gain curves, Fig. 19 is provided. During the test, output load and input voltage are considered as $R_o = 110\ \Omega$ and $V_i = 11$ V, respectively. The output power of the proposed converter at $D = 0.2$ is about 0.35 W with efficiency $\eta = 51\%$ and at $D = 0.8$ is about 146.6 W with efficiency $\eta = 94\%$.

From Fig. 19, it is observed that the experimental voltage gain is lower than theoretical, but it is nearly followed by theoretical results.

V. Conclusion

In this paper, a novel SEPIC-based structure for step-up and step-down dc–dc converter has been proposed. Continuous input current, using a single-switch, noninverting output and high gain of voltage are the advantages of the proposed converter. Steady-state analysis of the converter under CCM condition has been discussed. The voltage gain, voltage stress of the main switch, number of elements, and other specification of the proposed converter have been compared with some other step-up step-down converters and the privilege of the proposed converter has been justified. The maximum efficiency of the converter is about 97% and it occurs at about 18 W in boost state. Finally, the proposed converter has been implemented under the output power of 110 W with the efficiency of 93.3% and its feasibility has been verified by the experimental results.

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