Letters

Accurate Operating Analysis of Boundary Mode Totem-Pole Boost PFC Converter Considering the Reverse Recovery of MOSFET

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***Abstract*—The boundary conduction mode (BCM) totem-pole boost power factor correction (PFC) topology is becoming popular in high-efficiency and high power density applications because of its advantages of fewer devices and low conduction losses. The ideal design methodology for the BCM boost converter ignores the reverse recovery of MOSFETs' body diode and the resonance between the inductance and output junction capacitances of switches. However, as the switching frequency increases, these two factors affect the peak value of the inductance current and the switching frequency significantly, which are critical parameters for the boost PFC inductor design. In order to calculate the practical peak current and switching frequency range accurately, this letter proposes an analytical reverse recovery model of the body diode and presents accurate switching cycle operating modes. Either the predicted inductance peak current or the switching frequency range matches the measured result on a 600-W totem-pole boost PFC prototype.**

***Index Terms*—Analytical reverse recovery model, boundary conduction mode (BCM), resonance, totem-pole boost power factor correction (PFC).**

I. Introduction

WITH THE increasing requirements of power density and efficiency for an ac/dc converter, the boundary conduction mode (BCM) totem-pole power factor correction (PFC) rectifier shown in Fig. 1(a) [1] has become a popular solution in server and telecommunication application. The SR_1 and SR_2 are line frequency synchronous rectifiers; S_1 and S_2 are high-frequency switches. In a switching period, the totem-pole boost PFC converter equals a BCM boost converter shown in Fig. 1(b), where SR_1 and SR_2 are neglected.

For a BCM boost converter, the main switch [S_2 in Fig. 1(b)] can achieve zero-voltage switch (ZVS) when the input voltage is less than half of output voltage, or obtain valley switch (VS) when the input voltage is more than half of output voltage. The quasi-square-wave control can achieve full ZVS, but the rms current value is too large for a PFC application because of its fixed switching frequency and complementary control for two switches [2]–[4]. The triangular current mode (TCM) can also be utilized for achieving full ZVS when the complementary driving for S_1 and S_2 is adopted [5]–[7]. However, the TCM control method is a little bit complex. Hence, the digital signal processor is necessary and the cost is high. With the body diode freewheeling operating mode, the control strategy is simple, and the tradition analog controller can be utilized. Then, the BCM totem-pole boost PFC converter works like a conventional BCM boost PFC converter, except for the serious reverse recovery of the body diode.

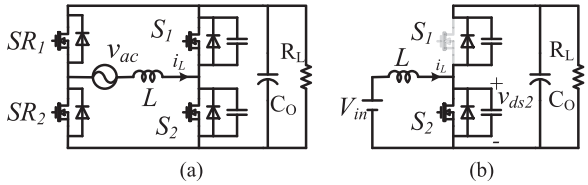

Fig. 1. Totem-pole boost PFC converter and its equivalent circuit. (a) Totem-pole boost PFC converter [1]. (b) Equivalent boost circuit at positive half cycle.

The ideal design methodology for the BCM boost converter usually ignores the influence of the negative inductance current [8] at low frequency (about 25–30 kHz). Huber *et al*. [9] proposed an approximately calculating method by considering the resonance process and neglecting the reverse recovery process. However, in a BCM totem-pole boost PFC, the freewheeling diode of switching frequency is the body diode, whose reverse recovery is severe and could last about 2 μs for a superjunction MOSFET in practical applications. Meanwhile, in order to improve the power density, the switching frequency will be designed to be higher than 100 kHz. Therefore, the ideal switching cycle model, which ignores the negative current in the inductance [8], is not suitable for BCM totem-pole boost PFC. The diode models have been discussed in previous publications [10]–[14]. The basic charge control model is widely used in circuit simulators, but it does not provide for reverse recovery of the diode [10]. The lumped charge control model [11] derived from the semiconductor charge transport equations can introduce the reverse recovery of diodes. The lumped charge control model is relatively easier to extract parameter, and it consumes less computation time [12]; it can be extended to simulate the body diode

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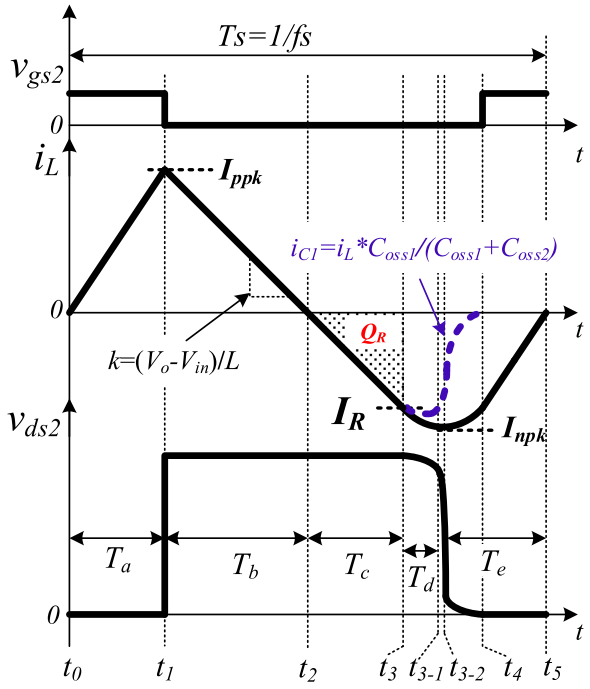

Fig. 2. Key waveforms in a switching period.

of CoolMOS [13]. Based on the same concept, Krihely and Ben-Yaakov [14] developed a behavior model of the reverse recovery of diode by discrete transition simulators (such as power simulation (PSIM)) with higher simulating speed and the ability to show parasitic processes. However, these diode models [11]–[14] mentioned above cannot provide analytical solution of the reverse recovery time and current. Therefore, they are usually used in simulators. However, in a PFC converter, every switching cycle is different during a line period, which consumes a lot of computing resources. In that, the analytical operating model of totem-pole boost PFC converter considering the reverse recovery is lacking; the engineers would like to try a rough estimated inductance and test the real current and frequency. Then, according to the frequency difference between the expectation and test, they modify the inductance by repeating the iterative trying and testing procedure, until the switching frequency can match the expected value.

In order to accurately predict the operating modes in a switching cycle, this letter proposes a simple analytical model for the reverse recovery of the body diode based on calibration and curve fitting methods. With the analytical reverse recovery model and accurate operating switching cycle modes, the peak current (I_{ppk}) and the range of the switching frequency (f_s) of the inductance can be calculated.

II. Accuracy Analytical Analysis of Switching Stages in a BCM Boost Converter

A. Brief Introduction of Operating Stages

Considering the reverse recovery of the body diode, a switching period of BCM boost converter can be divided into five stages shown in Fig. 2.

Stage 1 (t_0–t_1): At t_0, S_2 turns ON, the inductance current i_L flows through S_2, and it increases from zero to the positive peak value I_{ppk}.

Stage 2 (t_1–t_2): At t_1, S_2 turns OFF. Because the peak current is large, the transition interval of v_{ds2} is small and can be neglected. During this stage, the inductance current i_L flows through the body diode of S_1, and it decreases from I_{ppk} to zero.

Stage 3 (t_2–t_3): At t_2, i_L decreases to zero. Owing to the reverse recovery of S_1's body diode, the inductance current continues to flow through the body diode and decreases after t_2 until the diode starts to withstand reverse voltage.

Stage 4 (t_3–t_4): After t_3, the body diode of S_1 turns OFF, and the drain to source voltage of S_2 (v_{ds2}) begins to decrease from V_o because of the resonance between inductance L and output junction capacitances of S_1 and S_2. Meanwhile, the current i_L charges and discharges the output junction capacitance of S_1 and S_2, respectively. The current i_{C1}, which is flowing through C_{oss1} of S_1, is $i_L * C_{oss1}/(C_{oss1} + C_{oss2})$.

Stage 5 (t_4–t_5): At t_4, when v_{ds2} decreases to zero or valley, S_2 turns ON and the resonance ends. The inductance current increases until it returns back to zero again at t_5.

After t_5, another switching cycle begins. During one switching cycle, the body diode's reverse recovery and the resonance process affect the switching period significantly, which results in large variations of peak current and switching frequency compared to ideal design model. In order to carry out the accurate analysis of the switching cycle, the reverse recovery process will be analyzed in detail in the following sections.

B. Analytical Model for Reverse Recovery Stage

In order to predict the reverse recovery behavior of diodes, Dr. B. Jayant Baliga proposed a ramp-recovery analytical model in [15]. According to this simple physical model, the charge density (q_R) during stage 3 (t_2–t_3) can be obtained by the following equation:

$$q_R = \frac{1}{2}\frac{L_a}{M \cdot d - L_a}\frac{J_{\text{ppk}}^2}{a} \tag{1}$$

where J_{ppk} is the forward current density, a is the ramp rate of current density, L_a is the ambipolar diffusion length, d is the half of width of drift region, and $M = \frac{\cosh(-d/L_a)}{\sinh(d/L_a)} - \frac{\sinh(-d/L_a)}{\cosh(d/L_a)}$.

Because q_R and J_{ppk} are impossible to measure for power supply engineers, it should be replaced by the charge Q_R and the current I_{ppk}. Then, (1) can be rewritten as

$$Q_R = \frac{1}{2}\frac{L_a}{M \cdot d - L_a}\frac{I_{\text{ppk}}^2}{k} \tag{2}$$

where I_{ppk} is the positive peak value of inductance current, and k is the slope of inductance current shown in Fig. 2 ($k = (V_o – V_{in})/L$).

In a BCM boost converter, the charge Q_R is the area enclosed by i_L and the time axis from t_2 to t_3 in Fig. 2, and it can be calculated as

$$Q_R = \frac{1}{2}T_c I_R = \frac{1}{2}kT_c^2 \tag{3}$$

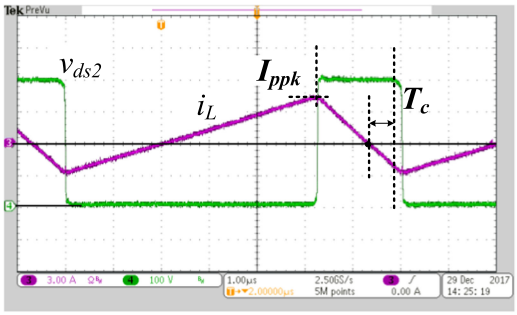

Fig. 3. Measured inductance current i_L and voltage v_{ds2} in a BCM boost prototype with IPL60R065C7 [16] (@100 V_{in} and 400 V V_o).

where I_R is the reverse current value when v_{ds2} begins to decrease. Then, by substituting (3) into (2), the time slot T_c (defined in Fig. 2) can be derived as

$$T_c = \sqrt{\frac{L_a}{M.d - L_a}} \frac{I_{\text{ppk}}}{k} = A_{QR} \frac{I_{\text{ppk}}}{k}. \tag{4}$$

Because parameters L_a and d still cannot be obtained from datasheet of MOSFET, $\sqrt{\frac{L_a}{M.d-L_a}}$ is considered as a virtual coefficient A_{QR} in this letter, which depends on the characteristics of the switch. After T_c is obtained, the current value I_R can be calculated in (5), where the current slope is assumed to be the same as that of stage 2

$$I_R = \frac{V_o - V_{\text{in}}}{L} T_c \tag{5}$$

where V_{in} is the input voltage, and V_o is the output voltage.

In above calculating procedure, A_{QR} is the key variable, which depends on the MOSFET. By measuring the I_{ppk} and T_c at a different k, namely different input and output voltages and inductance values, many discrete values of A_{QR} can be obtained from (4). In order to obtain the coefficient A_{QR} for a given MOSFET, the curve fitting method according to (4) is adopted to derive a formula of A_{QR} in the function of k.

First, a preliminary boost prototype is needed to generate the T_c with the given MOSFET and an inductance value derived from the ideal operating mode. The inductance current and the drain to source voltage of switch (v_{ds2}) can be measured by an oscilloscope shown in Fig. 3, and the positive peak value I_{ppk} can be measured from the inductance current waveform. Because T_c is corresponding to the starting point of the falling of v_{ds2}, it can be measured from the zero crossing of the inductance current to the starting point of falling behavior of v_{ds2}. Fig. 4(a) shows the measured T_c values at different peak currents with certain inductance (100 μH), input voltage (100 V), and output voltage (400 V). By curve fitting, the slope of solid line in Fig. 4(a) represents the A_{QR}/k under 100 V voltage condition. Because k is not constant in a PFC application, more T_c values at different k are needed to generate the relationship between A_{QR} and k.

Second, with the same prototype, T_c and I_{ppk} at different input voltages are measured and plotted in Fig. 4(b)–(d). The predicted T_c values with the A_{QR} calibrated at 100 V_{in} are also plotted

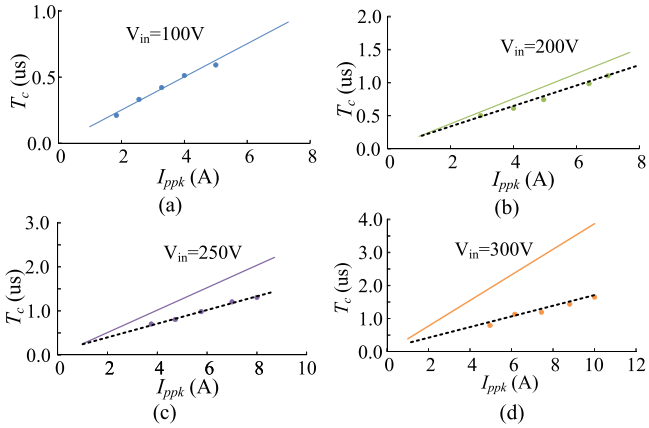

Fig. 4. Relationship between T_c and I_{ppk} at different V_{in} (IPL60R065C7) with the same $L = 100\,\mu$H and $V_o = 400$ V. (a) $V_{\text{in}} = 100$ V ($k = 3$). (b) $V_{\text{in}} = 200$ V ($k = 2$). (c) $V_{\text{in}} = 250$ V ($k = 1.5$). (d) $V_{\text{in}} = 300$ V ($k = 1.0$).

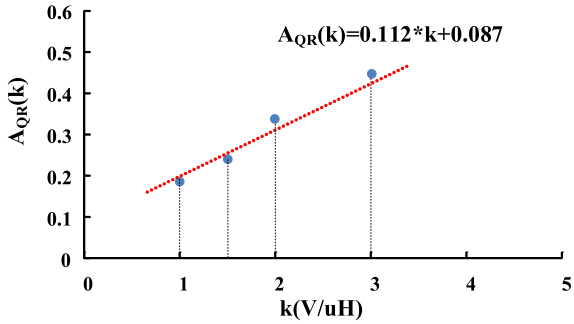

Fig. 5. Calibrated relationships between A_{QR} and k. (MOSFET: IPL60R065C7; $L = 100\,\mu$H).

by solid curves under other input voltages. It can be found that either the measured or predicted T_c is almost in proportional to the peak current I_{ppk} with the given input voltage, which means A_{QR} is almost constant under certain input and output voltages, namely certain k. But at higher input voltages in Fig. 4(b)–(d), the measured points of T_c (dash lines) are quite different to the predicted values (solid lines), which were calculated with the A_{QR} obtained at 100 V_{in}. Obviously, the value of A_{QR} obtained at 100 V input cannot represent itself in a whole input voltage range.

Fortunately, from the measured operating points in Fig. 4, a further calibration by curve fitting for $A_{QR}(k)$ can be made. In fact, the A_{QR} is influenced by the current slope k according to the physics model. Because k equals $(V_o – V_{\text{in}})/L$ with certain V_o, based on the slopes of dashed line generated by curve fitting in Fig. 4, the coefficient A_{QR} in function of k can be depictured in Fig. 5 and derived in (6) by curve fitting

$$A_{QR}(k) = 0.112 * k + 0.087. \tag{6}$$

For different MOSFETs, above calibration and curve fitting procedure can be repeated to derive the coefficient in function $A_{QR}(k)$.

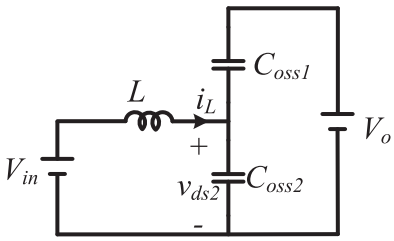

Fig. 6. Equivalent circuit in resonance process.

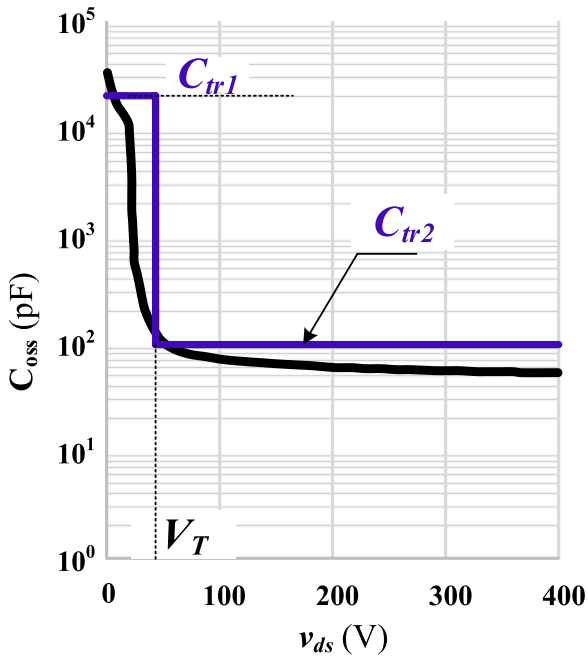

Fig. 7. Output junction capacitor of MOSFET [16], [17].

C. Analytical Analysis of Resonance Stage

When the v_{ds2} beings to decrease at t_3, the equivalent circuit of this stage is shown in Fig. 6. Because the output junction capacitance is nonlinear, a piecewise time-equivalent output junction capacitance [17] shown in Fig. 7 is used to calculate the whole stage 4 from t_3 to t_4. When the voltage v_{ds2} changes from zero to the threshold voltage V_T, the time-equivalent output junction capacitance C_{tr1} is used; from V_T to V_o, C_{tr2} is used, where C_{tr2} is much larger than C_{tr1}. Therefore, the resonance stage can be divided into three substages. At the first substage (t_3–t_{3-1}), v_{ds2} decreases from V_o to (V_o–V_T), and the equivalent capacitance C_{eq} is $(C_{tr1}+C_{tr2})$. At the second substage (t_{3-1}–t_{3-2}), v_{ds2} decreases from (V_o–V_T) to V_T, and the equivalent capacitance C_{eq} is $2*C_{tr2}$. At the third substage (t_{3-2}–t_4), voltage v_{ds2} decreases from V_T to 0 V, and the equivalent capacitance C_{eq} is also $(C_{tr1}+C_{tr2})$. Because the equivalent capacitance C_{eq} in the second substage is much less than that in other two substages, the time slot of the second substage is short enough to be ignored. And the inductance current does not almost change in the second substage. Hence, the inductance current after the first substage can be considered as the negative peak value I_{npk}. Then, the time slot T_d of the first substage can be calculated as

$$T_d \approx \frac{1}{\omega_r}\left[\sin^{-1}\frac{V_o - V_{\text{in}}}{\sqrt{(V_o - V_{\text{in}})^2 + (I_R Z_L)^2}} - \sin^{-1}\frac{V_o - V_T - V_{\text{in}}}{\sqrt{(V_o - V_{\text{in}})^2 + (I_R Z_L)^2}}\right]. \tag{7}$$

By assuming that the decreasing rate of inductance current is almost $(V_o$–$V_{\text{in}})/L$ from t_3 to t_{3-1}, the negative peak current can be calculated as

$$I_{\text{npk}} = \frac{V_o - V_{\text{in}}}{L}(T_c + T_d) \tag{8}$$

where T_c and T_d are both functions of I_{ppk} based on the above analysis.

In order to calculate the I_{ppk} and I_{npk}, simultaneously, another formula about I_{ppk} and I_{npk} is needed. Because the input current is the average value of inductance current in a switching period, another equation between I_{ppk} and I_{npk} can be obtained approximately in the following equation:

$$I_{\text{ppk}} = 2 \cdot I_{\text{in}} - I_{\text{npk}}. \tag{9}$$

By combining (4), and (7)–(9), the I_{ppk} and I_{npk} can be derived. The switching frequency can be calculated after I_{ppk} and I_{npk} are obtained. Then, based on the definitions of time slots in Fig. 2, the time period of each stage can be calculated as

$$T_a = \frac{I_{\text{ppk}}}{\frac{V_{\text{in}}}{L}} \tag{10}$$

$$T_b = \frac{I_{\text{ppk}}}{\frac{V_o - V_{\text{in}}}{L}} \tag{11}$$

$$T_c + T_d = \frac{I_{\text{npk}}}{\frac{V_o - V_{\text{in}}}{L}}. \tag{12}$$

By assuming that the inductance current slope from t_{3-2} to t_5 is V_{in}/L, the time slot T_e can also be calculated approximately

$$T_e \approx \frac{I_{\text{npk}}}{\frac{V_{\text{in}}}{L}}. \tag{13}$$

Then, the switching frequency can be obtained as

$$f_s = \frac{1}{T_a + T_b + T_c + T_d + T_e}. \tag{14}$$

D. Analytical Analysis of the PFC Application

In a totem-pole boost PFC converter, the input voltage v_{ac} is sinusoidal in the following equation:

$$v_{\text{ac}}(\theta) = \sqrt{2} V_{\text{rms}} \sin\theta \tag{15}$$

where V_{rms} is the rms value of input voltage. Assuming that the output power is almost constant P_o and the efficiency is η, the

ac input current I_{in} can be obtained as

$$I_{\text{in}}(\theta) = \sqrt{2}\frac{P_o}{\eta V_{\text{rms}}}\sin\theta. \tag{16}$$

Because the switching frequency is much higher than the line frequency, the input voltage and current can be considered as dc in a switching cycle. Therefore, the positive and negative peak values of inductance current during the line period can be obtained in (17) and (18), respectively

$$I_{\text{ppk}}(\theta) = 2 \cdot I_{\text{in}}(\theta) - I_{\text{npk}}(\theta) \tag{17}$$

$$I_{\text{npk}}(\theta) = \frac{V_o - v_{\text{ac}}(\theta)}{L}\left[T_c(\theta) + T_d(\theta)\right]. \tag{18}$$

Then, the switching frequency in the half line cycle can be obtained as

$$f_s(\theta) = \frac{1}{\frac{I_{ppk}(\theta)-I_{npk}(\theta)}{\frac{v_{ac}(\theta)}{L}} + \frac{I_{ppk}(\theta)-I_{npk}(\theta)}{\frac{V_o-v_{ac}(\theta)}{L}}} \tag{19}$$

It should be noted that although the peak values I_{ppk} and I_{npk} can be obtained from (4), (7), (17), and (18), the analytical solution for the peak current values is still difficult. Therefore, in the experimental verification results in Section III, the calculated peak current values are obtained by substituting the given points into these equations.

III. Experimental Verifications in a PFC Prototype

In order to verify the above analysis, a BCM totem-pole boost PFC prototype was fabricated. The ac input voltage is from 200 V_{ac} to 250 V_{ac}. The output is 400 V_{dc}. The rated power is 600 W and the MOSFETs are the same as the example in the A_{QR} calibration. The inductance value can be obtained from the following steps.

Step 1: In order to match the expected minimum frequency 90 kHz at the peak of 220 V_{ac} input, the minimum frequency and corresponding input voltage can be substituted into (19), where θ is $\pi/2$.

Step 2: By substituting input voltage 220 V_{ac} into (17) and (18), expressions for I_{ppk} and I_{npk} are obtained.

Step 3: Then, substituting (4) and (7) into (18), three equations with three variables (L, I_{ppk}, and I_{npk}) can be obtained.

Step 4: By a mathematics software (Mathcad), the expected inductance value can be calculated and is about 70 μH for the given Specs.

Then, the I_{ppk}, I_{npk}, and f_s can be calculated at any operating point according to the aforementioned steps.

According to the calculated inductance and peak currents, the inductor can be designed. The peak efficiency of the prototype is 98.7% without considering the driving and filter losses. The measured key waveforms are shown in Fig. 8 with half load and in Fig. 9 with full load, respectively.

In Fig. 10, the calculated and experimental peak currents are compared. It can be seen that the calculated peak currents according to the proposed analytical reverse recovery model are consistent with the measured peak values at different power levels. Meanwhile, the predicted results by ideal model [8] and

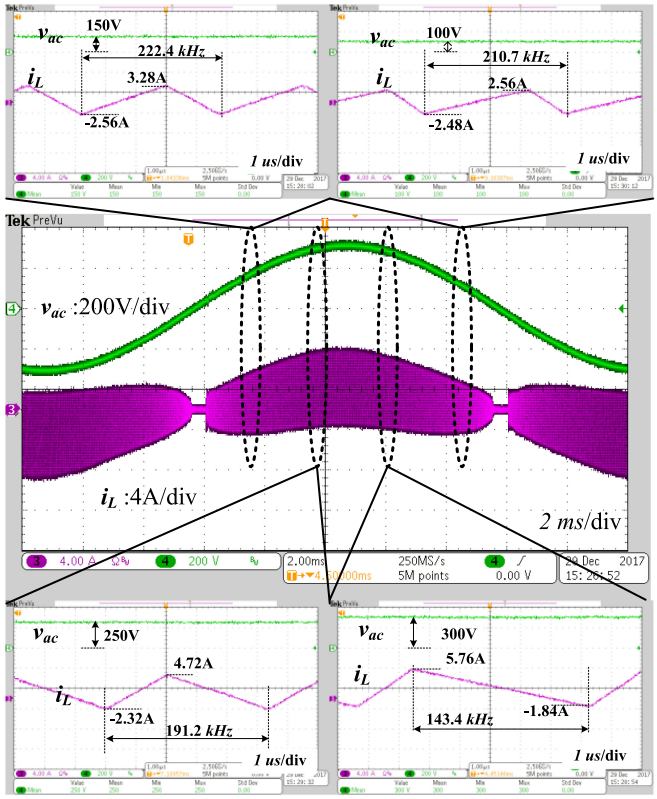

Fig. 8. Experiment waveform at 220 V_{ac}/ 300 W.

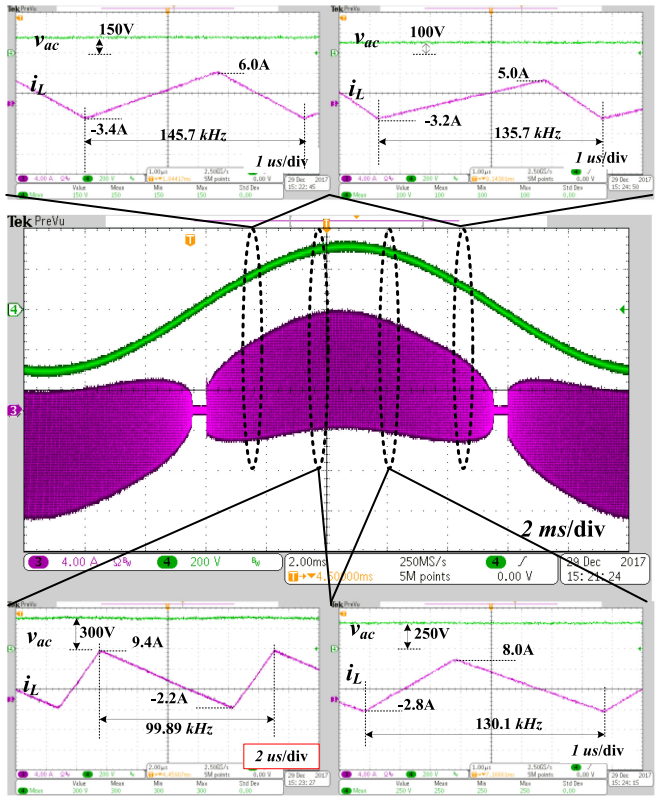

Fig. 9. Experiment waveform at 220 V_{ac}/ 600 W.

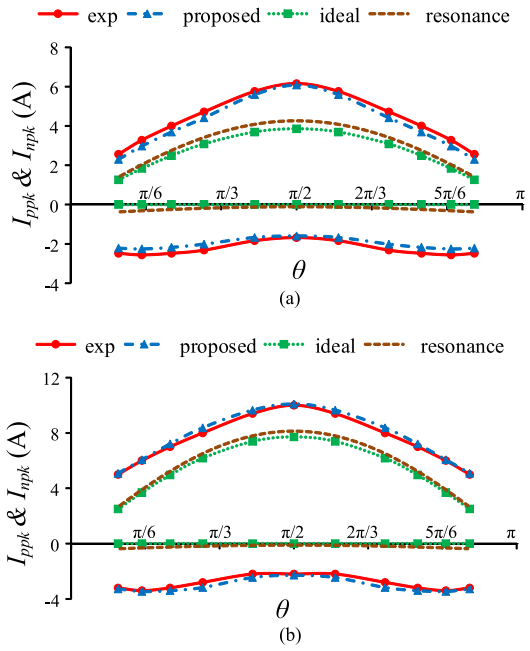

Fig. 10. Inductor current of experiment, ideal model, and proposed model. (a) 300-W output power. (b) 600-W output power.

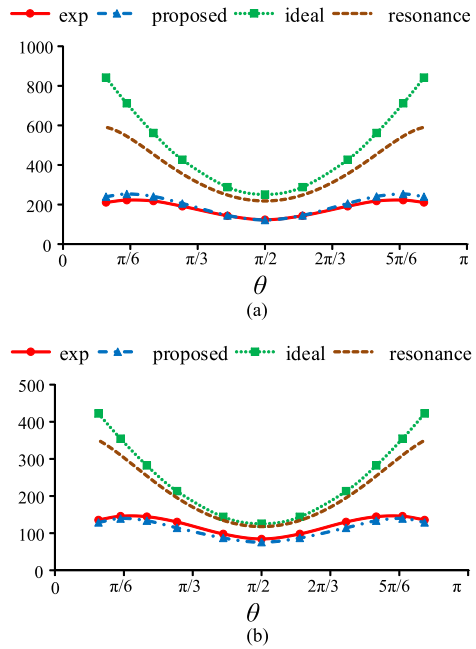

Fig. 11. Switching frequency ranges of experiment, ideal model, and proposed model. (a) 300-W output power. (b) 600-W output power.

resonance model [9] deviate to the experimental results seriously. The serious reverse recovery of MOSFET's body diode makes the peak current value of the inductance higher than that of the ideal model and resonance model apparently, which influences the design of the magnetic component.

The switching frequency ranges in half line cycle between the calculated and experimental results are compared in Fig. 11. It also illustrates that the proposed analytical switching cycle operating analysis is much more accurate than the ideal model.

IV. Conclusions

This letter proposes accurate analytical reverse recovery model of the body diode and switching cycle operating analysis for the BCM totem-pole boost PFC converter with body diode freewheeling control. With the proposed model, the accuracy of the predicted switching frequency and inductance current is improved significantly compared to that with the conventional ideal model. In the experimental verifications, the measured switching frequencies and peak currents are close to the predicted results with the proposed model. The proposed analytical analysis model can be used as an accurate design guideline for the inductor and the electromagnetic interference filter in a BCM totem-boost PFC converter.

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