

Accuracy Analysis of the Zero-Order Hold Model for Digital Pulse Width Modulation

Junpeng Ma^{1b}, *Student Member, IEEE*, Xiongfei Wang^{1b}, *Senior Member, IEEE*, Frede Blaabjerg^{2b}, *Fellow, IEEE*, Lennart Harnefors^{1b}, *Fellow, IEEE*, and Wensheng Song^{1b}, *Member, IEEE*

Abstract—This paper analyzes the accuracy of the zero-order hold (ZOH) model for the digital pulse width modulator (DPWM) in the s -domain. The s -domain model and the exact z -domain model for the current control of a single-phase inverter with an L -type filter are elaborated for quantifying the deviation of the ZOH model for the DPWM. The influences of the different computational delay and duty-cycle update modes on this deviation is analyzed in detail. The compensation method for this deviation of the ZOH model is proposed for accurately predicting the stability region of the control system in the s -domain. Simulations and experimental tests are executed to verify the effectiveness and correctness of the theoretical analysis.

Index Terms—Compensation method, digital pulse width modulator (DPWM), model accuracy, stability analysis, zero-order hold (ZOH).

I. INTRODUCTION

THE stability analysis of pulse width-modulated (PWM) converters has attracted significant attentions recently [1]. The current control loop is the innermost and fastest loop of the cascaded control loops, which are typically used in a converter control system. The proportional gain of the current controller determines the bandwidth of the current control loop [2], i.e., a large gain gives a high bandwidth and consequently a fast transient response of the current. This is important, e.g., for fault ride through [3], [4]. Yet, the proportional gain cannot be made so high that the stability of the current control loop is jeopardized. The upper limit of the proportional gain is dependent on how the PWM is implemented and the resulting total computational delay of the current controller [5].

Manuscript received July 6, 2017; revised December 1, 2017; accepted January 22, 2018. Date of publication January 30, 2018; date of current version September 28, 2018. This work was supported in part by the National Natural Science Foundation of China under Project 51577160, in part by European Research Council (ERC) under the European Union's Seventh Framework Program (FP/2007-2013)/ERC Grant Agreement [321149-Harmony], in part by the Doctoral Innovation Foundation of Southwest Jiaotong University, and in part by China Scholarship Council. Recommended for publication by Associate Editor R. Zane. (*Corresponding author: Xiongfei Wang.*)

J. Ma and W. Song are with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 610031, China (e-mail: junpeng_ma@163.com; songwsh@swjtu.edu.cn).

X. Wang and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: xwa@et.aau.dk; fbl@et.aau.dk).

L. Harnefors is with ABB Corporate Research, Vasteras 72178, Sweden (e-mail: lennart.harnefors@se.abb.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2018.2799819

The Digital PWM (DPWM) is widely used in power converters to generate switching pulses with a constant frequency. The duty cycle is updated once or twice per switching period at the peak and/or the valley of the triangular carrier, which are known as single- and double-update modes [6]. Meanwhile, the current and voltage are also sampled at the peak and/or the valley of the triangular carrier to avoid sampling harmonics due to the switching event [7]. In the case of this sampling and duty-cycle update mode, the grid-connected converter with the digital controller can be exactly modeled in the z -domain [8], and the digital controller parameters can be designed accordingly. However, the analysis of the control system in the z -domain requires a uniform sampling/duty cycle update frequency [9], which means that the z -domain model is not suitable for analyzing the network of multiple grid-connected converters with different sampling/switching frequencies. Moreover, for the future power-electronic-based power systems [6], the discrete z -domain model of converters is not readily compatible with the continuous dynamic behavior of electric power networks. Therefore, the continuous s -domain model of converters and, particularly, the accurate model of the sampling process and the DPWM are critical for the stability analysis and control of the future converter-based power systems.

In the DPWM process, there is a time delay between the instant of updating the reference signal and the instant when the switching event occurs. However, this time delay, and the PWM delay, are in some cases, neglected for simplification, i.e., the DPWM is modeled as a unity gain [10], [11], which can lead to the inaccurate/conservative design of the controller. In order to accurately predict the stability region of the control system, various models of DPWM have been proposed based on different methods. The DPWM can be taken into account by modeling it as a duty cycle-dependent transfer function by using the small-signal analysis [12]. However, this model can only be adopted for dc/dc converters in the steady-state operating point and is not readily applicable for grid-connected converters. Consequently, a simplified and universal model that considers the DPWM as a half-switching-period delay is reported [6], which can be further simplified by using a Padé approximation if found convenient [13], [14]. Yet, there exists a difference between this approximated model and the actual process of DPWM, especially for power converters with a low pulse ratio, i.e., the ratio of switching to fundamental frequency. A zero-order hold (ZOH) model improves the accuracy compared to the time-delay and Padé-approximation models [15]. Although a better

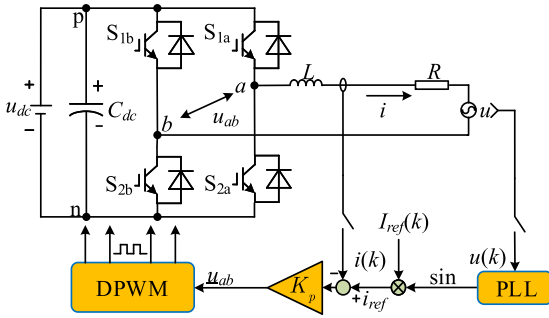


Fig. 1. Single-phase VSC with a proportional current controller.

accuracy is obtained, this paper shows that the ZOH model is still an approximation of the DPWM, and the compensation of the ZOH model deviation is necessary for accurately analyzing and designing the controller in the s -domain.

In the process of the sampling in the digital control system, the voltage and current signal need to be sampled ahead of the duty-cycle updating instant for avoiding any duty-cycle limitation [16]. This sampling process consequently introduces an extra delay, named as computational delay, which also affects the phase margin [17], especially for converters with a low sampling frequency [18]. Shifting the sampling instant toward the duty-cycle update instant provides a way to increase the bandwidth of the closed-loop system [19], [20]. Yet, such a shift of the sampling instant tends to introduce low-order current harmonics [9] and the fractional delay, which complicates the dynamic analysis of the control system. These effects are less adverse when the interval between the sampling instant and the duty-cycle-updating instant is much smaller than the switching period [21]. Consequently, this method is usually used in high-power converters with a low switching frequency [22]. As the reduction of the computational delay, the model accuracy of the DPWM plays a dominant role in the analysis of the stability region of the control system.

This paper evaluates first the accuracy of the ZOH model for the DPWM with the different computational delay and duty-cycle update modes, and then the compensation method for this equivalent model is proposed to accurately predict the stability region of the control system in the s -domain. The rest of this paper is organized as follows: Section II describes a single-phase voltage-source converter (VSC) with an inductance (L) filter. The ZOH model of the DPWM and the z -domain representation for the control loop discretized by the forward difference is explicitly identified. In Section III, the deviation of the equivalent ZOH model for DPWM is analyzed and a compensation method for the ZOH model is proposed and discussed, considering the different duty-cycle update modes and the computational delay. In Section IV, an experimental verification is carried out to confirm the effectiveness of the theoretical analysis. Section V concludes this paper.

II. CONTROL SYSTEM MODELS

A. System Description

Fig. 1 illustrates a single-phase L -filtered VSC, where u_{ab} and i are the converter output voltage and current, respectively, and u

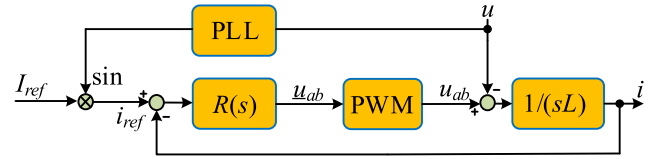


Fig. 2. Block diagram of the control loop with a proportional gain current controller.

represents the grid voltage. L and R are the filter inductance and resistance, respectively. For simplicity, a proportional current controller is considered to examine the stability region of the current loop.

The grid voltage u and the line current i in the static reference frame are defined as follows:

$$u = u_m \sin(\omega_0 t) \quad (1)$$

$$i = i_m \sin(\omega_0 t + \varphi_i). \quad (2)$$

Kirchhoff's voltage law is used to analyze the voltage across the inductor L . The voltage equation is

$$L \frac{di}{dt} = u - u_{ab}. \quad (3)$$

Therefore, the block diagram of the control loop with the current regulator $R(s)$ can be drawn in Fig. 2.

In this paper, the proportional gain K_p is applied in the current regulator. Without considering the dynamics of the DPWM and computational delay effect, the open-loop transfer function of the current loop is given as

$$G_o(s) = \frac{K_p}{sL}. \quad (4)$$

The closed-loop transfer function can be expressed as

$$G_{c1}(s) = \frac{G_o(s)}{1 + G_o(s)} = \frac{K_p}{sL + K_p}. \quad (5)$$

It is clear that the control system remains stable provided that K_p is positive. However, K_p is practically limited by aforementioned DPWM dynamics and computational delay [23].

B. ZOH Model for DPWM

The DPWM with the different duty-cycle update modes and computational delay are illustrated in Fig. 3, where T_{cp} is the computational duration of the control algorithm, and the duty cycle needs to be calculated before next duty-cycle update instant. Therefore, the sampling instant and duty-cycle computation should happen at least one computational duration in advance of the next duty-cycle update instant. Normally, the sampling instant occurs one sampling interval in advance of the duty-cycle update instant as shown in Fig. 3(a) and (b). Furthermore, the sampling instant can be shifted toward the next sampling instant to reduce the time delay. Due to the performance improvement of the microcontroller, the computational duration T_{cp} has been reduced dramatically, and the computational delay T_d between the sampling instant and the duty-cycle-updating instant can thus be set near to zero, as shown in Fig. 3(c) and (d). Moreover, to further reduce the time delay,

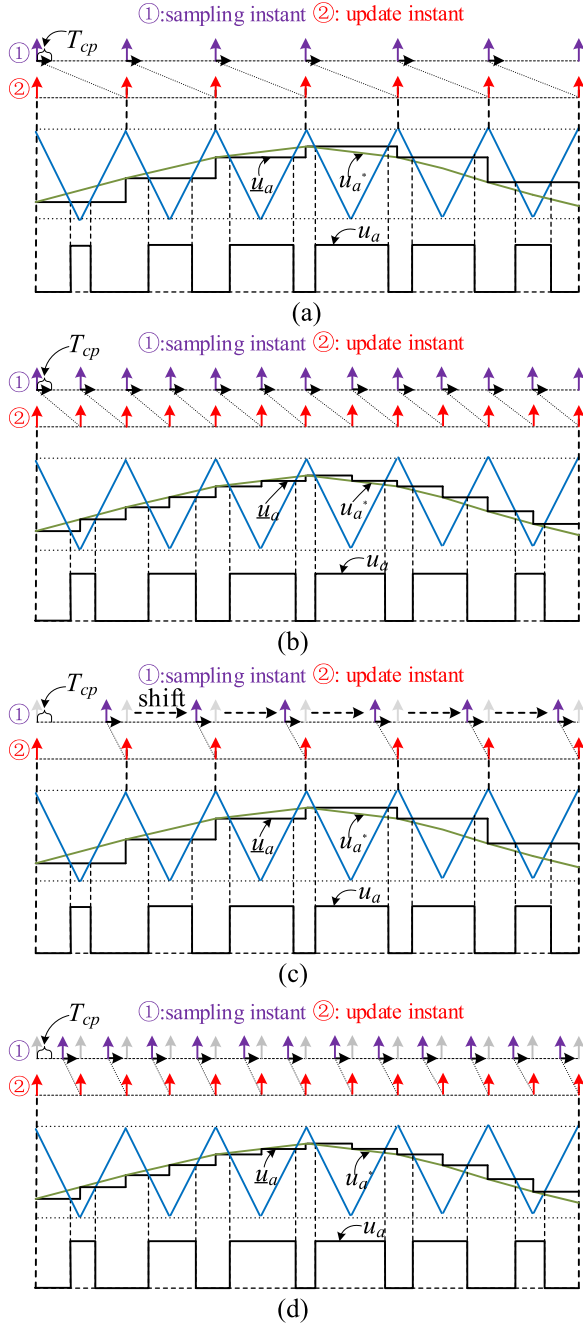


Fig. 3. DPWM with different update modes and computational delay. (a) Single update with one-step delay, (b) double update with one-step delay, (c) single update with a small computational delay, and (d) double update with a small computational delay.

the double-update mode is usually applied in DPWM shown in Fig. 3(b) and (d).

In Fig. 3, u_a^* is the ideal output voltage for the phase a of the converter. \underline{u}_a is the discrete form of u_a^* by the ZOH. u_a^* and \underline{u}_a can be expressed as

$$\begin{cases} u_a^* = -u_b^* = \frac{u_{ab}^*}{2} \\ \underline{u}_a = -\underline{u}_b = \frac{u_{ab}}{2} \end{cases} \quad (6)$$

where u_{ab}^* is the ideal output voltage of the converter. \underline{u}_{ab} is the discrete form of u_{ab}^* by the ZOH, which is calculated by the current regulator. u_b^* is the ideal output voltage for the phase b of the converter. \underline{u}_b is the discrete form of u_b^* by the ZOH.

In Fig. 3, \underline{u}_a is compared to the triangular carrier to generate the actual output voltage u_a for the phase a of the converter, which guarantees the area equivalence, that is

$$\underline{u}_a(k)T_h = \int_{kT_h}^{(k+1)T_h} u_a dt \quad (7)$$

where T_h is the duty-cycle update period, which is also the period of the ZOH.

The output voltage for the phase b also satisfies

$$\underline{u}_b(k)T_h = \int_{kT_h}^{(k+1)T_h} u_b dt. \quad (8)$$

According to (3), (6)–(8), the sampled current satisfies

$$\begin{aligned} i(k+1) &= i(k) + \frac{1}{L} \int_{kT_h}^{(k+1)T_h} u_{ab} dt - \frac{1}{L} \int_{kT_h}^{(k+1)T_h} u dt \\ &= i(k) + \frac{1}{L} \int_{kT_h}^{(k+1)T_h} (u_a - u_b) dt - \frac{1}{L} \int_{kT_h}^{(k+1)T_h} u dt \\ &= i(k) + \frac{1}{L} \underline{u}_{ab}(k)T_h - \frac{1}{L} \int_{kT_h}^{(k+1)T_h} u dt. \end{aligned} \quad (9)$$

The current dynamics caused by the signal \underline{u}_{ab} is different from the one caused by the actual output voltage u_{ab} within one switching interval. But at the duty-cycle update instant, the sampled current controlled by u_{ab} is equal to that controlled by \underline{u}_{ab} according to (9). Hence, the ZOH can be applied to model the DPWM process. The transfer function of the ZOH is given as

$$G_{zoh}(s) = \frac{1 - e^{-T_h s}}{T_h s}. \quad (10)$$

The open-loop transfer function with the ZOH model for the DPWM and the computational delay can be expressed as

$$G_{os}(s) = R(s)G_d(s)G_{zoh}(s)P_s(s) = K_p e^{-T_d s} \frac{1 - e^{-T_h s}}{T_h s} \frac{1}{sL} \quad (11)$$

where $G_d(s) = e^{-T_d s}$ represents the computational delay transfer function. $P_s(s)$ is the s -domain transfer function of the model for the single-phase inverter with L filter. By using the model shown in (11), the control system can be easily analyzed in the s -domain.

C. Discrete Control System Model

According to (9), the discrete current at the duty-cycle update instant satisfies

$$\frac{i(k+1) - i(k)}{\underline{u}_{ab}(k)} = \frac{T_h}{L} - \frac{1}{L\underline{u}_{ab}(k)} \int_{kT_h}^{(k+1)T_h} u dt. \quad (12)$$

Based on (12), the z -domain open-loop transfer function with the one-step delay can be expressed as

$$G'_{oz}(z) = R(z)G_{dz}(z)P_z(z) = z^{-1} \frac{T_h K_p}{(z-1)L} \quad (13)$$

where $P_z(z)$ is the z -domain transfer function of the control system without the computational delay. A fractional order delay is introduced into the transfer function of the control system if the sampling instant is shifted toward the duty-cycle update instant shown in Fig. 3(c) and (d). The z -domain open-loop transfer function is in this case expressed as

$$G_{oz}(z) = R(z)G_{dz}(z)G_{inv}(z) = \left\{ 1 - \frac{T_d}{T_h} + \frac{T_d}{T_h} z^{-1} \right\} \frac{T_h K_p}{(z-1)L}. \quad (14)$$

It is clear that (14) is equal to (13) if $T_d = T_h$. If $T_d \ll T_h$, that is

$$\frac{T_d}{T_h} \ll 1 \quad (15)$$

which implies that computational delay can be neglected.

The z -domain model shown in (13) is directly derived from (9), which is an accurate discrete description of the converter with L filter modulated by DPWM [8]. Therefore, this z -domain model can accurately describe the dynamics of the control system.

III. ACCURACY OF THE ZOH MODEL FOR DPWM

A. Deviation of the DPWM Model

The ZOH transfer function given in (10), can be expressed as an integrator subtracting a delayed integrator as

$$G_{zoh}(s) = \frac{1}{T_h} \left\{ \frac{1}{s} - \frac{1}{s} e^{-T_h s} \right\}. \quad (16)$$

According to (16), the output of the ZOH with a sinusoidal input is a cosine and a cosine with delay, that is

$$\begin{aligned} Y_{zoh}(t) &= \mathcal{L}^{-1} \{ G_{zoh}(s) \mathcal{L}[\sin(\omega t)] \} \\ &= \frac{1}{\omega T_h} [\cos(\omega t) - \cos(\omega t - \omega T_h)] \\ &= \frac{1}{T_h} \int_{t-T_h}^t \sin(\omega t) dt. \end{aligned} \quad (17)$$

It is clear from (17) that for any sinusoidal input, the output of the ZOH model is the average of the input signal within the time interval $t - T_h$ to t . On the other hand, due to \underline{u}_{ab}^* formed from u_{ab}^* by the ZOH as shown in Fig. 3, the average output of the DPWM is equal to u_{ab}^* expressed by (7), which is the average of the rectangular integral shown in Fig. 4. Therefore, there exists the deviation between the ZOH model for DPWM and actual modulating process, and this deviation is illustrated in Fig. 4. This deviation for a low-frequency modulating wave (high pulse ratio) shown in Fig. 4(a) is smaller than that for a high-frequency modulating wave (low pulse ratio); it means that this ZOH model for DPWM is not suitable for analyzing the control system in the high-frequency domain.

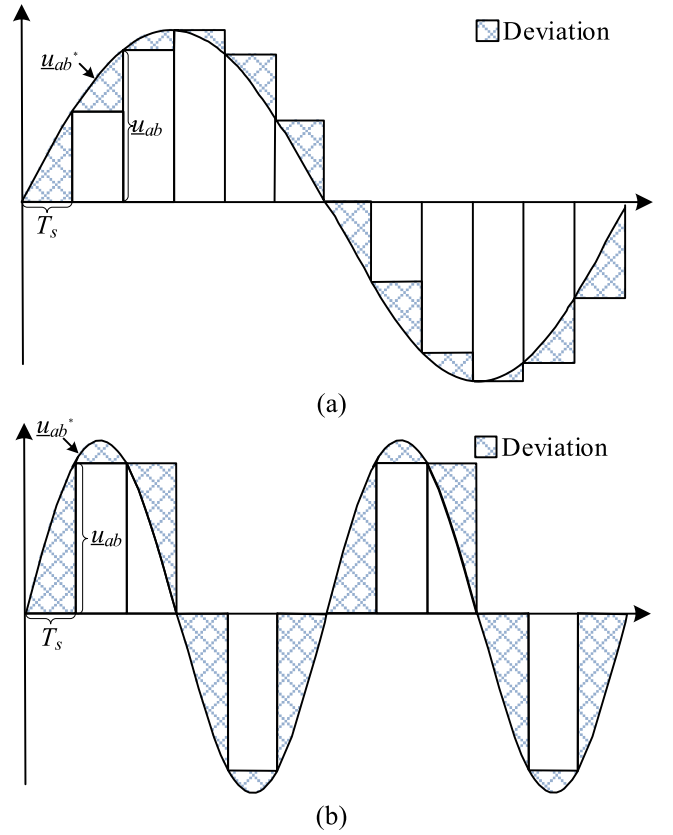


Fig. 4. Deviation of the ZOH model. (a) High carrier–fundamental frequency ratio and (b) low carrier–fundamental frequency ratio.

Therefore, the model of the control loop with the ZOH model will lead to an inaccurate stability criterion for the current controller. In contrast, the control system model given in (14) is directly discretized based on (9) and (12) using the forward difference, which accurately models the dynamic characteristic of the control system.

According to the s -domain transfer function shown in (11), the frequency response function of control loop with ZOH model below the Nyquist frequency is given as

$$\begin{aligned} G_{os}(j\omega) &= \frac{1 - e^{-T_h j\omega}}{j\omega T_h} \frac{K_p}{j\omega L} e^{-j\omega T_d} \\ &= \frac{K_p}{\omega L} \left| \frac{\sin(\omega T_h/2)}{\omega T_h/2} \right| e^{j\left(-\frac{\pi}{2} - \frac{\omega T_h}{2} - j\omega T_d\right)}. \end{aligned} \quad (18)$$

Similarly, based on the z -domain transfer function shown in (14), the frequency response function of the discrete model is expressed as

$$\begin{aligned} G_{oz}(e^{j\omega T_h}) &= \left(1 - \frac{T_d}{T_h} + \frac{T_d}{T_h} e^{-j\omega T_h} \right) \frac{T_h K_p}{(e^{j\omega T_h} - 1)L} \\ &= \left\{ \left(1 - \frac{T_d}{T_h} \right) + \frac{T_d}{T_h} e^{-j\omega T_h} \right\} \frac{T_h}{2L} \frac{K_p}{|\sin(\omega T_h/2)|} e^{j\left(-\frac{\pi}{2} - \frac{\omega T_h}{2}\right)}. \end{aligned} \quad (19)$$

The deviation of the s -domain transfer function with the ZOH equivalent model can be defined as

$$D(\omega) = \frac{G_{oz}(e^{j\omega T_h})}{G_{os}(j\omega)} = \left\{ \frac{\omega T_h/2}{\sin(\omega T_h/2)} \right\}^2 \left\{ \left(1 - \frac{T_d}{T_h}\right) e^{j\omega T_d} + \frac{T_d}{T_h} e^{j\omega(T_d - T_h)} \right\}. \quad (20)$$

The same methodology can be applied for analyzing the deviation of the s -domain transfer function with the ZOH equivalent model for different converter types and current controllers. The difference is the value of the deviation in (20).

B. Compensation for the DPWM Model

It can be seen from (20) that there is an obvious deviation of the frequency response between the accurate z -domain model in (19) and the s -domain transfer function with the ZOH model in (18), which needs to be compensated to obtain an accurate frequency response of the control loop in the s -domain. When $T_d \ll T_h$, the term of the last bracket in (20) can be simplified as

$$\begin{aligned} & \left(1 - \frac{T_d}{T_h}\right) e^{j\omega T_d} + \frac{T_d}{T_h} e^{j\omega(T_d - T_h)} \\ & \approx 1 + \frac{T_d}{T_h} [1 - \cos(\omega T_h)] + j \frac{T_d}{T_h} [\omega T_h - \sin(\omega T_h)] \approx 1 \end{aligned} \quad (21)$$

$D(j\omega)$ in (20) thereby can be simplified and the compensation coefficient is defined as

$$k_{\text{comp}}(\omega) = D(j\omega) \approx \left\{ \frac{\omega T_h/2}{\sin(\omega T_h/2)} \right\}^2. \quad (22)$$

It is deduced from (21) and (22) that when $T_d \ll T_h$, there is no phase deviation between the s -domain model and z -domain model. But the gain deviation still exists. Therefore, the proportional gain K_p should be compensated by (22), and the compensated gain K_{pc} for the s -domain model can be expressed as

$$K_{pc} = K_p / k_{\text{comp}}. \quad (23)$$

Based on (18), the phase crossover frequency f_{cro} satisfies

$$-\pi/2 - 2\pi f_{\text{cro}} T_h/2 - 2\pi f_{\text{cro}} T_d = -\pi. \quad (24)$$

f_{cro} can be solved from (24) as

$$f_{\text{cro}} = \frac{1}{2(T_h + 2T_d)}. \quad (25)$$

When $T_d = T_h$, f_{cro} satisfies

$$f_{\text{cro}} = \frac{1}{6T_h} = \begin{cases} \frac{1}{6} f_{\text{sw}} & \text{(single update)} \\ \frac{1}{3} f_{\text{sw}} & \text{(double update)} \end{cases} \quad (26)$$

TABLE I
SYSTEM PARAMETERS

Parameters	Value
The grid voltage u/Vrms	220
The frequency of the grid voltage f/Hz	50
DC-link-rated voltage	600
Sampling frequency f_{sw}/kHz	5
AC-side inductor L/mH	12

where f_{sw} is the switching frequency. Under the condition of the critical stability, according to (18), K_p should satisfy

$$\frac{1}{2\pi f_{\text{cro}} L} \left| \frac{K_p \sin(\pi/6)}{\pi/6} \right| = 1. \quad (27)$$

The critical proportional gain $K_{p,\text{crit}}$ can be solved from (27) as

$$K_{p,\text{crit}} = \frac{\pi L}{3T_h} \frac{\pi/6}{\sin(\pi/6)} = \begin{cases} \frac{\pi^2}{9} L f_{\text{sw}} & \text{(single update)} \\ \frac{2\pi^2}{9} L f_{\text{sw}} & \text{(double update)}. \end{cases} \quad (28)$$

The compensation coefficient at the critical frequency is

$$k_{\text{comp}}(2\pi f_{\text{cro}}) = \left\{ \frac{\pi/6}{\sin(\pi/6)} \right\}^2 = \frac{\pi^2}{9} \quad (29)$$

which is constant even if the duty-cycle update mode is changed. When $T_d \ll T_h$, and then T_d in (25) can be neglected and f_{cro} can be expressed as

$$f_{\text{cro}} = \frac{1}{2T_h} = \begin{cases} \frac{1}{2} f_{\text{sw}} & \text{(single update)} \\ f_{\text{sw}} & \text{(double update)}. \end{cases} \quad (30)$$

Similarly, under the critical stability condition, $K_{p,\text{crit}}$ satisfies

$$K_{p,\text{crit}} = \frac{\pi}{T_h} L \frac{\pi/2}{\sin(\pi/2)} = \begin{cases} \frac{\pi^2}{2} L f_{\text{sw}} & \text{(single update)} \\ \pi^2 L f_{\text{sw}} & \text{(double update)} \end{cases} \quad (31)$$

and the compensation coefficient at the phase crossover frequency is expressed as

$$k_{\text{comp}}(2\pi f_{\text{cro}}) = \left\{ \frac{\pi/2}{\sin(\pi/2)} \right\}^2 = \frac{\pi^2}{4}. \quad (32)$$

It is deduced from (26) to (32) that there is an obvious difference between the one-step delay and the small computational delay. The gain deviation of the s -domain transfer function with the ZOH equivalent model dramatically increases with the decreasing of the computational delay but is not affected by the duty-cycle update mode.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the correctness of the theoretical analysis, the simulation and experimental tests are performed and parameters for simulation and experiment are listed in Table I.

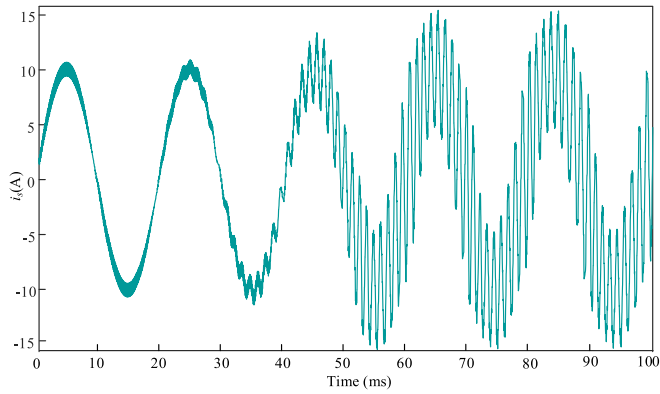


Fig. 5. Line current in the case of the single-update mode with one-step delay.

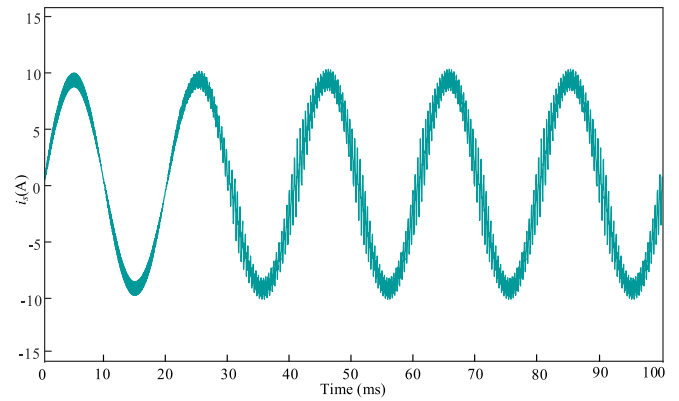


Fig. 7. Line current in the case of the single-update mode with a small computational delay.

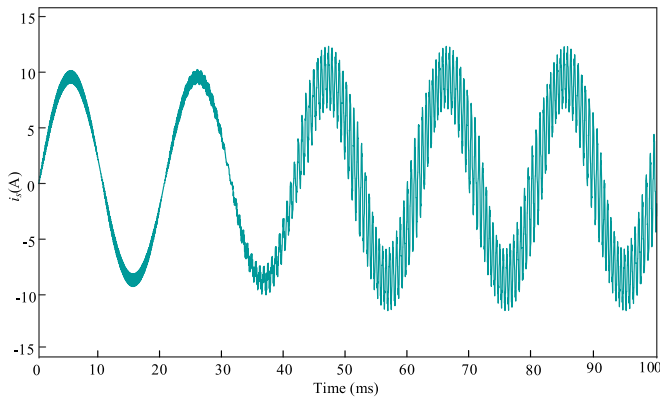


Fig. 6. Line current in the case of the double-update mode with one-step delay.

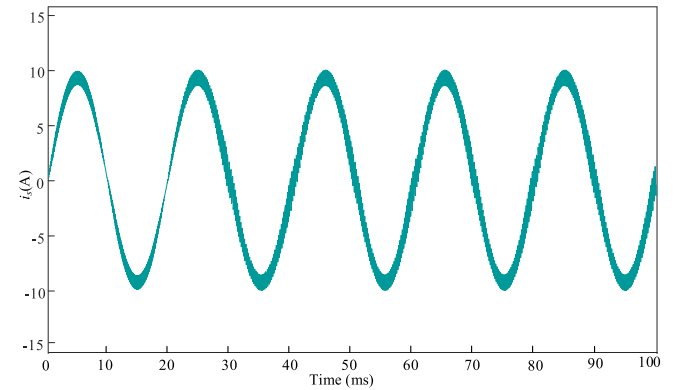


Fig. 8. Line current in the case of the double-update mode with a small computational delay.

A. Simulation Results

Fig. 5 shows the line current in the case of the single-update mode with one-step delay. The proportional gain K_p steps from 57 to 63 Ω at the time instant of 20 ms. According to (28), in this case, the critical proportional gain $K_{p,crit}$ calculated by using the ZOH model for DPWM is equal to 65.8 Ω and $f_{cro} = 833$ Hz. Yet, as shown in Fig. 5, the control system has become unstable when K_p rises to 63 Ω , which means that 65.8 Ω is not a correct critical proportional gain, and the compensated critical gain by using (23) is 60 Ω , which is located the range of 57–63 Ω , verifying the correctness of the theoretical analysis.

Fig. 6 shows the line current in the case of the double-update mode with one-step delay. In this case, the critical proportional gain and phase crossover frequency calculated by using the s -domain model with the ZOH model for DPWM are equal to 131.59 Ω and 1666 Hz, respectively. As shown in Fig. 6, the control system becomes unstable when K_p is increased from 115 to 125 Ω , which is lower than 131.59 Ω but the compensated proportional critical gain is 120 Ω located in this range. And the compensation coefficient solved by (22) is still equal to $\pi^2/9$, which is not affected by different duty-cycle update modes.

Fig. 7 shows the line current in the case of the single-update mode with a small computational delay (20 micro- s). The critical proportional gain of the s -domain model with the ZOH model for DPWM and phase crossover frequency calculated by

(30) and (31) are 296 Ω and 2500 Hz, respectively. However, the control system becomes unstable when the proportional gain is increased from 115 to 125 Ω . This range just covers the compensated proportional gain 120 Ω ; it can be known that the s -domain model with the ZOH model for DPWM has a large deviation when the computational delay is small. This deviation can be effectively compensated by using the compensation coefficient.

Fig. 8 shows the line current in the case of the double-update-mode with a small computational delay. The critical proportional gain by solving the s -domain model with the ZOH model is 592 Ω , and the phase crossover frequency is 5000 Hz. The control system becomes unstable when the proportional gain rises from 230 to 250 Ω at the time instant of 20 ms. This instability of the line current is not obvious for the reason that the resonant frequency is the same as the switching frequency. The current ripple when the current is near to zero is increased dramatically, which implies that the control system has become unstable. The compensated proportional gain is 240 Ω , which is located in the range of 230–250 Ω . The compensation coefficient is $\pi^2/4$, which is coincident with the value solved by (32). Hence, the proposed compensated method can effectively compensate the proportional gain solved by using the s -domain model with the ZOH model for DPWM.

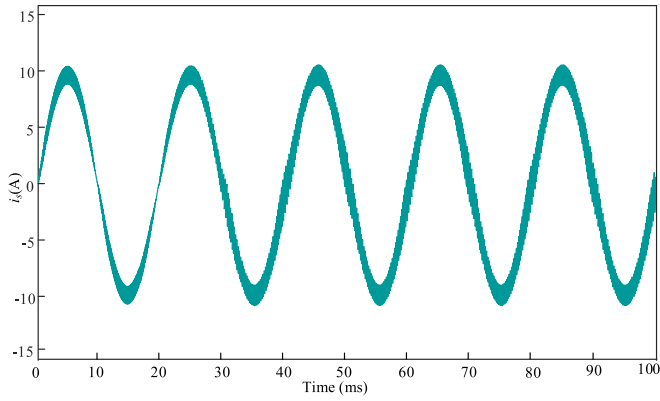


Fig. 9. Line current in the case of the double-update mode with a small computational delay ($L = 10$ mH).

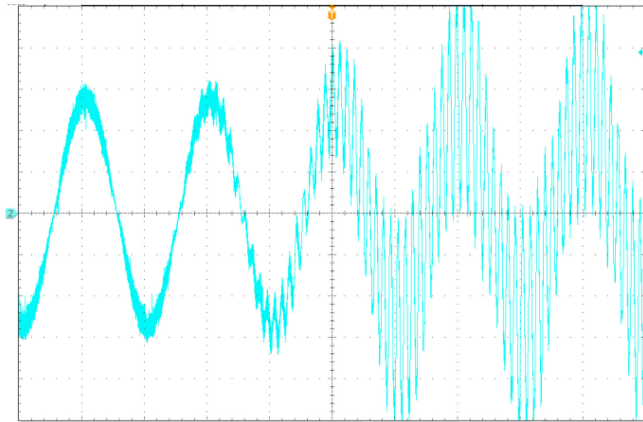


Fig. 10. Measured Line current in the case of the single-update mode with one-step delay ($i: 2$ A/div).

In Fig. 9, the double-update mode with a small computational delay is tested under the condition of $L = 10$ mH. In this case, the proportional gain can be solved as 493.5Ω by using the s -domain model with the ZOH model for DPWM. The proportional gain of the controller steps from 195 to 205Ω at the instant 20 ms, and the control system becomes unstable at this instant. Therefore, the critical proportional gain is located in the range of 195 – 205Ω other than 493.48Ω , and the compensated proportional gain calculated by (23) is equal to 200Ω located in this range, which again proves the effectiveness of the compensated method.

B. Experimental Results

The parameter of the experimental test is the same with that of the simulation. Fig. 10 shows the line current in the case of the single-update mode with one-step delay. In this case, the proportional gain compensated by (23) is equal to 60Ω . However, this critical value is varied from 57 to 63Ω in experiments, due to the inherent nonlinearities brought by the hysteresis of the filter inductor and the dead time of the converter. This slight variation correlates with the compensated value of 60Ω . On the contrary, the stability region solved by (28) without the compensation is 65.797Ω , out of the range.

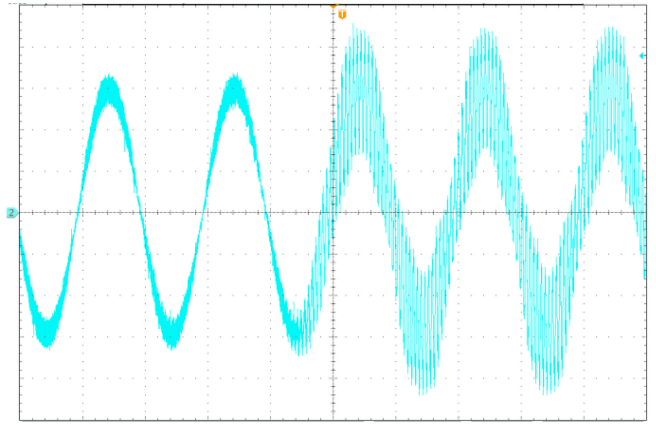


Fig. 11. Measured Line current in the case of the double-update mode with one-step delay ($i: 2$ A/div).

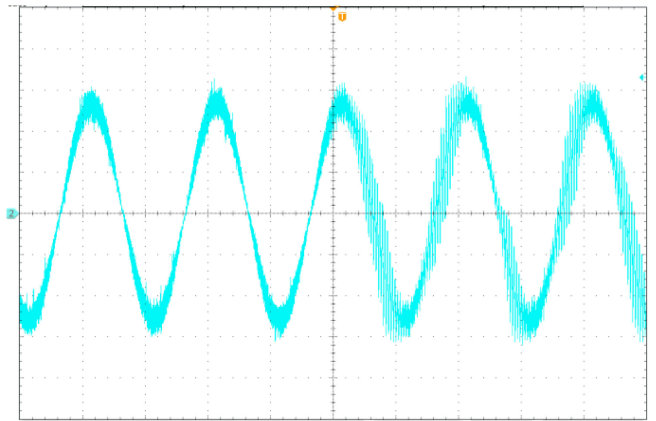


Fig. 12. Measured Line current in the case of the single-update mode with a small computational delay ($i: 2$ A/div).

Fig. 11 shows the experimental results in the case of the double-update mode with one-step delay. Similarly, the proportional gain and phase crossover frequency can be solved by (26) and (28), and the control system becomes unstable when the proportional gain is increased from 115 to 125Ω , which is lower than 131.59Ω solved by (28). Yet, the compensated proportional gain is 120Ω , which is correlated to the range of 115 – 125Ω . The experimental result is the same to the simulation result and again verifies the correctness of the compensated method.

Similarly, the line current in the case of the single-update mode with the small computational delay shown in Fig. 12 becomes unstable while the K_p is suddenly changed from 115 to 125Ω . The compensated $K_{pc} = 120 \Omega$, which coincides with the experimental results. However, the proportional gain K_p solved by (31), which is not compensated by (23), is equal to 296Ω , which is much far from the experimental results. Therefore, it is necessary to compensate the proportional gain in the case of the small computational delay.

Furthermore, the double-update mode with a small computational delay is tested in Fig. 13, which shows that the control system becomes resonant with the increase of the proportional

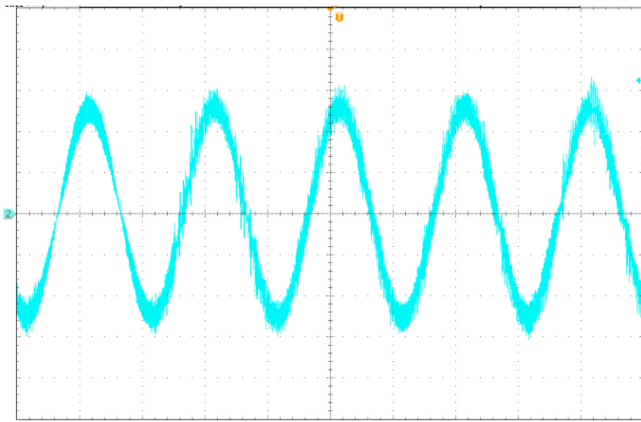


Fig. 13. Measured Line current in the case of the double-update mode with a small delay ($i: 2 \text{ A/div}$).

gain from 230 to 250Ω , which is much lower than 592Ω solved by using the ZOH model for DPWM. The compensated value 240Ω is located in the range of 230 – 250Ω , which coincides with the simulation result. Therefore, the experimental result verifies the correctness of the proposed method.

V. CONCLUSION

This paper presents an accuracy analysis of the equivalent ZOH model for DPWM. A compensation method is derived to compensate the model deviation. The proposed analysis method and compensation method can be developed to different current controllers and converter types. From the theoretical analysis and the experimental verification, the following conclusions can be drawn.

- 1) The phase response of the ZOH model for DPWM is accurate.
- 2) The gain deviation of the ZOH model at the crossover frequency is small with the one-step delay but increases dramatically when the computational delay is reduced. Therefore, the model deviation should be compensated in the case of the small computational delay.
- 3) The gain deviation at the phase crossover frequency is not varied with the duty-cycle update modes; the compensation coefficient hereby is constant at the phase crossover frequency.

REFERENCES

- [1] Y. Wang, X. Wang, F. Blaabjerg, and Z. Chen, "Harmonic instability assessment using state-space modeling and participation analysis in inverter-fed power systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 806–816, Jan. 2017.
- [2] X. Wang, F. Blaabjerg, and P. C. Loh, "Grid-current-feedback active damping for LCL resonance in grid-connected voltage-source converters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 213–223, Jan. 2016.
- [3] Y. Yang, F. Blaabjerg, and H. Wang, "Low-voltage ride-through of single-phase transformerless photovoltaic inverters," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1942–1952, May/June 2014.
- [4] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltage-source converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54–69, Mar. 2016.

- [5] H. Fujita, "A single-phase active filter using an H-bridge PWM converter with a sampling frequency quadruple of the switching frequency," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 934–941, Jul. 2009.
- [6] X. Wang, F. Blaabjerg, and W. Wu, "Modeling and analysis of harmonic stability in an AC power-electronics-based power system," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6421–6432, Dec. 2014.
- [7] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: A survey," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 691–703, Oct. 1998.
- [8] C. Luca, M. Dragan, M. Paolo, and Z. Regan, *Digital Control of High-Frequency Switched-Mode Power Converters*. New York, NY, USA: Wiley, 2015.
- [9] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*. Seattle, WA, USA: Morgan & Claypool, 2015.
- [10] Y. Liao, Z. Liu, G. Zhang, and C. Xiang, "Vehicle-grid system modeling and stability analysis with forbidden region based criterion," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3499–3512, May 2016.
- [11] W. Song, X. Feng, and K. M. Smedley, "A carrier-based PWM strategy with the offset voltage injection for single-phase three-level neutral-point-clamped converters," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1083–1095, Aug. 2013.
- [12] D. M. VandeSype, K. D. Gusseme, A. P. VandenBossche, and J. A. Melkebeek, "Small-signal Laplace-domain analysis of uniformly-sampled pulse-width modulators," in *Proc. IEEE 35th Annu. Power Electron. Spec. Conf.*, Jun. 2004, pp. 4292–4298.
- [13] V. Blasko, V. Kaura, and W. Niewiadomski, "Sampling of discontinuous voltage and current signals in electrical drives: A system approach," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1123–1130, Sep. 1998.
- [14] Y. Liao, Z. Liu, G. Zhang, and C. Xiang, "Vehicle-grid system stability analysis considering impedance specification based on norm criterion," in *Proc. IEEE Conf. Expo Transp. Electrification Asia-Pacific*, Jun. 2016, pp. 118–123.
- [15] H. Shan *et al.*, "The research on the digital controlled effect of performance on the PWM inverter," in *Proc. IEEE 30th Int. Telecommun. Energy Conf.*, Sep. 2008, pp. 1–6.
- [16] D. Yang, X. Ruan, and H. Wu, "A real-time computation method with dual sampling mode to improve the current control performance of the LCL-type grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4563–4572, Jul. 2015.
- [17] L. Harnefors, X. Wang, A. G. Yepes, and F. Blaabjerg, "Passivity-based stability assessment of grid-connected VSCs—An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 116–125, Mar. 2016.
- [18] M. Odavic, V. Biagini, M. Sumner, P. Zanchetta, and M. Degano, "Multi-sampled carrier-based PWM for multilevel active shunt power filters for aerospace applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 1483–1488.
- [19] J. Allmeling and H. Stemmler, "A fast current control technique for active filters with low switching frequency," in *Proc. 27th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2001, pp. 1125–1131.
- [20] P. Mattavelli, F. Polo, F. D. Lago, and S. Saggini, "Analysis of control-delay reduction for the improvement of UPS voltage-loop bandwidth," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2903–2911, Aug. 2008.
- [21] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of LCL-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3414–3427, Jul. 2014.
- [22] W. Song, J. Ma, L. Zhou, and X. Feng, "Deadbeat predictive power control of single phase three level neutral-point-clamped converters using space-vector modulation for electric railway traction," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 721–732, Jan. 2016.
- [23] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009.



Junpeng Ma (S'15) received the B.S. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2013, where he is currently working toward the Ph.D. degree in electrical engineering.

His current research interests include modeling, control, and modulation of grid-tied power converters.



Xiongfei Wang (S'10–M'13–SM'17) received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2006, the M.S. degree from the Harbin Institute of Technology, Harbin, China, in 2008, both in electrical engineering, and the Ph.D. degree in energy technology from Aalborg University, Aalborg, Denmark, in 2013.

Since 2009, he has been with the Aalborg University, where he is currently an Associate Professor in the Department of Energy Technology. His research interests include modeling and control of grid-connected converters, harmonics analysis and control, passive and active filters, stability of power electronic-based power systems.

Dr. Wang serves as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is also the Guest Editor for the Special Issue "Grid-Connected Power Electronics Systems: Stability, Power Quality, and Protection" in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He was recipient of the Second Prize Paper Award and the Outstanding Reviewer Award of IEEE TRANSACTIONS ON POWER ELECTRONICS in 2014 and 2017, respectively, the Second Prize Paper Award at IEEE Industry Applications Society Industrial Power Converter Committee in 2017, and the Best Paper Awards at IEEE Power Electronics for Distributed Generation Systems 2016 and IEEE Power & Energy Society General Meeting 2017.



Frede Blaabjerg (S'86–M'88–SM'97–F'03) received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1995.

He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. At Aalborg University, he became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017, he became a Villum Investigator. He has authored/coauthored more than 500 journal papers in the fields of power electronics and its applications. He is the coauthor of two monographs and editor of six books in power electronics and its applications. His current research interests include power electronics and its applications such as in wind turbines, photovoltaic systems, reliability, harmonics and adjustable speed drives.

Dr. Blaabjerg was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been the Distinguished Lecturer for the IEEE Power Electronics Society (PELS) from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. He is nominated in 2014, 2015, 2016, and 2017 by Thomson Reuters to be between the most 250 cited researchers in engineering in the world. In 2017, he became Honoris Causa at University Politehnica Timisoara, Romania. He was recipient of 24 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, and the Villum Kann Rasmussen Research Award 2014.

Dr. Blaabjerg was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been the Distinguished Lecturer for the IEEE Power Electronics Society (PELS) from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. He is nominated in 2014, 2015, 2016, and 2017 by Thomson Reuters to be between the most 250 cited researchers in engineering in the world. In 2017, he became Honoris Causa at University Politehnica Timisoara, Romania. He was recipient of 24 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, and the Villum Kann Rasmussen Research Award 2014.



Lennart Harnefors (S'93–M'97–SM'07–F'17) received the M.Sc., Licentiate, and Ph.D. degrees in electrical engineering from the Royal Institute of Technology (KTH), Stockholm, Sweden, and the Docent (D.Sc.) degree in industrial automation from Lund University, Lund, Sweden, in 1993, 1995, 1997, and 2000, respectively.

Between 1994 and 2005, he was with Mälardalen University, Västerås, Sweden, where from 2001 he was a Professor of electrical engineering. Between 2001 and 2005, he was, in addition, a Part-Time Visiting Professor of electrical drives with the Chalmers University of Technology, Goteborg, Sweden. Since 2005, he has been with ABB, where he is currently a Senior Principal Scientist at Corporate Research, Västerås. He is, in addition, a Part-Time Adjunct Professor of power electronics with KTH. His research interests include control and dynamic analysis of power electronic systems, particularly grid-connected converters, ac drives, and wide-bandgap-transistor switching circuits.

Dr. Harnefors is an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and of *IET Electric Power Applications*.



Wensheng Song (M'13) received the B.S. degree in electronic and information engineering and the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2006 and 2011, respectively.

He is currently an Associate Professor with the School of Electrical Engineering, Southwest Jiaotong University. From September 2009 to September 2010, he was a Visiting Scholar with the Department of Electrical Engineering and Computer Science, University of California at Irvine, USA.

From July 2015 to December 2015, he was a Visiting Scholar with the University of Alberta, Edmonton, Canada. His current research interests include digital control and modulation methods of electrical ac–dc–ac railway traction drive systems, and multilevel converters.