# Simultaneous DC Current Balance and Common-Mode Voltage Control With Multilevel Current Source Inverters

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***Abstract*—The current source converter (CSC) has been popular in high-power medium-voltage applications. To increase the system power capacity and reduce the output harmonics, parallel connection of CSCs with multilevel current output is a practical approach. There are mainly two types of parallel based configurations. The structure with an independent dc link for each paralleled CSC can be regarded as the first configuration, where the dc current flowing into each CSC can be controlled from the rectifier side independently. The second type is constructed with only one current source rectifier (CSR) on the grid side and paralleled current source inverters (CSIs) on the load side, which could potentially reduce the cost and size of the system. However, with a common dc source, the dc current for each CSC should be carefully controlled with proper modulation design. At the same time, the common-mode voltage (CMV), which increases the motor line-to-ground voltage and causes additional stress to the insulation system, should also be suppressed. In this paper, with a focus on the shared dc-link structure, we thoroughly analyze the dc-link current flow and common-mode loop circuit. We propose a multilevel modulation strategy of the parallel CSI system considering the requirement of dc current balancing and CMV reduction to improve the overall system performance. The effectiveness of the proposed method is verified by both simulation and experiment in a transformerless parallel CSC system.**

***Index Terms*—Circulating current, common-mode current (CMC), common-mode voltage (CMV), current source converter (CSC), dc current balance, multilevel modulation.**

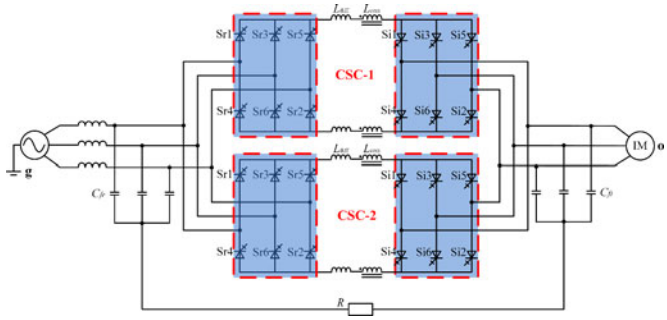


Fig. 1. Parallel-connected CSC system with independent dc link.

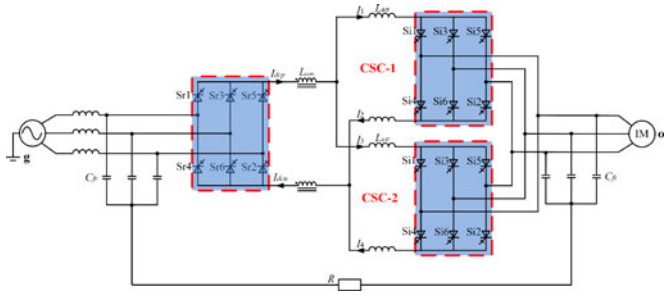


Fig. 2. Parallel-connected CSC system with shared dc link.

## I. Introduction

A CURRENT source converter (CSC) can provide the advantages of an inherent four-quadrant operation, reliable short-circuit protection, motor-friendly waveforms, and voltage-boosting capability, which make the CSC widely applied in medium-voltage (MV) drives, flexible ac transmission system, high-voltage direct current system, solar photovoltaics, and data center supplies [1]–[5]. Multilevel topologies for CSCs can improve the system power capacity and harmonic performance, which have attracted considerable attention in recent years [6]–[10]. Among them, a multilevel CSC system with a parallel converter operation is a practical way to increase the system current rating and power quality at the same time.

There are mainly two types of parallel CSC configurations based on recent research. The first configuration has two back-to-back CSC systems in parallel and share the same input and output filters, as shown in Fig. 1. This topology has independent dc links for each current source inverter (CSI), where it is easy to balance the dc-link currents with proper control of the rectifiers. A dc-link current ripple reduction modulation for this direct parallel topology by proper selection of redundant switching states was introduced in [11].

Another type of parallel CSC configuration is comprised of one single current source rectifier (CSR) and two parallel CSIs, as shown in Fig. 2. The two CSIs share the same dc link, while the total dc current can be controlled to be constant by the CSR. This configuration can take advantage of high capacity thyristors in the front end and pulse width modulation (PWM)

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CSI inverter at the load side, and could have the potential of lower weight and cost compared to the first configuration. But the dc current balance becomes a main concern here, mainly due to the following reasons:

1) the tolerance in the dc-link inductances and winding resistances;
2) differences of on-state voltages of devices; and
3) variations in time delay of the gating signals of the two inverters [1].

The unbalanced dc current can degrade the ac output quality, make the system unstable, and even damage the devices due to overcurrent [12]. As the dc-link currents for each CSI cannot be controlled independently, a control scheme by choosing proper dwell time of medium vectors is proposed to ensure current sharing between the two CSIs [13], [14], the small vectors were not allowed as they increase the switching frequency and system losses in those methods. Moreover, the parallel topologies without using an insolation transformer will result in circulating current, which will increase the power losses, deteriorate the output waveform quality, and even damage the semiconductor devices; a switching loss optimized modulation based circulating current suppression method applied in a parallel CSR system is introduced in [15]. However, most of the previous researches on the parallel CSC system focused on the dc balance without considering the common-mode voltage (CMV) suppression. Moreover, the influence of common-mode (CM) choke on the dc current balance is not analyzed.

In the transformerless CSC system, the CM choke is implemented to attenuate the CMV. Moreover, the neutral points of input and output filters are connected by a damping resistance, which is used to reduce the motor voltage stress, as shown in Figs. 1 and 2 [16]. In that case, the possible CM resonance problem should be a concern due to the $LC$ series connection with adjustable output frequency. Several CMV suppression methods to reduce the CM choke and damping resistance size are developed in the single CSC system [17]–[20]. Previous research has applied multilevel modulation based CMV suppression method on the direct parallel back-to-back CSCs [21], but the CMV control for the second topology in Fig. 2 has not be studied so far.

This paper focuses on the second CSI parallel topology, as shown in Fig. 2. In Section II, the equivalent dc-link circuit and general dc current balance strategy is introduced. Then, the CM loop circuits with different locations of CM choke are compared in detail, and the dc current balance while considering the CM choke influence is thoroughly analyzed. A multilevel modulation based dc current balancing method considering CMV reduction is proposed in Section III. Section IV shows the simulation and experimental results to verify the discussions and proposed method. The conclusion is provided in Section V.

## II. DC-Link Equivalent Circuit and DC Current Balance Strategy

The general dc-link equivalent circuit is shown in Fig. 3, where $L_1 - L_4$ are the differential inductors ($L_1 = L_2 = L_3 = L_4 = L$), $R_1 - R_4$ represent the choke internal resistances,

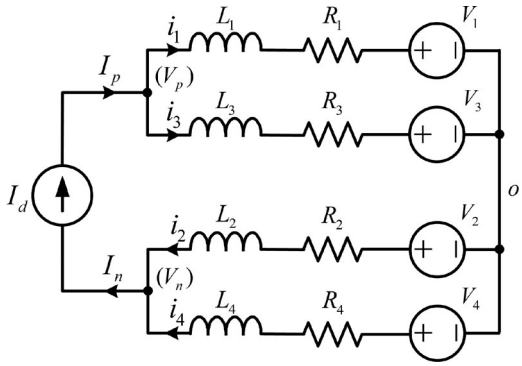


Fig. 3. DC-link equivalent circuit.

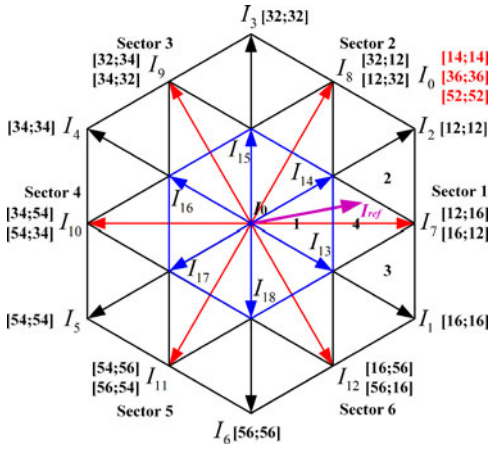


Fig. 4. Space vector diagram of a parallel CSC system.

$V_1 - V_4$ represent the inverter-side dc-link voltage, the values are the output phase voltage based on the switching states, $I_p$ and $I_n$ mean the total positive and negative dc current, respectively, and $i_1$ and $i_3$ represent the positive dc current for each CSI, whereas $i_2$ and $i_4$ represent the negative dc current for each CSI. The on-stage voltages of semiconductor devices and voltage drops on the inductor internal resistances are ignored for simplification; the dc-link current can be expressed as

$$\begin{cases} i_1 = \frac{1}{L}\int (V_1 - V_p)dt;\ i_3 = \frac{1}{L}\int (V_3 - V_p)dt \\ i_2 = \frac{1}{L}\int (V_2 - V_n)dt;\ i_4 = \frac{1}{L}\int (V_4 - V_n)dt \end{cases}$$
$$\Rightarrow \begin{cases} \Delta i_p = i_1 - i_3 = \frac{1}{L}\int (V_1 - V_3)dt \\ \Delta i_n = i_2 - i_4 = \frac{1}{L}\int (V_2 - V_4)dt \end{cases} \quad (1)$$

where $V_p$ and $V_n$ are the rectifier-side positive and negative dc-link voltage, and $\Delta i_p$ and $\Delta i_n$ represent the dc-link current difference of positive and negative bus between the two CSIs. To balance the dc current, $\Delta i_p$ and $\Delta i_n$ should be reduced to be close to zero. As $V_1 - V_4$ changes with the switching states, the switching states of a parallel system are introduced as following.

The space vector diagram for the parallel CSC system is shown in Fig. 4. There are 19 vectors in total and they can be divided into 4 different types according to their lengths, namely large $(I_1 - I_6)$, medium $(I_7 - I_{12})$, small $(I_{13} - I_{18})$, and zero

TABLE I
DC CURRENT INFLUENCE UNDER DIFFERENT SWITCHING STATES

| Vector type | Current vector | Vector length | Switching states | DC current influence |
|---|---|---|---|---|
| Zero | $I_0$ | 0 | [14;14], [36;36], [52;52] | $\Delta i_p$ X; $\Delta i_n$ X |
| | | | [14;36], [36;52], [52;14] | If $V_{ab}/V_{bc}/V_{ca} > 0$, $\Delta i_p$ $\downarrow$; $\Delta i_n$ $\uparrow$ |
| | | | [16;34], [32;56], [54;12] | If $V_{ab}/V_{bc}/V_{ca} > 0$, $\Delta i_p$ $\downarrow$; $\Delta i_n$ $\downarrow$ |
| Large | $I_1$ | $1.15I_d$ | [16;16] | $\Delta i_p$ X; $\Delta i_n$ X |
| Medium | $I_7$ | $I_d$ | [16;12] | $\Delta i_p$ X; If $V_{bc} > 0$, $\Delta i_n$ $\uparrow$ |
| Small | $I_{13}$ | $0.58I_d$ | [16;14] | $\Delta i_p$ X; If $V_{ab} > 0$, $\Delta i_n$ $\downarrow$ |
| | | | [16;36] | $\Delta i_n$ X; If $V_{ab} > 0$, $\Delta i_p$ $\downarrow$ |
| | | | [16;52] | If $V_{ca} > 0$, $\Delta i_p$ $\uparrow$; If $V_{bc} > 0$, $\Delta i_n$ $\uparrow$ |
| | | | [12;56] | If $V_{ca} > 0$, $\Delta i_p$ $\uparrow$; If $V_{bc} > 0$, $\Delta i_n$ $\downarrow$ |

($I_0$) vectors, which are $1.15I_d$, $I_d$, $0.58I_d$, and 0, respectively ($I_d$ is the value of total dc current). As shown in the dc-link equivalent circuit analysis, the inverter-side voltage can influence the balance of dc currents. In the parallel CSC system, the reference current is normally synthesized by the three adjacent vectors. To select the proper vectors, the nearest three adjacent vectors are chosen to form the reference vector considering the triangle where the reference is located. The dwell time of each vector is calculated based on the following equation:

$$\begin{cases} I_x T_1 + I_y T_2 + I_z T_3 = I_{\text{ref}} \\ T_1 + T_2 + T_3 = T_s \end{cases} \tag{2}$$

where $I_x$, $I_y$, and $I_z$ are the three adjacent vectors chosen to form the reference vector, $T_1$, $T_2$, and $T_3$ are the dwell time for each vector, and $T_s$ is the sampling time.

Assuming the reference vector located in the area 4 of sector 1, as shown in Fig. 4. The three adjacent vectors $I_{13}$, $I_{14}$, and $I_7$ are selected to synthesize the reference vector. Taking the switching state [16;12] as an example, $V_1 - V_4$ will be equal to phase voltage $V_a$, $V_b$, $V_a$, and $V_c$ under this switching state, respectively. Based on (1), $\Delta i_p$ will have no change, whereas $\Delta i_n$ can be adjusted based on the values of $V_b$ and $V_c$. if $V_b > V_c$, $\Delta i_n$ will increase (otherwise, it will decrease).

Based on similar analysis, the dc current influence caused by other switching states can be derived, and are listed in Table I, where symbol "$\times$" means no influence, "$\downarrow$" means dc current decrease, and "$\uparrow$" means increase. It shows that the large vectors have no influence on the dc current as the turn-on devices of each CSI are the same, which means the inverter-side dc-link voltage of each CSI are same. Therefore, the dc currents will stay constant under these switching states. The same conclusion is also applied for some zero vectors with the same switching states for each CSI. For other switching states, as they can result in different inverter-side dc-link voltages, the dc currents can be changed by them.

Based on the above-mentioned analysis, a general dc current balance strategy is shown in Fig. 5, the desired switching states can be selected to adjust the dc current with the information of inverter-side phase voltage and the symbols of $\Delta i_p$ and $\Delta i_n$. Once the symbols of $\Delta i_p$ and $\Delta i_n$ are detected, the proper switching states can be chosen to make them close to zero based on Table I.

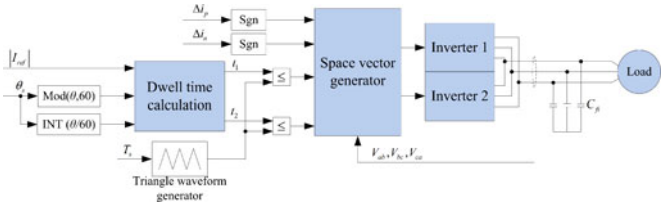


Fig. 5. Multilevel-based dc current balance strategy.

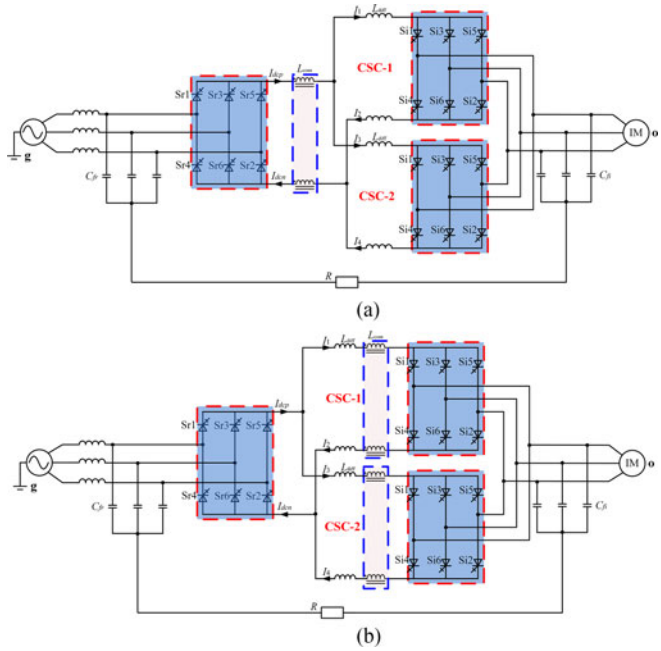


Fig. 6. System diagram with (a) shared and (b) independent CM choke.

## III. DC CURRENT BALANCE AND CMV REDUCTION WITH MULTILEVEL MODULATION

### A. Comparison With Shared and Independent CM Choke

The paralleled CSC topology with shared dc-link can be further analyzed when considering the CM choke position, which can be implemented either in the shared dc bus or the two independent inverter-side dc buses. Fig. 6(a) and (b) shows the two different system diagrams with shared and independent CM choke, respectively. The shared CM mode choke topology could

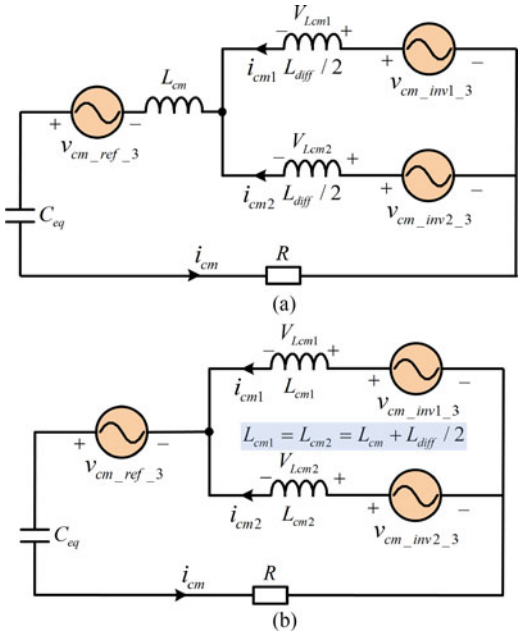


Fig. 7. Common-mode loop circuit with (a) shared and (b) independent CM choke.

reduce size and cost of the system. However, the influences of CM choke on the CM loop and dc balance performance for these two configurations need to be carefully investigated. The following part will compare the two structures with CM loop and dc-link circuit analysis.

Fig. 7(a) and (b) shows the CM loop circuit with shared and independent CM choke, respectively. The CM current (CMC) is excited by the CMV produced by the rectifier and inverters, where the third-order component is the main concern [19]. That means, the dominant CMV component produced by the rectifier ($V_{\mathrm{cm\_ref\_3}}$) is 180 Hz under fixed 60-Hz grid frequency, whereas the dominate CMV components produced by the two inverters ($V_{\mathrm{cm\_inv1\_3}}$, $V_{\mathrm{cm\_inv2\_3}}$) are three times of the motor-side frequency. Based on the CM loop circuit, the total impedance of equivalent circuit can be expressed as

$$\begin{cases} Z_1 = j\omega\left(\frac{L_{\mathrm{diff}}}{4} + L_{\mathrm{cm}}\right) + \frac{1}{j\omega C_{\mathrm{eq}}} + R \\ Z_2 = j\omega\left(\frac{L_{\mathrm{diff}}}{4} + \frac{L_{\mathrm{cm}}}{2}\right) + \frac{1}{j\omega C_{\mathrm{eq}}} + R \end{cases} \tag{3}$$

where $Z_1$ and $Z_2$ represent the total impedance of the CM loops with shared CM choke and independent choke, respectively, $L_{\mathrm{diff}}$ is the differential choke, $L_{\mathrm{cm}}$ is the CM choke, $C_{\mathrm{eq}}$ represents the equivalent capacitance of the input and output filters, which equals $3C_{fr}C_{fi}/(C_{fr}+C_{fi})$, and $R$ is the damping resistor.

Normally, $L_{\mathrm{cm}}$ is much larger than $L_{\mathrm{diff}}$, which can block the majority CMV. Fig. 8 shows the system impedance curve changed with output frequency of the two systems based on the simulation parameters listed in Section IV. It is obvious that the value of $Z_1$ is smaller than that of $Z_2$ in low-frequency region, whereas larger in high-frequency range. The resonance frequency of an independent CM choke system is almost $\sqrt{2}$ times larger than that of a shared CM choke system as the equivalent inductance reduced to nearly half. Therefore, higher CMC will be generated under resonance point for the independent choke structure due to the higher CMV compared with shared choke one.

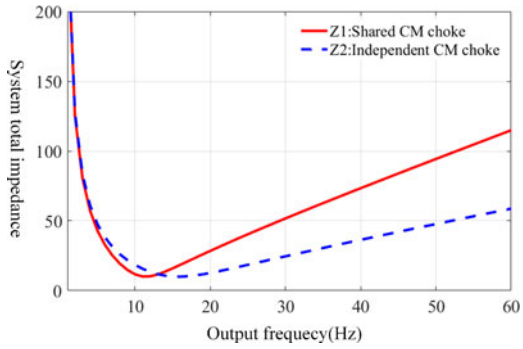


Fig. 8. System impedance with shared and independent CM choke.

Based on the equivalent CM loop circuit, as shown in Fig. 7, the circulating current and CMC expressions can be also derived. Noting that the inverter-side CMV is proportional to the output frequency, which may cause CM loop resonance and result in high CMC near the resonance point when the output frequency is located in a certain region. This paper therefore focuses on the inverter-side CMV. The circulating current and CMC in the shared choke and independent choke configurations are shown as (4) and (5) based on the superposition theory, where the effects of third-order CSI CMV is considered

$$\begin{cases} i_{\mathrm{cr\_}s} = \dfrac{(\dot{v}_{\mathrm{cm\_inv1\_3}} - \dot{v}_{\mathrm{cm\_inv2\_3}})/2}{1/2j\omega L_{\mathrm{diff}}} \\ i_{\mathrm{cm\_}s} = \dfrac{(\dot{v}_{\mathrm{cm\_inv1\_3}} + \dot{v}_{\mathrm{cm\_inv2\_3}})/2}{1/4j\omega L_{\mathrm{diff}} + j\omega L_{\mathrm{cm}} - j/\omega C_{\mathrm{eq}} + R} \end{cases} \tag{4}$$

$$\begin{cases} i_{\mathrm{cr\_}i} = \dfrac{(\dot{v}_{\mathrm{cm\_inv1\_3}} - \dot{v}_{\mathrm{cm\_inv2\_3}})/2}{1/2j\omega L_{\mathrm{diff}} + j\omega L_{\mathrm{cm}}} \\ i_{\mathrm{cm\_}i} = \dfrac{(\dot{v}_{\mathrm{cm\_inv1\_3}} + \dot{v}_{\mathrm{cm\_inv2\_3}})/2}{1/4j\omega L_{\mathrm{diff}} + 1/2j\omega L_{\mathrm{cm}} - j/\omega C_{\mathrm{eq}} + R} \end{cases} \tag{5}$$

where $i_{\mathrm{cr\_}s}$ and $i_{\mathrm{cm\_}s}$ are the circuiting current and CMC of the shared CM choke system, $i_{\mathrm{cr\_}i}$ and $i_{\mathrm{cm\_}i}$ represent the circuiting current and CMC of the independent CM choke system, and $\dot{v}_{\mathrm{cm\_inv1\_3}}$ and $\dot{v}_{\mathrm{cm\_inv2\_3}}$ are the vector form of third-order CMV caused by the two parallel CSIs. The main difference between (4) and (5) is the system impedance, which is shown in Fig. 8. It shows that the system impedance of the independent CM choke structure is smaller comparing to that of the shared CM choke structure under higher output frequency range, which will result in higher CMC.

When considering the influence of CM choke on dc current balance, a more detailed dc-link circuit that include the CM choke is shown in Fig. 9, where $U_{a,b,c}$ is the rectifier-side phase voltage and $V_{a,b,c}$ is the inverter-side phase voltage. Their values are dependent on the switching states. Compared to the general dc-link circuit shown in Fig. 3, the shared CM choke has no influence on the dc current balance as the voltage drop caused

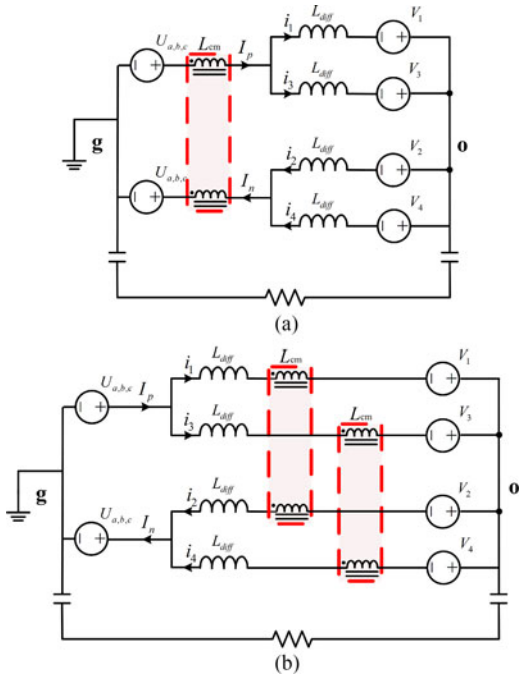


Fig. 9. DC-link circuit with (a) shared and (b) independent CM choke.

by the CM choke is on the total dc bus, whereas the total dc current can be controlled to be constant. But the independent CM chokes can cause unbalanced voltage drops on the independent dc buses, the dc balance strategy that just adjusted the CSI switching states will take longer transient time to balance due to the large CM choke.

Moreover, it can be seen from (4) and (5) that the CMV in the system could affect the circulating current between two CSIs and therefore the dc current balancing considering the CMV effects is very important, particularly for the shared CM choke configuration. This CMV effects for dc current balancing control has not be studied in the literature yet.

### *B. CMV Suppression Method Based on Multilevel Modulation*

Based on the above-mentioned analysis, dc current balance is the prior task for parallel CSIs with the shared rectifier structure. Meanwhile, the CMC excited by CMV can also challenge the performance of the system. When considering the circulating current and CMC produced by both rectifiers and inverters, the total circulating current $(i_{\rm cr})$ and CMC $(i_{\rm cm})$ can be expressed as

$$\begin{cases} i_{\rm cr} = i_{\rm cm1} - i_{\rm cm2} = (i_2 - i_1) - (i_4 - i_3) \\ i_{\rm cm} = i_{\rm cm1} + i_{\rm cm2} = (i_2 - i_1) + (i_4 - i_3) \end{cases} \tag{6}$$

where $i_{\rm cm1}$ and $i_{\rm cm2}$ are the CMC flowing through CSI-1 and CSI-2, which are equal to the differences of negative and positive currents of the corresponding CSI. The circulating current can be zero under balance condition when assuming $i_1 = i_3$ and $i_2 = i_4$. However, the CMC can still be a problem, which makes positive and negative dc current for each CSI unequal,

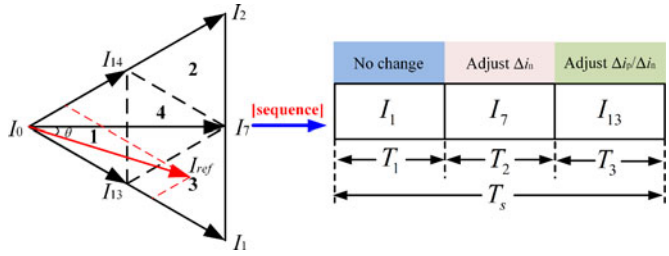


Fig. 10. Space vector sequence when reference located in sector 1 area 3.

leading to $i_1 \neq i_2$ and $i_3 \neq i_4$ even under balance situation. If the CMC is high, a large difference of positive and negative dc current can deteriorate the output waveform or even make the system unstable. Thus, a dc current balance modulation while considering the CMV suppression is proposed to improve the system performance. The average value of CMV $(\rm CMV_{ave})$ produced in each sampling period with multilevel modulation can be shown as

$$|\rm CMV_{ave}| = |T_1 \cdot CMV_1 + T_2 \cdot CMV_2 + T_3 \cdot CMV_3| \tag{7}$$

where $\rm CMV_1$, $\rm CMV_2$, and $\rm CMV_3$ are the CMV produced by the three adjacent vectors $I_x$, $I_y$, and $I_z$, $T_1$, $T_2$, and $T_3$ represent the corresponding dwell times, respectively. Their expressions and exact values caused by different switching states are listed in [21]. As each vector may have multiple associations of switching states in a parallel CSC system, proper switching state combination can result in smallest $\rm CMV_{ave}$. Previous researches adopted (7) as a target function to design the optimized switching sequence and minimize the CMV, especially the third-order component achieved good results in the single CSC system [19], [20].

The proposed method that further considers the CMV suppression based on the general dc current balance strategy is introduced in Section II. As the large vector switching states and some switching states of zero vector (shown in Table I) have no influence on dc current, this method utilizes zero, small, and medium vectors (instead of only medium vectors proposed in [13] and [14]) to balance the dc currents. Specifically, the medium vectors in even sectors can affect positive currents, whereas the medium vectors in odd sectors can adjust negative dc currents. The small vectors in all sectors can adjust both positive and negative currents, which is the key to minimize $\rm CMV_{ave}$ produced in each sampling period. For example, the switching states that only influence $\Delta i_p$ or $\Delta i_n$ can be adopted to balance positive or negative dc currents, whereas other redundant switching states can both adjust $\Delta i_p$ and $\Delta i_n$ are used to minimize CMV by comparing which switching state combination produces smallest $\rm CMV_{ave}$ as expressed in (7). As a more specific example, when the current reference located in sector 1 area 3, the modulation sequence is shown in Fig. 10. The medium vector $I_7$ can only adjust $\Delta i_n$ whereas the small vector $I_{13}$ can adjust both $\Delta i_p$ and $\Delta i_n$, thus the redundant switching states of $I_{13}$ can be selected to reduce $\rm CMV_{ave}$.

The flowchart of proposed method is shown in Fig. 11. The first step is to identify the small triangle where the ref-

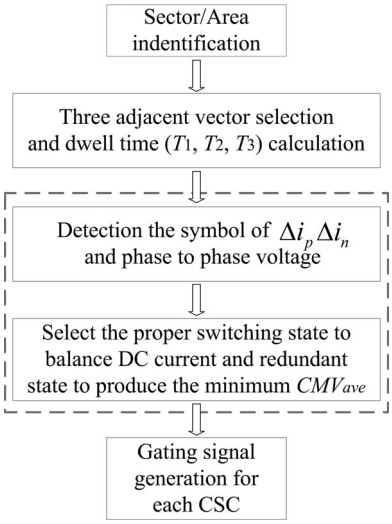


Fig. 11. Flowchart of dc current balance and CMV reduction method.

TABLE II
SIMULATION AND EXPERIMENT PARAMETERS

| | Parameters | Simulation values | Experiment values |
|---|---|---|---|
| CSR | Grid voltage (line to line) | 208 V | 208 V |
| | Nominal power | 10 kVA | 10 kVA |
| | Grid frequency | 60 Hz | 60 Hz |
| | Line inductance | 2.5 mH | 2.5 mH |
| | Input filter capacitance | 160 $\mu$F | 160 $\mu$F |
| DC link | Differential-mode inductor | 10 mH | 10 mH |
| | Common-mode inductor | 100 mH | 100 mH |
| | CM resistance | 10 Ω | 10 Ω |
| | CM resonance frequency | 30 Hz | 30 Hz |
| CSI | CSI output capacitance | 120 $\mu$F | 120 $\mu$F |
| | RL load | 5.76 Ω/20 mH | 5.76 Ω/5 mH |

erence is located, then the nearest three adjacent vectors will be selected to form the reference, and their dwell times can be calculated using (2). The switching state sequence is designed to balance the dc current by considering the symbols of inverter-side phase voltage, and $\Delta i_p$ and $\Delta i_n$ according to the dc current adjustment logic are summarized in Table I. When choosing the switching state of small vectors, the $\mathrm{CMV_{ave}}$ produced by all possible switching state combinations will be compared, the proper switching states which produce smallest $\mathrm{CMV_{ave}}$ will be selected, as a result, this modulation method can balance dc current and minimize CMV simultaneously.

## IV. Simulation and Experimental Results

The parameters of the simulation and experimental system are listed in Table II. The main purpose of this section is to verify the influence the CM choke and effectiveness of the dc current balance scheme while considering the CMV reduction. The simulation results of shared and independent CM choke structures are compared first, then the proposed methods are verified with simulation and experimental results for the shared CM choke structure.

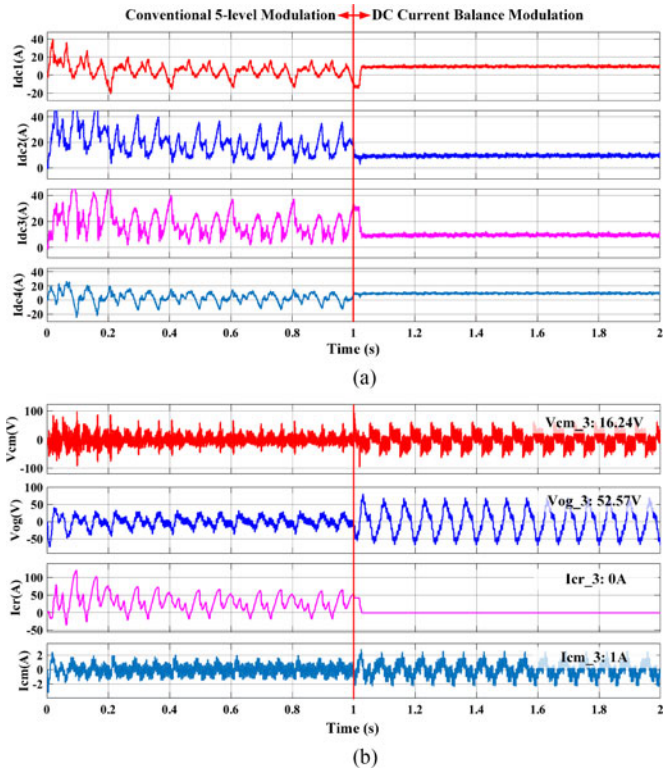


Fig. 12. DC-link current and CMV waveforms with shared CM choke at 5 Hz. (a) DC-link current and (b) CMV/CMC.

### A. DC Current Balance With Shared and Independent CM Choke

As discussed in Section III, the different CM choke positions will result in different CM loop circuit, which influence CMC value and the dc balance performance. Figs. 12 and 13 show the dc current, CMV, circulating current, and CMC waveforms adopting the conventional five-level modulation and general dc current balance scheme for the shared and independent CM choke system at 5 Hz. Figs. 14 and 15 show the waveforms when output frequency is 20 Hz. The total dc current are controlled as 20 A by adjusting the displacement angle of CSR and the modulation index of CSI is set as 0.8. The modulation method is switched from the conventional five-level modulation to the general dc current balance method at the time of 1 s. As can be seen, the general dc balance modulation, which is adopted in either the shared or independent CM choke system, can work effectively. But it takes longer time for the independent CM choke system to finally balance the current. Also, the lower the output frequency, the longer the transient time. This is consistent with the analysis in Section III. The inverter-side third-order CMV of the two systems stay almost the same under different output frequencies (16.24 V and 19.23 V at 5 Hz, 61.37 V and 56.99 V at 20 Hz) as same modulation was adopted. Due to different system impedances, the third-order CMC excited by inverter-side CMV of the shared CM choke system is higher than that of the independent CM choke system at lower frequency (1 A compared with 0.86 A), whereas its value will be much lower under higher frequency (1.68 A compared with 4.37 A).

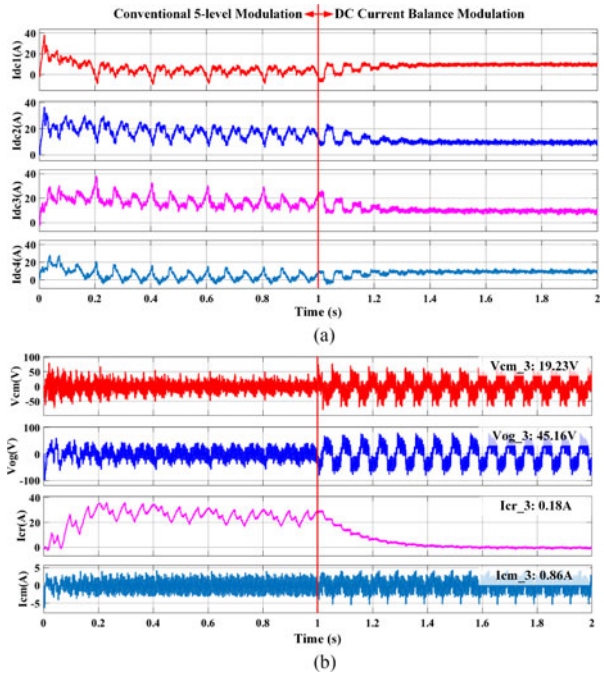


Fig. 13. DC-link current and CMV waveforms with independent CM choke at 5 Hz. (a) DC-link current and (b) CMV/CMC.

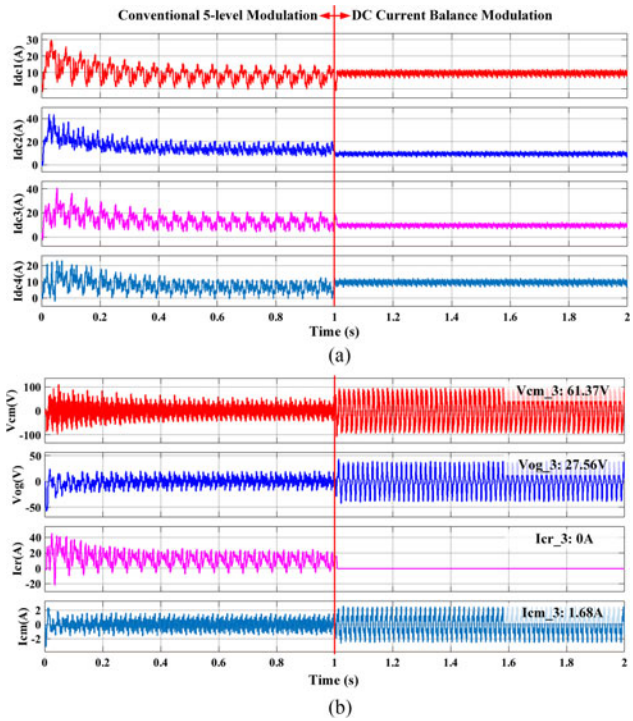


Fig. 14. DC-link current and CMV waveforms with shared CM choke at 20 Hz. (a) DC-link current and (b) CMV/CMC.

In addition, the circulating current of the shared CM choke system will be more serious than that of the independent CM choke system without considering the dc current balance, whereas it is controlled at a very small value under well-balanced

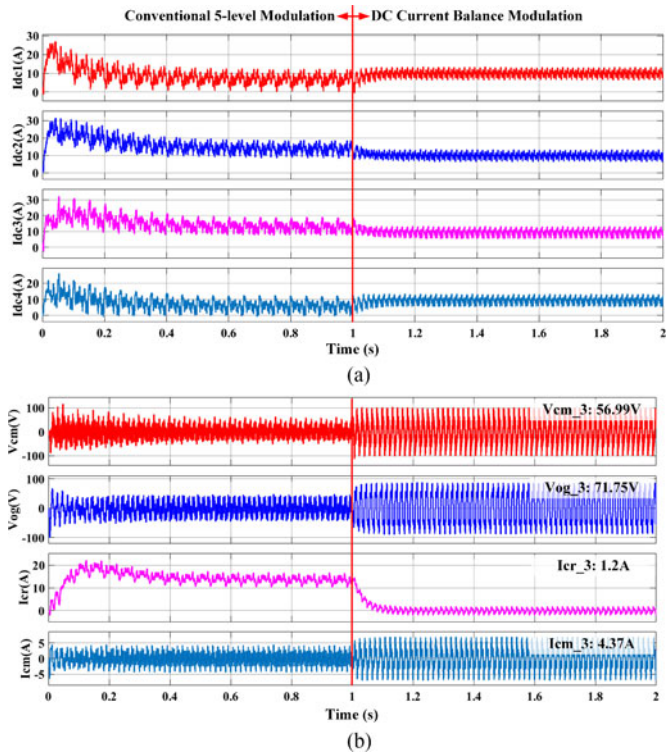


Fig. 15. DC-link current and CMV waveforms with independent CM choke at 20 Hz. (a) DC-link current and (b) CMV/CMC.

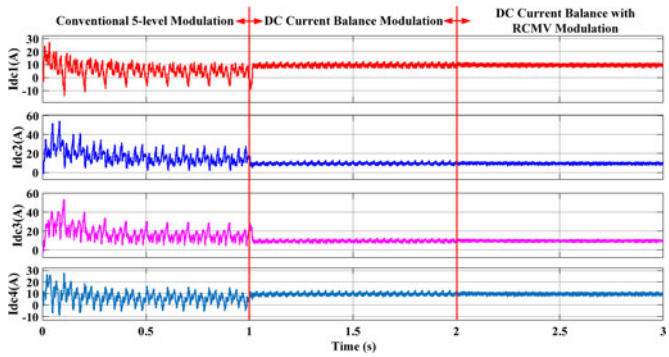


Fig. 16. Simulation results of dc current waveforms.

situation for both structures although the independent choke system has slower transient.

### B. DC Current Balance With CMV Reduction

Fig. 16 shows the dc current waveforms for the shared CM choke structure, with conventional five-level modulation, the general dc current balance scheme when all switching states are adopted to balance the dc current and the proposed dc current balance with reduced CMV modulation. The total dc current are controlled as 20 A by adjusting the displacement angle of CSR. The CSI output frequency is 10 Hz and modulation index is 0.8. At $t = 1$ s, the modulation method is switched from the conventional five-level modulation to the general dc current balance control. At $t = 2$ s, the modulation method is further

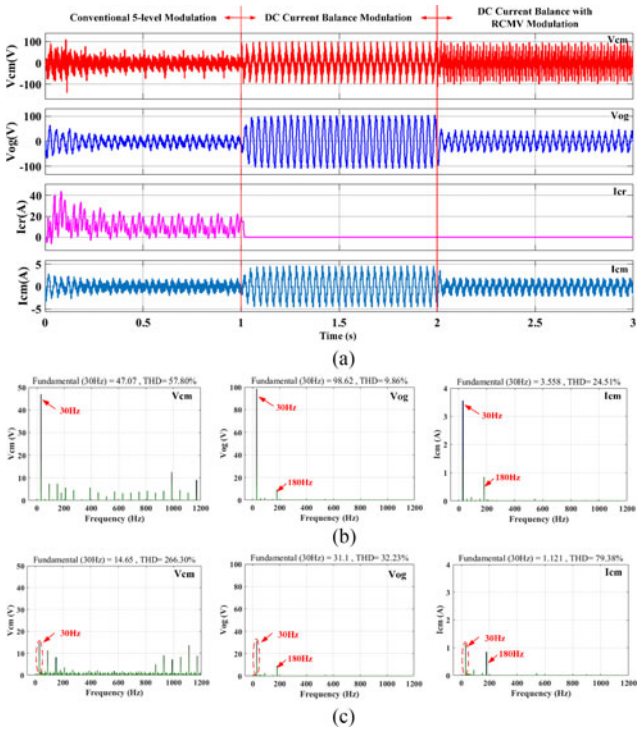


Fig. 17. CMV/CMC and circulating current waveforms. (a) Common-mode voltage/current and circulating current waveform. (b) FFT result of DC current balance modulation. (c) FFT result of DC current balance with RCMV modulation.

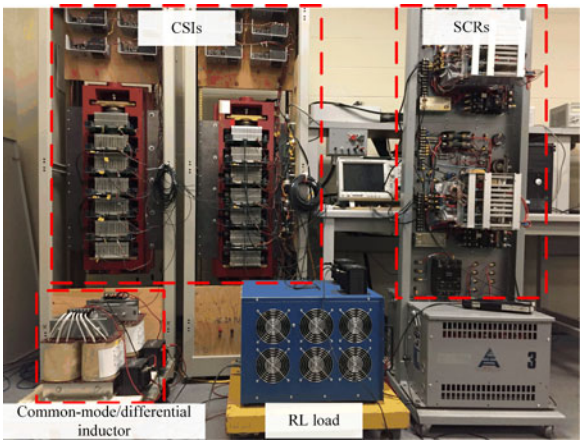


Fig. 18. Experimental setup of a parallel CSC system.

switched to the proposed method. As the waveform shows, the conventional five-level modulation which aims at minimizing the switching times cannot properly balance the dc currents. As a result, the output current quality is affected. When the dc current balance modulation is applied, the dc current can be obviously improved to be around 10 A with very small ripples. Finally, the dc current can be further improved when applying the proposed method, which can further reduce the CMV while keeping the dc current balance.

Fig. 17 shows the CMV, circulating current, and CMC waveforms while adopting the three modulation methods for the

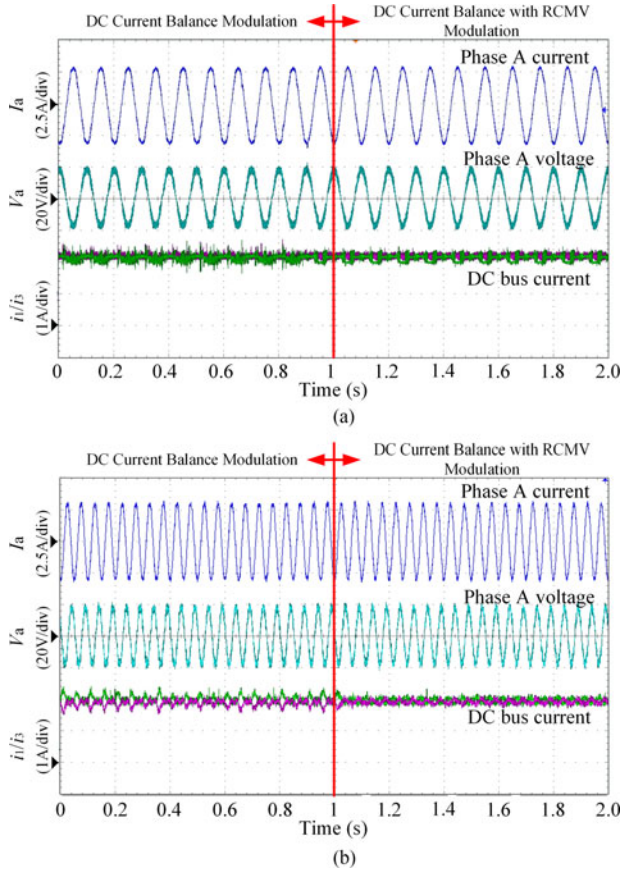


Fig. 19. Experimental results of dc current. (a) DC current at 10 Hz output. (b) DC current at 20 Hz output.

shared CM choke structure. As the conventional five-level modulation cannot make the system work properly, the fast Fourier transform (FFT) results just compare the other two methods. As can be seen, the proposed method can effectively reduce CMV and CMC while improving the dc current balancing performance, which can further improve the output current quality. Thus, the effectiveness of the proposed method can be verified.

To further validate the proposed methods, experiments are conducted on a 10-kVA/208-V/60-Hz transformerless PWM CSC system with *RL* load, the experimental parameters are listed in Table II. The experimental setup is shown in Fig. 18, where a thyristor-based CSR is used as the rectifier to keep the total dc current constant and the inverter side has two CSIs in parallel. The shared dc-link CM inductor structure is adopted to block the system CMV, whereas the differential inductors are implemented to limit the current ripples.

The experimental results of dc current are shown in Fig. 19(a) and (b), where the total dc current is controlled to be 4 A. The output frequency is 10 Hz and 20 Hz, respectively. The CSI modulation index is 0.8. At the time of 1 s, the modulation method is switched from dc current balance modulation to the proposed methods. The dc current $i_1$ and $i_3$ are constant around 2 A, which share the total dc current very well. More importantly, the proposed method can furtherly improve the balance performance with smaller fluctuation. This is mainly because

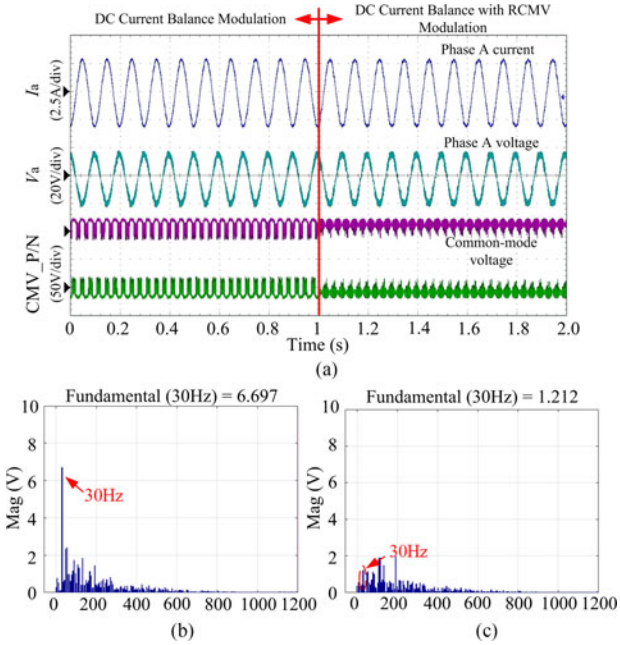


Fig. 20. Experimental results of CMV at 10 Hz. (a) Inverter-side CMV. (b) CMV FFT with DC current balance modulation. (c) CMV FFT with modulation.

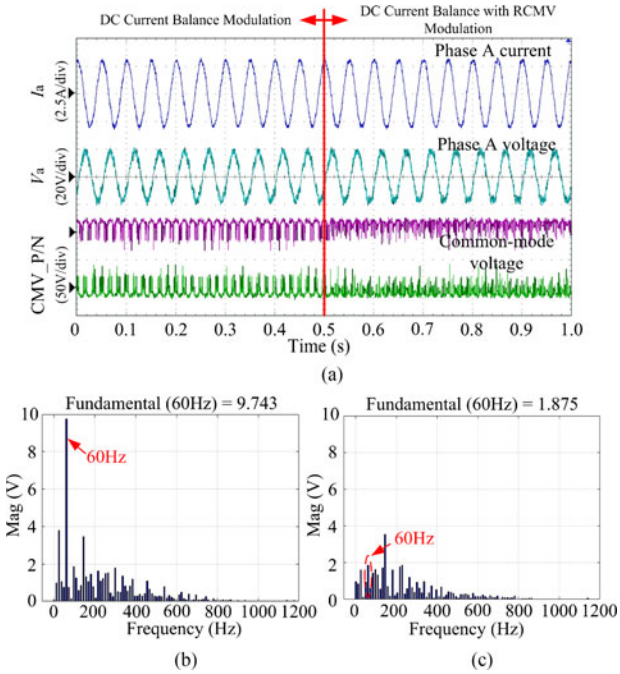


Fig. 21. Experimental results of CMV at 20 Hz. (a) Inverter-side CMV. (b) CMV FFT with DC current balance modulation. (c) CMV FFT with proposed modulation.

the suppression of CMV can reduce the system CMC and, thus, reduces the total dc fluctuation.

Figs. 20 and 21 show the inverter-side CMV waveforms and their FFT analysis results at 10 Hz and 20 Hz, respectively. The CMV reduced effectively when switching from general dc current balance modulation to the proposed modulation at the time of 1 s. The FFT results show that the third-order CMV reduced from 6.7 V to 1.2 V at 10 Hz, and 9.7 V to 1.9 V at 20 Hz while keeping the dc current balanced, which verify the effective of the proposed method.

## V. Conclusion

The parallel operation of CSCs with multilevel modulation is a practical way to improve the system power rating and output quality. This paper analyzes the different topologies of parallel CSCs and focuses on the shared dc-link structure that can potentially reduce the system size and cost. The equivalent dc-link circuit and general dc current balance strategy with proper switching sequence design is introduced first. The CM loop circuits and dc-link circuits for the shared and independent CM choke structures are compared in detail, and the circulating current and CMC excited by CMV are derived. Moreover, a multilevel modulation based dc current balancing method considering CMV reduction by optimizing the redundant switching state selection is proposed to reduce the CMV while keeping the dc current balanced. The simulation and experimental results validate the theoretical analysis and confirm that the proposed method can balance the dc current and reduce CMV effectively.

## References

[1] B. Wu, *High-Power Converters and AC Drives*. Hoboken, NJ, USA: Wiley, 2006, pp. 189–218.

[2] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro, "Current-source converter and cycloconverter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2786–2797, Jul. 2008.

[3] R. E. Torres-Olguin, A. Garces, M. Molinas, and T. Undeland, "Integration of offshore wind farm using a hybrid HVDC transmission composed by the PWM current-source converter and line-commutated converter," *IEEE Trans. Energy Convers.*, vol. 28, no. 1, pp. 125–134, Mar. 2013.

[4] B. Sahan, A. N. Vergara, and N. Henze, "A single-stage PV module integrated converter based on a low-power current-source inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2602–2609, Jul. 2008.

[5] F. Xu, B. Guo, Z. Xu, L. M. Tolbert, F. Wang, and B. J. Blalock, "Paralleled three-phase current-source rectifiers for high-efficiency power supply applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 3, pp. 2388–2397, May.–Jun. 2015.

[6] R. Abe *et al.*, "Development of multiple space vector control for direct connected parallel current source power converters," in *Proc. Power Convers. Conf.*, 1997, pp. 283–288.

[7] S. Kwak and H. A. Toliyat, "Multilevel converter topology using two types of current-source inverters," *IEEE Trans. Ind. Appl.*, vol. 42, no. 6, pp. 1558–1564, Nov.–Dec. 2006.

[8] Z. Bai and Z. Zhang, "Conformation of multilevel current source converter topologies using the duality principle," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2260–2267, Sep. 2008.

[9] M. M. Bhesaniya and A. Shukla, "Current source modular multilevel converter: Detailed analysis and STATCOM application," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 323–333, Feb. 2016.

[10] K. Gnanasambandam, A. K. Rathors, A. Edpuganti, D. Srinivasan, and J. Rodriguez, "Current-fed multilevel converters: An overview of circuit topologies, modulation techniques, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3382–3401, May 2017.

[11] A. Hu, D. Xu, J. Su, and B. Wu, "DC-link current balancing and ripple reduction for direct parallel current-source converters," in *Proc. IECON 2012, 38th Annu. Conf. IEEE Ind. Electron. Soc.*, 2012, pp. 4955–4960.

[12] Z. Bai, H. Ma, D. Xu, and W. Bin, "Control strategy with a generalized DC current balancing method for multimodule current-source converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 366–373, Jan. 2014.
[13] N. Binesh and B. Wu, "5-level parallel current source inverter for high power application with DC current balance control," in *Proc. IEEE Int. Elect. Mach. Drives Conf.*, 2011, pp. 504–509.
[14] D. Xu, N. R. Zargari, B. Wu, J. Wiseman, B. Yuwen, and S. Rizzo, "A medium voltage AC drive with parallel current source inverters for high power applications," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, 2005, pp. 2277–2283.
[15] F. Xu, B. Guo, Z. Xu, L. M. Tolbert, F. Wang, and B. J. Blalock, "SiC based current source rectifier paralleling and circulating current suppression," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 402–408.
[16] N. Zhu, D. Xu, N. R. Zargari, M. Kazerani, and F. Liu, "Common-mode voltage reduction methods for current-source converters in medium-voltage drives," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 995–1006, Feb. 2013.
[17] J. Shang and Y. Li, "A space vector modulation method for common-mode voltage reduction in current source converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 374–385, Jan. 2014.
[18] A. Hu, D. Xu, B. Wu, J. Wang, and J. Su, "Reference-trajectory-optimized SVM for high-power current-source converters to improve harmonic performance and reduce common-mode voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3488–3498, Jul. 2015.
[19] Y. Lian, Y. Zhang, Y. Li, N. R. Zargari, and Z. Cheng, "Common-mode resonance suppression in transformerless PWM current-source drive," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5721–5731, Aug. 2016.
[20] Y. Lian, Y. W. Li, Z. Quan, N. R. Zargari, and Z. Cheng, "SVM strategies for common-mode current reduction in transformerless current-source drives at low modulation index," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1312–1323, Feb. 2017.
[21] L. Ding, Z. Quan, and Y. W. Li, "Common-mode resonance suppression for parallel CSC-fed high power medium voltage drives with multilevel modulation," in *Proc. Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 593–598.

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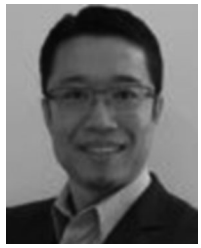

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