Modular Multilevel Converters (MMCs) Controlled by Model Predictive Control With Reduced Calculation Burden

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***Abstract*—Model predictive control (MPC) for modular multilevel converter (MMC) systems has drawn attention among researchers in recent years due to its straightforward implementation, ability to control multiple objectives in a single cost function, and excellent dynamic response. Even though MPC seems promising for the MMC, it suffers from an excessive increase in computational complexity when the number of submodules (SMs) per arm (N) is increased. The computational load can be reduced by decoupling the SM capacitor voltage control from the cost function and balancing them in an external voltage sorting algorithm. In this paper, a further reduction of computations in the MPC is achieved by the preselection of control options that can satisfy the control objectives in the next sampling time. The preselection algorithm generates a greatly reduced number of control options to be computed by a straightforward MPC loop at each sampling time. In addition, the MPC together with the preselection algorithm can generate $2N + 1$ output voltage levels in the MMC while maintaining a low dv/dt in the output voltage and suppressing the circulating currents in MMCs with considerable number of SMs. The steady-state and dynamic performance of the MMC operating with the proposed method is verified by simulation and experimental results.**

***Index Terms*—Circulating current, computational burden, model predictive control (MPC), modular multilevel converter (MMC), total harmonic distortion (THD).**

I. Introduction

OVER the past few years, multilevel converters have garnered interest for industrial implementation in high-power and medium-to-high-voltage applications due to their reduced total harmonic distortion (THD) and low semiconductor power losses [1]. Neutral point clamped (NPC) and cascaded H-bridge (CHB) topologies are the conventional multilevel converters that have been applied in industrial applications. However, some of the drawbacks of NPC topology are its low modularity and scalability, asymmetric power losses in semiconductors, and increased complexity in the control of the neutral point voltage as the number of output levels increases [2]. The CHB solves the problems presented by the NPC; yet, the requirement of isolated dc sources, which are realized by a considerable number of diode rectifiers fed by multipulse transformers, makes its implementation costly and bulky [3].

In 2003, Lesnicar and Marquardt introduced the modular multilevel converter (MMC) [4]. It rapidly drew attention because it does not suffer from the drawbacks of conventional multilevel converters. Furthermore, in comparison with the CHB, the cost, and complexity of scalability and redundancy are reduced [5]. Consequently, the MMC became very attractive for applications such as high-voltage direct current transmission and medium-voltage drive applications [6]–[8].

When the MMC operates as an inverter, there are three control objectives that need to be met for appropriate operation. First, the output current or voltage must be controlled at the appropriate magnitude, frequency, and phase. Second, the circulating current flowing through the MMC legs must be controlled at a certain value. Third, the capacitor voltages of the submodules (SMs) must maintain their reference voltage to avoid deterioration of the THD at the output terminals of the MMC [1], [5]. Several papers have been published that address the controllability of the MMC using proportional-integral (PI) controllers with different dispositions of carrier-based pulse width modulation. However, the number of PI loops increases when the controller targets additional control over the circulating currents or SM capacitor voltages, which increases the complexity of the controller [9]–[13]. In the recent past, model predictive control (MPC) garnered attention and was widely applied to several power converter topologies because of its straightforward design and ability to manage several control objectives while achieving an excellent dynamic response in the systems [14]–[16], [27], [28]. For the aforementioned reasons, the MPC has emerged as an attractive option for the control of MMC systems.

Initially, the direct finite control set (FCS)-MPC considering all possible switching states (C_{2N}^{N} switching states) in the cost function to target the three control objectives was applied to the MMC with $N + 1$ output voltage levels, where N is the number of SMs in an arm of the MMC [17]–[20]. However, the number of control options considered in the cost function is dramatically increased with N, making its practical application impossible for the MMC with more than a few SMs. Later, an indirect FCS-MPC that decouples the control of the SM capac-

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itor voltages from the cost function by controlling them in an external voltage sorting algorithm was proposed in [21]. This action improved the algorithm complexity and reduced the total number of control options to $(N+1)^2$ for an MMC with $2N+1$ output voltage levels. A fast MPC (FMPC) based on the indirect FCS-MPC that analyzes the nearest levels to the last output level of the controller was introduced in [22] to reduce the total number of control options to only three for an $N+1$ output voltage level MMC. Yet, the complexity of the MPC loop increases, and the control options look-up table must be carefully selected according to N. Several previous works on MPC for the MMC focused on the case of the MMC with $N+1$ output voltage levels, because this configuration reduces the computational complexity of MPC methods [22]–[25]. Nevertheless, the MMC with $N+1$ output voltage levels has inferior THD performance with respect to the ac-side currents compared to the MMC operating with $2N+1$ output voltage levels. The FMPC algorithm can be extended to achieve $2N+1$ output voltage levels in the MMC. However, besides the additional increase in complexity of the MPC loop of the algorithm, the very limited number of control options cannot ensure the correct controllability of the circulating currents if N is large. In [26], researchers took into consideration the $2N+1$ output voltage level case for MMCs with hundreds of SMs by not fixing the number of inserted SMs of the MMC legs to N, which effectively suppressed the circulating current. Nevertheless, the complexity of the algorithm for the reduction of control options in the study is high, which increases the computational load of the MPC per control option; in addition, when applied to MMCs with a small number of SMs, it has lower performance than the FMPC in terms of number of control options evaluated and algorithm complexity.

The present paper proposes a preselection algorithm for the control options to be evaluated in the next sampling time of the controller, with the goal of reducing the computational complexity in a straightforward and conventional indirect FCS-MPC loop, while being able to produce $2N+1$ output voltage levels and control the circulating currents. The preselection algorithm analyzes the actual control output of the controller to generate a set of control options that cause the number of inserted SMs to the legs to be $N-1$, N, and $N+1$ for MMCs with a small number of SMs. Simultaneously, these control options potentially produce the output voltage levels nearest to the last output voltage level produced by the controller. Thus, the number of generated control options that can cover the control objectives in the next sampling time is only five. In addition, the proposed method can be easily extended to include the control options that improve the controllability of the circulating currents in MMCs with a considerable number of SMs, without affecting the controllability of the output currents. The proposed preselection method manages to maintain low computational complexity in the MPC while retaining the ability to control the circulating currents in MMCs with a substantial number of SMs by preselecting more control options, which causes the number of inserted SMs in the leg to exceed $N+1$ and $N-1$. Contrary to previous studies on MPC for the MMC, the MPC in this study does not need a look-up table containing all the possible control options, because the preselection method generates them at each sampling time. The SM capacitor voltages are balanced by an external voltage sorting algorithm. The correct tracking of the control objectives is demonstrated by simulations in a three-phase 15-level MMC ($N=7$) and a 41-level MMC ($N=20$), and the experimental validation is presented for a single-phase seven-level MMC prototype ($N=3$).

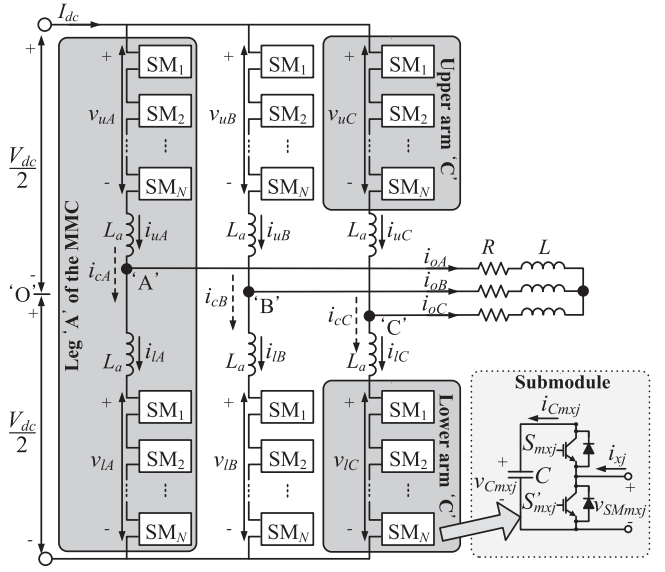

Fig. 1. Circuit configuration of a three-phase MMC and its submodule structure.

This paper is organized as follows. Section II introduces the MMC topology, operation, and its mathematical model. The proposed preselection algorithm and the employed MPC method are explained in Section III. The simulation results and experimental validation are shown in Sections IV and V, respectively. The conclusions of the study are presented in Section VI.

II. Topology of the MMC and Its Mathematical Model

A. Topology and Principles of Operation of the MMC

A three-level MMC is displayed in Fig. 1 to explain its principles of operation. The three-phase MMC is composed of three legs (one leg per phase), and each leg contains two arms (upper and lower arm) that are mutually connected by means of the arm inductors L_a, which are used to limit di/dt in the arm currents. An arm is realized by N cascaded SMs that can have different topologies such as half-bridge, full-bridge, NPC, etc. [1], [5]. Because the half-bridge SM is the most common topology in use, it is adopted in the current study. As seen in Fig. 1, the SM is constructed with a capacitor C connected to two in-series switches S_{mxj} and S'_{mxj}, where the subscript m represents the SM numeration in an arm ($m=1, 2, 3\ldots, N$), subscript x represents the upper and lower arm ($x=u, l$), and subscript j represents the phase or leg of the MMC ($j=A, B, C$).

The capacitor voltage in an SM v_{Cmxj} should be maintained at its nominal value V_{dc}/N for proper operation of the MMC. Thus, one of the control objectives in the MMC is to balance all the capacitor voltages at their nominal value. Switches S_{mxj} and S'_{mxj} can control the output voltage of each submodule

$v_{\mathrm{SM}mxj}$. Hence, when S_{mxj} is turned ON ($S_{\mathrm{mxj}} = 1$) and S'_{mxj} is turned OFF, the output voltage of the submodule $v_{\mathrm{SM}mxj}$ is set to the capacitor voltage v_{Cmxj}. On the other hand, when S_{mxj} is turned OFF ($S_{\mathrm{mxj}} = 0$) and S'_{mxj} is turned ON, the SM is bypassed, and $v_{\mathrm{SM}mxj}$ is equal to zero. By means of $v_{\mathrm{SM}mxj}$, the arm voltages in each phase v_{uj} and v_{lj} can be realized. Both v_{uj} and v_{lj} can contain up to $N+1$ levels with a voltage ranging from zero to V_{dc} depending on the modulation index of the controller [2]. With the differential voltage between v_{uj} and v_{lj}, the output voltage of the converter v_{jO} can be generated with a voltage ranging from $-V_{\mathrm{dc}}/2$ to $V_{\mathrm{dc}}/2$ with a maximum of $2N+1$ voltage levels; and, as a result, the control objective for the correct tracking of the output current i_{oj} can be achieved. The last control objective is accomplished with the common mode voltages of v_{uj} and v_{lj}, whose proper values can minimize the circulating currents i_{cj}.

B. Mathematical Model of the MMC

By means of Kirchhoff's current law in the output node j in Fig. 1, the current relationships between the upper arm current i_{uj} and lower arm current i_{lj} are given as

$$i_{oj}(t) = i_{uj}(t) - i_{lj}(t) \tag{1}$$

$$i_{cj}(t) = \frac{1}{2}\left[i_{uj}(t) + i_{lj}(t)\right] - \frac{1}{3}I_{\mathrm{dc}} \tag{2}$$

where i_{oj} is the output current in phase j, i_{cj} is the circulating current flowing through leg j, and I_{dc} is the current flowing in the dc side of the MMC.

In the same manner, by application of Kirchhoff's voltage law to the upper arm and lower arm of leg j with the respective phase-j load, represented by R and L, the following expressions are obtained:

$$\frac{V_{\mathrm{dc}}}{2} - v_{uj}(t) - L_a\frac{di_{uj}(t)}{dt} - Ri_{oj}(t) - L\frac{di_{oj}(t)}{dt} = 0 \tag{3}$$

$$-\frac{V_{\mathrm{dc}}}{2} + v_{lj}(t) + L_a\frac{di_{lj}(t)}{dt} - Ri_{oj}(t) - L\frac{di_{oj}(t)}{dt} = 0. \tag{4}$$

By adding (3) and (4) and using the relationships in (1) and (2), the dynamic behavior of the phase-j output current in the MMC is deduced as

$$\frac{di_{oj}(t)}{dt} = \left(\frac{1}{2L + L_a}\right)\left[v_{lj}(t) - v_{uj}(t) - 2Ri_{oj}(t)\right] \ . \tag{5}$$

Similarly, the dynamic behavior of the circulating current in leg j is obtained by the difference between (3) and (4), and it is expressed as

$$\frac{di_{cj}(t)}{dt} = \left(\frac{1}{2L_a}\right)\left[V_{\mathrm{dc}} - v_{uj}(t) - v_{lj}(t)\right]. \tag{6}$$

From (5) and (6), it can be deduced that the phase-j output current i_{oj} can be controlled by the differential voltage between v_{lj} and v_{uj}. On the other hand, the circulating current in leg j, i_{cj}, is controlled by the common mode voltage of v_{uj} and v_{lj}.

The dynamic equation of the capacitor voltage in each SM v_{Cmxj} is obtained by means of the current flowing through the capacitor i_{Cmxj} as follows:

$$\frac{dv_{\mathrm{Cmxj}}(t)}{dt} = \frac{i_{\mathrm{Cmxj}}(t)}{C} \tag{7}$$

where i_{Cmxj} is given by the switching signal S_{mxj} and the arm current i_{xj} expressed as follows:

$$i_{\mathrm{Cmxj}}(t) = S_{\mathrm{mxj}}(t)i_{xj}(t). \tag{8}$$

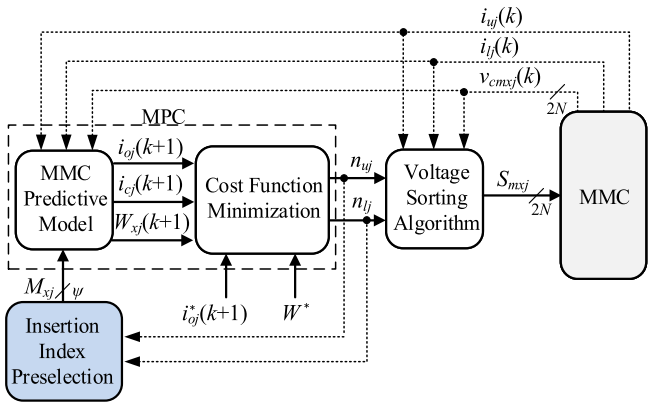

Fig. 2. Block diagram of the MPC strategy with the proposed preselection method.

III. MPC Method and the Proposed Preselection Algorithm for the MMC

The block diagram of the presented MPC strategy is shown in Fig. 2. Similar to the conventional indirect FCS-MPC, the control of the phase-j output currents, leg-j circulating currents, and arms energy balancing control is performed by the predictive controller by means of the insertion indexes n_{uj} and n_{lj}, while the voltage balancing of the capacitors inside the SMs is controlled by the external voltage sorting algorithm. This section presents a fast preselection algorithm that generates a reduced number of control options that can produce $2N+1$ output voltage levels and control the output currents and circulating currents in the MPC algorithm for MMCs with any number of SMs.

A. Predictive Model of the MMC

At each sampling time, measurements in the MMC are carried out and processed by the controller to output the control signals S_{mxj} that ensure correct tracking of the reference signals of the controller. Because the MPC operates in the discrete-time domain, the forward Euler approximation presented in (9) is considered to obtain the discrete-time model from the previously presented model in the continuous-time domain:

$$\frac{dz(t)}{dt} \approx \frac{z(k+1) - z(k)}{T_{\mathrm{sp}}} \tag{9}$$

where z represents the variable of the control objectives, T_{sp} is the sampling period, and k is the sampling instant of the controller.

Using (5) and (9), the phase-j output current dynamics is then obtained in the discrete-time domain as follows:

$$i_{oj}(k+1) = \left(\frac{T_{\rm sp}}{2L+L_a}\right)\left[v_{lj}^{p}(k) - v_{uj}^{p}(k)\right] + \left(1 - \frac{2RT_{\rm sp}}{2L+L_a}\right) i_{oj}(k). \quad (10)$$

Similarly, by substituting (9) into (6), the discrete-time dynamics of the leg-j circulating currents is deduced as

$$i_{cj}(k+1) = \left(\frac{T_{\rm sp}}{2L_a}\right)\left[V_{\rm dc} - v_{lj}^{p}(k) - v_{uj}^{p}(k)\right] + i_{cj}(k). \quad (11)$$

As observed in (10) and (11), the predicted currents for the sampling time $k+1$ require measurements of currents i_{oj} and i_{cj}, and the arm voltages v_{xj}^{p}. The arm voltages v_{xj}^{p} are evaluated in the sampling time k with the preselected insertion indexes M_{xj} that were obtained in the sampling time $k-1$. Thus, the evaluated arm voltage is given as follows:

$$v_{xj}^{p}(k) = \frac{M_{xj}}{N}\sum_{m=1}^{N} v_{\rm Cmxj}(k)\,. \quad (12)$$

The predicted sum of the SM capacitor voltages in the arms of leg j in the MMC is obtained by discretization of (7) with (9), and it is given by

$$\sum v_{Cxj}^{p}(k+1) = M_{xj} i_{xj}(k)\frac{T_{\rm sp}}{C} + \sum_{m=1}^{N} v_{\rm Cmxj}(k). \quad (13)$$

Assuming that all the SM capacitor voltages are well balanced, the energy stored at the sampling instant $k+1$ in each arm of leg j of the MMC is

$$W_{xj}(k+1) = \frac{C}{2N}\left[\sum v_{\rm Cxj}^{p}(k+1)\right]^2. \quad (14)$$

Thus, the energy balance between the arms of a leg of the MMC can be achieved by the prediction of (14), which can guarantee the correct steady-state operation of the average value of the SM capacitor voltages as $V_{\rm dc}/N$.

B. Cost Function Minimization

After evaluating all the control options of M_{xj}, the predicted values i_{oj}, i_{cj}, and W_{xj} are introduced into a cost function to be compared with their reference values as follows:

$$g = \lambda_o\left|i_{oj}^{*}(k+1) - i_{oj}(k+1)\right| + \lambda_c\left|i_{cj}(k+1)\right| + \lambda_W\left|W^{*} - W_{xj}(k+1)\right| \quad (15)$$

where λ_o, λ_c, and λ_W are the weighing factors of the cost function and are obtained using the method presented in [29] and [30], resulting in $\lambda_o = 1$, $\lambda_c = 0.05$, and $\lambda_W = 1 \times 10^{-7}$. The reference of the output current is represented by i_{oj}^{*}, and the reference of the energy stored in each arm is given by $W* = CV_{\rm dc}^2/2N$. The control option of M_{xj} that yields the minimum value of the cost function is selected, and the optimal insertion indexes n_{uj} and n_{lj} to be applied at the instant k are obtained. Fig. 3(a) displays the flowchart of the MPC method employed in this paper for five preselected control options ($\psi = 5$). The preselection method, which is explained later in the paper, on certain occasions can generate insertion indexes M_{xj} with absurd values such as negative numbers or numbers higher than N; these illogical values are bypassed and are not computed by the MPC.

C. Voltage Sorting Algorithm

In this study, the voltage sorting algorithm applied in [22] is used to balance all the capacitor voltages of the MMC $v_{\rm Cmxj}$. The algorithm reads the insertion indexes to be applied, n_{uj} and n_{lj}, and decides which SMs to connect or bypass inside each arm of the MMC according to the sign of the arm current i_{xj} and the magnitude of the capacitor voltages $v_{\rm Cmxj}$. Consequently, if $i_{xj} > 0$, the algorithm connects n_{xj} SMs with the lowest voltages in the respective arm and bypasses all the others. On the other hand, if $i_{xj} < 0$, the algorithm connects n_{xj} SMs with the highest voltages and bypasses the others. Hence, the switching signals $S_{\rm mxj}$ to be applied in the sampling time k are obtained. The flowchart of the voltage sorting algorithm is presented in Fig. 3(b).

D. Insertion Index Preselection Method for the MMC

The proposed preselection algorithm generates the insertion indexes M_{xj} to be evaluated by the MPC in the next sampling time $k+1$ to generate $2N+1$ levels in the output voltage of the MMC while retaining the ability to control the circulating currents. The basis of the proposed algorithm is that the possible combinations of insertion indexes that can be applied by the controller in the next sampling time depend on the sum of the insertion indexes s_j, which is given as

$$s_j = n_{uj} + n_{lj}. \quad (16)$$

Unlike other previous studies, the number of inserted SMs in a leg s_j is not fixed as N in this study. However, to maintain a reduced computational complexity, s_j is limited as $(N-\delta,\, N-\delta+1,\, N-\delta+2,\, \ldots,\, N+\delta)$, where δ is the sum boundary. The issue of the circulating current controllability and a guideline for the selection of δ with respect to the number of SMs in the MMC are given in the Appendix. It is demonstrated that the preselection method for MPC applied to MMCs with a small number of SMs ($N < 13$) can operate correctly with $\delta = 1$.

Table I shows the $3N+1$ optimal combinations with sum of the indexes s_j equal to $N-1$, N, and $N+1$ ($\delta = 1$) that can control circulating currents in MMCs with a small number of SMs while being able to produce $2N+1$ output voltages. In addition, the output level numeration h_j, given by (17), is also listed in the table. It is observed that odd levels are realized by one combination whose $s_j = N$, whereas even levels are realized with two combinations whose s_j values equal $N-1$ and $N+1$. Note that if only odd levels are generated by the controller (with the number of inserted SMs permanently fixed to N), the number of output levels is $N+1$. Fig. 4 shows the voltage content of each output level h_j. One can verify that the lowest output level ($h_j = 1$) contains the voltage $-V_{\rm dc}/2$, whereas the highest output level ($h_j = 2N+1$) has an output

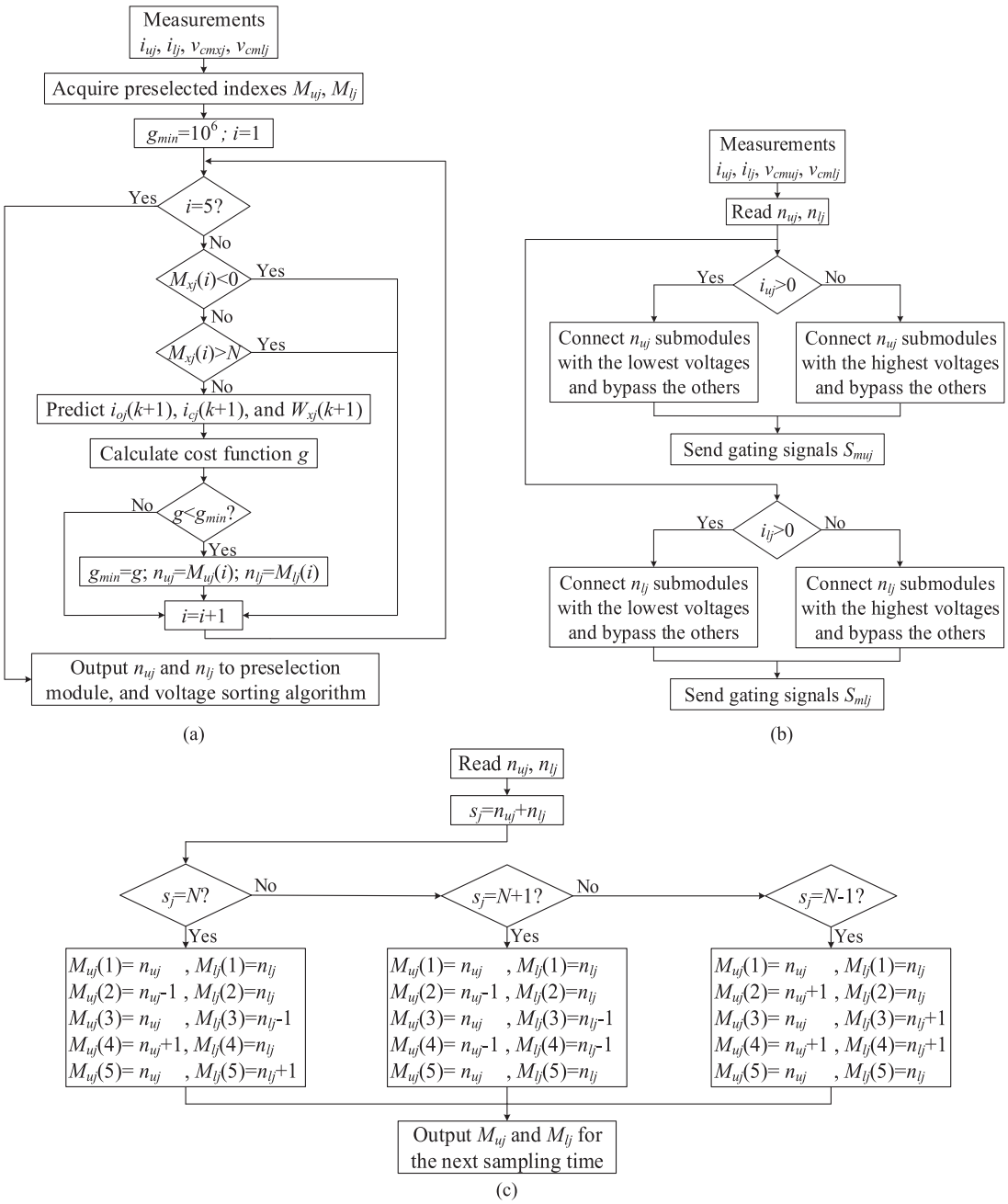

Fig. 3. Flowchart of the MPC operating with the proposed preselection algorithm with $\delta = 1$ ($\psi = 5$). (a) MPC, (b) SM capacitor voltage sorting algorithm, and (c) proposed preselection algorithm for reduction of computational complexity.

voltage of $V_{\rm dc}/2$:

$$h_j = n_{lj} - n_{uj} + N + 1. \tag{17}$$

The flowchart of the proposed preselection algorithm for $\delta = 1$ is illustrated in Fig. 3(c). The preselection algorithm only considers the three possible s_j values to generate the insertion indexes to be evaluated by the MPC in the next sampling time $k+1$. Thus, at each sampling time k, the preselection algorithm generates the insertion indexes whose sums s_j are $N-1$, N, and $N+1$. For example, when the indexes applied by the controller at the instant k are $n_{uj} = N-1$ and $n_{lj} = 1$, the odd output level $h_j = 3$ is produced, and the sum of the insertion indexes s_j is N. In this case, the preselection algorithm finds the combinations whose s_j values equal $N-1$ and $N+1$. The first values preselected by the algorithm are the original insertion indexes $M_{uj}(1) = N-1$ and $M_{lj}(1) = 1$. The second and third preselected combinations are realized by subtracting one from the original upper and lower insertion indexes, respectively. Thus, the second preselected insertion indexes are $M_{uj}(2) = N-2$ and $M_{lj}(2) = 1$, and the third preselected indexes are $M_{uj}(3) = N-1$ and $M_{lj}(3) = 0$, resulting in the first combinations with $s_j = N-1$ for the even output levels $h_j = 4$ and $h_j = 2$, respectively. The fourth and

TABLE I
COMBINATIONS OF INSERTION INDEXES FOR $2N+1$ OUTPUT VOLTAGE LEVELS IN MMCS WITH $\delta = 1$

Upper index n_{uj}	Lower index n_{lj}	Sum of indexes s_j	Output level h_j
N	0	N	1
N	1	$N+1$	2
$N-1$	0	$N-1$	2
$N-1$	1	N	3
$N-1$	2	$N+1$	4
$N-2$	1	$N-1$	4
$N-2$	2	N	5
...	...	...	...
1	$N-1$	N	$2N-1$
1	N	$N+1$	$2N$
0	$N-1$	$N-1$	$2N$
0	N	N	$2N+1$

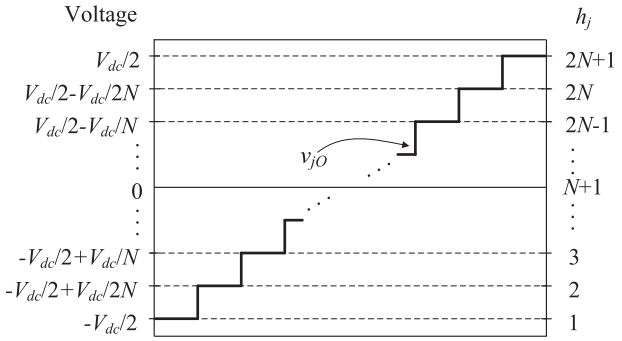

Fig. 4. Output voltage values and output levels h_j in the MMC with $2N+1$ levels.

fifth preselections are carried out by adding one to the original upper and lower insertion indexes, respectively. This results in the second combinations with $s_j = N+1$ for the even output levels $h_j = 2$ and $h_j = 4$, whose insertion indexes are given by $M_{uj}(4) = N$ and $M_{lj}(4) = 1$, and $M_{uj}(5) = N-1$ and $M_{lj}(5) = 2$, respectively. As a result, when the controller selects the insertion indexes resulting in an odd output level such as $h_j = 3$ at the instant k, the preselection technique builds five control options that can produce the output levels 2, 3, and 4, ensuring a low dv/dt in the output voltage while retaining the ability to control the circulating currents. In the other case, when the indexes applied by the controller at the instant k are $n_{uj} = N$ and $n_{lj} = 1$, the even output level $h_j = 2$ is produced, and the sum of the insertion indexes s_j is $N+1$. As a result, combinations of insertion indices whose s_j values are N and $N-1$ must be found by the preselection algorithm. The first combination of insertion indexes to be preselected by this technique is the original combination applied by the controller at the instant k, $M_{uj}(1) = N$ and $M_{lj}(1) = 1$. The second and third combinations to be preselected are the ones whose s_j values are equal to N. The second preselected insertion indexes are realized by subtracting one only from the original upper insertion index, giving $M_{uj}(2) = N-1$ and $M_{lj}(2) = 1$, which results in the odd level $h_j = 3$. The third combination preselected is obtained by subtracting one from the original lower insertion index, $M_{uj}(3) = N$ and $M_{lj}(3) = 0$, resulting in the odd level $h_j = 1$. The fourth combination of insertion indexes to be preselected is the one that produces $s_j = N-1$. This is achieved by subtracting one from both the original insertion index values as $M_{uj}(4) = N-1$ and $M_{lj}(4) = 0$, which results in the second combination for the even output level $h_j = 2$. It is demonstrated in the example that, with $h_j = 2$ as the output of the controller in the sampling instant k, the preselected combination of insertion indexes for the next sampling time $k+1$ includes the upper level $h_j = 3$ and the lower level $h_j = 1$, while including both combinations that generate the same level $h_j = 2$. Given that the number of preselected combinations is four in this case, which is different to the five control options preselected in the previous case, the algorithm adds the fifth control, with the original values, in order to keep the number of control options evaluated by the MPC constant, as observed in Fig. 3(c). In the same manner as the previous example, when the controller outputs a combination whose s_j value is $N-1$ in the sampling time k, the preselection algorithm obtains the combination of insertion indexes whose s_j values are N and $N+1$ by adding one to the original insertion indexes instead of subtracting one as in the previous example. Because preselected insertion indexes can be negative or higher than N, which is absurd, the MPC algorithm filters out those cases, as seen in Fig. 3(a).

E. Extension of the Proposed Preselection Algorithm for Improved Controllability of Circulating Currents

The algorithm can be extended to larger δ for better controllability of circulating currents when N is considerably large. Similar to the case with $\delta = 1$, the basis of the algorithm is to find at each sampling time the vicinity of control options whose sj values are $N-\delta$, $N-\delta+1$, $N-\delta+2$, ..., and $N+\delta$, and furthermore, at the same time can produce the output levels closest to the previous level applied. Thus, the algorithm continues adding one to or subtracting one from the original insertion indexes until all the combinations of s_j, limited by δ, are preselected.

Fig. 5 shows the relationship between s_j and the output levels with $\delta = 4$. From Fig. 5, we can observe that if $\delta = 1$, as mentioned before, there are two control options that can realize even output levels. If the boundary is increased to $\delta = 2$, two additional control options appear in the odd output levels, except for the extreme levels $h_j = 1$ and $h_j = 2N+1$ because they can only be generated by combinations whose sj values are N. When the boundary is $\delta = 3$, two more control options are added to the even output levels. Thus, it can be concluded from Fig. 5 that each time δ is increased by one, the increment of the two additional control options per output level is exchanged between odd and even output levels. Table II shows the number of control options generated by the preselection algorithm with respect to the sum boundary.

IV. SIMULATION RESULTS

Simulations for the three-phase MMC displayed in Fig. 1 were performed with the parameters listed in Table III using the PSIM software to verify the effectiveness of the proposed MPC with the preselection method.

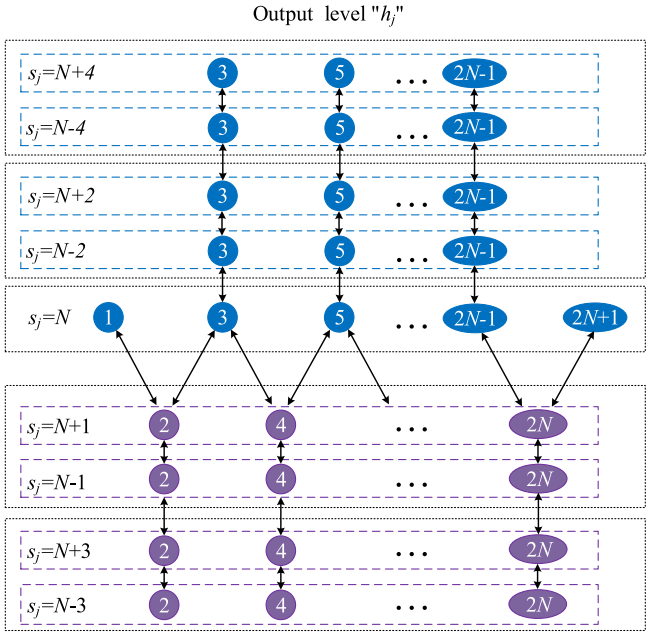

Fig. 5. Behaviors of the output levels h_j and the sum of insertion indexes s_j with $\delta = 4$ in the proposed method.

TABLE II
NUMBER OF CONTROL OPTIONS PRESELECTED BY THE PROPOSED METHOD WITH DIFFERENT SUM BOUNDARIES

Preselection algorithm	Sum boundary (δ)				
	1	2	5	10	δ
Control options (ψ)	5	8	17	32	$3\delta + 2$

TABLE III
PARAMETERS OF THE MMC SYSTEM IN THE STUDY

Symbol	Parameter	Simulation	Experiment
$V_{\rm dc}$	DC-link voltage (V)	7000	150
N	SMs per arm	7	3
V_C	SM capacitor voltage (V)	1000	50
C	SM capacitance (μF)	3300	2200
L_a	Arm inductance (mH)	5	3.5
L	Load inductance (mH)	10	10
R	Load resistance (Ω)	23	20
f	Output frequency (Hz)	60	60
S	MMC rated power (kVA)	710	0.15
$T_{\rm sp}$	Sampling period (μs)	100	100

Fig. 6 shows the steady-state operation of the MPC working with the proposed preselection algorithm. The 15 output voltage levels in phase A are achieved for the MMC with $N = 7$ and are displayed in Fig. 6(a). At every modification of the phase-A output level, the voltage realizes only one step change from the previous level, which ensures a minimum value for dv/dt. The three-phase output currents are shown in Fig. 6(b) with a THD of 0.85% and balanced operation. The circulating currents in the three legs of the MMC are suppressed and are shown in Fig. 6(c). The capacitor voltages of the SMs in leg A of the

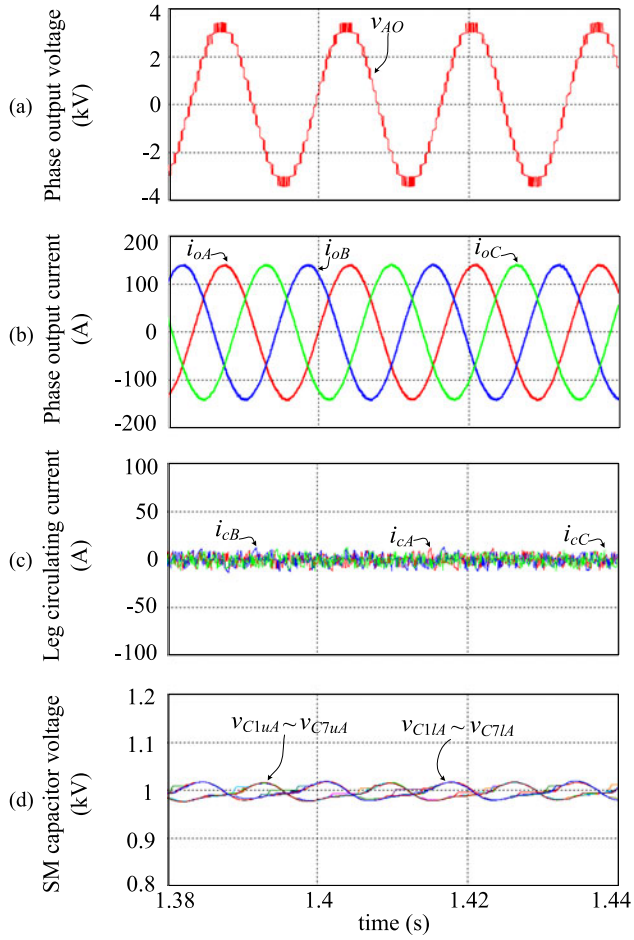

Fig. 6. Simulation waveforms of steady-state operation with the proposed method and $\delta = 1$. (a) Phase-A output voltage, (b) three-phase output currents, (c) circulating currents of the MMC, and (d) phase-A SM capacitor voltages.

MMC, shown in Fig. 6(d), are balanced around its reference voltage. The steady-state simulations confirm the correct operation of the MMC with the proposed method.

The dynamic response of the system to a 72% output power decrement (700–200 kW), managed by reducing the peak output current references from 140 A to 78 A at $t = 1.52$ s, is displayed in Fig. 7. As observed in Fig. 7(a), the number of output voltage levels decreases rapidly from 15 to 9. Thus, the THD of the output currents shown in Fig. 7(b) increases from 0.85% to 1.53%. The circulating currents of the MMC appearing in Fig. 7(c) continue to be suppressed after the step change in the output power. In Fig. 7(d), the SM capacitor voltages can continue to be balanced at the reference value with a reduced voltage oscillation because of the reduction in the power present in the arms of the MMC. The correct operation of the proposed method with MPC was verified for the step response to the output power.

The FMPC, originally presented in [22] for the $N + 1$ case, has been extended to its $2N + 1$ output voltage levels configuration and its simulation results are displayed in Fig. 8. The FMPC's algorithm for $2N + 1$ levels is realized by including to the control options look-up table the control options whose s_j are $N + 1$ and $N - 1$, as explained in Fig. 5; thus, the FMPC

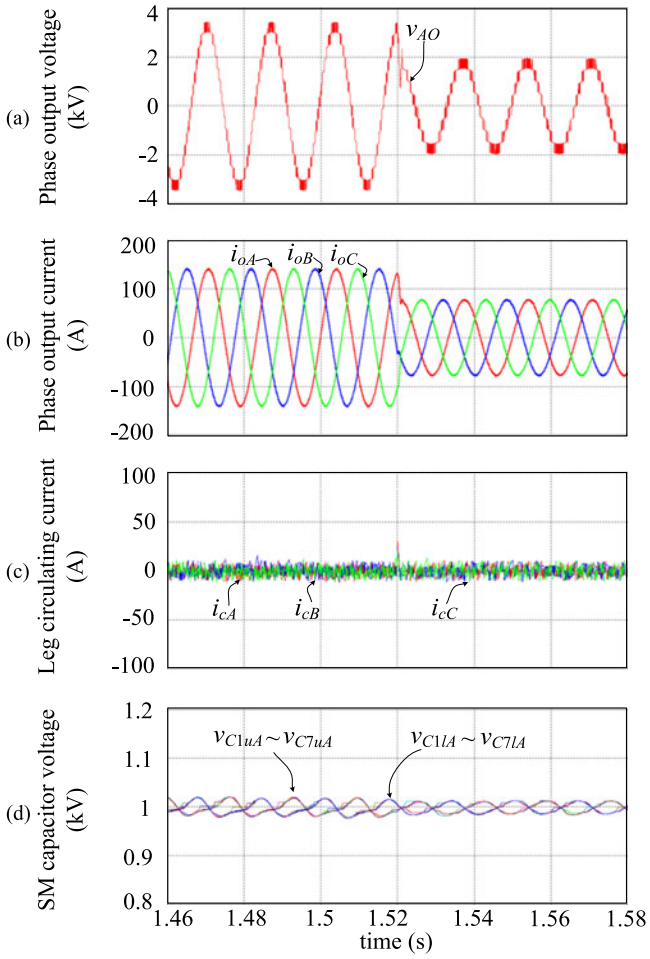

Fig. 7. Simulation waveforms of dynamic response with the proposed method and $\delta = 1$. (a) Phase-A output voltage, (b) three-phase output currents, (c) circulating currents of the MMC, and (d) phase-A SM capacitor voltages.

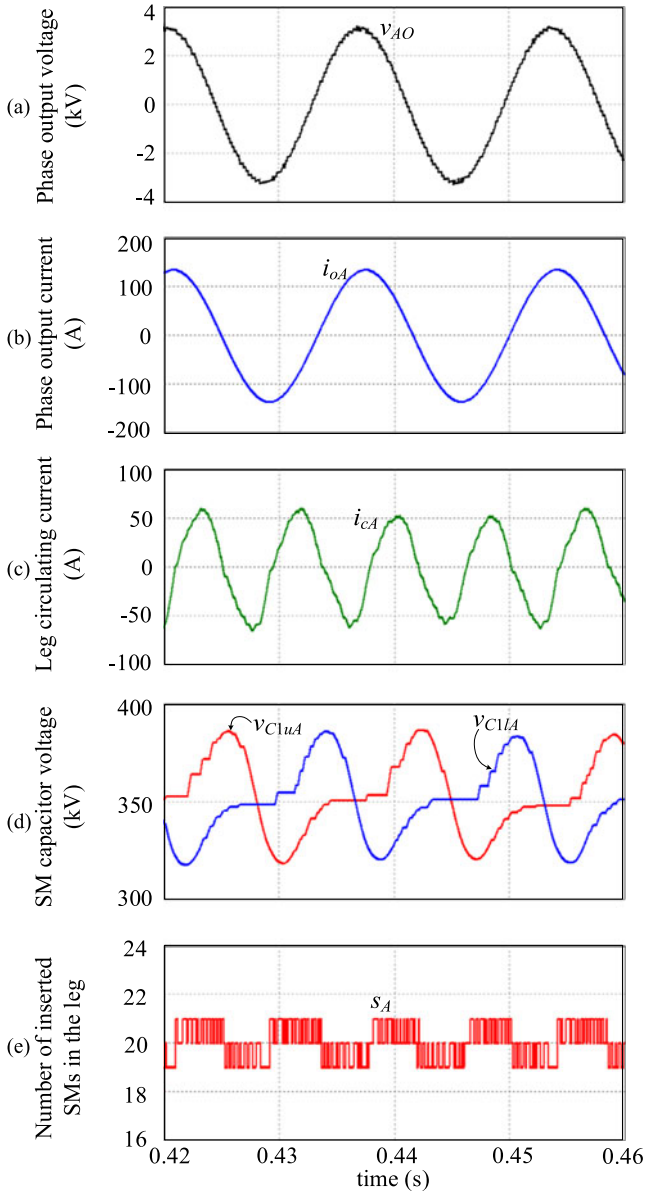

Fig. 8. Simulation waveforms of the FMPC method with $2N + 1$ output voltage levels ($N = 20$). (a) Phase-A output current, (b) phase-A output current, (c) leg-A circulating current, (d) SM capacitor voltages in upper and lower arms, and (e) sum of insertion indexes in leg A.

runs five control options every sampling time. However, this increases the computational complexity per control option of the FMPC as it will be shown later in the paper. A 41-level MMC ($N = 20$) with the same parameters listed in Table III is used for the simulation. Even though the FMPC has great performance in MMCs with low number of SMs, its controllability on the circulating currents cannot be guaranteed in MMCs with larger number of SMs, as shown in Fig. 8(c). Furthermore, its $N + 1$ output voltage level application will have lower performance than Fig. 8(c) in terms of circulating current suppression. Fig. 8(d) shows the sum of the insertion indexes that are applied to the system by the controller.

The proposed method and the effect of the sum boundary on the controllability of the system is presented in Fig. 9. Similar to the FMPC in Fig. 8, $N = 20$ and the same parameters listed in Table III are adopted for the simulation. We can observe that, initially, the preselection algorithm only generates the control options limited by $\delta = 1$ ($\psi = 5$). As a result, the MPC is unable to effectively suppress the circulating currents as in the FMPC. At time $t = 0.44$ s, the preselection algorithm is changed to be limited by $\delta = 3$ ($\psi = 11$). We can see that the MPC algorithm is rapidly able to suppress the circulating currents by using $s_j = N + 3$ in the transient time. However, as seen in the steady-state operation, the controller can handle correct control with only $\delta = 2$. This verifies the derivations in the Appendix.

V. Experimental Validation

A practical single-phase prototype for the MMC, shown in Fig. 10(a), was built. The software was implemented on a digital signal processor (DSP) board (TMS320F28335), which receives the sensed signals from arm currents and SM capacitor voltages, and outputs the gating signals to the MMC, as seen in Fig. 10(b). The interconnections of the single-phase prototype are shown in Fig. 10(c). For an effective practical implementation of the MPC, the delay compensation method for two-level voltage

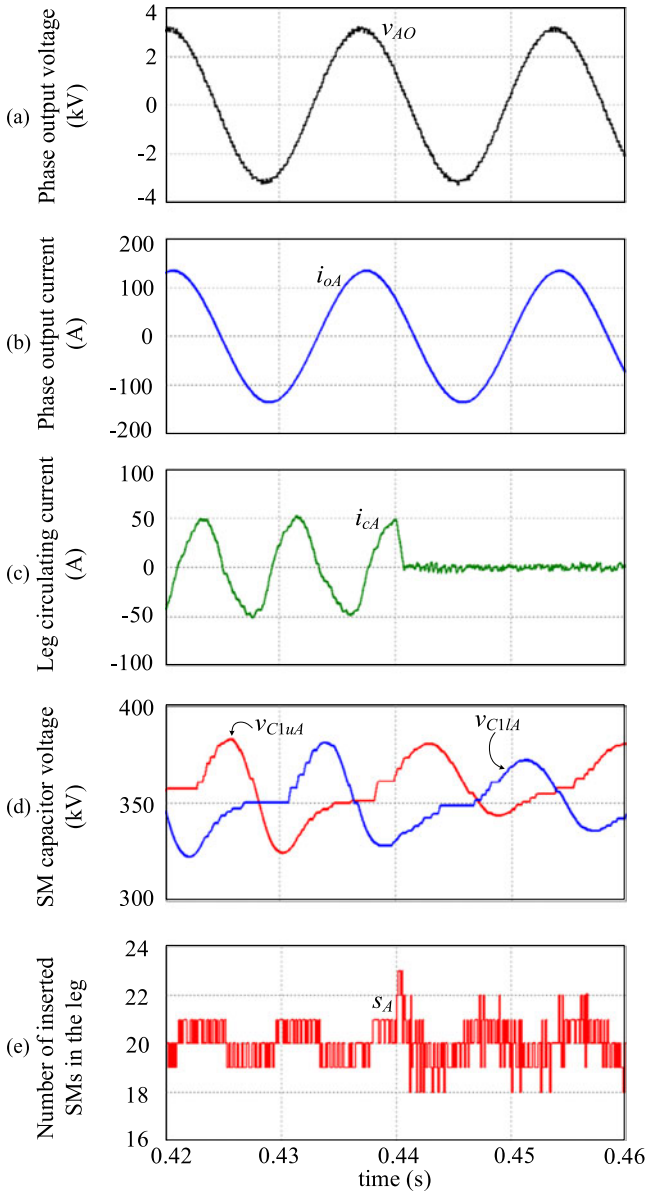

Fig. 9. Simulation waveforms of the proposed method and the effects of δ on the controllability of the circulating currents $(N = 20)$. (a) Phase-A output current, (b) phase-A output current, (c) leg-A circulating current, (d) SM capacitor voltages in upper and lower arms, and (e) sum of insertion indexes in leg A.

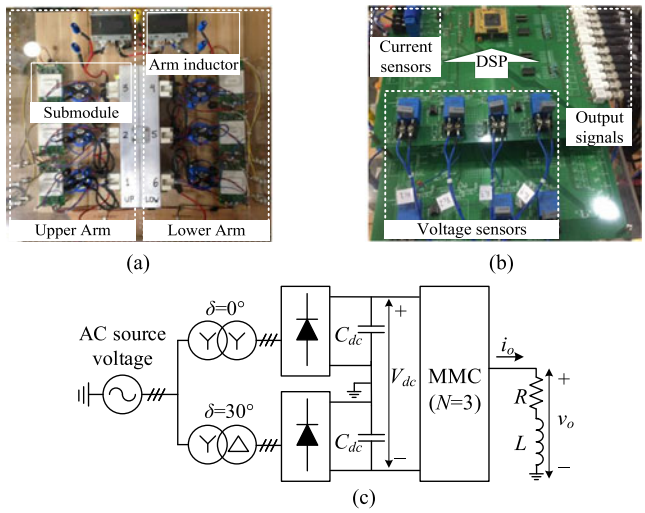

Fig. 10. Experimental setup of the single-phase MMC. (a) Single-phase prototype, (b) control board, and (c) circuit diagram of the experimental setup.

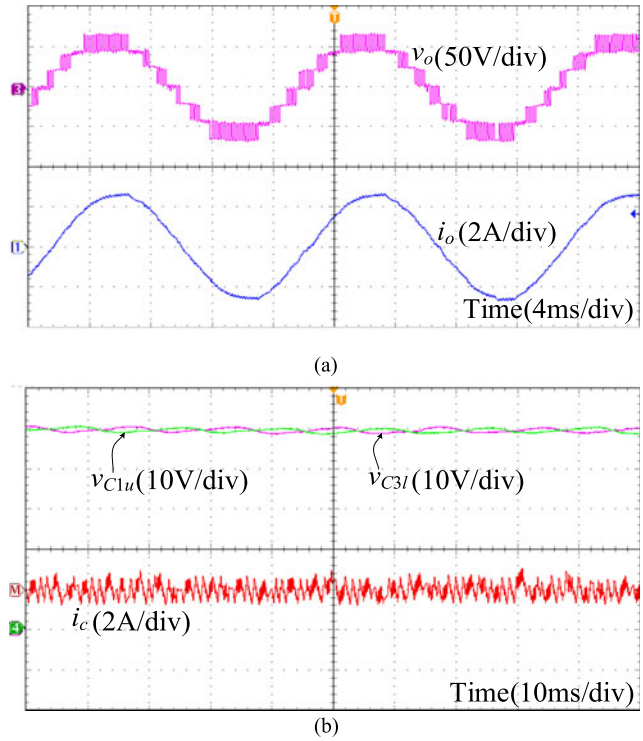

Fig. 11. Experimental waveforms of steady-state operation with the proposed method. (a) Output voltage v_o and output current i_o, and (b) circulating current and SM capacitor voltages.

source inverters presented in [29] and [30] is adopted in this study. The parameters used in the experiments are listed in Table III.

Fig. 11 depicts the experimental results of the MMC operation with the preselection algorithm for MPC. The output voltage and output current are shown in Fig. 11(a). The output voltage can successfully produce seven levels $(2N + 1)$, and the THD of the output current is 1.9%. Fig. 11(b) displays the circulating current and SM capacitor voltages in the upper and lower arm of the MMC. The suppression of the circulating currents and proper balancing of the SM capacitor voltages are verified.

The dynamic response to a reduction in the output power from 100 to 40 W in the experimental system is displayed in Fig. 12. The proper reduction in output voltage levels and tracking of the new reference current after the step change is shown in Fig. 12(a). After the step change, the circulating current continues to be suppressed, while the SM capacitor voltages remain balanced, as shown in Fig. 12(b).

The step change to the low-frequency operation is presented in Fig. 13. The operating frequency is reduced from 60 to 20 Hz in the experiment. It is observed that the controller continues to produce $2N + 1$ output voltage levels and maintains good

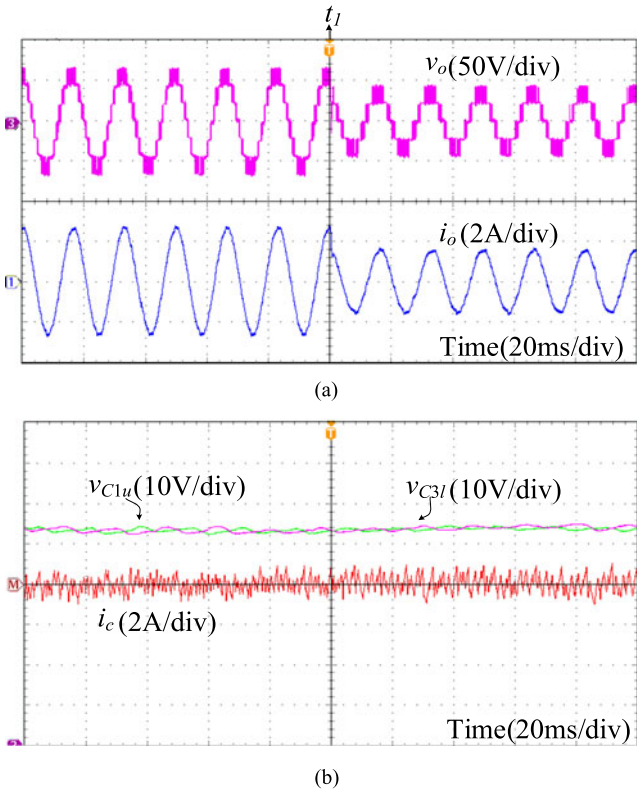

Fig. 12. Experimental results of the dynamic performance of the proposed method with a reduction in output power. (a) Output voltage v_o and output current i_o, and (b) circulating current and SM capacitor voltages.

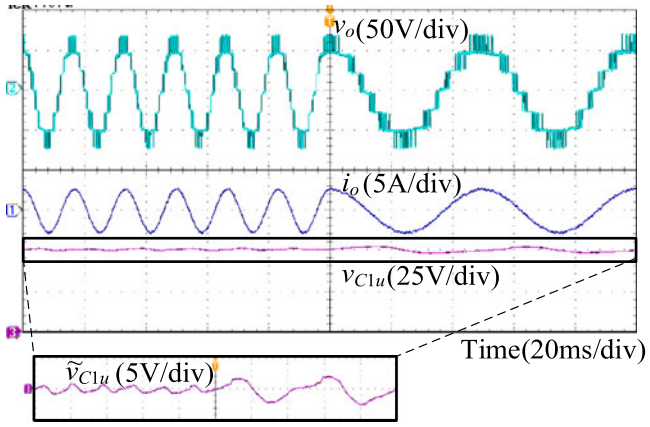

Fig. 13. Experimental results of the change of frequency of operation of the MMC from 60 to 20 Hz.

performance in its output current. The SM capacitor voltage is zoomed to show its ac fluctuation. As expected in the low-frequency operation range, the peak-to-peak voltage fluctuation of the SM capacitance is increased. This increase is proportional to the reduction in frequency [8]

The computational complexity in this paper is presented in terms of DSP clock cycles. The FMPC presented in [22] is compared to the proposed method in Table IV. For the sake of a fair comparison, both methods must evaluate five control options every sampling instant and must be able to generate $2N+1$ output

TABLE IV
COMPUTATIONAL COMPLEXITY OF THE PROPOSED METHOD AND THE FMPC

Strategy	Control options evaluated per sampling time	DSP cycles per one control option in the MPC loop
Proposed Method ($\delta = 1$)	5	181
FMPC ($2N+1$)	5	8132

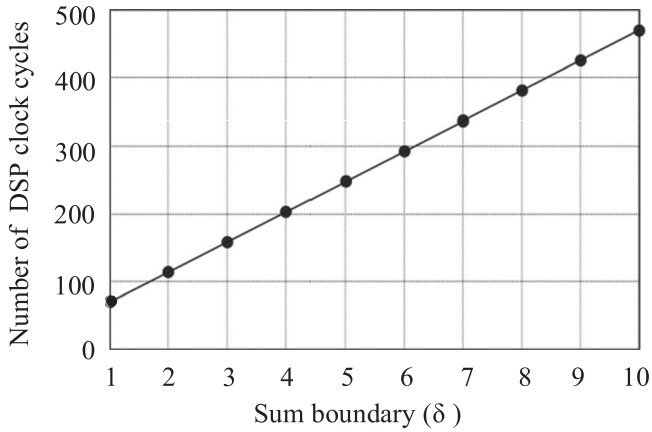

Fig. 14. Effect of the increase in the sum boundary on the computational burden of the proposed preselection algorithm.

voltage levels. Thus, the sum boundary δ was set to 1 ($\psi = 5$) in the proposed method, and the FMPC was implemented to generate $2N+1$ output voltage levels. When one control option is executed by the MPC loop of the proposed method, 181 DSP clock cycles are required, which translates to 1.2 μs. On the other hand, when one control option is executed in the FMPC, 8132 DSP clock cycles are required, meaning 54.2 μs. The proposed method dramatically improves the computational complexity of the FMPC with $2N+1$ output voltage levels. This is because FMPC with $2N+1$ output voltage levels requires five branches of MPC loops, which are accessed by complex conditionals. If the control options whose s_j are $N+2$ and $N-2$ were added to the FMPC, two additional MPC branches would be added and the computational complexity will be further aggravated. Fig. 14 shows that the number of DSP clock cycles required by the preselection algorithm increases linearly when the sum boundary δ is incremented. However, we can observe that this increment does not have a significant impact compared to the computational burden of the proposed MPC algorithm in Table IV because the preselection operation is carried out one time per sampling instant.

VI. CONCLUSION

This paper proposed a preselection algorithm to reduce the computational load in a single MPC loop for MMCs. The proposed algorithm generates a greatly reduced number of control options to be evaluated by the MPC in the next sampling time. Thus, it does not require the look-up table containing all control options in the MMC. In addition, the proposed method along with the MPC can generate $2N+1$ output voltage levels with

low dv/dt while being able to suppress the circulating currents effectively in MMCs with substantial number of SMs. The controllability of the output current, circulating current, and SM capacitor voltage balancing by the proposed preselection method with the MPC was verified with steady-state and dynamic responses in simulations and experiments. The study has shown a significant reduction in the computational complexity of the MPC loop compared to the conventional FMPC method. Additionally, the proposed preselection algorithm can maintain low computational complexity when the number of control options to generate is increased.

APPENDIX

Equation (12) has shown that the upper and lower arm voltages in the phase j of the MMC are derived by means of the insertion indexes and the voltages in the SM capacitors. Furthermore, as observed in [8], the energy fluctuation in the arms of the MMC, which is directly proportional to the SM capacitor voltage fluctuation, contains a fundamental and second-order harmonic component. To simplify the analysis, a unity modulation index and zero phase lag angle are considered in [8, eq. (8)]. Thus, the magnitude of the harmonic component is half the fundamental component in the SM capacitor voltages. This produces the arm voltages

$$v_{lj}^{p}(k) = n_{lj} \times \left[\frac{V_{\rm dc}}{N} - \hat{V}_f \sin\left(2\pi f \cdot kT_{\rm sp}\right) - \frac{\hat{V}_f}{2}\sin\left(4\pi f \cdot kT_{\rm sp}\right)\right] \tag{A1}$$

$$v_{uj}^{p}(k) = n_{uj} \times \left[\frac{V_{\rm dc}}{N} + \hat{V}_f \sin\left(2\pi f \cdot kT_{\rm sp}\right) - \frac{\hat{V}_f}{2}\sin\left(4\pi f \cdot kT_{\rm sp}\right)\right] \tag{A2}$$

where $\hat{V}_f$ is the fundamental component in the SM capacitor voltages.

Fig. 15 shows the oscillation of an SM in the upper arm of the MMC. It is observed that the magnitude of the fundamental component is approximately 39% of the peak-to-peak fluctuation in the SM capacitor voltage over a fundamental period ($\hat{V}_f \approx 0.39\Delta V_C$). Assuming a typical voltage tolerance band of 10% in each SM capacitor voltage, ($\Delta V_C = 0.1V_{\rm dc}/N$) $\hat{V}_f$ can be deduced.

We can rewrite (11) by substituting (A1) and (A2) into it as follows:

$$i_{cj}(k+1) = \frac{T_{\rm sp}V_{\rm dc}}{2L_a} \times \left[1 - \frac{s_j}{N} + (N+s_j)\frac{\hat{V}_f}{2V_{\rm dc}}\sin\left(2\pi f \cdot kT_{\rm sp}\right)\right] + i_{cj}(k). \tag{A3}$$

Note that the first part of (A3), depending on its sign, is responsible for the increment or decrement of the circulating currents in the next sampling time $k+1$. Thus, the key part in the controllability of the circulating current lies in this expression and its sign, which is rewritten as follows:

$$\gamma = 1 - \frac{s_j}{N} + (N+s_j)\frac{\hat{V}_f}{2V_{\rm dc}}\sin\left(2\pi f \cdot kT_{\rm sp}\right). \tag{A4}$$

To maintain the controllability of the circulating currents, γ should be able to produce positive and negative signs at any time to increase and decrease the circulating currents in the next sampling instant, respectively. Considering one of the worst-case scenarios, when the ac component in (A4) reaches its maximum negative magnitude ($\sin\left(2\pi f \cdot kT_{\rm sp}\right) = -1$), γ must be able to produce a positive value with the same or a higher value of the ac component. By following this condition and replacing sj by $N+\delta$ in (A4), the constraint for δ is derived as follows:

$$\delta \geq \text{ceil}(0.075N) \tag{A5}$$

where ceil is a function that returns the closest higher integer to its input. Thus, it can be recommended that, to maintain controllability of the circulating currents, δ should be at least 7.5% of N.

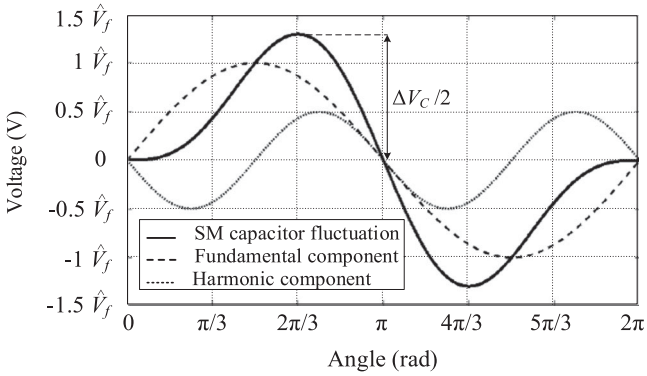

Fig. 15. Waveform of the fluctuation in an SM capacitor voltage in the lower arm over a fundamental period.

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