Improved High Step-Up *Z*-Source DC–DC Converter With Single Core and ZVT Operation

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***Abstract*—A previously proposed high step-up dc–dc converter based on *Z*-source circuit is improved such that conduction losses of the converter and current stress of its power switch are reduced. The improved converter contains only one magnetic core and all of the inductors are coupled. It is shown that using one core allows us to use windings with lower copper resistance that results in reducing resistive losses of the coupled inductors. Also, by rearranging two diodes of the converter, the switch current and its conduction loss are reduced. In addition, a previously proposed auxiliary circuit for zero-voltage-transition operation is employed with a minor modification that makes it possible to use a relatively large snubber capacitor that significantly decreases current–voltage overlap of the main switch at turn-off instant. Improvement in the overall efficiency of the presented structure over the existing high step-up *Z*-source converter is demonstrated by implementing a 100-W prototype of each converter for 30- to 300-V voltage conversion.**

***Index Terms*—Coupled inductor, dc–dc converter, high step-up, impedance-source, photovoltaic (PV), single magnetic core, switched capacitor, zero voltage transition (ZVT), *Z*-source.**

I. Introduction

EMPLOYMENT of renewable energy sources has become a critical requirement in today's world regarding the concerns about the fossil fuels. Among the renewable sources, solar energy has attracted much attention due to its availability in almost everywhere. A drawback of photovoltaic (PV) cells relates to their low output voltage that requires to be increased in many applications. A possible solution is to use a dc–dc power converter with a high voltage gain to boost up the low voltage of PV panels to the desired level. So far, a lot of research has been conducted on proposing new circuit topologies suited for the so-called high step-up applications [1]–[7]. Some of the known techniques used for extending the voltage conversion ratio of the converters include cascading the converters, integrating them such that their outputs are in series [1]–[3], using the coupled inductors [4], using the switched capacitors [5]–[7], and their combinations.

Z-source converter is one of the popular circuit topologies that has a higher voltage gain compared with the regular boost converter [8]. Its concept was first proposed by Peng in 2003 [9]. In the traditional *Z*-source converter, the input voltage source and the output voltage have separate ground references. However, there is a new structure for *Z*-source converter with a common ground between input and output [10]. Recently, so many converters derived from the *Z*-source topology have been proposed representing some improvements in voltage gain. A topological review of impedance-source networks is conducted in [11]. Also, Liu *et al.* [12] propose a new family of high step-up converters deduced from these networks. In [13], various *Z*-source networks are combined to develop hybrid *Z*-source converters with enhanced boost factor. Quasi-*Z*-source (QZS) networks are other circuit configurations derived from the *Z*-source topology that are used to develop new converters [14], [15]. For instance, Patidar and Umarikar [16] introduce a nonisolated high step-up converter based on the QZS topology. Also, there are several isolated QZS-based converters that are suited for high-power applications [17]–[20]. A nonisolated high step-up *Z*-source dc–dc converter with coupled inductors and switched capacitors was proposed in 2015 that provides very high voltage gains even with a small turns ratio of the coupled inductors [21]. However, conduction and switching losses of the power switch can limit the converter efficiency.

On the other hand, requirement of using the power converters with high efficiency has led to develop approaches for reducing their total losses. For instance, soft-switching techniques are widely applied to decrease the switching losses. Zero-voltage-transition (ZVT) and zero-current-transition (ZCT) techniques are effective methods in which an auxiliary circuit is employed to provide soft-transition conditions for the semiconductor devices. These methods have extensively been investigated for years and many auxiliary circuits have been introduced. Some of these circuits provide soft-transition conditions only for the main switch and the auxiliary switch operates under hard switching [22], some of them impose extra current or voltage stress on the main switch [23], and some are line or load dependent [24]. Nevertheless, a novel ZVT auxiliary circuit with coupled inductor was introduced in 2007 that provides soft-transition conditions for both the main and auxiliary switches in a wide range of line or load variations without increasing the main switch stress [25].

The main objective of this paper is to improve the previously proposed converter in [21] from the efficiency point of view. For this purpose, the copper resistance of the inductors is reduced by coupling them into one magnetic component. It is shown that how coupling the inductors can reduce their resistance.

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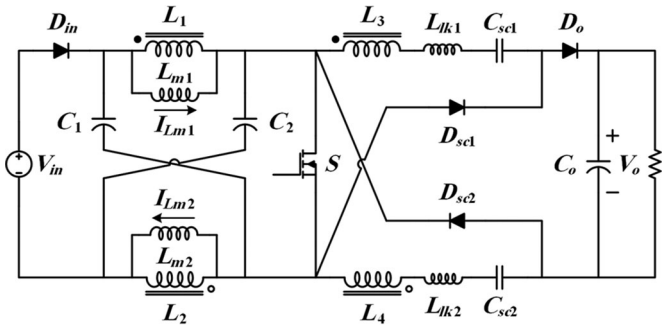

Fig. 1. Previously proposed high step-up *Z*-source dc–dc converter [21].

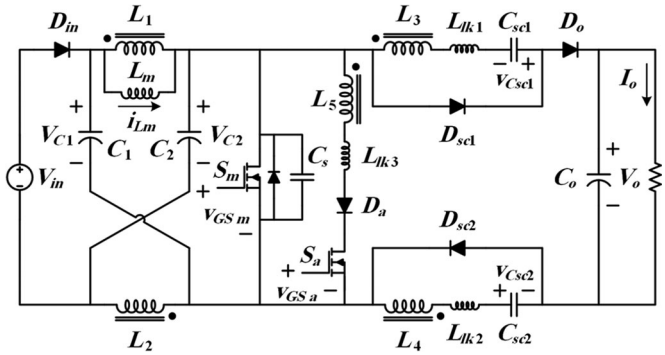

Fig. 2. Improved high step-up *Z*-source converter with ZVT operation.

Therefore, the resistive losses of the inductors, which are quite high especially for the inductors at the converter input, are reduced. Also, the current stress of the power switch is decreased by rearranging the two diodes of the converter that results in lower conduction loss of the switch. Moreover, the converter total losses can further be reduced by using ZVT or ZCT techniques. Here, the ZVT auxiliary circuit proposed in [25] is employed with a minor modification that allows the snubber capacitor to be large enough to significantly decrease the main switch loss at turn-off instant.

Other sections of the paper are organized as follows. Section II introduces the improved converter and presents its operating principles. Mechanism of reducing the conduction losses is discussed in Section III and the employed ZVT auxiliary circuit is analyzed in Section IV. Experimental results measured from the implemented prototypes of the converter proposed in [21] and the improved one are presented in Section V where a comparison between the converters is made. The paper ends with a conclusion given in Section VI.

II. Improved Converter With ZVT Operation

Fig. 1 shows the high step-up *Z*-source dc–dc converter proposed in [21]. This converter contains four inductors out of which L_1 is coupled to L_3, and L_2 is coupled to L_4. The presented converter in this paper, illustrated in Fig. 2, is an improved structure for the mentioned converter that has lower losses. In the improved converter, all the four inductors (L_1–L_4) are coupled together so that they share a common magnetic core. Switched capacitor diodes D_{sc1} and D_{sc2} are rearranged such that they are connected to other points of the converter compared with

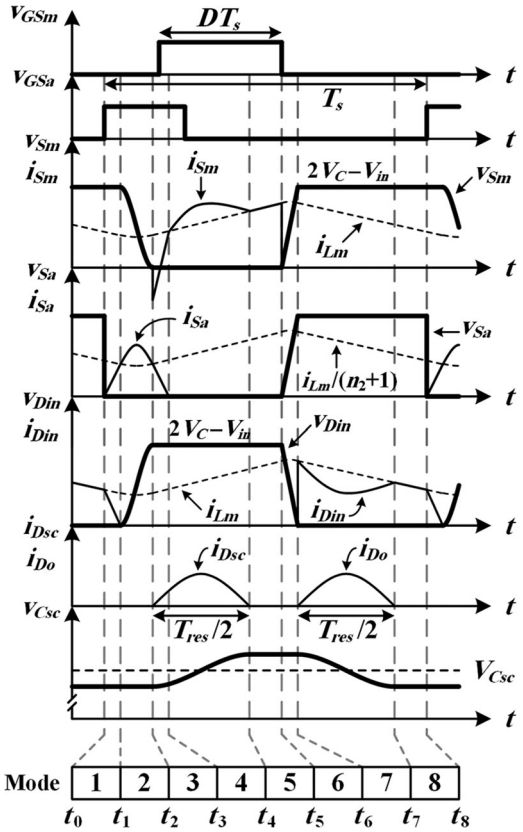

Fig. 3. Theoretical waveforms of the improved converter.

Fig. 1. In addition to the main components of the converter proposed in [21], an auxiliary circuit, consisting of an snubber capacitor C_s, an extra winding L_5 on the existing magnetic core, an auxiliary switch S_a, and an auxiliary diode D_a, is added in parallel with the main switch S_m providing the ZVT operation. In Fig. 2, the coupled inductors are modeled by a magnetizing inductance L_m, three leakage inductances L_{lk1}–L_{lk3}, and an ideal transformer with five windings. For easier analysis, the leakage inductances on the side of L_1 and L_2 are neglected.

A. Operating Principles

The improved converter has eight operating modes under steady-state condition. Fig. 3 shows the theoretical waveforms corresponding to these modes. In the figure, $i_{D\mathrm{sc}}$ is the current of D_{sc1} and D_{sc2}, and $v_{C\mathrm{sc}}$ is the voltage of C_{sc1} and C_{sc2}. Also, voltages V_{C1} and V_{C2} are denoted by V_C. The converter operation is analyzed in continuous conduction mode (CCM) and inductors L_1 and L_2 are assumed to have the same number of turns. Also, capacitors C_1, C_2, and C_o are considered to be large enough that their voltage ripples can be neglected. If inductors L_1–L_5, respectively, have the number of turns equal to N_1–N_5, the turns ratios n_1 and n_2 are defined as follows:

$$n_1 \triangleq N_3/N_1 = N_4/N_2, \quad n_2 \triangleq N_5/N_1. \tag{1}$$

Prior to Mode 1, it is assumed that only the input diode is conducting and the other semiconductor devices are off.

Mode 1 [t_0, t_1]: Before turning the main switch ON, the snubber capacitor must be discharged. As long as the input diode is conducting, the voltage of C_s cannot change. Therefore, the auxiliary switch turns ON and the current of L_{lk3} linearly rises. Linear increase in the current provides the zero-current-switching (ZCS) turn-on condition for S_a and D_a. Simultaneously, the current of $D_{\rm in}$ linearly decreases until it reaches zero. The input diode turns OFF under ZCS condition and this mode ends.

Mode 2 [t_1, t_2]: When the input diode turns OFF, C_s discharges through a resonance with L_{lk3}. Thus, the voltage of C_s reduces to zero and the body diode of S_m conducts.

Mode 3 [t_2, t_3]: Capacitor voltages V_{C1} and V_{C2} are applied to inductors L_1 and L_2, respectively. Polarity of the voltage across L_5 reverses and the current of L_{lk3} linearly decreases. While the body diode of S_m is conducting, the main switch can be turned ON under zero-voltage-switching (ZVS) condition. Reduction in the current of L_{lk3} results in increasing the current through the main switch. Meanwhile, L_{lk1} resonates with C_{sc1} and L_{lk2} resonates with C_{sc2}. These resonances provide the ZCS turn-on condition for D_{sc1} and D_{sc2}. At the end of this mode, the current of L_{lk3} reaches zero so that S_a and D_a turn OFF under ZCS condition.

Mode 4 [t_3, t_4]: During this mode, the main switch is ON and the resonance between the leakage inductances and the switched capacitors continues. Therefore, C_{sc1} and C_{sc2} are charged within a half-cycle of the resonance. The resonant currents through L_3 and L_4 make the main switch current higher than i_{Lm}. When the resonance finishes, D_{sc1} and D_{sc2} turn OFF under ZCS condition.

Mode 5 [t_4, t_5]: This mode is the remaining time of the main switch on-state and it continues until S_m is turned OFF.

Mode 6 [t_5, t_6]: When the main switch turns OFF, snubber capacitor C_s limits the increase rate of its voltage. So, the main switch turn-off takes place under ZVS condition. Once the voltage of S_m reaches to $2V_C - V_{\rm in}$, the input diode turns ON under ZVS condition and the main switch voltage is clamped.

Mode 7 [t_6, t_7]: Voltage polarity of the inductors reverses and D_o starts conducting. Due to the resonance of L_{lk1} and L_{lk2} with C_{sc1} and C_{sc2}, the output diode turn-on happens under ZCS condition. This resonance discharges the switched capacitors and reduces the current of $D_{\rm in}$ lower than i_{Lm}. After a half-cycle of the resonance, the resonant current reaches zero and D_o turns OFF under ZCS condition.

Mode 8 [t_7, t_8]: During this mode, just the input diode is conducting and the output capacitor provides the load current. This mode continues until S_a turns ON again.

B. Voltage Gain

Operation of the improved converter is similar to that of the existing counterpart shown in Fig. 1 except for the ZVT operation. As a result, both converters have the same voltage conversion ratio as given in [21], which is given as follows:

$$M = \frac{V_o}{V_{\rm in}} = \frac{2n_1 + 1}{1 - 2D}, \qquad \text{for} \quad D < 0.5 \tag{2}$$

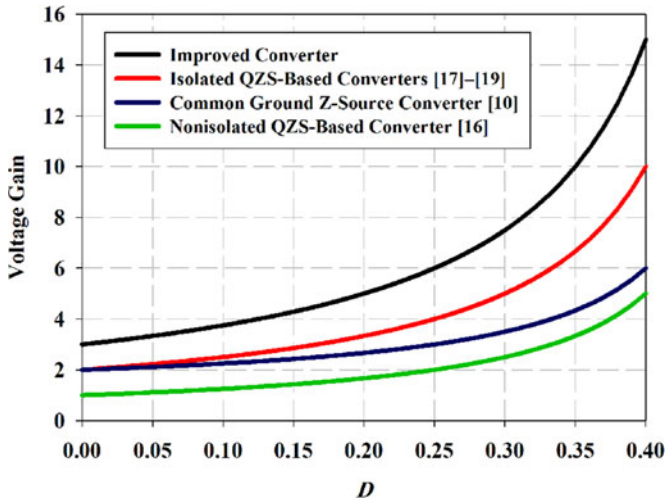

Fig. 4. Voltage gain of the converters in terms of various values of *D*.

where *D* is the operating duty cycle of the main switch as indicated in Fig. 3. According to (2), the voltage gain of this converter is inversely proportional to 1–2*D* that restricts the operating duty cycle below 0.5. Whereas, the high step-up converters based on the boost topology have a voltage conversion ratio inversely proportional to 1–*D*. Equation (2) is plotted in Fig. 4 in terms of various values of *D* for constant n_1 equal to 1. Furthermore, the voltage gains of the other *Z*-source-based high step-up converters proposed in [10] and [16]–[19] are shown in the figure. As observed, the improved converter can provide higher voltage conversion ratios compared with the others.

III. Mechanism of Reduction in Conduction Losses

In comparison with the existing converter shown in Fig. 1, the improved structure has two main differences: the use of one magnetic core instead of two cores and the rearrangement of the switched capacitor diodes. These structural differences result in lower conduction losses that are analyzed in this section.

A. Effect of Using One Magnetic Core

It is theoretically shown that how using one magnetic core in the improved converter reduces the wire length and, consequently, the resistance of the inductors.

Generally, the minimum number of wire turns needed for an inductor to avoid its core from saturation is directly proportional to its inductance L and the maximum current I_{Lp}, and it is inversely proportional to the core cross-sectional area A_c as indicated by

$$N \propto L\, I_{Lp}/A_c. \tag{3}$$

Now, it is supposed that the existing and the improved converters are both designed for the same output power P_o, input voltage $V_{\rm in}$, and output voltage V_o such that they operate over an identical CCM range. To compare the minimum number of wire turns required for the inductors of each converter, the three mentioned parameters (inductance, peak current, and core cross-sectional area) must be regarded for their inductors.

To obtain the magnetizing inductance current, the improved converter is considered during the off-time interval of the main switch (Modes 7 and 8). A KCL equation at the input node gives

$$i_{Din} = i_{L1} + i_{Lm} + i_{C1}. \tag{4}$$

Generally, i_{L1} is determined by the current of other inductors due to the magnetic coupling and it can be written as

$$i_{L1} = -\left[i_{L2} + n_1\left(i_{L3} + i_{L4}\right) + n_2 i_{L5}\right]. \tag{5}$$

Within Modes 7 and 8, the inductor currents are given by

$$i_{L2} = i_{C1} + i_{Do}, \quad i_{L3} = i_{L4} = i_{Do}, \quad i_{L5} = 0. \tag{6}$$

Using (4)–(6), i_{Lm} is obtained as

$$i_{Lm} = i_{Din} + \left(2\,n_1 + 1\right) i_{Do}. \tag{7}$$

If (7) is integrated over $[t_6,\, t_8]$, the magnetizing inductance average current is calculated as

$$I_{Lm} = \left[I_{\text{in}} + \left(2n_1 + 1\right) I_o\right] / \left(1\ -\ D\right). \tag{8}$$

Using (2), the above equation is written as

$$I_{Lm}\left(I_o\right) = \frac{1 + \eta\left(1 - 2\,D\right)}{\eta\left(1\ -\ D\right)}\ M\,I_o \tag{9}$$

where η is the converter efficiency and $I_{Lm}(I_o)$ indicates that I_{Lm} is a function of I_o. According to (9), for a given input and output voltage, I_{Lm} linearly varies with the output current. If the converter losses are neglected, (9) is simplified to

$$I_{Lm}\left(I_o\right) \cong 2\,M\,I_o. \tag{10}$$

Following a similar procedure for the converter of Fig. 1, the magnetizing inductance average currents I_{Lm1} and I_{Lm2} are obtained as [21] follows:

$$I_{Lm1} = I_{Lm2} = \frac{1 + \eta\left(1 - 2\,D\right)}{2\,\eta\left(1\ -\ D\right)}\ M\,I_o. \tag{11}$$

Comparison of (9) with (11) implies that the magnetizing inductance average current of the improved converter is twice the average current of each magnetizing inductance in the existing counterpart.

On the other hand, the magnetizing inductance must be designed such that it ensures the converter operation in CCM over the entire range of the output current. For this, the following equation can be employed as follows:

$$L_m = \left(DV_C\right) / \left(f_s \Delta I_{Lm}\right) \tag{12}$$

where $f_s = 1/T_s$ is the switching frequency and ΔI_{Lm} is the current ripple of L_m over a switching cycle. If $I_{o\,\min}$ is the minimum output current, ΔI_{Lm} must be chosen such that

$$\Delta I_{Lm} \le 2\,I_{Lm}\left(I_{o\,\min}\right). \tag{13}$$

In accordance with (9)–(13), it can be concluded that if both the converters are assumed to operate in CCM over the same output current range, the improved converter needs a magnetizing inductance that is a half of each magnetizing inductance required for the existing counterpart.

For better comparison, it is assumed that the magnetic components in each of the converters occupy the same space. Therefore, instead of two cores of the existing converter, one core with an approximately double cross-sectional area can be used for the improved structure. In other words, if the existing converter contains two cores with the cross-sectional area A_c, the improved structure uses one core with the cross-sectional area $2A_c$.

Based on the foregoing discussion, (3) signifies that inductor L_1 in the improved converter needs a half of wire turns required for the corresponding inductor in the existing counterpart. Regarding the same turns ratio for the coupled inductors, all the inductors of the improved converter will have a half of wire turns needed for the respective inductors in the existing counterpart.

Since the improved converter uses a magnetic core with a double cross-sectional area, the length of each turn of wires on this core is approximately $\sqrt{2}$ times the wire length on the smaller cores of the existing counterpart.

It is concluded that for the same conditions of output power, voltage gain, CCM range of operation, and volume of the magnetic components, the wire length of each inductor used in the improved converter is $1/\sqrt{2}$ times shorter than that in the existing counterpart. As a result, if the wire thickness of the corresponding inductors is identical, the copper resistance of the inductors in the improved converter will be smaller by the same factor of $1/\sqrt{2}$.

B. Effect of Rearranging the Diodes

In the converter shown in Fig. 1, when the switch turns ON, diodes D_{sc1} and D_{sc2} also conduct and switched capacitors C_{sc1} and C_{sc2} are charged. The charging current of the capacitors passes through the switch as well. However, in the improved converter, the switched capacitor diodes are rearranged such that this current does not pass through the main switch that results in reducing the root-mean-square (RMS) value of its current. According to the operating principles presented in Section II, the main switch current during Modes 4 and 5 is obtained using a KCL equation as

$$i_{Sm} = i_{L1} + i_{Lm} - i_{C2} \tag{14}$$

where

$$i_{L1} = -\left[i_{L2} + n_1\left(i_{L3} + i_{L4}\right)\right] \tag{15}$$

$$i_{L2} = -i_{C2}, \quad i_{L3} = -i_{\text{Dsc1}}, \quad i_{L4} = -i_{\text{Dsc2}}. \tag{16}$$

Using (14)–(16), the current of S_m is written as

$$i_{Sm} = i_{Lm} + 2\,n_1\,i_{\text{Dsc}} \tag{17}$$

where i_{Dsc} denotes the current of D_{sc1} and D_{sc2}. On the other hand, the switch current of the existing converter during its conduction interval is obtained as [21]

$$i_S = i_{Lm1} + i_{Lm2} + 2\left(n\ +\ 1\right) i_{\text{Dsc}} \tag{18}$$

where *n* is the turns ratio of the coupled inductors. To measure the effectiveness of rearranging the diodes in reducing the main switch conduction loss, a quantity denoted by ${\Delta I_{\text{sw}}}^2$ is defined

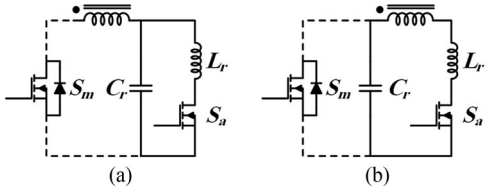

Fig. 5. Auxiliary circuits for ZVT operation. (a) Auxiliary circuit proposed in [25]. (b) Modified auxiliary circuit.

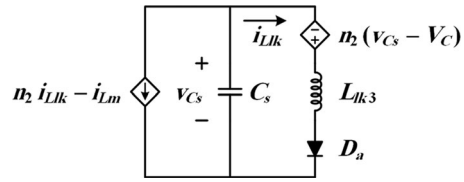

Fig. 6. Equivalent circuit of the improved converter during Mode 2.

as the difference between the square values of the switch RMS currents as

$$\Delta {I_{\rm sw}}^2 \triangleq {I_S}^2 - {I_{Sm}}^2 = \frac{1}{T_s}\int_{T_s} {i_S}^2 dt - \frac{1}{T_s}\int_{T_s} {i_{Sm}}^2 dt \tag{19}$$

where I_S and I_{Sm} are the RMS values of the switch current in the existing and the improved converters, respectively. If the defined quantity $\Delta {I_{\rm sw}}^2$ is multiplied by the switch on-resistance, it implies the amount of reduction in the switch conduction loss achieved by the improved converter. Using (17)–(19) and some mathematical manipulations, $\Delta {I_{\rm sw}}^2$ is approximately calculated as

$$\Delta {I_{\rm sw}}^2 \cong \left[(2n_1+1)\left(T_s/T_{\rm res}\right)\pi^2 + 8M\right] {I_o}^2 \tag{20}$$

where $T_{\rm res}$ is the resonant period of L_{lk1} with C_{sc1} or L_{lk2} with C_{sc2} as indicated in Fig. 3. Equation (20) signifies that $\Delta {I_{\rm sw}}^2$ is a quadratic function of the output current so that the effect of diode rearrangement on loss reduction is more revealed in high output currents.

IV. Analysis of the ZVT Auxiliary Circuit

As shown in Fig. 5(a), the ZVT auxiliary circuit proposed in [25] is placed across the main switch S_m and it contains a resonant capacitor C_r, a resonant inductor L_r, an auxiliary unidirectional switch S_a, and a winding coupled with the main inductor of the converter.

Generally, in an auxiliary circuit with ZVT operation, there is a capacitor that limits the increase rate of the main switch voltage at turn-off instant. As the capacitance of this capacitor increases, the current–voltage overlap of the main switch at turn-off instant reduces. However, this results in extending the time interval of the capacitor discharge through a resonance with the resonant inductor before turning the main switch ON. Therefore, the operating duty cycle of the main switch is restricted. If the auxiliary circuit proposed in [25] is modified such that the resonant capacitor is placed across the main switch, the circuit shown in Fig. 5(b) is obtained, which is the same auxiliary circuit used in the improved converter of Fig. 2. This modified circuit represents a desired feature: the equivalent capacitance shown by the resonant inductor during the capacitor discharge becomes smaller. This makes it possible to use a larger capacitance while its discharge time remains sufficiently short.

To demonstrate the stated feature, the improved converter is considered during Mode 2 in which the snubber capacitor C_s discharges. The simplified equivalent circuit of the converter in this situation is illustrated in Fig. 6. As observed, inductor L_5 acts as a dependent voltage source and a series inductance L_{lk3} while the Z-source network is treated as a dependent current source. According to the equivalent circuit, the resonant frequency f_0 is calculated as

$$f_0 = (n_2+1)/\sqrt{L_{lk3}C_s}. \tag{21}$$

This equation signifies that the equivalent capacitance shown by L_{lk3} is reduced by a factor of $1/(n_2+1)^2$. The capacitor C_s should be large enough to reduce the current–voltage overlap of the main switch. Its value can be designed just like a regular snubber capacitor given by

$$C_s = (I_{Lm}\, t_r)/(2V_C - V_{\rm in}) \tag{22}$$

where t_r is the desired rise time of the switch voltage. As the turns ratio n_2 increases, the equivalent capacitance shown by L_{lk3} reduces more. However, the current of L_{lk3} rises and drops faster that can inversely affect the ZCS operation of S_a and D_a.

TABLE I
Common Components Employed in the Prototypes

Component	Part number or value
Main switch S_m or S	IRFP260
Input diode $D_{\rm in}$	MBR20150
Diodes D_{sc1}, D_{sc2}, and D_o	MUR460
Capacitors C_1 and C_2	47 μF/100 V
Switched capacitors C_{sc1} and C_{sc2}	470 nF/100 V
Output capacitor C_o	22 μF/400 V

V. Experimental Results

To compare the performance of the existing and the improved converters in practice, a laboratory prototype of each converter is implemented and experimental results are provided. The converters are both designed to convert 30-V input voltage to 300-V output voltage with nominal power of 100 W and switching frequency of 50 kHz. The common components employed in the prototypes are listed in Table I. In addition to these components, the improved converter uses an auxiliary switch (S_a: IRF840), an auxiliary diode (D_a: MUR460), and a snubber capacitor (C_s = 22 nF/400 V). Also, Table II represents specifications of the coupled inductors used in each converter. It is observed in Fig. 7, which shows the photograph of the implemented prototypes, that the existing converter uses two magnetic cores, whereas the improved structure has one larger core. Regarding the core parameters listed in Table III, the magnetic cores of both converters occupy the same space. Also, the core of the

TABLE II
PARAMETERS OF THE COUPLED INDUCTORS

Parameter	Existing converter	Improved converter
Magnetizing inductance	$L_{m1} = L_{m2} = 300\ \mu$H	$L_m = 150\ \mu$H
Leakage inductance	$L_{lk1} = L_{lk2} = 8\ \mu$H	$L_{lk1} = L_{lk2} = 6\ \mu$H, $L_{lk3} = 10\ \mu$H
Turns ratio	$n = 1$	$n_1 = n_2 = 1$

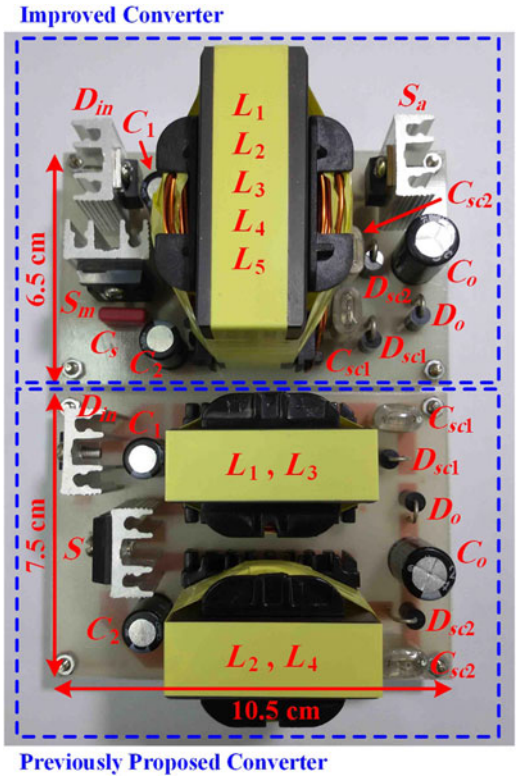

Fig. 7. Photograph of the implemented prototypes.

TABLE III
PARAMETERS OF THE MAGNETIC CORES

Parameter	Existing converter	Improved converter
Core	EE42 × 42	EE55 × 55
Core size	42 × 30 × 50 mm	55 × 35 × 60 mm
Cross-sectional area	182 mm^2	354 mm^2

improved converter has a cross-sectional area that is two times the area of each core in the existing counterpart.

Experimental waveforms of the improved converter under the full-load condition are illustrated in Fig. 8. As shown in Fig. 8(a), voltage of the main switch becomes zero prior to the switch turn-on providing the ZVS condition. It is observed from the enlarged waveforms that discharging the snubber capacitor takes 0.7 μs. Whereas a half-cycle of the resonant period of C_s and L_{lk3} is equal to 1.5 μs. Also, at the switch turn-off instant, its voltage and current have a slight overlap that reduces the turn-off loss. Waveforms of the auxiliary switch are shown in

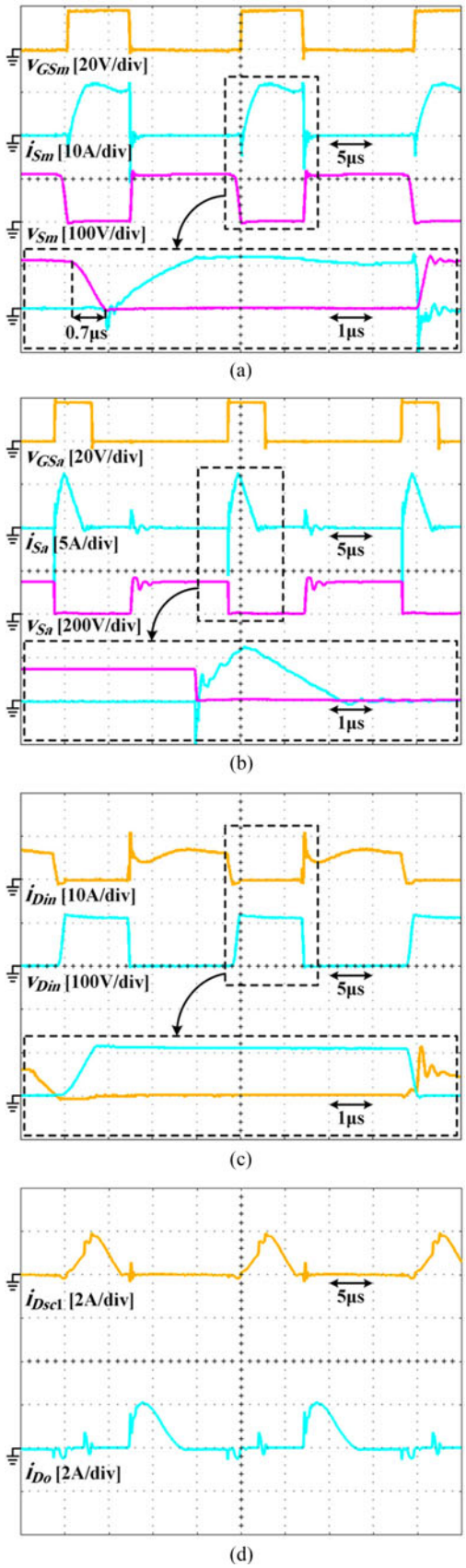

Fig. 8. Experimental waveforms of the improved converter. (a) Main switch S_m. (b) Auxiliary switch S_a. (c) Input diode $D_{\rm in}$. (d) Switched capacitor diode D_{sc1} and output diode D_o.

TABLE IV
WINDING PARAMETERS OF THE COUPLED INDUCTORS

Parameter	Existing converter		Improved converter	
	L_1, L_2	L_3, L_4	L_1, L_2	L_3, L_4, L_5
Number of wire turns	40	40	20	20
Wire length [cm]	340	350	240	255
Wire thickness [mm]	1	0.6	1	0.6
DC resistance [Ω]	0.15	0.45	0.10	0.30

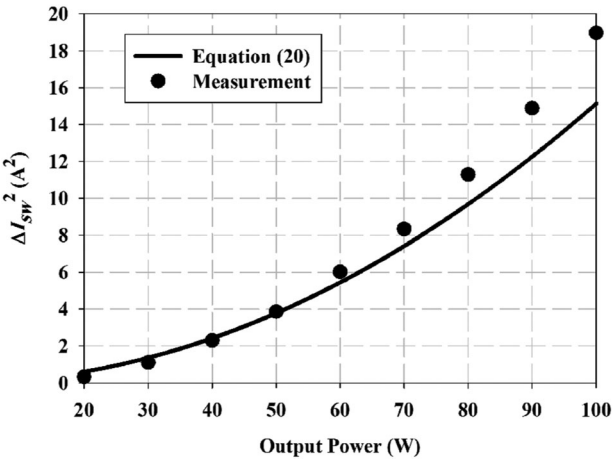

Fig. 9. $\Delta I_{\rm sw}^2$ in terms of various output power levels.

Fig. 8(b). As observed, the switch turns ON and OFF under ZCS condition. Fig. 8(c) shows the input diode waveforms where the soft-switching operation is observed. As illustrated in Fig. 8(d), current of the switched capacitor diodes and the output diode is a half-sinusoidal shape resulting in switching under zero current.

As stated in Section III, employing one magnetic core in the improved converter makes it possible to use the windings with shorter wire length and lower copper resistance. Winding parameters of the coupled inductors including the number of wire turns, the length and thickness of the wires, and their dc resistances are listed in Table IV. As observed, the copper resistance of each inductor in the improved converter is lower than the resistance of the corresponding inductor in the existing counterpart.

To demonstrate the effect of rearranging the switched capacitor diodes on reducing the main switch current, RMS value of the switch current for various output power levels (from 20% to 100% of the nominal power) is measured from each of the implemented prototypes. Thereby, the defined quantity $\Delta I_{\rm sw}^2$ is calculated in practice and the results are plotted in Fig. 9. Furthermore, the figure shows the theoretical values of $\Delta I_{\rm sw}^2$ as given in (20). As observed, the measured values match the theoretical ones especially in low output power levels. However, the error due to the approximation used in (20) becomes larger when the output power increases.

Fig. 10 shows the efficiency of the implemented prototypes calculated by measuring the input and output average powers under different load conditions. For better comparison, efficiency of the improved converter is measured with and without ZVT

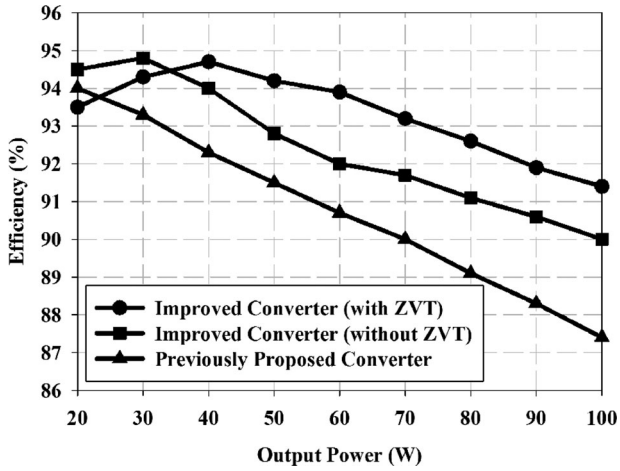

Fig. 10. Efficiency of the prototypes in terms of various output power levels.

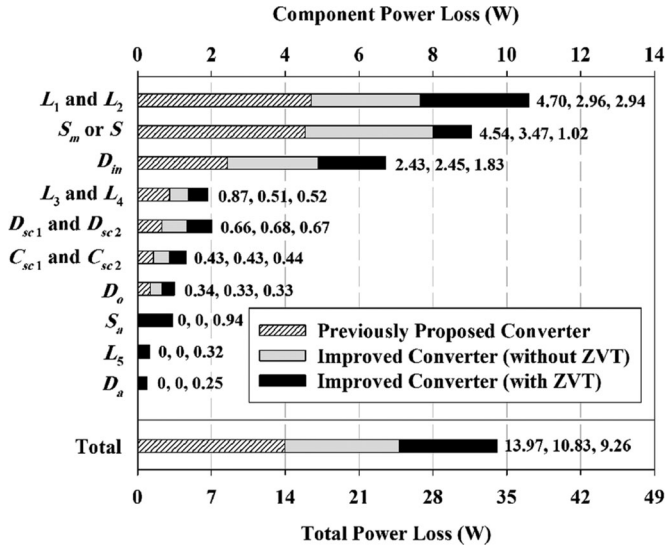

Fig. 11. Loss distribution between the components under full-load condition.

operation. When measuring the efficiency without ZVT operation, the auxiliary switch is kept OFF and the snubber capacitor is removed. As observed, reduction in the copper resistances of the coupled inductors and current reduction of the main switch enhance the converter efficiency. In addition, the ZVT operation further increases the overall efficiency. However, at low power levels, losses of the auxiliary circuit become dominant, which results in degrading the converter efficiency.

To emphasize the efficiency improvement of the new structure with respect to the previously proposed converter, their component losses are compared through simulation. Both converters are simulated using OrCAD PSPICE software under full-load condition for the components given in Tables I and II, and inductor resistances given in Table IV. Loss distribution between the components of each converter is plotted in Fig. 11. In simulation, equivalent series resistances (ESRs) of the capacitors C_{sc1} and C_{sc2} are also included, which are obtained by measurement from the employed capacitors. ESRs of other capacitors are ignored due to their small values. The plot shows that the main

TABLE V
CONDUCTION LOSSES OF THE IMPROVED CONVERTER COMPONENTS

Component	Resistance [Ω]	RMS current [A]	Power loss [W]
Main switch S_m	0.055	4.11	0.93
Auxiliary switch S_a	0.85	1.01	0.87
Inductors L_1 and L_2	0.1	3.85	2×1.48
Inductors L_3 and L_4	0.3	0.92	2×0.25
Inductor L_5	0.3	1.01	0.31
Capacitors C_{sc1} and C_{sc2}	0.25	0.92	2×0.21
Component	Voltage drop [V]	Average current [A]	Power loss [W]
Input diode D_{in}	0.5	3.63	1.82
Auxiliary diode D_a	1.1	0.24	0.26
Diodes D_{sc1} and D_{sc2}	1	0.34	2×0.34
Output diode D_o	1	0.33	0.33

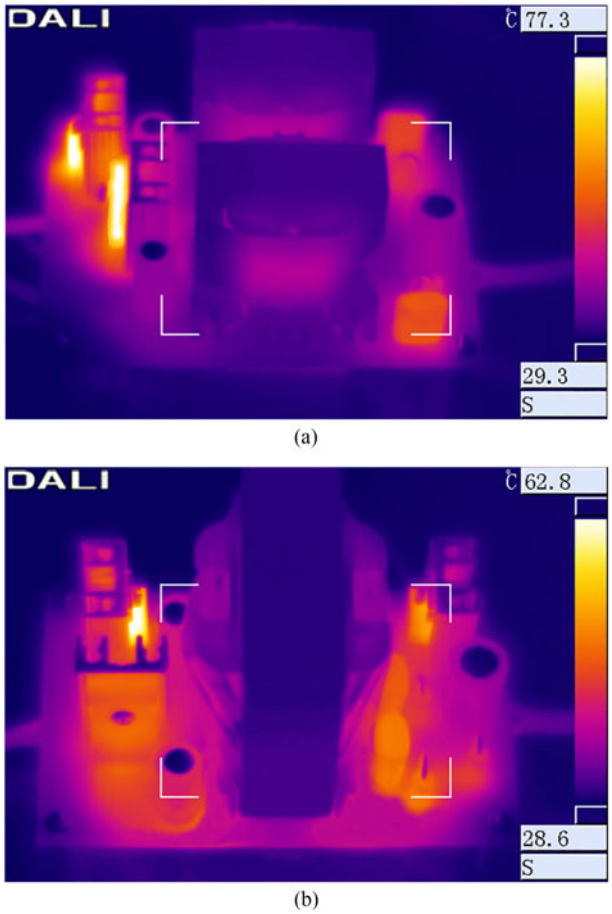

Fig. 12. Thermal photos of the implemented prototypes. (a) Previously proposed converter. (b) Improved converter.

part of power losses in the converter of Fig. 1 are related to the inductors L_1 and L_2, the main switch S, and the input diode D_{in} whose losses are reduced in the improved structure. Moreover, the power losses associated with the auxiliary circuit are less than the total reduced losses gained by ZVT operation.

To further analyze the improved converter losses, conduction losses of the components are approximately calculated under full-load condition based on datasheet parameters and current values. As listed in Table V, resistances of the switches and forward voltage drops of the diodes are extracted from the respective datasheets and the current values are measured from the implemented prototype. Comparing the component losses given in Fig. 11 with the corresponding values of Table V signifies that conduction losses are dominant in the improved structure that is in accordance with soft-switching performance of the converter.

Fig. 12 shows thermal photographs of the implemented prototypes under full-load condition that have been taken with DL700 infrared camera from DALI Technology. As observed in Fig. 12(a), the power switch and the input diode have the highest temperature in the previously proposed converter. The plot shown in Fig. 11 predicts that the inductors dissipate a relatively high power as well. However, their temperature does not rise too much. Since, their size is large and they have good heat exchange with surroundings. According to Fig. 12(b), the main switch of the improved converter has a lower temperature compared to the switch in Fig. 12(a). It should be noted that the maximum temperature in the improved structure is lower than that in the previously proposed converter.

VI. CONCLUSION

This paper presents an improved structure for one of the previously proposed high step-up *Z*-source dc–dc converter to reduce its conduction losses and also a modified ZVT auxiliary circuit is applied to reduce the switching losses. In the improved converter, all the inductors are coupled and only one magnetic core is employed. This makes possible the use of windings with half the number of wire turns and, consequently, wire length of the windings becomes shorter by an approximate factor of $1/\sqrt{2}$. Therefore, resistive losses of the coupled inductors are reduced by the same factor. Furthermore, rearranging the switched capacitor diodes reduces the current of the main switch. As shown, reduction in the conduction loss is a quadratic function of the power level so that the power loss is decreased more in heavy loads. On the other hand, using the ZVT auxiliary circuit with a minor modification enables the circuit to employ a relatively large snubber capacitor to decrease the current–voltage overlap of the main switch at turn-off instant. Improved performance of the presented structure with respect to the existing high step-up *Z*-source converter is emphasized by implementing two identical 100-W prototypes from these converters for 30- to 300-V voltage conversion.

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