Impedance-Based Analysis and Stabilization of Active DC Distribution Systems With Positive Feedback Islanding Detection Schemes

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***Abstract*—Active dc distribution systems are gaining widespread acceptance in modern power distribution grids. Islanding detection is very crucial for safety and protection purposes in active distribution systems; therefore, distributed generators (DGs) are usually equipped with active islanding detection methods to detect grid disconnection conditions. The high penetration level of tightly regulated converters to interface both DGs and loads and the poorly damped *LC* networks structured by the filtering inductors, feeder impedances, and bus capacitors can cause severe stability problems. This paper presents an impedance-based analysis of a grid-connected dc active distribution system, where DGs equipped with active positive feedback islanding detection schemes and a high penetration level of constant power loads (CPLs) are considered. The output impedance of a DG equipped with active islanding detection schemes is derived, and the interactions of the system impedances are discussed to characterize the dynamics of the dc distribution system. Moreover, the performance of multiple DG systems with the islanding detection schemes is investigated and thoroughly addressed. A simple, yet effective, stabilization method is also developed. Detailed time-domain nonlinear simulations and experimental results validate the analytical results.**

***Index Terms*—Active anti-islanding, active damping, constant power loads (CPLs), dc distribution systems, distributed generation, impedance analysis, Nyquist impedance ratio, stability.**

NOMENCLATURE

I_{ref}	Reference current command.
V	Voltage at the point of common coupling (PCC).
I_g	DC grid current.
I_L	DC grid Load current.
$\sim$	Small-signal perturbation.
$*$	Reference voltage and current command for VSC controller.
X^o	Steady-state quantity of $x(t)$.
ω	Positive feedback high-pass filter cut-off frequency.
R_T	Combined filter and ac grid resistance.
L_T	Combined filter and ac grid inductance.
$I^g_{d,q}$, $U^g_{d,q}$, $V^g{}_{Fd,Fq}$	dq-current and voltage in the ac-grid reference frame.
P_s, Q_s	Injected active and reactive power to the ac grid.
ω_g	AC grid angular frequency.
$I_{cd,cq}$, $U_{cd,cq}$, $V_{Fcd,Fcq}$	dq-current and voltage in the converter reference frame.
P_{ext}	External injected power from the dc distribution network to the VSC dc port.
M^o_{cd}, M^o_{cq}	Steady-state duty ratios of the VSC in dq frame.

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I. INTRODUCTION

DIRECT current power distribution systems are intensively emerging into existing power networks because most of the environmentally friendly energy resources and new loads are intrinsically dc or include a dc conversion stage within the power conditioning process [1]–[3]. The research work in the emerging area of dc systems is not complete in many areas. One of the most important problems is the islanding detection in grid-connected dc distribution systems, which is a crucial requirement for the safety of maintenance personnel and to avoid improper operation, which might arise when the grid is unintentionally disconnected [4]. Several passive islanding detection techniques were proposed for ac systems to detect the islanding state [5]–[8]. However, unlike ac systems, dc distribution systems have limited monitoring features because the voltage magnitude is the only signal available for monitoring. Therefore, the positive feedback (PFB) active islanding technique is usually employed for islanding detection in dc systems due to its simplicity and practicality [9].

DC systems have distinct properties such as the tightly regulated nature of the connected loads, which can be viewed by the dc network as constant power loads (CPLs) that insert an incremental negative resistance to the dc network leading to degradation of the system stability [10], [11]. Moreover, dc systems are characterized by the existence of dc bus stabilizing and smoothing filtering capacitors [12], [13], those capacitors with the dc distribution feeder impedance construct poorly damped

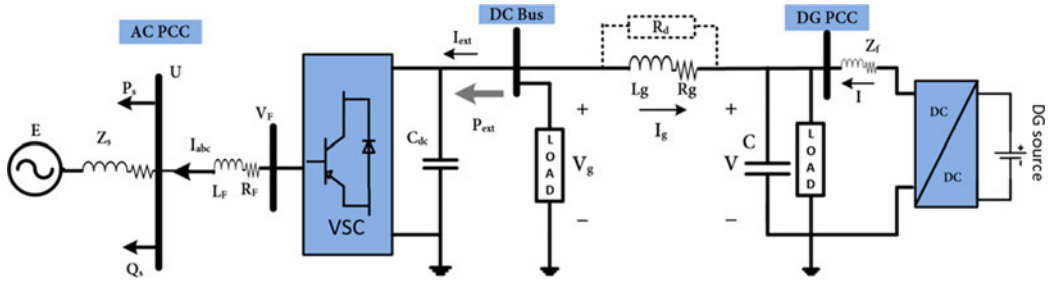

Fig. 1. Typical grid-connected dc distribution system.

LC networks that interact negatively with the connected CPLs leading to reduction in the system stability margin. Therefore, the impact of the PFB schemes in a grid-connected dc distribution system becomes of significant importance when the demand from the CPLs is relatively high [14].

The overall system dynamics can be investigated using small-signal model-based analysis, where the system stability is assessed via the eigenvalues of the developed overall state-space matrix. The eigenvalues-based analysis gives full information about the overall system dynamics; however, the model becomes more complicated as the number of connected components increases. Further, all the system parameters need to be available to the system integrator to develop the aggregated model accurately. On the other hand, the impedance-based analysis can be adopted to assess the system stability without the need for the entire system information, which facilitates investigating complicated systems with reduced computational tools including the physical system and controller dynamics.

The impedance analysis has been widely used to examine the stability of dc distribution systems [15]–[20]. In [15], the voltage source converter (VSC) output impedance was reshaped by injecting internal-model-based active damping signal at VSC control loops, such that the VSC can supply constant power load with high stability margin. In [16], based on the Nyquist admittance ratio criterion, the input/output admittances of hybrid ac/dc system were mathematically developed to evaluate the overall system stability, and active compensators are proposed to reshape the input dc-side admittance of the VSCs. In [17], the impedance model was used to analyze an active dc-distribution system, where a dynamic droop controller was proposed to provide active damping to a multiple-source multiple-load system. In [18], the impedance models of two droop control strategies to control a dc microgrid were developed to compare their steady-state power-sharing and dynamic performances in the multisource system. In [19], the frequency response of the dc-side impedances for a VSC-based high-voltage dc (VSC-HVdc) system was used to investigate the system resonance. In [20], the Nyquist stability criterion was used in a VSC-HVDC; the factors affecting the system stability were characterized. Moreover, in [21], the passivity method was employed to investigate the stability and the performance of a multibus medium-voltage dc distribution system, where an allowable impedance region was introduced to the Nyquist contour of the bus impedance, to ensure adequate system damping performance.

The interactions dynamics of an active dc grid-connected distribution system with a high penetration level of CPLs and DG units equipped with PFB islanding detection schemes were recently investigated with the help of the eigenvalues-based analysis [14]. However, the impedance-based analysis has not been used yet to assess and investigate the dynamics of the hybrid system. Driven by the previously mentioned motivations and advantages offered by the impedance-based methods, this paper presents an impedance-based analysis and stabilizer design of a grid-connected dc active distribution system, where DGs equipped with active PFB islanding detection schemes and high penetration level of CPLs are considered. With the help of the impedance-based analysis, the main contributions of this paper to the research field are as follows.

1) Investigating and characterizing the impact of the PFB islanding detection schemes on the system stability for both grid-connected and islanding modes.
2) Determining the marginal PFB gain settings required for islanding detection and the conditions to maintain the system stability for grid-connected operation.
3) Determining the effective frequency range of the PFB detection on the DG output impedance, which gives more insights into the dynamics of the active islanding schemes in dc grids.
4) Developing a stabilizing loop to mitigate instabilities caused by the CPL and PFB islanding detection schemes interactions; the proposed stabilizer enhances the overall system stability, particularly with multiple DG operation.

This paper is organized as follows. Section II presents the linearized small-signal model of a typical dc distribution system, the concept of active islanding detection schemes in dc grids, and the derivation of the output impedance for each of the system components considering the PFB effect. In Section III, the stability of the grid-connected dc system with and without the feedback schemes is assessed; moreover, the multiple DG operation and the stability enhancement methods are discussed. In Section IV, time-domain nonlinear simulations and experimental results verifying the analytical results are presented. Finally, the concluding remarks are drawn in Section V.

II. System Modeling

The grid-connected dc distribution network under investigation is shown in Fig. 1, where the ac utility grid and the interfacing VSC work together to support the dc system at a

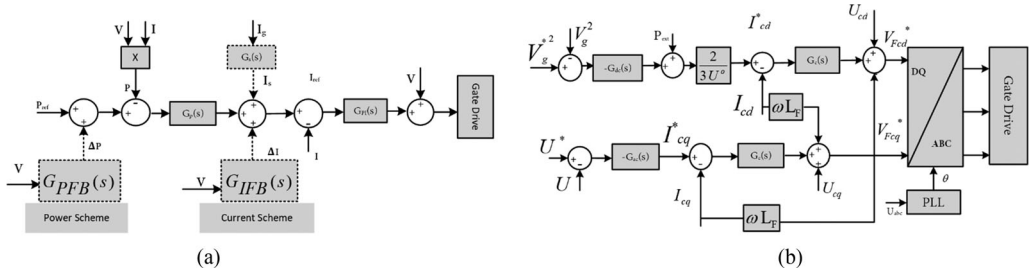

Fig. 2. Controller block diagram. (a) DG unit. (b) VSC.

regulated voltage. The VSC is operated to regulate the dc bus voltage (V_g) and to regulate the ac point of common coupling (U) to its nominal rated value. The active dc distribution system is represented by the dc bus at the VSC output port (DC bus), supplying local load and remote active dc bus (DG PCC) via distribution feeder of impedance (L_g, R_g). A DG unit equipped with PFB scheme for islanding detection purposes, a composite load (R), and the equivalent bus capacitance (C) that represent the effect of converters output capacitors and the stabilizing bus capacitors, are connected at the DG PCC. To enhance the overall system damping capability, a damping stabilizing impedance (R_d) is connected across the feeder impedance. It is worth mentioning that the stabilizing impedance is not a physical system component; however, it mimics the damping current component injected by the DG unit to improve the system stability. The modeling details of the system components (VSC, DG, loads, dc feeder) and their equivalent output impedances are presented in the following sections. Practical and typical parameters for the cables, converters, and controllers of the system in Fig. 1 are used and given in the Appendix.

A. DGs and DC Distribution System Dynamics

The dynamics of the dc distribution network is developed by considering the DG unit dynamics, which is operated to inject a fixed amount of power (P) to the dc distribution system, with two linear compensators ($G_p(s)$ and $G_{PI}(s)$), as indicated in Fig. 2(a). The outer loop compensator ($G_p(s)$) ensures that the injected power by the DG unit is tracking the commanded reference (P_{ref}), whereas the inner loop ($G_{\rm PI}(s)$) is responsible for regulating the DG current (I) injected at the DG PCC. The closed-loop transfer function of the inner current loop can be modeled by a low-pass filter with a time constant (τ), where $1/\tau$ is the closed-loop current control bandwidth [22]. The composite load connected in the investigated system is modeled by a pure resistance (R_{Ldc}), and a CPL, represented by its incremental negative resistance ($-R_{CPL}$) [13], [23], [24]. The resistance (R) is the equivalent composite load resistance. The dc system in Fig. 1 is linearized around a steady-state point (V^o, I^o, I_g^o). The linearized model of the system of Fig. 1 without the PFB loops in the s-plane is given by

$$\tilde{V}_g = \tilde{V} + \tilde{I}_g Z_g, \;\; Z_g = R_g + sL_g \tag{1}$$

$$\tilde{I} + \tilde{I}_g = \tilde{I}_c + \tilde{I}_L \tag{2}$$

$$\tilde{I}_L = \frac{\tilde{V}}{R}, \tilde{I}_C = \tilde{V} sC, \text{ and } R = R_{Ldc}//-R_{CPL} \tag{3}$$

$$\tilde{P} = I^o \tilde{V} + V^o \tilde{I} \tag{4}$$

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) \tag{5}$$

$$\tilde{I} = \frac{\tilde{I}_{ref}}{\tau s + 1} = \frac{\tilde{I}_{ref}}{G_i(s)}, G_i(s) = \tau s + 1 \tag{6}$$

$$\tilde{P}_{ext} = -(V_g^o \tilde{I}_g + I_g^o \tilde{V}_g) + \frac{\tilde{V}_g^2}{R_L} \tag{7}$$

where R_L represents the local load at the dc bus.

B. PFB Islanding Detection Schemes

The concept of PFB islanding detection schemes for dc grids was first presented in [9]. The schemes are based on injecting disturbing signal to the inner current control loop reference command (current scheme), or the outer power control loop reference command (power scheme), which derives the DG unit to an unstable operating condition.

1) Current Loop Disturbance Scheme: The current loop disturbance scheme for islanding detection is employed by adding a current disturbance (ΔI) to the reference DG unit current (I_{ref}), the disturbing current (ΔI) is obtained by processing the DG PCC voltage by a high-pass filter, as shown in Fig. 2(a); the filter output is the DG voltage deviation, which is converted into a current disturbance signal applied to the inner control loop of the DG via the current PFB gain (K_{IFB}).

For the current scheme, the small-signal DG unit reference current given in (5) will be modified to

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) + G_{IFB}(s)\tilde{V} \tag{8}$$

where $G_{IFB}(s) = K_{IFB}\frac{s}{s+\omega}$.

2) Power Loop Disturbance Scheme: The main idea of the power scheme is to add a power disturbance (ΔP) to the DG unit output power to derive the DG unit to an unstable operating point. The disturbance (ΔP) is added to the reference power command in the outer loop of the DG controller; this disturbance is directly proportional to the deviation of the PCC voltage. Like the current disturbance scheme, according to Fig. 2(a), the disturbance is obtained by applying the measured voltage to a high-pass filter and converted into a power signal via the power PFB gain (K_{PFB}).

Following the same approach of the previous scheme, the change in the DG unit reference current given in (5) will be

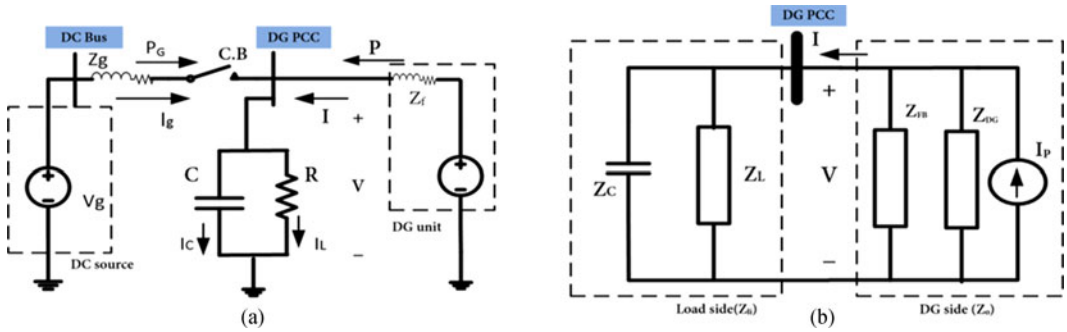

Fig. 3. Islanding detection equivalent circuits. (a) Simplified dc distribution system. (b) Impedance model circuit.

modified to

$$\tilde{I}_{ref} = G_p(s)\left[(\tilde{P}_{ref} - \tilde{P}) + G_{PFB}(s)\tilde{V}\right] \tag{9}$$

where $G_{PFB}(s) = K_{PFB}\frac{s}{s+\omega}$.

C. Impedance Analysis

In this section, the output impedance of the DG unit is developed with/without the PFB detection schemes so that the characteristics of PFB schemes can be easily demonstrated. The validation of the derived impedances is presented in the Appendix.

1) DG Unit Output Impedance Without PFB Schemes: By setting $\tilde{P}_{ref} = 0$ in (5), solving (4) and (5), the DG reference injected current ($\tilde{I}_{ref}$) is given by

$$\tilde{I}_{ref} = -G_p(s)I^o\tilde{V} - G_p(s)V^o\tilde{I}. \tag{10}$$

Solving (6) and (10), the DG unit output impedance without the PFB schemes (Z_{dg}) is given by

$$Z_{dg} = -\frac{\tilde{V}}{\tilde{I}} = \frac{G_i(s) + V^oG_p(s)}{I^oG_p(s)}. \tag{11}$$

2) DG Unit Output Impedance With Current Scheme: By setting $\tilde{P}_{ref} = 0$ in (8), solving for (4), (6), and (8), the DG reference injected current ($\tilde{I}_{ref}$), with the current scheme employed, is given by

$$\tilde{I}_{ref} = -G_p(s)I^o\tilde{V} - G_p(s)V^o\tilde{I} + G_{PFB}(s)\tilde{V}. \tag{12}$$

Solving (6), and (12), the relation between the voltage and the current can be given by

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_{IFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)}. \tag{13}$$

The expression given in (13) illustrates the impact of the PFB on the DG unit output current dynamics, and hence, (13) can be reformulated as the total DG output admittance $Y_o(s)$, which equals the summation of the DG unit output admittance and the PFB admittance, as given in the following:

$$Y_o(s) = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{IFB}, \text{ where } Y_{dg}(s) = \frac{G_p(s)I^o}{G_p(s)V^o + G_i(s)}, Y_{IFB}(s) = \frac{-G_{IFB}(s)}{G_p(s)V^o + G_i(s)}. \tag{14}$$

3) DG Unit Output Impedance With Power Scheme: Like the current scheme, by setting $\tilde{P}_{ref} = 0$ in (9), and solving for (4), (6), and (9), the DG injected current ($\tilde{I}$) dynamics is given by

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_p(s)G_{PFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)}. \tag{15}$$

Similar to the equivalent DG output admittance obtained in (14) for the current scheme, the DG current dynamics given in (15) for the power scheme can be reformulated as the total DG output admittance $Y_o(s)$, which equals the summation of the DG unit output admittance and the PFB admittance, as given in the following:

$$Y_o(s) = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{PFB}, \text{ where } Y_{dg}(s) = \frac{G_p(s)I^o}{G_p(s)V^o + G_i(s)}, Y_{PFB}(s) = \frac{-G_p(s)G_{PFB}(s)}{G_p(s)V^o + G_i(s)}. \tag{16}$$

D. Islanding Detection Gain Margins

The equivalent dc network for islanding detection purposes is shown in Fig. 3(a), where the ac utility and the ac/dc converter can be modeled as a stiff voltage source, plus an $R-L$ segment (Z_g) representing the short model of the distribution feeder. For islanding detection purposes only, the load is modeled as a pure resistance due to the absence of reactive power term in dc systems; furthermore, a resistive load has the largest nondetection zone [8], [25]. The DG unit is modeled by a dc voltage-source connected to a dc/dc converter to the PCC. The primary objective of the previous model is to study the islanding operating condition, i.e., when the circuit breaker (C.B) is open. For this operating condition, the impedance equivalent model can be developed as indicated in Fig. 3(b), where the DG unit equipped with the PFB schemes is modeled by a current

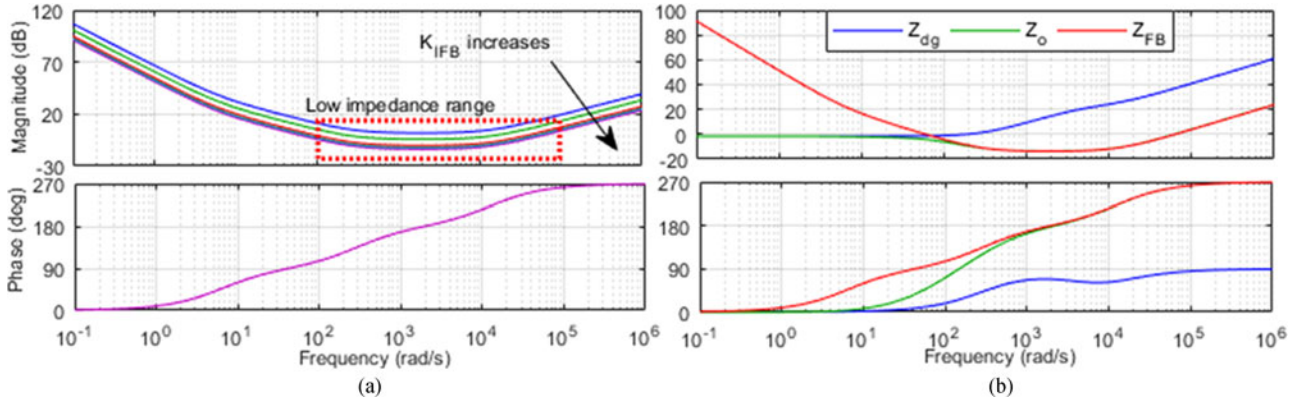

Fig. 4. DG unit output impedance, current scheme. (a) Bode plots of PFB impedance. (b) Equivalent output impedance.

source ($I_P(s)$) and its output impedances ($Z_{dg}(s)$) and ($Z_{FB}(s)$), whereas the bus capacitance (C) and the load are modeled by their impedances ($Z_C(s)$) and ($Z_L(s)$), respectively. The circuit depicted in Fig. 3(b) can be used to check the marginal conditions (PFB gains) for islanding detection by dividing the circuit into source-side impedance ($Z_o(s)$) and load-side ($Z_{Li}(s)$). The source-side impedance is the equivalent of the DG output impedance (Z_{dg}) and the PFB impedance (Z_{FB}), whereas the load-side impedance is the combination of the load and bus capacitor impedances. To ensure successful islanding detection, the voltage at the DG PCC given in (17) should be driven into an unstable state, which can be achieved if the impedance ratio (Z_{Li}/Z_o) violates the Nyquist criterion.

$$V(s) = I_P(s)Z_{Li}(s)\frac{1}{1+Z_{Li}/Z_o}. \tag{17}$$

It should be mentioned that the overall system stability via the Nyquist Criterion is guaranteed if the characteristic equation $(1 + Z_{Li}(s)/Z_o(s))$ has no zeros (z) in the right-half s-plane [26]. According to the Nyquist criterion, z can be determined by the summation of the number of clockwise encirclements of the $(-1,\ 0)$ point and the number of poles (p) of the open-loop transfer function $Z_{Li}(s)/Z_o(s)$. Because the open-loop poles are the union of the load impedance $Z_{Li}(s)$ poles and the DG unit output admittance $Y_o(s)$ poles, there are no open-loop poles (p) in the right-half side of the s plane, because the poles of the output admittance $Y_o(s)$ are originally formed from the outer and inner loops compensators [see (14) and (16)], which are originally well designed to provide damped system behavior. Similarly, $Z_{Li}(s)$ is formed from the bus capacitance and load impedances, which would not have any poles in the right-half side of the s-plane. Accordingly, the system stability can be determined by checking the number of encirclements around $(-1,\ 0)$. It is worth mentioning that if there are one or more clockwise encirclements around $(-1,\ 0)$, the system will be considered unstable, regardless of the number of open-loop poles (p) [26].

1) Current Scheme Islanding Detection Gain Margins: The frequency responses of the DG unit output impedance with/without the PFB current scheme and its equivalent output impedance are depicted in Fig. 4. It is obvious that the magnitude of the PFB output impedance decreases with increasing the feedback gain over the entire frequency range, whereas the phase-shift angle does not show any variation with the PFB gain, as depicted in Fig. 4(a). On the other hand, the DG intrinsic output impedance (Z_{dg}) resembles a constant positive resistance at the low-frequency range, whereas the impedance magnitude and phase-shift angle increase dramatically at higher frequencies, as shown in Fig. 4(b). Furthermore, it is evident that the equivalent impedance (Z_o) at the DG PCC has almost the same characteristics of the DG intrinsic impedance at the low-frequency range, whereas the equivalent impedance magnitude coincides with the PFB impedance at the medium- and high-frequency range. It is also evident that the PFB impedance adds 180° phase shift to the equivalent impedance at the medium- and high-frequency ranges, which demonstrates the destabilizing effect of the PFB impedance.

The conditions for islanding detection can be obtained if the Nyquist criterion for the impedance ratio is violated. The Nyquist plots for the impedance ratio (Z_{Li}/Z_o) at different PFB gains are shown in Fig. 5(a). It is clear that the Nyquist contour does not encircle $(-1,\ 0)$ when the PFB gain is set to zero, which indicates the system is stable for the islanding operation and hence, the failure of islanding condition detection. On the other hand, increasing the PFB gain shifts the Nyquist contours toward $(-1,\ 0)$ until the Nyquist contours sharply intersect the real axis at $(-1, 0)$ with 0 dB gain margin. The gain at this point is the marginal gain for islanding detection (4.35 A/V), which means a marginal stability condition at this gain value. For a better understanding of system dynamics, the gains are represented in their normalized values with the marginal gain as the base value. To ensure successful islanding detection, the PFB gain should be set to a value higher than 1.0 p.u. because the gain margin further decreases with the PFB gain, as indicated in Fig. 5(a); this gain margin drops to -1.6 dB and -3.55 dB for feedback gains 1.2 p.u. and 1.5 p.u., and at a frequency of 250 rad/s and 240 rad/s, respectively.

2) Power Scheme Islanding Detection Gain Margins: Similar to the current scheme, the PFB impedance developed in

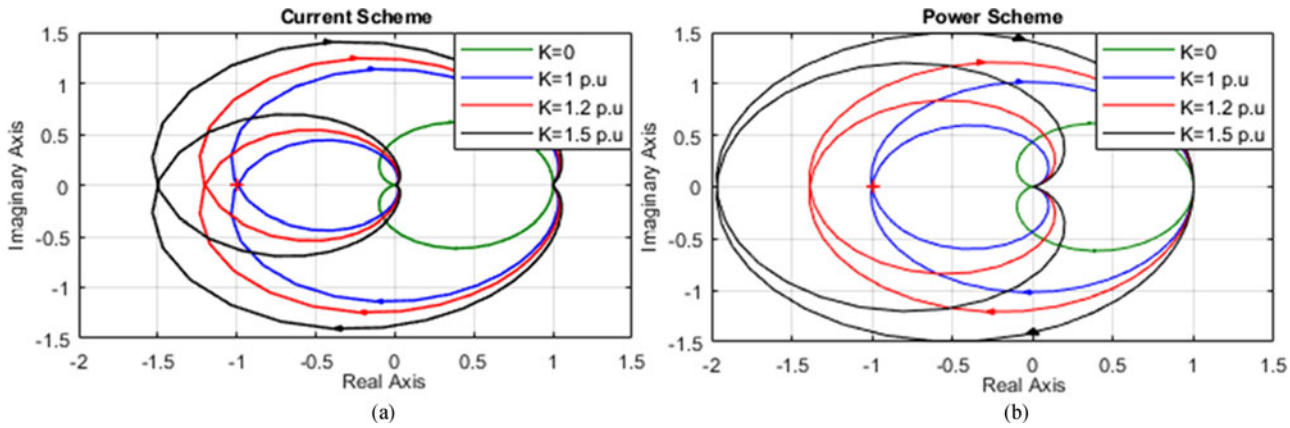

Fig. 5. Nyquist plots with different PFB gains. (a) Current scheme. (b) Power scheme.

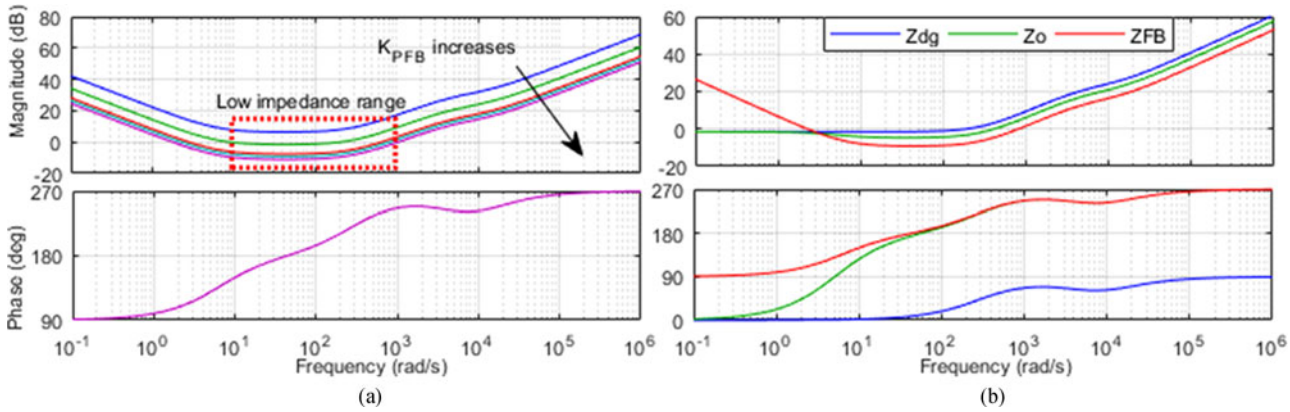

Fig. 6. DG unit output impedance, power scheme. (a) Bode plots of PFB impedance. (b) Equivalent output impedance.

(16) shows a reduction in its magnitude with the feedback gain variation, whereas the phase-shift angle is kept unchanged, as indicated in Fig. 6(a). It can be observed that the destabilizing effect of the PFB impedance appears in different specific ranges for both schemes. The current scheme PFB impedance is effective in the frequency range from 100 to 10^5 rad/ s, where the impedance magnitude drops to its minimum value, whereas the PFB impedance is effective from 10 to 10^3 rad/ s for the power scheme. The different effective range variation is because the disturbance signal for the power scheme is injected to the power controller outer loop with a bandwidth lower than the inner current controller loop. Therefore, PFB impedances are effective in the frequency range where the perturbation signal is injected. The impact of the PFB power scheme on the DG output impedance is portrayed in Fig. 6(b), unlike the current scheme; the equivalent DG output impedance (Z_o) does not coincide with the PFB impedance for the medium- and high-frequency ranges; however, the impedance magnitude is still showing reduction within the power scheme effective range with 180° additional shift in its phase angle.

The Nyquist plots of the impedance ratio (Z_{Li}/Z_o) for the power scheme are shown in Fig. 5(b) in order to investigate the islanding detection margins. It is clear that the stability criterion is violated if the feedback gain is greater than the marginal gain (1230 W/V = 1 p.u.), and hence the Nyquist contours can clearly encircle $(-1, 0)$ with significant negative gain margin. The gain margin drops to -2.84 dB and -5.87 dB for feedback gains 1.2 p.u. and 1.5 p.u., and at a frequency of 30 rad/s and 28 rad/s, respectively.

E. VSC and AC Grid-Side Dynamics

The overall system dynamics of the grid-connected dc distribution network given in Fig. 1 can be accurately evaluated by developing the ac/dc VSC and ac grid dynamics. Fig. 2(b) shows the VSC controller block diagram, where the VSC is controlled to regulate the dc bus voltage (V_g) and the ac PCC voltage (U) to enhance the ac system stability for weak grid conditions [27]. The VSC is interfaced to the ac side via the reactor ($R_F - L_F$) and to the dc bus via the dc-link smoothing capacitor (C_{dc}). The ac grid dynamics shown in Fig. 1 is represented by a stiff voltage source (E), and the strength at the PCC is measured through the impedance (Z_s). The VSC is synchronized to the ac grid by employing the vector-current control and using the standard dq-frame three-phase phase-locked loop (PLL). The dynamics of the interfacing ac/dc VSC and the ac grid can be modeled using the ac grid $d-q$ reference frame [28], where the d-axis of the reference frame is chosen to align with the ac

grid stiff voltage source (E). The small-signal model of the ac network dynamics is given by (18)–(23):

$$\tilde{V}^g_{Fdq} = \underbrace{\begin{bmatrix} R_T + sL_T & -\omega_g L_T \\ \omega_g L_T & R_T + sL_T \end{bmatrix}}_{Z_T} \tilde{I}^g_{dq} \tag{18}$$

$$\tilde{U}^g_{dq} = \underbrace{\begin{bmatrix} R_s + sL_s & -\omega_g L_s \\ \omega_g L_s & R_T + sL_s \end{bmatrix}}_{Z_S} \tilde{I}^g_{dq} \tag{19}$$

$$\tilde{P}_s = 1.5\left(\begin{bmatrix} I^o_{cd} & I^o_{cq} \end{bmatrix}\tilde{U}_{cdq} + \begin{bmatrix} U^o_{cd} & U^o_{cq} \end{bmatrix}\tilde{I}_{cdq}\right) \tag{20}$$

$$\tilde{Q}_s = 1.5\left(\begin{bmatrix} -I^o_{cq} & I^o_{cd} \end{bmatrix}\tilde{U}_{cdq} + \begin{bmatrix} U^o_{cq} & -U^o_{cd} \end{bmatrix}\tilde{I}_{cdq}\right) \tag{21}$$

$$\tilde{U} = \frac{U^o_{cd}}{U^o}\tilde{U}_{cd} + \frac{U^o_{cq}}{U^o}\tilde{U}_{cq}. \tag{22}$$

The dc-link voltage dynamics can be written as [22]

$$s(\tilde{V}_g^2) = \frac{2}{C_{dc}}P_{ext} - \frac{2}{C_{dc}}\left[\tilde{P}_s + T_P\tilde{P}_s s\right] + \frac{2}{C_{dc}}\left[T_Q\tilde{Q}_s s\right] \tag{23}$$

where $T_P = \frac{2L_F P^o_s}{3U^{o2}}$ and $T_Q = \frac{2L_F Q^o_s}{3U^{o2}}$.

Fig. 2(b) shows the controller dynamics of the VSC, where the converter outer loops regulate the dc-link voltage $(V_g)^2$ and the ac PCC voltage (U) via two linear PI compensators ($G_{dc}(s)$ and $G_{ac}(s)$), respectively. The inner loop is based on the vector current control that employs two PI controllers ($G_c(s)$) to regulate the converter currents to their reference values generated by the outer loops. The outer and inner loops dynamics are modeled in the converter $d-q$ reference frame, as given in the following:

$$\tilde{I}^*_{cd} = \frac{2}{3U^o}\left[-G_{dc}(s)\left(\tilde{V}^{2*}_g - \tilde{V}^2_g\right) + P_{ext}\right] \tag{24}$$

$$\tilde{I}^*_{cq} = -\left[G_{ac}(s)(\tilde{U}^* - \tilde{U})\right] \tag{25}$$

$$\tilde{V}_{Fcdq} \cong \overset{*}{\tilde{V}}_{Fcq} = \tilde{U}_{cdq} + \underbrace{\begin{bmatrix} G_c(s) & -\omega_g L_F \\ \omega_g L_F & G_c(s) \end{bmatrix}}_{Z_L}\tilde{I}_{cdq} + \underbrace{\begin{bmatrix} \frac{M^o_{cd}}{2} \\ \frac{M^o_{cq}}{2} \end{bmatrix}}_{M}\tilde{V}_g + \begin{bmatrix} \tilde{I}^*_{cd} \\ \tilde{I}^*_{cq} \end{bmatrix}G_c(s). \tag{26}$$

The function of the PLL block in Fig. 2(b) is to extract the ac PCC phase-shift angle (θ), which is used to obtain the dq voltages and currents used by the VSC controllers. The grid and the converter reference frames quantities (voltages and currents) should be related so that the system dynamics are accurately included in the entire system model. The angle (θ) relates the voltage and the currents of the converter reference frame to the ac grid reference frame, as given in the following:

$$\left(X^g = X_c e^{j\theta}\right) \tag{27}$$

where X^g is the current or the voltage vector in the ac grid reference frame, and X_c is the current or the voltage vector in the converter reference frame. The transformation of the voltages and currents between the reference frames can be obtained by linearizing (27) as presented in the Appendix.

The PLL dynamics can be modeled by [22]

$$\tilde{\theta} = \begin{bmatrix} 0 & \frac{g_{\mathrm{PLL}}(s)}{s} \end{bmatrix}\tilde{U}_{cdq} = [G_{\mathrm{PLL}}(s)]\tilde{U}_{cdq} \tag{28}$$

where the PLL compensator $g_{\mathrm{PLL}}(s) = K_{p\mathrm{PLL}} + \frac{K_{i\mathrm{PLL}}}{s}$, and $K_{p\mathrm{PLL}}$, $K_{i\mathrm{PLL}}$ are the compensator gains.

F. VSC Output Impedance

The ac grid impedance in the converter reference frame (Z^C_S) can be developed by solving (19), (27), and (28). The voltage dynamics at the PCC is given by

$$\tilde{U}_{cdq} = [{Z_S}^C]\tilde{I}_{cdq} \tag{29}$$

where $[{Z_S}^C] = [I - [T_{2\theta} + T_{2dq}Z_S T_{3\theta}]G_{\mathrm{PLL}}(s)]^{-1}[T_{2dq}][Z_S][T_{3dq}]$ is the ac grid impedance matrix in the converter reference frame. Expressions for $T_{2\theta}$, T_{2dq}, $T_{3\theta}$,and T_{3dq} can be found in the Appendix.

Similarly, the impedance from the VSC to the ac grid stiff bus in the converter reference frame ($Z_T{}^C$) can be derived by solving (18), (27), and (29). The voltage dynamics at the VSC terminals is given by

$$\tilde{V}_{cdq} = [{Z_T}^C]\tilde{I}_{cdq} \tag{30}$$

where $[{Z_T}^C] = [T_{dq}][Z_T][T_{3dq}] + [T_\theta + T_{dq}Z_T T_{3dq}][G_{\mathrm{PLL}}(s)][{Z_S}^C]$ is the total impedance matrix in the converter reference frame.

Because the dc-port voltage dynamics given in (23) does not show direct and linear relationship between the voltage (V_g) and the current (I_{ext}), the VSC output admittance can be derived by linearizing the externally injected power at the VSC side input, as given in the following:

$$\underset{ext}{\tilde{P}} = (I^o_{ext} + Y_{vsc}V^o_g)\tilde{V}_g = Y_1(s)\tilde{V}_g,$$
$$Y_1(s) = (I^o_{ext} + Y_{vsc}(s)V^o_g). \tag{31}$$

Substituting (31) in (23) and linearizing $\tilde{V}^2_g = 2\overset{o}{V}_g\tilde{V}_g$, the dc-port dynamics can be given by

$$2s\overset{o}{V}_g\tilde{V}_g = \frac{2}{C_{dc}}(Y_1(s)\tilde{V}_g) - \frac{2}{C_{dc}}\left[\tilde{P}_s + T_P\tilde{P}_s s\right] + \frac{2}{C_{dc}}\left[T_Q\tilde{Q}_s s\right]. \tag{32}$$

To obtain the VSC admittance, expressions of $\tilde{P}_s$ and $\tilde{Q}_s$ need to be eliminated from (32), this can be achieved by substituting the ac grid impedance in the converter reference frame developed in (29) in (20) and (21) to obtain the new expressions for $\tilde{P}_s$ and $\tilde{Q}_s$, as given in the following:

$$\tilde{P}_s = Z_{ps}\tilde{I}_{cdq},\ Z_{ps} = 1.5\left(\begin{bmatrix} I^o_{cd} & I^o_{cq} \end{bmatrix}[{Z_S}^C] + \begin{bmatrix} U^o_{cd} & U^o_{cq} \end{bmatrix}\right)$$
$$\tilde{Q}_s = Z_{qs}\tilde{I}_{cdq},\ Z_{qs} = 1.5\left(\begin{bmatrix} -I^o_{cq} & I^o_{cd} \end{bmatrix}[{Z_S}^C] + \begin{bmatrix} U^o_{cq} & -U^o_{cd} \end{bmatrix}\right). \tag{33}$$

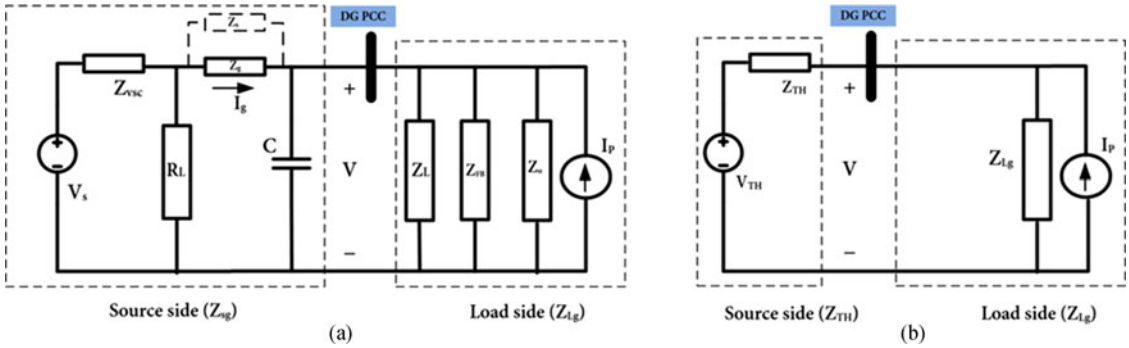

Fig. 7. Grid-connected mode equivalent circuits. (a) Impedance model of dc distribution system. (b) Two-impedance equivalent circuit.

Solving (32) and (33), the dc-port dynamics can be modified into

$$2V_g^o s\tilde{V}_g = \frac{2}{C_{dc}}(Y_1(s)\tilde{V}_g) + \frac{2}{C_{dc}} Z_{pq}\tilde{I}_{cdq},$$
$$Z_{pq} = T_Q s Z_{qs} - (1 + T_P s) Z_{ps}). \tag{34}$$

The reference currents $\tilde{I}^*_{cdq}$ are reformulated as a function of the dc-port voltage (V_g) and the currents $\tilde{I}_{cdq}$, by solving (22), (24), (25), and (29). The reference currents $\tilde{I}^*_{cdq}$ are given in (35)

$$\tilde{I}^*_{cdq} = \underbrace{\begin{bmatrix} [0 \quad 0] \\ G_{ac}(s)[1 \quad 0][{Z_S}^C] \end{bmatrix}}_{A_1} \tilde{I}_{cdq} + \underbrace{\begin{bmatrix} \frac{2}{3U^o_{cd}}(Y_1(s) + 2V_g^o G_{dc}(s)) \\ 0 \end{bmatrix}}_{A2} \tilde{V}_g. \tag{35}$$

Substituting (35) in (26), and solving with (29) and (30), the currents are expressed as a function of the dc-port voltage in (36)

$$\tilde{I}_{cdq} = A_3\tilde{V}_g,\ A_3 = [{Z_T}^C - {Z_S}^C - Z_L - A_1 G_c(s)]^{-1}[A_2 G_c(s) + M]. \tag{36}$$

Solving (34) and (36), the VSC output admittance is given by

$$Y_{vsc}(s) = \frac{1}{Z_{vsc}(s)} = C{V_g}^o s - Z_{pq}A_3 - \frac{I^o_{ext}}{V^o_g}. \tag{37}$$

III. Stability Analysis of Grid-Connected System

In this section, the stability analysis of the grid-connected dc network with the help of the small-signal impedances developed in the previous section is discussed for the system shown Fig. 1. For the grid-connected mode, it is important to ensure that the system has a safe stability margin when the PFB islanding detection schemes are used. In the following analysis, the marginal feedback gain developed in the previous section is considered as the base value to normalize the results for better comparative analysis. To consider the worst case scenario of the loading condition, the composite load is assumed to be a purely constant power load, the DG unit is functioning at different operating conditions, the DG unit is located at 1.0 km away from the dc bus, and the bus capacitance and other system parameters are set to their rated and nominal values outlined in the Appendix.

A. Grid-Connected Stability Margins

Fig. 7(a) shows the small-signal impedance equivalent circuit for the grid-connected dc distribution network given in Fig. 1, where the ac/dc converter DG unit and its dc/dc converter equipped with PFB islanding detection schemes are represented by their output impedances developed in the previous section [29]. To check the system stability using the Nyquist criterion, the two-impedance equivalent circuit is developed as depicted in Fig. 7(b). The source subsystem impedance (Z_{TH}) includes the VSC output impedance (Z_{vsc}), local load at the VSC port (R_L), dc grid feeder impedance (Z_g), and the bus capacitance (C), whereas the load subsystem impedance (Z_{Lg}) includes the DG unit impedance (Z_{dg}), PFB impedance (Z_{FB}), and the composite load (R) connected at the DG PCC. The voltage at the DG PCC (V) can be developed similar to that in (17) as given in (38) by

$$V(s) = (V_{TH}(s) + I_P(s)Z_{TH}(s))\ \frac{1}{1 + Z_{TH}(s)/Z_{Lg}(s)} \tag{38}$$

where $V_{TH}(s)$ is the Thevenin's equivalent voltage for the source subsystem.

It is clear that the expression given in (38) for the voltage at DG PCC resembles an input/output transfer function system at which the stability of the voltage ($V(s)$) is guaranteed if the impedance ratio (Z_{TH}/Z_{Lg}) satisfies the Nyquist stability criterion provided that the input of the transfer function expressed by ($V_{TH} + I_P Z_{TH}$) is originally stable; i.e., $Z_{TH}(s)$ has no poles in the right-hand side of the s-plane. Furthermore, to consider the number of encirclements around (–1, 0) as a stability criterion, the expression ($Z_{TH}(s)/Z_{Lg}(s)$) must not have poles in the right-hand side of the s-plane.

B. System Stability Without PFB

Fig. 8 shows the Bode diagrams of the subsystem impedances for the grid-connected dc network without the PFB schemes being employed at different operating conditions. It is clear that the source-side impedance (Z_{TH}) has a positive resistive behavior for the low-frequency range and capacitive behavior

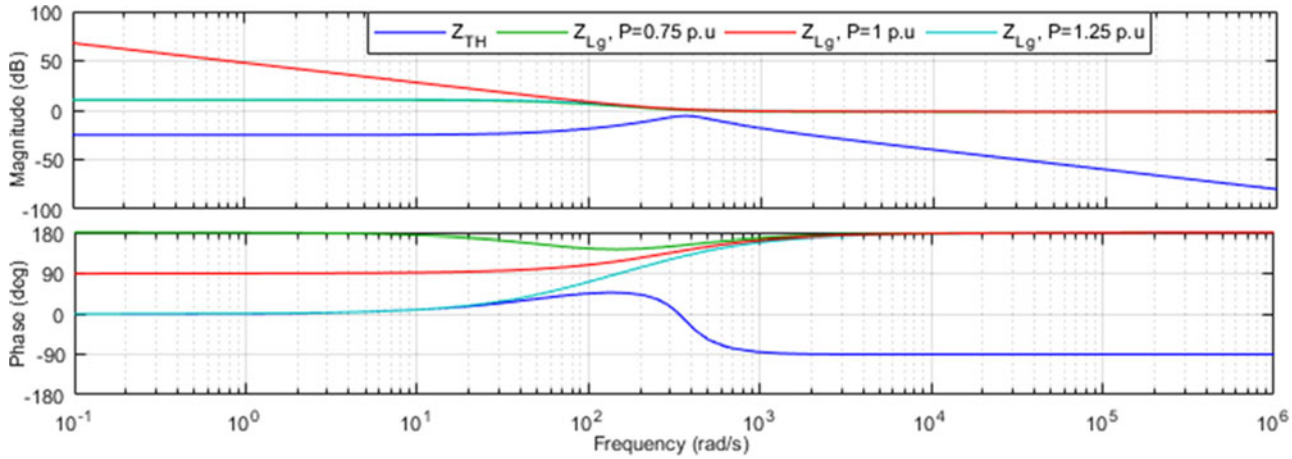

Fig. 8. Bode plot of source-side and load-side impedances for grid-connected operation without the PFB schemes.

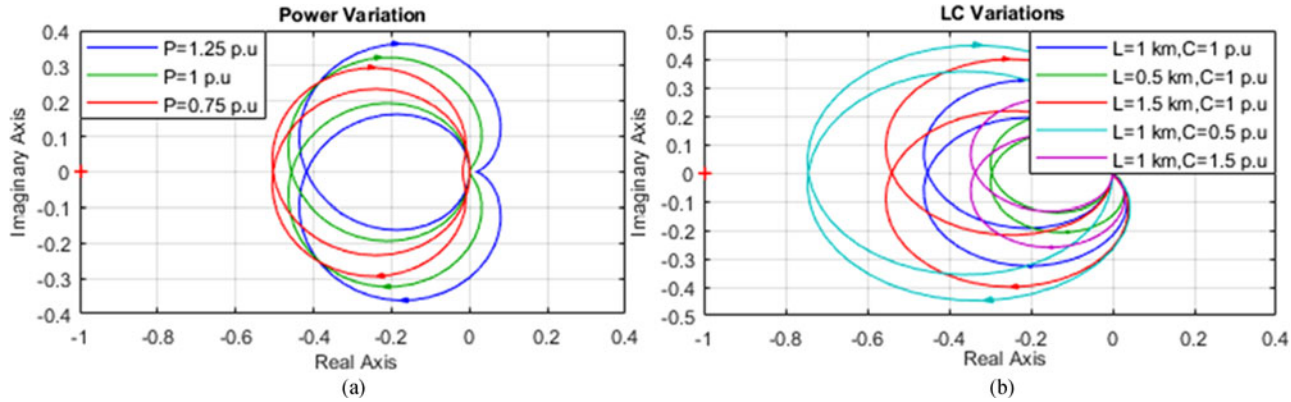

Fig. 9. Nyquist plots for grid-connected operation without PFB methods. (a) DG unit power variation. (b) Variation of feeder length and bus capacitance.

for the medium- and high-frequency range with a resonance peak located at the corner frequency of the *LC* network generated from the feeder inductance and the bus capacitance. On the other hand, it is noted that the magnitude of the load-side impedance Z_{Lg} has a very large value for rated loading and generation conditions (1 p.u.), whereas this magnitude drops to a constant value for other operating conditions. Furthermore, the phase angle of Z_{Lg} tends to move from 0° to 180° when the DG unit delivers power less than the load demand, indicating a negative resistance behavior.

The overall system stability is investigated by the Nyquist plots of the system impedance ratio at different DG operating conditions, as portrayed in Fig. 9(a). It is evident that the system stability is degraded as the DG unit injected power decreases, with 1.7 dB drop in the gain margin if the DG output power drops from 1.25 to 0.75 p.u. This agrees with the impedance behavior in Fig. 8, where the negative resistance behavior for low power operation is expected to reduce the system stability margin. The overall system stability margin is further investigated in Fig. 9(b) by varying the DG unit location and the bus capacitance (C). The stability margin is remarkably affected by varying the bus capacitance at the PCC, where the system gain margin drops by 4.31 dB for 0.5 p.u. bus capacitance, and is improved to 9.46 dB for 1.5 p.u. capacitance. On the other hand, longer dc feeders have negative impacts on the system stability. The gain margin drops by 1.5 dB if the DG unit moves 0.5 km away from its original location, whereas the stability is further enhanced if the DG unit moves 0.5 km toward the DC bus, resulting in 3.73 dB improvement in the system gain margin.

C. Stability of Grid-Connected System With PFB Schemes

1) Current Scheme: With the PFB gain set to 1 p.u., the frequency response of the load-side impedance (Z_{Lg}) of the grid-connected system at different DG output power levels is shown in Fig. 10(a). It is clear that Z_{Lg} has no significant variation in the low-frequency range if compared to the case where the PFB scheme is disabled (see Fig. 8). However, it can be observed that the system impedances interactions have remarkable variation in the frequency range close to the *LC* network resonance frequency, where Z_{Lg} shows a reduction in the magnitude regardless of the DG output power with almost the same phase-shift angle. It is worth mentioning that the interactions between the system impedances are maximized around the *LC* resonance frequency because the PFB scheme has its destabilizing effect in a frequency range close to the *LC* network resonance

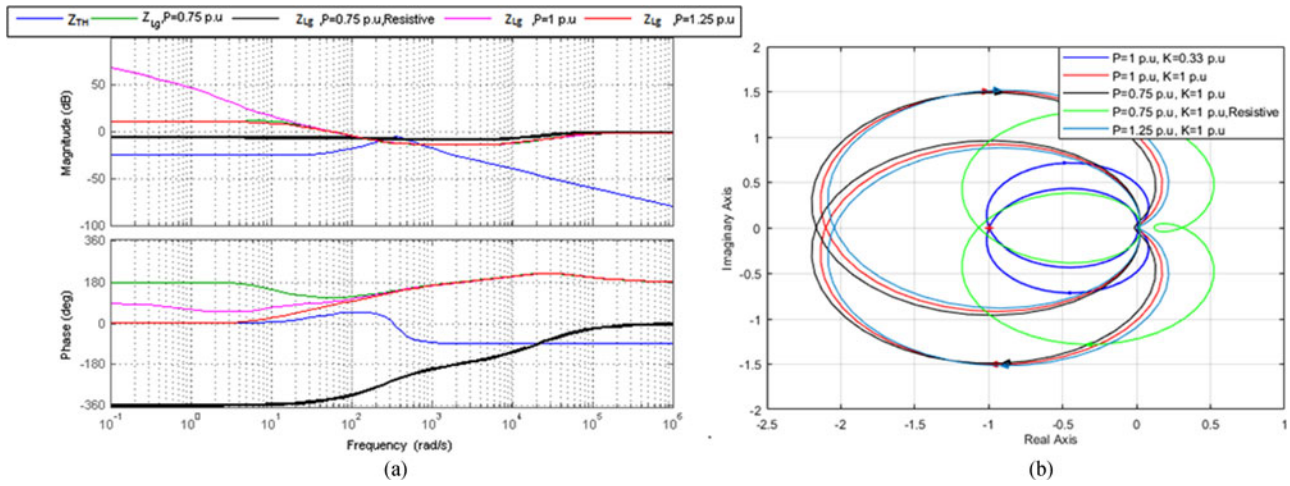

Fig. 10. Grid-connected operation with the current scheme. (a) Bode plot of source and load impedances. (b) Nyquist plots.

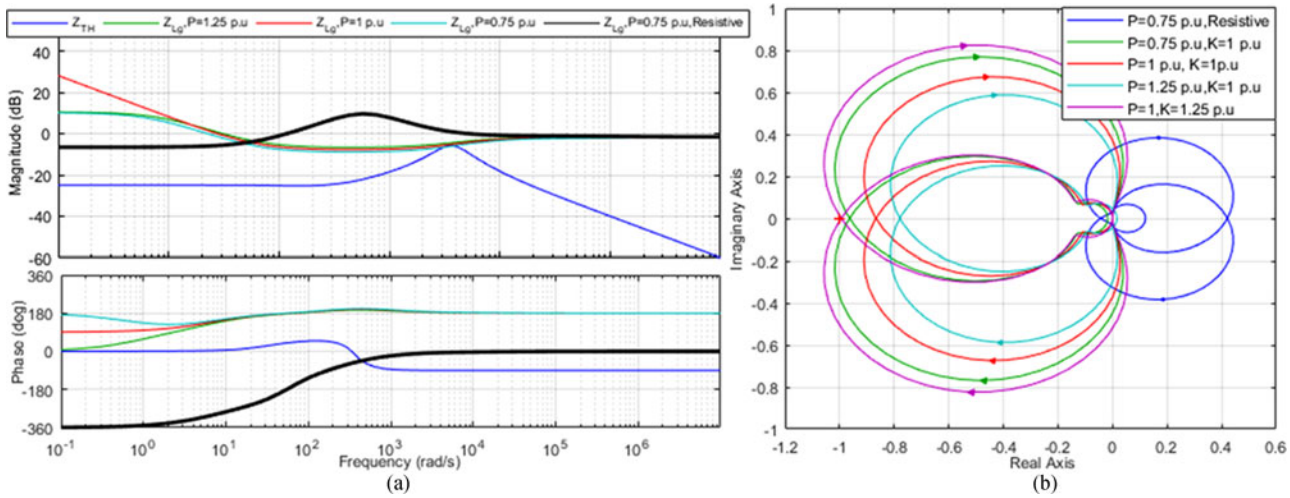

Fig. 11. Grid-connected operation with the power scheme. (a) Bode plot of source and load impedances. (b) Nyquist plots.

frequency. However, the interactions are minimized if a resistive load replaced the CPL at the DG PCC demonstrating the impact of the loading nature on the system dynamics.

The system stability margins are investigated with the help of the Nyquist plots as indicated in Fig. 10(b). It is clear that the impedance interactions around the resonance frequency drive the system to an unstable state if the PFB gain is set to 1 p.u., with –6.5 dB gain margin at 414 rad/s; moreover, the grid-connected system is marginally stable with 0.33 p.u. PFB gain, which is not sufficient to detect the islanding condition. It is also noted that the DG operating point has less effect on the overall system stability with the current PFB scheme being employed. On the other hand, replacing the CPL with resistive load improves the stability remarkably; however, the system is still unstable with –0.4 dB gain margin.

2) Power Scheme: Unlike the current scheme, the power scheme shows higher stability margins even with high CPL penetration level (1 p.u.), as illustrated by the source and load impedances in Fig. 11(a). It is observed that the load-side impedance of the power scheme in the low-frequency range has a similar frequency response as in the current scheme at different loading conditions. However, the power scheme has less intersection between the subsystems impedances close to the *LC* network resonance frequency range. This is because the effective frequency range for the power scheme is located behind the frequency range, where the *LC* network shows its peak. Furthermore, it is noticed that impedances intersections are completely eliminated if the load is purely resistive.

Although the impedance intersection is reduced, the system still has a very poor stability margin as clarified by the Nyquist plots indicated in Fig. 11(b). The system is marginally stable with 1.25 p.u. feedback gain when the DG unit is delivering its rated power. Furthermore, the grid-connected system shows a stability improvement, where the gain margin increases by 0.92 dB with the DG unit output power delivering 25% more than its rated value, whereas the gain margin drops by 0.92 dB as the injected power goes down to 0.75 p.u. It should be noted that although the stability is improved for the power scheme if

compared to that in the current scheme, it shows poor stability margins if the feedback gain is set slightly higher than its marginal gain, and the system can easily lose its stability with grid uncertainties.

D. Stability Enhancement

From the previous analysis, the investigated grid-connected dc distribution system with CPLs and DGs equipped with PFB islanding detection techniques exhibits severe stability problems, particularly with the current scheme and with poor stability margin for the power scheme. The instability problems are originated from the interactions between the source-side and load-side impedances at the proximity of the *LC* network resonance frequency; those interactions increase when the PFB schemes are used. Therefore, a stabilizer is required to enhance the overall system stability.

Because most of the previously proposed stabilizing methods used the bus voltage as a feedback signal to stabilize the system [30]–[32], the functionality of these damping methods loop might conflict with the PFB loop resulting in unsuccessful islanding detection. This is because the stabilizing loop works to stabilize the voltage, whereas the PFB loop works to destabilize the voltage. To avoid the malfunction of each loop, the stabilizing loop that could offer this feature should be derived based on the dc grid current signal so that the stabilizing loop is only active in the grid-connected mode. This is because the grid current will diminish for islanding operation, and hence, the stabilizing loop will be idle. The stabilizing current component (I_s) can be obtained by dividing the voltage drop across the line (V_{drop}) by a resistor R_d to resemble connecting a virtual resistor across the terminals of the dc feeder impedance, as depicted in Fig. 1. The stabilizing current is given by

$$I_s = \frac{V_{drop}}{R_d} = \frac{I_g(R_g + sL_g)}{R_d} = \frac{L_g}{R_d}\left(s + \frac{R_g}{L_g}\right) I_g. \quad (39)$$

A low-pass filter is employed to the stabilizer transfer function to avoid the differentiator problems in (39). Furthermore, to limit the stabilizer operation to transient states, a high-pass filter is added to the stabilizer transfer function; then, the stabilizing current I_s is given by

$$I_s = K_d \frac{s+\omega_1}{s+\omega_2}\ \frac{s}{s+\omega_3} I_g = G_s(s) I_g \quad (40)$$

where $\omega_1 = \frac{R_g}{L_g}$ is the cutoff frequency of the low-pass filter, $K_d = \frac{\omega_2 L_g}{R_d}$ is the stabilizing gain, and ω_3 is the cutoff frequency of the high-pass filter.

Accordingly, the reference current for the islanding detection schemes given in (8) and (9) are modified to include the stabilizing loop dynamics depicted in Fig. 2(a). The updated reference currents are given by (41) and (42) for the current and power schemes, respectively,

$$\tilde{I}_{ref} = G_p(s)(\tilde{P}_{ref} - \tilde{P}) + G_{IFB}(s)\tilde{V} + G_s(s)\tilde{I}_g \quad (41)$$

$$\tilde{I}_{ref} = G_p(s)\left[(\tilde{P}_{ref} - \tilde{P}) + G_{PFB}(s)\tilde{V}\right] + G_s(s)\tilde{I}_g. \quad (42)$$

E. DG Unit Output Impedance With PFB Schemes and Stabilizing Impedance

1) Current Scheme: Reformulating (1) and using (37), the grid current (I_g) can be given by

$$\tilde{I}_g = -Y_{dc}(s)\tilde{V},\ Y_{dc}(s) = \frac{1}{Z_{dc}(s)},\ Z_{dc}(s) = Z_{vsc}(s) + Z_g(s). \quad (43)$$

Solving (4), (41), and (43), the dynamics of the DG unit output current is given in the following:

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_{IFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} - \frac{G_s(s)Y_{dc}(s)\tilde{V}}{G_p(s)V^o + G_i(s)}. \quad (44)$$

The expression in (44) can be reformulated as the total output admittance ($Y_o(s)$) seen at the DG PCC, which equals the summation of the DG output admittance, the PFB admittance, and the stabilizing loop admittance, as given in the following:

$$Y_o = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{IFB} + Y_{IS} \quad (45)$$

where $Y_{dg} = \frac{G_p(s)I^o}{G_p(s)V^o+G_i(s)}$, $Y_{IFB} = \frac{-G_{IFB}(s)}{G_p(s)V^o+G_i(s)}$, and $Y_{IS} = \frac{G_s(s)Y_{dc}(s)}{G_p(s)V^o+G_i(s)}$.

2) Power Scheme: Solving (4), (42), and (43), the dynamics of the DG output current is given in (46)

$$\tilde{I} = \frac{-G_p(s)I^o\tilde{V}}{G_p(s)V^o + G_i(s)} + \frac{G_p(s)G_{PFB}(s)\tilde{V}}{G_p(s)V^o + G_i(s)} - \frac{G_s(s)Y_{dc}(s)\tilde{V}}{G_p(s)V^o + G_i(s)}. \quad (46)$$

Similar to the impedance derived in (45), the expression in (46) can be reformulated as the total output admittance ($Y_o(s)$) seen at the DG unit bus, which is the combination of the DG unit output admittance, the PFB admittance, and the stabilizing loop admittance, as given in the following:

$$Y_o = -\frac{\tilde{I}}{\tilde{V}} = Y_{dg} + Y_{IFB} + Y_{PS} \quad (47)$$

where $Y_{dg} = \frac{G_p(s)I^o}{G_p(s)V^o+G_i(s)}$, $Y_{IFB} = \frac{-G_{IFB}(s)}{G_p(s)V^o+G_i(s)}$, and $Y_{PS} = \frac{G_s(s)Y_{dc}(s)}{G_p(s)V^o+G_i(s)}$.

3) Impedance-Based Design Principles of the Proposed Stabilizer: The stabilizing admittances obtained in (45) and (47) are identical, which indicates that the stabilizing loop impedance is independent of the islanding detection scheme being employed. The design of the stabilizing compensator (impedance) can be simply obtained by the proper selection of the parameters given in (40). The first parameter ω_1 can be calculated based on the ratio between the feeder resistance and inductance, as given in (39), which is fixed and readily known to the designer through the line characteristics offered by the manufacturer. The corner frequency ω_2 is selected such that the dc-grid current dynamics including the resonance frequency of the *LC* network are completely injected to the stabilizing compensator, so that ω_2 is recommended to be higher than ten times the resonance frequency of the *LC* network. The cutoff frequency ω_3 is de-

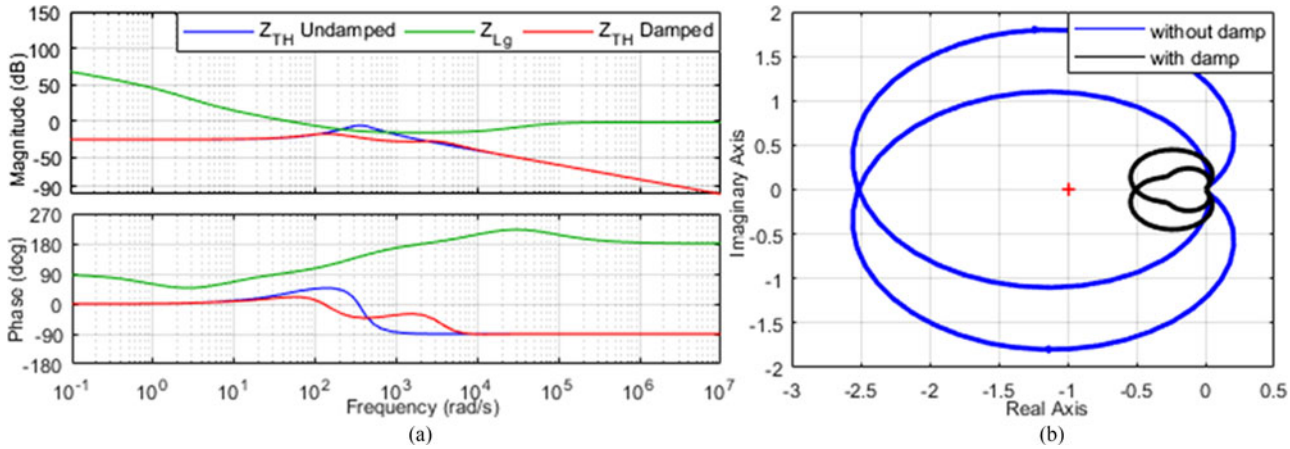

Fig. 12. Grid-connected operation with current scheme and the stabilizing loop enabled. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

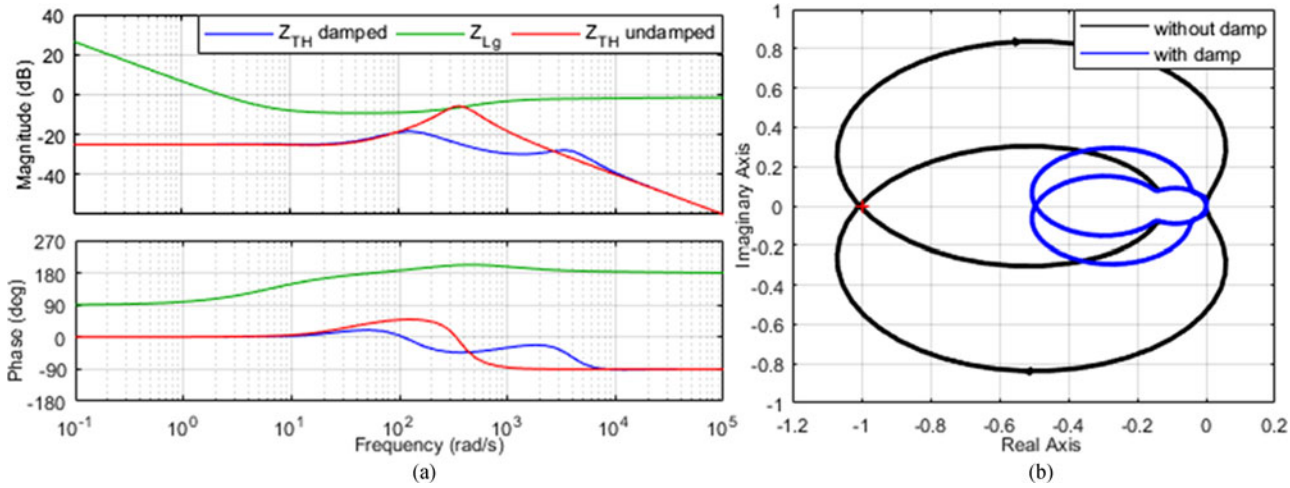

Fig. 13. Grid-connected operation with power scheme and the stabilizing loop enabled. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

signed to preserve the effective range of the stabilizing compensator so that it is still capable of including the resonance frequency dynamics of the dc-grid current; therefore, ω_3 is selected to be as small as possible (few Hz). Finally, the stabilizing gain K_d could be chosen such that the grid-connected system gain margin is higher than 6 dB and the phase margin is set to 60°, as recommended in [33], to guarantee acceptable stability margins.

The impact of the stabilizing loop on the dynamics of the dc grid-connected system can be evaluated with the help of the equivalent impedance circuit developed in Fig. 7, where the stabilizing impedances obtained in (45) and (47) are added to the source-side impedance to mimic the stabilizing effect of a physical resistance of connected across the feeder impedance.

For the current scheme, with the PFB gain set to 1.25 p.u., it is clear that the source-side impedance resonance peak has been significantly damped, as illustrated by the impedance frequency response shown in Fig. 12(a). The dynamics of the stabilizing impedance is effective in the range of the *LC* network resonance frequency, leading to no intersections between the source and the load-side impedances, which indicates absolute system stability. The stability of the entire system is verified with the help of the Nyquist plots presented in Fig. 12(b). It is obvious that the system shows a remarkable stable behavior with the damping loop employed, in which the gain margin has increased from –8 dB with the damping loop deactivated to 6 dB by setting the stabilizing gain to 40 p.u. This is also accompanied by an infinite phase margin as the Nyquist contour does not cross the unit circle.

Similarly, for the power scheme, the frequency response depicted in Fig. 13(a) shows that the impedance intersections are completely eliminated with the stabilizing loop being activated; further, the source-side equivalent impedance shows well-damped behavior at the *LC* resonance range. Furthermore, the overall marginal stability is improved by shifting the Nyquist contours away from $(-1, 0)$, where the gain margin is significantly improved to 6 dB with infinite phase margin (see Fig. 13(b)) with the stabilizing gain set to 30 p.u. It should be noted that the source-side phase angle is shifted toward 0° at the *LC* resonance frequency proximity, for both schemes, indicating the positive resistance damping effect of the stabilizing impedance.

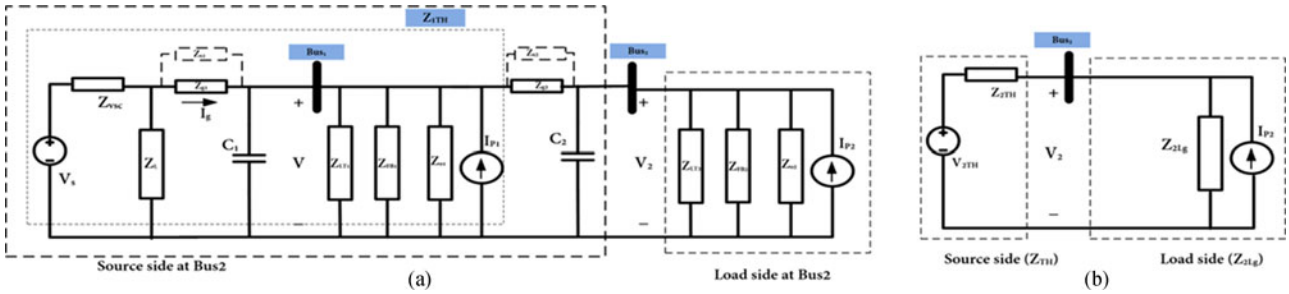

Fig. 14. Multiple DG dc distribution network. (a) Two-DG impedance model of dc distribution system. (b) Two-impedance equivalent circuit.

F. System Expandability

The system capacity can be expanded to meet the growth of the load demand that requires adding more DG units at different locations; the DGs can be connected at the same PCC or different locations of the distribution feeder (radial distribution configuration). Because the radial configuration has shown more stability issues than the other configurations, a two-DG radial distribution system is considered to assess the overall system dynamics with multiple DGs.

The small-signal impedance equivalent circuit of the two-DG radial system is shown in Fig. 14(a), where the system in Fig. 7 is expanded by extending the dc distribution feeder (Z_{g2}) to Bus 2, where a second DG unit, composite load, and bus capacitance are connected at the terminals of Bus 2. The two-subsystem equivalent circuit is depicted in Fig. 14(b), where the interactions between the initially stable single bus system and the new system added are investigated. The source-side impedance (Z_{2TH}) counts for all the components connected behind the equivalent bus capacitance (C_2), whereas the load-side impedance (Z_{2Lg}) represents the equivalent impedances of the second DG unit equipped with PFB schemes and the load connected to the same bus. The DG unit with PFB schemes, load, VSC impedances/admittances, and the two-subsystem dynamics developed in the previous section, remain unchanged except for the voltage at Bus2 given in (48) to consider the dynamics of the new components added to the existing system. The stabilizing impedances developed in (45) and (47) are updated to consider the dynamics of the entire grid impedance seen at Bus 2, as given in (49):

$$V_2(s) = (V_{2TH}(s) + I_{P2}(s)Z_{2TH}(s))\frac{1}{1 + Z_{2TH}(s)/Z_{2Lg}(s)}. \tag{48}$$

$V_{2\mathrm{TH}}$ is the Thevenin's equivalent voltage for the source subsystem seen by Bus2; $Z_{2\mathrm{TH}}$ is the Thevenin's equivalent impedance for the source subsystem seen by Bus2; and Z_{2Lg} is the Thevenin's equivalent impedance for the load subsystem seen by Bus2:

$$Y_{2S} = \frac{G_{2s}(s)Y_{2dc}(s)}{G_{2p}(s)V_2{}^o + G_i(s)}. \tag{49}$$

$G_{2s}(s)$ is the stabilizing compensator for DG2, and

$$Y_{2dc}(s) = \frac{1}{Z_{2dc}(s)},\ Z_{2dc}(s) = Z_{1\mathrm{TH}}(s) + Z_{2g}(s)$$

where $Z_{1\mathrm{TH}}$ is the Thevenin's equivalent impedance for the system between the VSC and bus 1, and Z_{2g} is the dc grid impedance of the feeder between Bus1 and Bus2.

The performance of the two-DG radial system is assessed with the help of the frequency response and Nyquist plots, with both DG units delivering their rated power and the CPLs consuming their rated power. The first DG unit is located 0.5 km away from the VSC bus, and the second bus is located 1 km away from the first bus. Fig. 15(a) shows the frequency response of the two subsystems with the PFB schemes disabled. It is clear that the source-side impedance has two peaks close to the resonance frequency of the two *LC* networks seen by both DGs, and that there is no intersection with the load subsystem impedance at Bus2 indicating a stable system. The multiple DG system stability is further verified by the Nyquist plot shown in Fig. 15(b). With the current scheme activated, the source-side impedance shows an increase in the magnitude in the frequency range of the first *LC* network resonance.This change represents the impact of the PFB current scheme employed by the first DG unit, which is expected to affect the source-side impedance of the multiple DG system as indicated in (48). The load-side impedance shows a magnitude reduction because of the PFB effect employed in the second DG unit. The PFB effect causes the two subsystem impedances to intersect at the frequency range of the *LC* networks developed. The frequency response interactions are mapped into the Nyquist plot in Fig. 15(b), where the Nyquist contour encircles $(-1, 0)$ with a significant negative high gain margin close to –16.5 dB indicating an unstable system with the current scheme employed.

With the power scheme being activated, the frequency response of the source-side impedance magnitude shows a smaller peak close to the *LC* resonance of the first bus if compared to the current scheme, as demonstrated in Fig. 16(a). The load-side impedance at Bus2 shows a reduction in the magnitude with the power islanding scheme activated leading to an intersection with the source-side impedance around the resonance frequency of the second *LC* network. The impedances interactions are transformed into the Nyquist contours in Fig. 16(b). The gain margin with the PFB power scheme employed is close to −5 dB, which indicates system instability with the power detection scheme. Therefore, employing the stabilizing loop to the multiple DG system becomes mandatory to mitigate the overall system instability issues for both islanding detection schemes.

The impact of the stabilizing loop on the multi-DG system for both islanding detection schemes is examined with the Nyquist

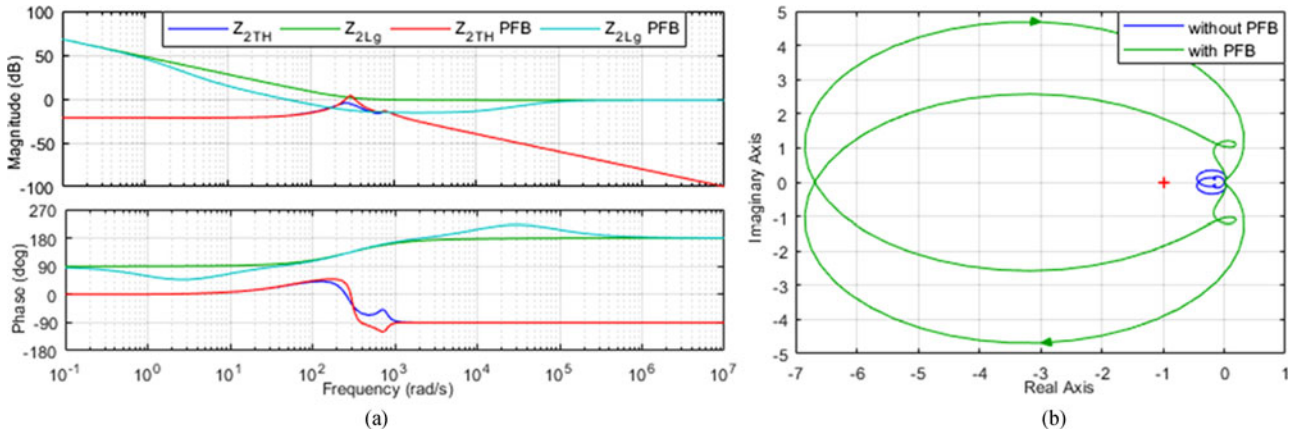

Fig. 15. Multiple DG operation, current scheme. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

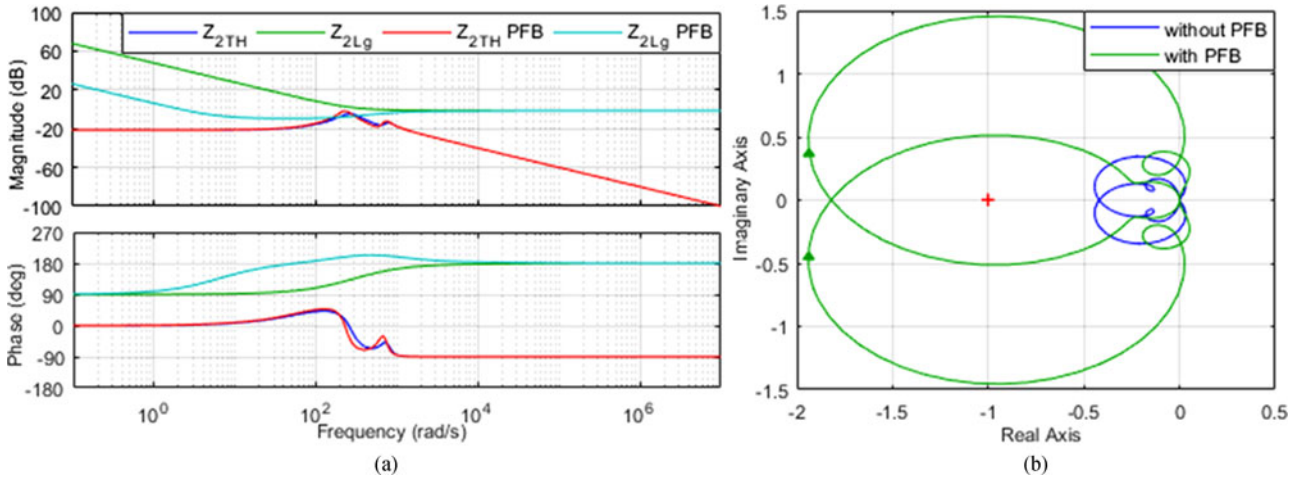

Fig. 16. Multiple DG operation, power scheme. (a) Bode plot of source-side and load-side impedances. (b) Nyquist plots.

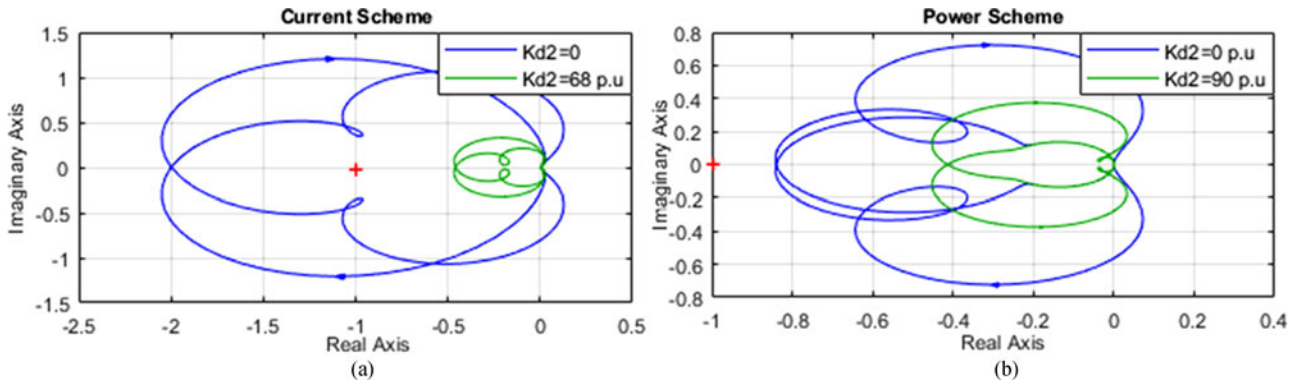

Fig. 17. Nyquist plots for damped multiple DG operation. (a) Current scheme. (b) Power scheme.

criterion, as shown in Fig. 17. For the current scheme [see Fig. 17(a)], it is clear that the system is only stable with the stabilizing loop activated for both DG units; the gain margin is 6 dB when the stabilizing gain of the second DG is set to 68 p.u. The Nyquist contours encircle $(-1, 0)$ if the second DG unit stabilizing loop is not functioning resulting in -6 dB gain margin. Similarly, the Nyquist plots shown in Fig. 17(b) verify the stability enhancement achieved by the stabilizing loop for the expanded system with the power scheme. It should be noted that with the stabilizing loop enabled for both DG units, the system stability margin is improved significantly, where the system gain margin is increased by 6 dB with the stabilizing gain

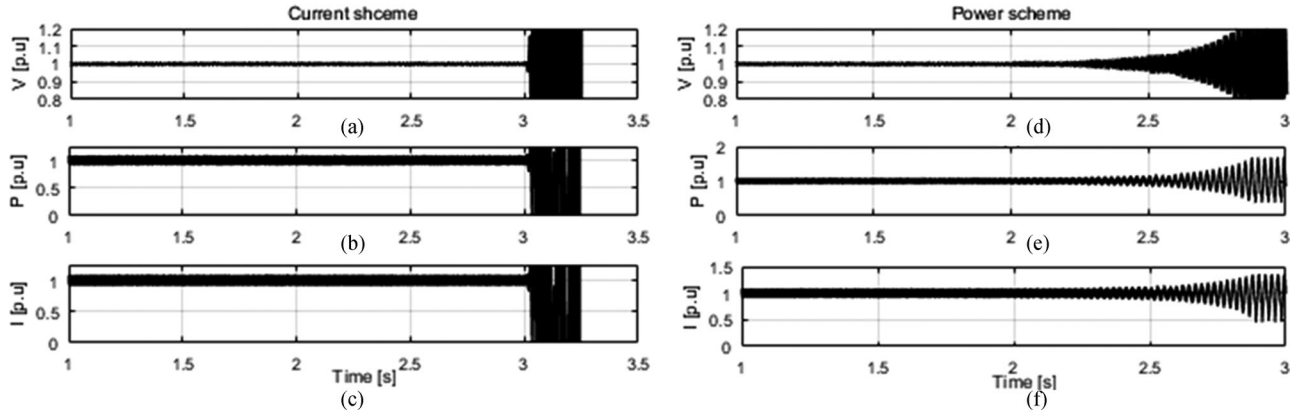

Fig. 18. System response without stabilizing loop for the current and power schemes, respectively: (a), (d) voltage at the PCC, (b), (e) DG output power, and (c), (f) injected current.

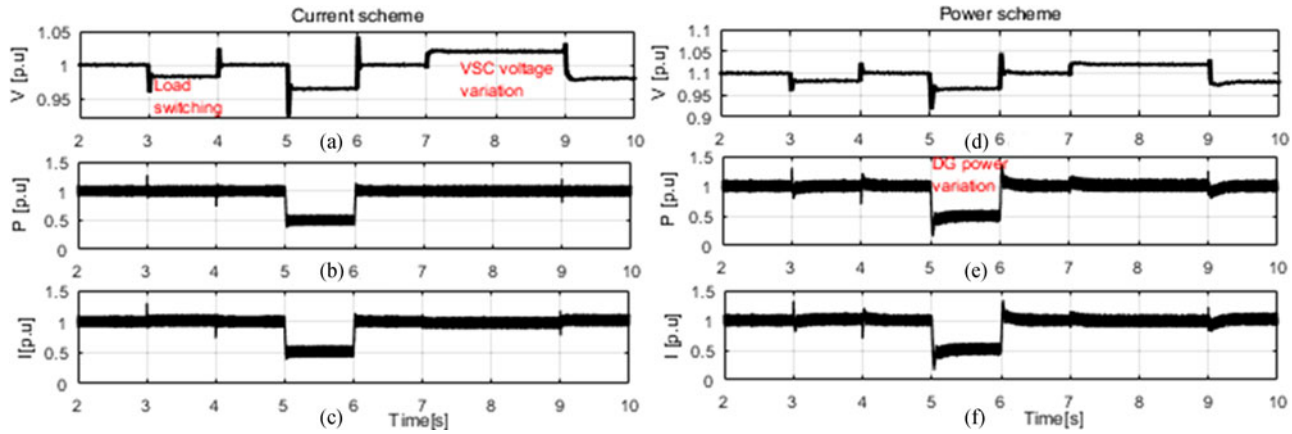

Fig. 19. System response with stabilizing loop applied to the current and power schemes, respectively: (a), (d) voltage at the PCC, (b), (e) DG output power, and (c), (f) DG output currents.

of the second DG set to 90 p.u. The gain margin was limited to 1.9 dB with only activating the stabilizing loop of the first DG.

IV. Simulation and Experimental Results

A. Nonlinear Simulation Results

In this section, time-domain simulation studies based on the detailed nonlinear models of the system components, under the MATLAB/Simulink environment, are conducted to evaluate the stability performance of the typical dc distribution system shown in Fig. 1. The grid-connected system performance is investigated with the PFB islanding detection schemes. The PFB gains are set to 1.25 p.u. for the current and the power schemes with a DG located at 1.0 km away from the VSC. Furthermore, the performance of the two-DG system equipped with both PFB islanding detection schemes is examined with the stabilizing loop being enabled.

1) System With PFB Schemes: Fig. 18(a) and (d) show the responses of the DG unit voltage equipped with the current and power islanding detection schemes, respectively. For the current scheme, with the PFB gain set to its marginal detection value (1 p.u.), the grid-connected system goes to an unstable state when the PFB scheme is activated at $t = 3$ s; this agrees with the instability condition given by the Nyquist plot given in Fig. 10(b). On the other hand, with the power scheme employed, the DG voltage starts to oscillate when the PFB gain is set to 1.25 p.u. at $t = 2$ s, and the voltage then goes to an unstable state dramatically because of the PFB effect. It is clear that the system response confirms the Nyquist criterion results shown in Fig. 11(b). It should be noted that the current and the power responses [see Fig. 18(b)–(f)] are driven into an unstable condition indicating the unstable behavior for the entire system quantities.

2) System With Stabilization Loop: The test employed to examine the grid-connected system without the PFB detection schemes, and with the stabilizing gains set to the values obtained in Section III, is conducted to investigate the impact of the stabilizing loop on the DG unit performance. The system response for both schemes is shown in Fig. 19; the stabilizing loop can preserve the system stability with the PFB schemes being activated. Furthermore, the voltage response shows a well-damped behavior with overshoots less than 5% against the system disturbances imposed by load switching, the VSC, and DG unit reference power variation, as presented in Fig. 19(a) and (d) for the current and power schemes, respectively. It is noted that the output power response of the DG unit with the power scheme

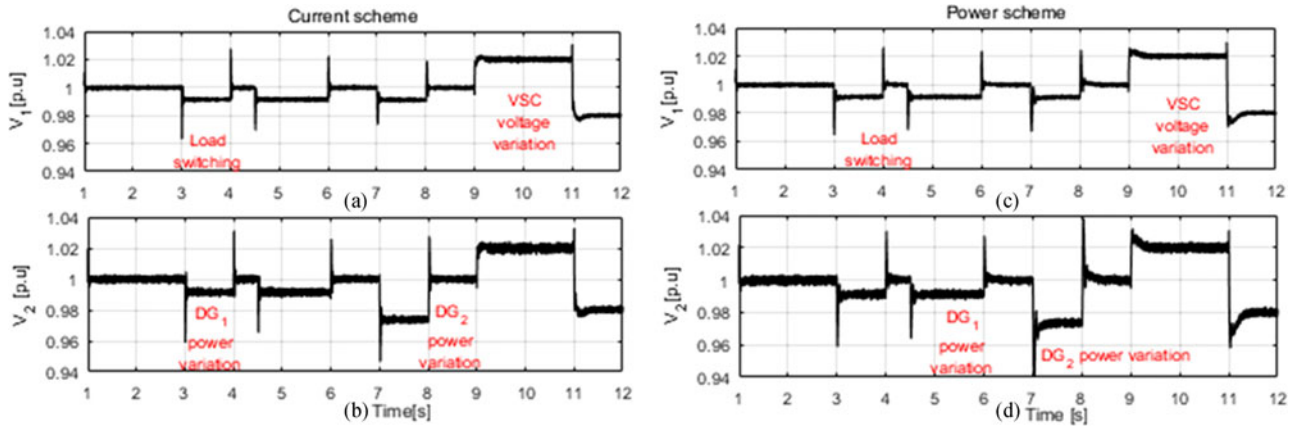

Fig. 20. Stabilized system response of two DG operation equipped with the current and power schemes: (a), (c) voltage at DG1 and (b), (d) voltage at DG2.

shows an increased overshoot for the external disturbances applied to the system, whereas the current scheme shows negligible power overshoots for the same disturbances applied as indicated in Fig. 19(b) and (e), respectively. Similar overshoots can be observed in the DG injected current in Fig. 19(c) and (f). The imposed overshoots on the power and current waveform are generated because of the perturbation component induced by the PFB loop, which is added to DG outer controller, as illustrated in Fig. 2(a).

3) Multiple DG Operation: The performance of the two-DG system is evaluated when both DGs are equipped with the PFB islanding detection schemes, and the proposed stabilizing loop is enabled. The system performance is evaluated for the following scenario: initially, the output power of both DG units is 1 p.u., the load at Bus1 is increased to 125% at time $t = 3$ s for 1.0 s. The reference power command for the first DG is dropped by 0.25 p.u. at $t = 4.5$ s, then the DG is retained to its rated power at $t = 6$ s. The reference command of the second DG is decreased to 0.75 p.u. for 1.0 s, and then, it is returned to 1 p.u. at $t = 8$ s. The PFB and the stabilizing gains are set to the values developed in Section III. The first DG is located at 0.5 km from the VSC, and the second DG is located 1.0 km away from the first one.

The voltage response of the two buses under investigation with the DG units equipped with PFB islanding detections schemes is shown in Fig. 20. The load switching is associated with a minor overshoot of magnitude 0.03 p.u. at both buses for both schemes; similarly, the output power variation for both DG units causes overshoots at the system buses with an almost identical magnitude. It is clear that the system was able to respond smoothly to the variation of the dc grid voltage generated at the VSC port, ensuring the capability of the system to reject the external system disturbances successfully. It should be noted that the overshoots on bus voltages with the PFB power scheme are slightly higher than the overshoots with the PFB current scheme; this is expected in the multiple DG operation case because of the PFB effect discussed in the single DG operation.

4) Fault Analysis: The performance of the dc distribution system is investigated under various types of faults that could happen in the ac and dc sides. Several case studies were carried out to evaluate the impact of the PFB islanding detection and stabilizing loop proposed on the system dynamics under faulty conditions; only significant results are presented in this section. Fig. 21 shows the dc grid response to a line-to-ground fault on the ac side at time $t = 1.5$ s. The dc bus and DG bus voltages show sustained oscillations of magnitude 0.05 p.u. and at the double of the ac grid frequency (120 Hz), whereas the average dc-link voltage is regulated at 1 p.u. until the fault is cleared at $t = 2$ s. The DG output power shows an oscillating response at double the ac grid fundamental frequency during the fault interval. These oscillations are superimposed on the DG output power because of the PFB loop component added to the inner loop of the current scheme and the outer loop of the power scheme. It is obvious that the dc voltage succeeded to recover to its nominal value in approximately 0.2 s after the fault is cleared for both islanding detection schemes, which preserves the fault ride-through feature of the hybrid network during the faulty conditions on the ac side.

Furthermore, the system performance is evaluated under faults occurring on the dc-side at different locations for both the islanding detection schemes, as illustrated in Fig. 22. The dc network is subjected to line-to-ground fault events at $t = 1.5$ s with fault impedance of 0.0012 p.u. at the DC bus (VSC terminals), dc feeder midpoint, and at the DG bus. It is clear that the voltages at the DC bus and the DG bus drop to zero for a fault condition at the dc-link bus, whereas a fault occurring at the midpoint of the dc feeder causes the VSC voltage to drop by 60% and to collapse at the DG bus totally. During the DG bus fault interval, the DG bus voltage falls to zero as expected, whereas the VSC voltage drops to 50% of its rated value. It is clear that the system retained its operating condition successfully after the fault is cleared at $t = 1.6$ s. The current scheme shows a shorter recovery time (0.4 s) than the power scheme (0.55 s); however, both responses indicate an acceptable voltage ride-through performance on the dc side.

B. Experimental Results

A laboratory-scale dc distribution system, based on the system shown in Fig. 1, is used to validate the impedance-based

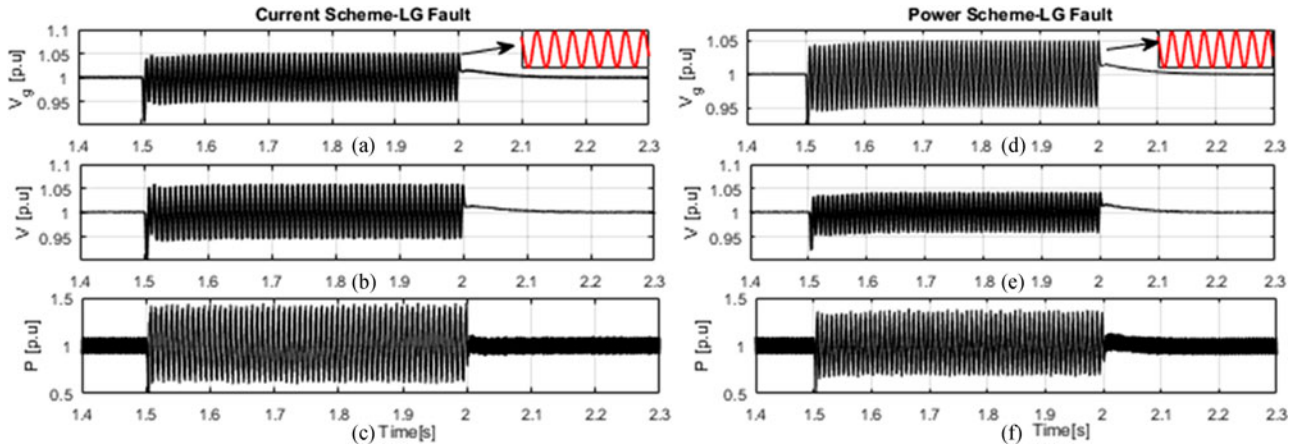

Fig. 21. DC distribution system response to L-G ac grid fault: (a), (d) VSC voltage. (b), (e) DG voltage. (c), (f) DG power.

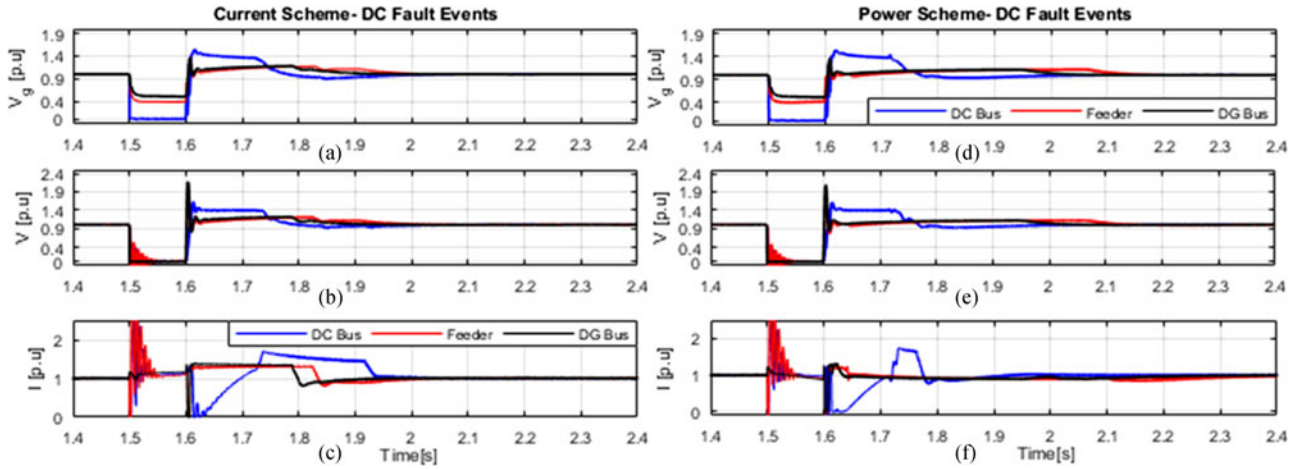

Fig. 22. DC distribution system response to dc faults at different locations. (a), (d) VSC voltage. (b), (e) DG voltage. (c), (f) DG current.

stability analysis conducted in the previous sections. Two Semistack-IGBT H-bridge-based converters are used to implement the ac/dc VSC and dc/dc converter that interfaces the DG unit to a variable load box through an *LC* filter. The distribution feeder line impedance is represented by an $R-L$ segment, which connects the dc grid source (VSC output) to the DG PCC. The dSPACE1104 control system is used to implement the proposed control scheme in real time. The pulse width modulation algorithm is implemented on the slave processor (TMS320F240-DSP) of the dSPACE controller. The dSPACE interfacing board is equipped with eight digital-to-analog channels and eight analog-to-digital channels to interface the measured signals to/from the control system. The software code is generated by the Real-Time Workshop under the MATLAB/Simulink environment. The switching frequency is 10 kHz. The current and voltage sensors used are HASS 50-S and LEM V 25-400, respectively. The parameters of the experimental setup are given in the Appendix. A view of the system setup is shown in Fig. 23.

The dc grid-connected system is investigated with the islanding detection schemes being enabled and the stabilizing loops disabled. The system response is shown in Fig. 24 for both

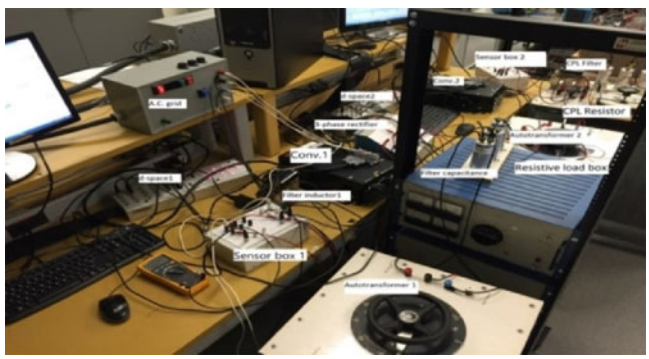

Fig. 23. Laboratory-scale setup of the dc distribution system.

schemes, where the feedback gains are set to values very close to the marginal gains for islanding detection. The dc distribution system voltage, current, and power exhibit oscillations with the PFB schemes being activated at $t = t_o$, and the system retains its stable operation when the PFB gains are set back to zero again at $t = t_1$.

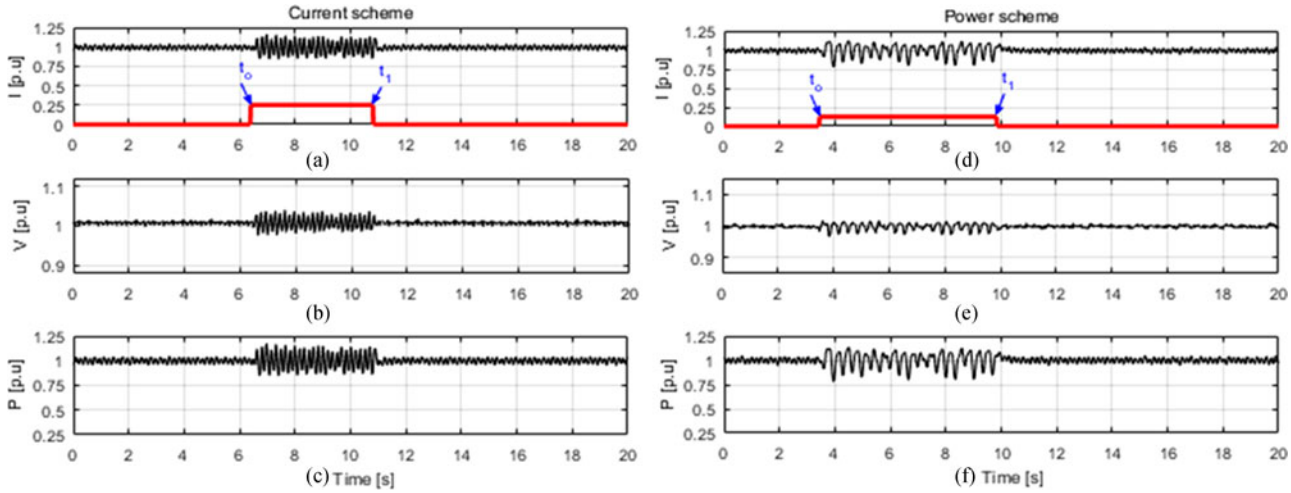

Fig. 24. Experimental results without stabilizing loop for DG equipped with current and power schemes, respectively: (a), (d) DG current, (b), (e) DG voltage, and (c), (f) DG output power.

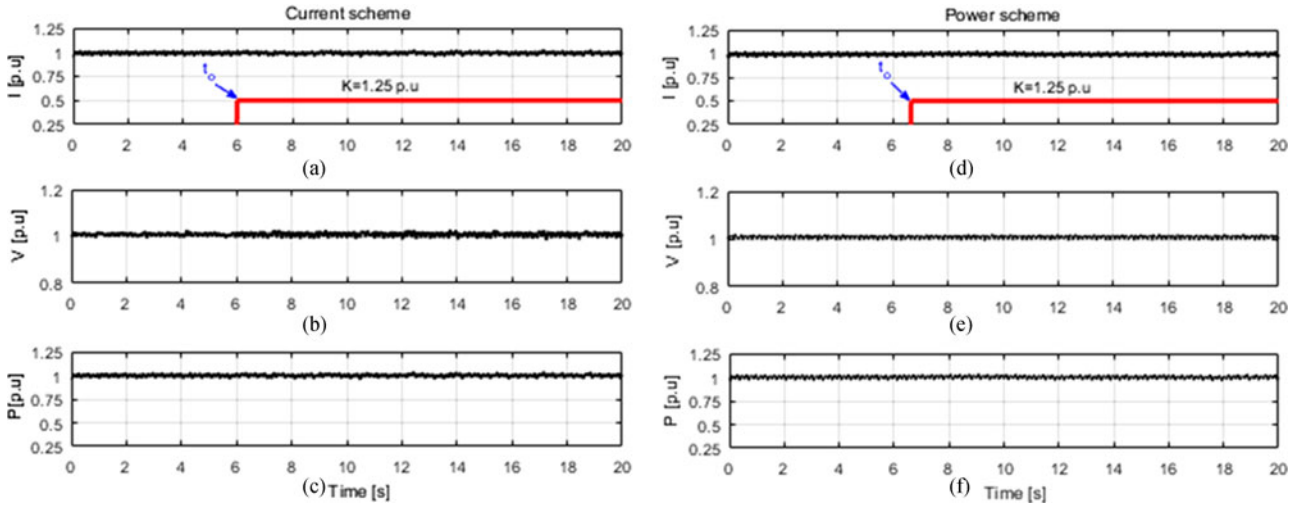

Fig. 25. Experimental results with stabilizing loop for DG equipped with current and power schemes, respectively: (a), (d) DG current, (b), (e) voltage, and (c), (f) DG output power.

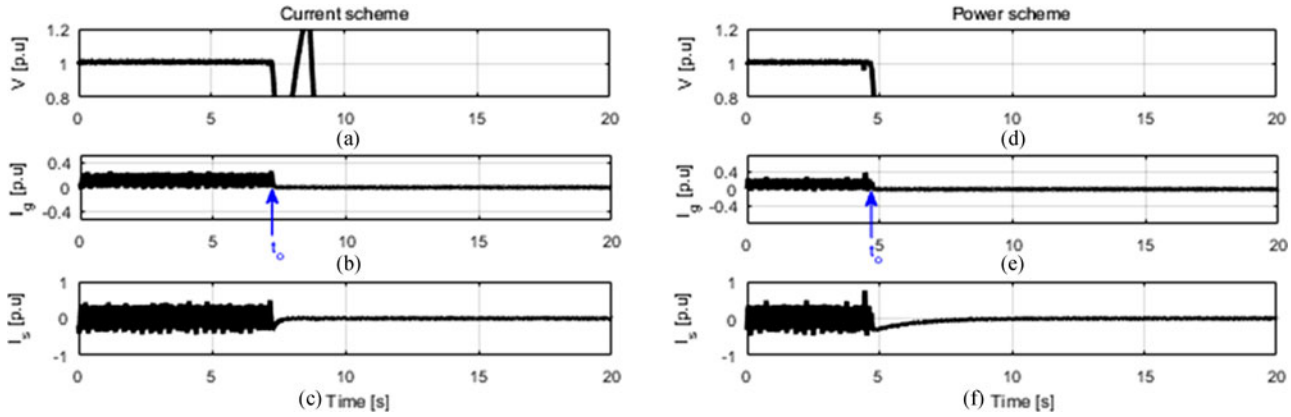

Fig. 26. Experimental results for islanding condition detection with the stabilizing loop applied, for DG equipped with current and power schemes, respectively: (a), (d) DG voltage, (b), (e) dc-grid current, and (c), (f) stabilizing current.

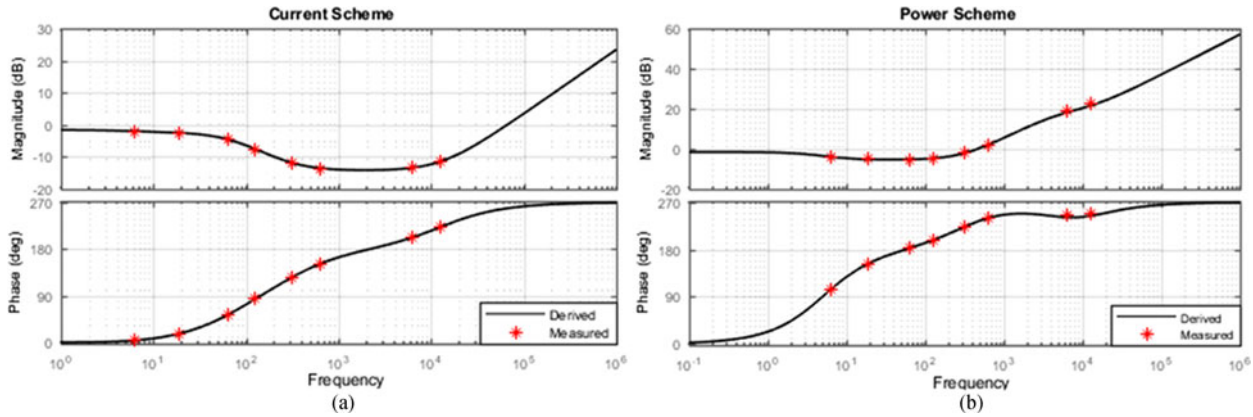

Fig. 27. Impedance validation for DG equipped with islanding detection schemes: (a) Current scheme. (b) Power scheme.

The system stability margin is remarkably improved when the stabilizing loop is activated, whereas the DG unit is equipped with the PFB islanding detection schemes. Fig. 25 shows the stabilized system response with the PFB gains set to 1.25 p.u. It is obvious that the stabilizing current succeeded in preserving the system stability when the PFB gains are suddenly activated at $t = t_o$ proving the functionality of the stabilizing loop. Finally, the islanding detection test was conducted to ensure the proper operation of the islanding detection schemes during the islanding events with the stabilizing loop enabled. The test is performed by setting the power mismatch between the load and the DG power to 0.15 p.u. to allow dc grid current flow, and hence the stabilizing loop input is not zero; furthermore, the connected load is a pure resistance to consider the worst case scenario for islanding detection. The current scheme results are shown in Fig. 26(a)–(c), where the system loses its stability when the islanding event occurs at $t = t_o$. Similarly, the power scheme method succeeded to detect the islanding event occurring at $t = t_o$, as depicted in Fig. 26(d) and (f). The stabilizing current (I_s) drops to zero when the grid is disconnected for both islanding detection schemes. The islanding test verified that both islanding detection schemes can work properly together and that there is no conflict between the operations of both loops, whereas the stabilizing loop is effective only when the grid is connected.

V. Conclusion

This paper presented a small-signal impedance analysis of a grid-connected dc distribution system considering its specific features. Detailed output impedances were developed for the VSC and the DG unit equipped with two active islanding detection methods. With the help of the impedance frequency response plots and the Nyquist impedance ratio criterion, the marginal gain to detect islanding was developed. Furthermore, the stability of the grid-connected system with the PFB schemes being employed was further evaluated. The following are the findings.

1) The impact of the islanding detection schemes on the DG output impedance appears in the bandwidth frequency range of the DG control loop, where the perturbation signal was injected.
2) The current PFB scheme has more negative impacts on the system stability if compared to the power scheme.
3) The instability in the grid-connected mode results from the interaction between the two subsystems impedances in the *LC* resonance frequency proximity.
4) The high CPL penetration level reduces the system stability margin remarkably, and its negative stability impact reduces the system overall stability margin.
5) Both schemes exhibit instability problems when applied to a multi-DG system.

The instability problem was mitigated by developing a grid-current-based stabilizing loop to the inner loop of the DG controller to enhance the system stability for single- and multi-DG systems. The damped system showed a remarkable stability improvement for single and multiple DG systems. The theoretical results were verified using detailed nonlinear simulations and experimental results using a laboratory-scale setup.

Appendix

A. Simulation System Parameters

DC distribution system rating: 500 V, 0.3 MW, cable parameters: 28.3 mΩ/km, 250 μH/km; $C = 10$ mF, power control loop bandwidth = 675 rad/s, current control loop bandwidth = 2 kHz, $\omega = 2\pi$ rad/s, $\omega_1 = 113.65$ rad/s, $\omega_2 = 5000$ rad/s, $\omega_3 = 2\pi$ rad/s.

AC grid and VSC: 5 MVA, 208 V, $G_{dc}(s) = 1.75 + 50/s$, $G_{ac}(s) = 33366/s$, VSC filter parameters: 50 μH, 0.6 mΩ, $K_{p\mathrm{PLL}} = 1.2\,\mathrm{rad}^2/\mathrm{s/V}$, $K_{i\mathrm{PLL}} = 1.2\,\mathrm{rad}^3/\mathrm{s}$.

B. Experimental System Parameters

DC distribution system: 50 V, bus capacitance = 150 μF, $G_p(s) = 0.2 + 0.1/s$, dc/dc converter filter reactance = 1.6 mH/0.016 Ω, converter switching frequency = 10 kHz, dc feeder parameters: 3.6 mH / 0.048 Ω.

AC grid and VSC: $G_{dc}(s) = 0.5 + 8/s$, $G_c(s) = 5 + 5/s$, VSC filter parameters:0.50 mH, 0.2 mΩ, $K_{p\mathrm{PLL}} = 1.2\,\mathrm{rad}^2/\mathrm{s/V}$, $K_{i\mathrm{PLL}} = 1.2\,\mathrm{rad}^3/\mathrm{s}$, converter switching frequency = 10 kHz.

C. Voltage and Current Frame Transformation

The transformation of the voltages and currents between the reference frames can be obtained by linearizing (27) into the following:

$$\tilde{U}_{cdq} = [T_{2dq}]\tilde{U}^{g}_{dq} + [T_{2\theta}]\tilde{\theta} \quad (27\text{-a})$$

$$\tilde{I}^{g}_{dq} = [T_{3dq}]\tilde{I}_{cdq} + [T_{3\theta}]\tilde{\theta} \quad (27\text{-b})$$

$$\tilde{V}_{Fcdq} = [T_{dq}]\tilde{V}^{g}_{Fdq} + [T_{\theta}]\tilde{\theta} \quad (27\text{-c})$$

where

$$[T_{2dq}] = \begin{bmatrix} \cos(\theta_o) & \sin(\theta_o) \\ -\sin(\theta_o) & \cos(\theta_o) \end{bmatrix},\ [T_{3dq}] = \begin{bmatrix} \cos(\theta_o) & -\sin(\theta_o) \\ \sin(\theta_o) & \cos(\theta_o) \end{bmatrix},$$

$$[T_{dq}] = \begin{bmatrix} \cos(\theta_o) & \sin(\theta_o) \\ -\sin(\theta_o) & \cos(\theta_o) \end{bmatrix}$$

$$[T_{2\theta}] = \begin{bmatrix} -U^{g_o}_{d}\sin(\theta_o) + U^{g_o}_{q}\cos(\theta_o) \\ -U^{g_o}_{d}\cos(\theta_o) - U^{g_o}_{q}\sin(\theta_o) \end{bmatrix},$$

$$[T_{3\theta}] = \underbrace{\begin{bmatrix} -I^{o}_{cd}\sin(\theta_o) - I^{o}_{cq}\cos(\theta_o) \\ I^{o}_{cd}\cos(\theta_o) - I^{o}_{cq}\sin(\theta_o) \end{bmatrix}}_{T3},$$

$$[T_{\theta}] = \begin{bmatrix} -V^{g_o}_{d}\sin(\tilde{\theta}_o) + V^{g_o}_{q}\cos(\theta_o) \\ -V^{g_o}_{d}\cos(\theta_o) - V^{g_o}_{q}\sin(\theta_o) \end{bmatrix}.$$

D. Derived Impedance Validation

The correctness of the derived impedances is validated following the same approach presented in [34], where the DG unit with the PFB islanding detection schemes is excited by a sinusoidal voltage source (0.02 p.u.) to inject variable frequency signals (1–1000 Hz) that excite different frequency modes of the DG. The output impedance can be obtained by measuring the corresponding voltage and current components for each of the injected frequency by the sinusoidal voltage source; these components are extracted with the help of the fast Fourier transform block embedded in the MATLAB Simulink library. Fig. 27 shows the frequency response of the derived and measured impedances for both schemes. The close matching in the magnitude and the phase angle between the derived and measured impedances validates the analytical results obtained in (14) and (16).

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