High Step-Up DC–DC Converter With Active Soft-Switching and Voltage-Clamping for Renewable Energy Systems

Liangzong He, *Member, IEEE*, Zhipeng Zheng, and Dong Guo

***Abstract*—A novel high step-up dc–dc converter with a coupled inductor and a switched capacitor is proposed in this paper, which is widely used in the renewable energy system as the front-end stage for low voltage sources. The combinational employment of the switched capacitor and the coupled inductor makes high voltage gain achievable without extreme duty cycle, resulting in reduced voltage stress on power switches. Hence, MOSFETs with low resistance $R_{DS}(ON)$ could be utilized as the main switch to reduce conduction loss. Meanwhile, due to the leakage inductance of the coupled inductor, the current falling rate becomes controllable, and the reverse-recovery problem of the output diode is alleviated. Importantly, by incorporating an active clamped-circuit, not only are voltage spikes caused by leakage inductance restrained, but also zero-voltage switching could be obtained for the main and auxiliary switches. Specially, the clamped circuit plays a role of energy transfer to boost the gain as well. Finally, a prototype with a power rating of 500 W is implemented to verify the performance of the proposed converter.**

***Index Terms*—Active clamp, high gain, switched capacitor, zero-voltage switching (ZVS).**

I. Introduction

In RENEWABLE energy systems with photovoltaic (PV) and fuel cells, high step-up dc–dc converters are in pressing demand because the low voltage generated by the PV and fuel cells should be boosted to a relatively high-standard dc bus voltage for the grid connection, as shown in Fig. 1. For instance, the output voltage of the most fuel-cell stacks or individual PV cells should be less than 40 V in consideration of cost and reliability issues for household applications, which means that a front-end dc–dc converter with over ten times voltage gain is essential to converse low output voltage of the fuel-cell stack or PV to a standard high bus voltage before a 220-V ac output grid connected. How to extend voltage gain, reduce the voltage stress on the switches, and improve the conversion efficiency constitute the main concerning issues [1]–[3].

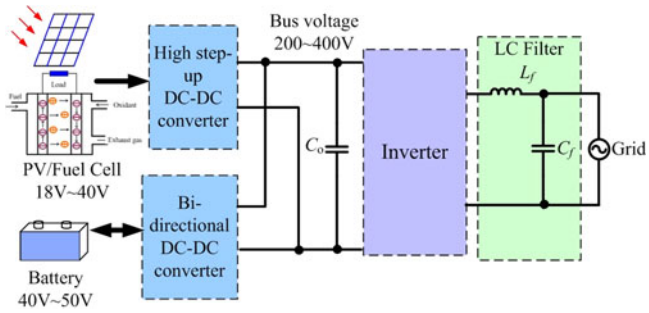

Fig. 1. General schematic of a renewable power generating system.

There are several approaches to attain high gain. Beyond all doubt, the conventional boost converter could not be qualified to provide a high voltage gain. High voltage stress on switches and extreme duty cycle, which results in huge conduction and switching loss and slow transient response, makes it weakly competitive in high step-up applications. Although some improved boost topologies have been reported, the above-mentioned issues have never been solved well due to the inherent defect of this kind of converters [4], [5].

Some isolated converters, such as fly-back, forward, push–pull, half-bridge, and full-bridge, by changing the turn ratio of a transformer are another approach to achieve a high step-up voltage gain [6], [7]. However, the main switches of these converters will suffer from high voltage spikes and high power dissipation due to the leakage inductor of the transformer. What is more, the power transformer volume blocks the development of a compact converter. Furthermore, the loss will increase because all the energy should be transferred through the transformer to the load in the isolated converters. To solve these drawbacks, a nondissipative snub circuit and an active clamp circuit have to be utilized. In addition, it is ineluctable to bring about addition cost.

To achieve a high step-up voltage gain with the improved conversion efficiency, various single power stage topologies have been developed as well in recent years. The switched-capacitor converter (SCC) is one of such hot classes of converters [8], [9]. Unfortunately, the main disadvantage of the SCC topology captures their poor regulation, resulting in pulsating input cur-

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rent and fixed voltage conversion ratio. Even that some research works have made considerable effort to improve the regulation ability for SCCs [10]–[14], the regulation margin is still limited. Also, there is no report about regulation methods for high gain if the voltage levels of SCCs have been extended. Coupled-inductor-based technology is another solution for gain extension [15], [16]. However, the leakage inductance of the coupled inductor and the parasitic capacitor of the output diode maybe resonate together, and a proper snub circuit is required to absorb the voltage ringing on the output diode, and the use of additional protection circuit increases both the cost and complexity of the circuit. Meanwhile, the pulsating input current and high peak current flowing through the clamp capacitor kills system efficiency further.

Considering the shortages of single solution in high gain applications, the combinatorial utilization of a coupled inductor and voltage multiplier is proposed [17]–[24]. Extended voltage gain, reduced voltage stress across switches, and alleviated diode reverse-recovery could be obtained for those converters. However, soft-switching realization becomes a major concerning problem to be solved in those converters due to their high frequency switching operation, which will result in heavy press in heat dissipation under a hard-switching operation. An active clamp converter with voltage multiplier is reported in [25]–[27], which is a good choice for high gain applications. Even that ZVS-off is realized for main switch and clamped switch, the turn-on operation of those switches is still in hard switching. Also, voltage stress of the output diode is up to output voltage, and a relative large turn ratio of coupled inductor should be employed to satisfy the high-gain requirement. A passive snubber circuit, which provides zero-voltage switching (ZVS) or zero-current switching (ZCS) for switches, is presented in [28] and [29]. In this snubber circuit, additional coupled inductor along with a capacitor–diode combination is required, which increases component count in some extent. A high-gain converter with an active clamp and a ZVS operation is presented in [30], but the four active switches operation brings about control complexity and secondary winding of the coupled inductor that never participates in voltage gain enhancement.

In the paper, considerable effort has been focused on the realization of soft switching and active clamping for an ultrahigh-gain and high-efficiency converter with concise structure and low cost. In the proposed converter, leakage inductance of the coupled inductor is used to limit the current falling rate, as compared with [31]. Meanwhile, this entire leakage energy of the coupled inductor is employed to provide ZVS for the main and auxiliary switches as well. A capacitor in the clamped circuit not only absorbs the voltage spike, but also undertakes as a resonant capacitor. In addition, part of the energy stored in the clamp circuit could be transferred to the load rather than fed back to input power source, as compared with [32]. In other words, the active clamped-circuit has participated in promoting gain. Those distinctive merits of the proposed converter contribute to reduce the switching loss and, thus, enable it to operate at higher switching frequency with high efficiency. Also, the power density could be improved due to the reduced size of magnetic components. Switched capacitor extends voltage gain in the meantime and suffers from part of voltage stress giving rise to reduced voltage stress on the switches. Because of that it is available to adopt switches with low on-state resistance $(R_{\mathrm{DS(ON)}})$. Additionally, the reverse recovery problem of the output diode will be eliminated due to the presence of leakage inductance.

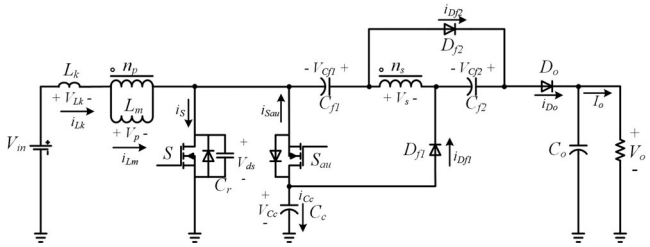

Fig. 2. Proposed soft-switching high step-up dc–dc converter.

The paper is organized as follows. The topology description and operation principles are introduced in Section II. Then, the performance of the proposed converter is analyzed in Section III. ZVS condition of the proposed converter is analyzed in Section IV. Finally, a prototype of a 500-W output power and 400-V output voltage is implemented to verify excellent performance of the proposed converter in Section V.

II. Proposed Converter and Operation Principle

The proposed converter with the coupled inductor and voltage multiplier is shown in Fig. 2, along with normal direction of current through the elements. The coupled inductor is represented by its equivalent transformer model, which includes an ideal transformer, magnetizing inductance L_m, and leakage inductance L_k referred to the primary. The voltage multiplier consists of two switched-capacitors C_{f1} and C_{f2} and feedforward diodes D_{f1} and D_{f2}. Switched capacitors C_{f1} and C_{f2} are charged in parallel and discharged in series by the secondary side of the coupled inductor when the main switch S is turned ON and turned OFF, respectively. The active clamped-circuit is composed of auxiliary switch S_{au} and clamped capacitor C_c. Thus, leakage inductance energy of the coupled inductor is recycled to the capacitor C_c, and voltage stress of the main switch *S* will be clamped. Besides, the recycled energy in capacitor C_c can be transferred to switched capacitor C_{f1}, which extends the voltage gain further. The output diode D_o and output capacitor C_o play the similar roles to their's in a normal boost converter.

Before the operation analysis, the following conditions are assumed.

1) The magnetizing current is operated in a continuous mode.
2) The switches and other components are considered to be an ideal device without parasitic parameters except the leakage inductance for the coupled inductor and parasitic capacitor C_{r} for the main switch.

There are eight operation modes in one switching period. Key waveforms of the converter are shown in Fig. 3, and the simplified equivalent circuit for each mode is sketched in Fig. 4. The operation modes are described as follows.

Mode 1 $[t_0-t_1]$: In the mode, main switch S is turned ON and voltage across C_r maintains zero during the whole mode,

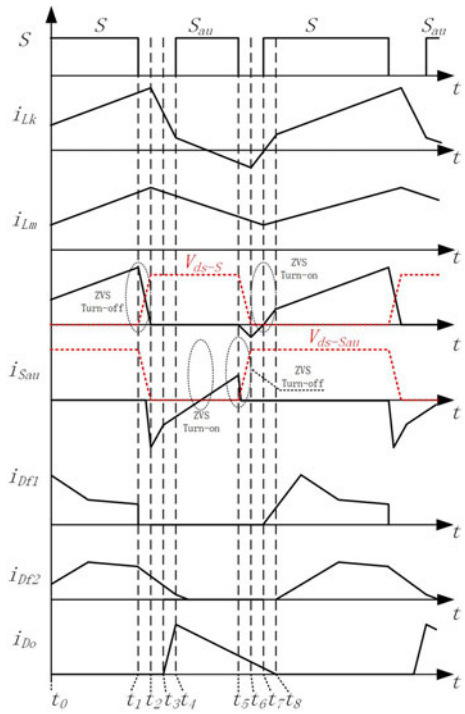

Fig. 3. Key waveforms of the proposed converter.

while auxiliary switch $S_{\rm au}$ remains in off-state. The current of magnetizing inductance L_m and leakage inductance L_k increases linearly. The switched capacitor C_{f1} is charged through the clamped capacitor C_c, the feedforward diode D_{f1}, and the secondary winding of the coupled inductor. At the same instant, switched capacitor C_{f2} is charged through feedforward diode D_{f2} and the secondary winding of the coupled inductor, as shown in Fig. 4(a). Output diode D_o is reverse biased, and output capacitor C_o transfers its energy to load. The current of magnetizing inductance L_m and leakage inductance L_k are given by

$$i_{\rm Lm}(t) = i_{\rm Lm}(t_0) + \frac{V_p}{L_m}(t - t_0) \tag{1}$$

$$i_{\rm Lk}(t) = i_{\rm Lk}(t_0) + \frac{V_{\rm in} - V_p}{L_k}(t - t_0) \tag{2}$$

where $V_p = V_{\rm in} L_m/(L_m + L_k)$.

Mode 2 $[t_1{-}t_2]$: The mode starts at t_1, when main switch S is turned OFF. The parasitic capacitor C_r of the main switch is charged by the leakage inductor current. Voltage across main switch S will increase from 0 to $V_{\rm Cc}$ gradually. Thus, main switch S is turned OFF under zero-voltage condition. Switched capacitor C_{f2} is still charged while C_{f1} will stop being charged. The drain-to-source voltage of the main switch $V_{\rm ds\_S}$ and the current of leakage inductance L_k are expressed as

$$v_{\rm ds\_S}(t) = V_{\rm in}(1 - \cos(\omega_1(t - t_1))) + i_{\rm Lk}(t_1)Z_1 \times \sin(\omega_1(t - t_1)) \tag{3}$$

$$i_{\rm Lk}(t) \approx i_{\rm Lm}(t_1)\cos(\omega_1(t - t_1)) + \frac{V_{\rm in} - v_{\rm ds\_S}(t1)}{Z_1} \times \sin(\omega_1(t - t_1)) \tag{4}$$

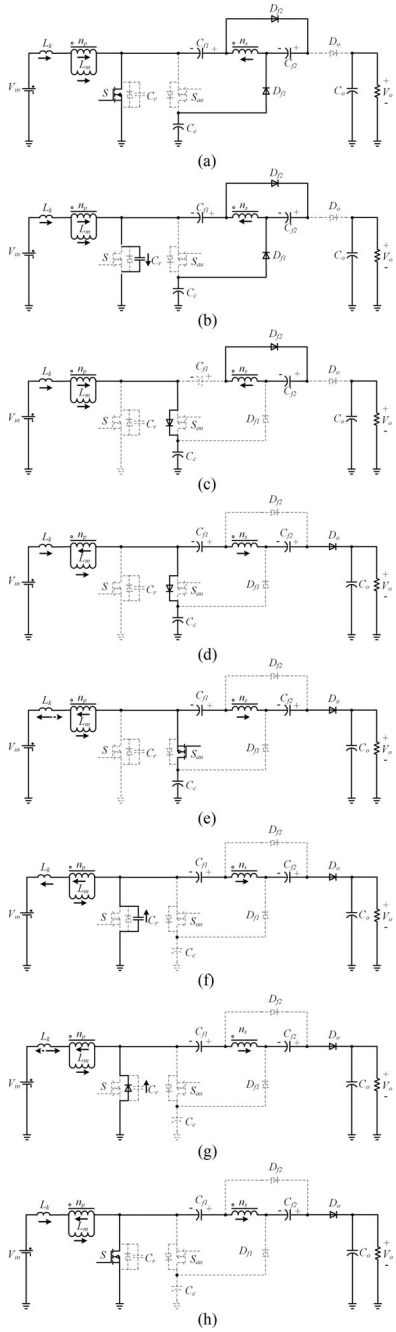

Fig. 4. Equivalent circuits for each operation mode (dashed and solid arrows represent current direction at the beginning/end of the mode, respectively): (a) Mode 1 $(t_0{-}t_1)$. (b) Mode 2 $(t_1{-}t_2)$. (c) Mode 3 $(t_2{-}t_3)$. (d) Mode 4 $(t_3{-}t_4)$. (e) Mode 5 $(t_4{-}t_5)$. (f) Mode 6 $(t_5{-}t_6)$. (g) Mode 7 $(t_6{-}t_7)$. (h) Mode 8 $(t_7{-}t_8)$.

where $\omega_1 = 1/\sqrt{C_r(L_m + L_k)}$ and $Z_1 = \sqrt{(L_m + L_k)/C_r}$. Notice that the voltage across C_r will reach up to $V_{\rm Cc}$ at the end of this mode.

Mode 3 $[t_2{-}t_3]$: The mode starts at t_2, when drain-to-source voltage of the main switch $v_{\rm ds\_S}$ reaches up to $V_{\rm Cc}$. The antiparallel body diode of auxiliary switch $S_{\rm au}$ begins to conduct, and feedforward diode D_{f1} is reverse biased, as shown in Fig. 4(c). Leakage inductance L_k begins to resonate with clamped capac-

itor C_c, thus input power source $V_{\rm in}$, clamped capacitor C_c, and leakage inductance L_k compose a resonant loop. The current of clamped capacitor is obtained as

$$i_{\rm Cc}(t) = i_{\rm Lk}(t) \approx i_{\rm Lk}(t3)\cos(\omega_2(t-t_3)) + \frac{V_{\rm Lk}(t)}{Z_2} \times \sin(\omega_2(t-t_3)) \quad (5)$$

where $\omega_2 = 1/\sqrt{L_k C_c}$,$Z_2 = \sqrt{L_k/C_c}$ and $\omega_2 = 1/\sqrt{L_k C_c}$, $Z_2 = \sqrt{L_k/C_c}$.

Notice that voltage across C_r is clamped to $V_{\rm Cc}$ during the whole mode. Hence, voltage stress of main switch S will be clamped to $V_{\rm Cc}$. Since capacitance value of clamped capacitor C_c is much larger than that of C_r, most of the magnetizing current is diverted through the antiparallel body diode of $S_{\rm au}$ to charge C_c. Meanwhile, the current of magnetizing inductance L_m starts to decrease. Consequently, the current $i_{\rm Df2}$ will decrease slowly down to zero at t_3, and the reverse-recovery problem of feedforward diode D_{f2} is alleviated.

Mode 4 $[t_3{-}t_4]$: At t_3, feedforward diode D_{f2} is reverse biased, and output diode D_o starts to conduct. Input voltage $V_{\rm in}$, magnetizing inductance L_m, switched capacitors C_{f1} and C_{f2} release their energy to load in series. Leakage inductance L_k continues to resonate with clamped capacitor C_c. In order to achieve ZVS for auxiliary switch $S_{\rm au}$, switch $S_{\rm au}$ should be turned ON before the resonate current $i_{\rm Cc}$ changes its direction.

Mode 5 $[t_4{-}t_5]$: At t_4, auxiliary switch $S_{\rm au}$ is turned ON under ZVS condition. Then, leakage inductance current $i_{\rm Lk}$ will reverse its direction, as shown in Fig. 4(e). Input power source $V_{\rm in}$, magnetizing inductance L_m, capacitors C_{f1} and C_{f2} release continuously their energy to load in series. The same as previous mode, $v_{\rm Cr}$ continues to maintain clamped voltage $V_{\rm Cc}$ until the end of this mode.

Mode 6 $[t_5{-}t_6]$: At t_5, auxiliary switch $S_{\rm au}$ is turned OFF. A new resonant loop is composed of input power source $V_{\rm in}$, leakage inductance L_k, and parasitic capacitor C_r of the main switch S. Parasitic capacitor C_r is discharged by leakage inductance current i_k. Voltage across capacitor C_r decreases and can be given by

$$v_{\rm Cr}(t) = v_{\rm ds\_}S(t) \approx V_{\rm in} - V_p - (V_{\rm in} - V_p - v_{\rm Cr}(t_5)) \times \cos(\omega_3(t-t_5)) + i_{\rm Lk}(t_5)Z_3\sin(\omega_3(t-t_5)) \quad (6)$$

where $\omega_3 = 1/\sqrt{L_k C_r}$ and $Z_3 = \sqrt{L_k/C_r}$.

The mode ends at t_6, when the parasitic capacitor is discharged by leakage inductance current completely. In addition, parasitic capacitor voltage $v_{\rm Cr}$ decreases to zero. Therefore, the following relation is established:

$$\frac{1}{2}L_k {i_{\rm Lk}}^2(t_5) \geq \frac{1}{2}C_r {v_{\rm Cr}}^2(t_5) \quad (7)$$

Mode 7 $[t_6{-}t_7]$: At t_6, the antiparallel body diode of main switch *S* starts to conduct and $v_{\rm Cr}$ becomes to zero, as shown in Fig. 4(g). Input power source $V_{\rm in}$, magnetizing inductance L_m, capacitors C_{f1} and C_{f2} still release their energy to load in series. Then, leakage inductance current $i_{\rm Lk}$ will reverse its direction. In order to reach ZVS for main switch S, it should be turned ON during this interval.

Mode 8 $[t_7{-}t_8]$: At t_7, main switch S is turned ON under ZVS condition and $v_{\rm Cr}$ continues to be zero. The current of magnetizing inductance L_m and leakage inductance L_k starts to increase linearly. The current of output diode D_o starts to decrease linearly. At t_8, output diode D_o is reverse biased and switched capacitors C_{f1} starts to be charged by C_C and the secondary winding of coupled-inductor in series. After that, the cycle repeats.

III. Performance Analysis and Design Considerations

To simplify the circuit performance analysis, the leakage inductance L_k is neglected first, and the voltage on the switched capacitor and clamped capacitor is considered to be a constant voltage source over whole switching period.

A. Voltage Gain

When switch S is turned ON, the magnetizing inductance L_m is charged by the input voltage, as shown in Fig. 4(a). Voltage across magnetizing inductance is given by

$$V_{p\_\rm on} = V_{\rm in} \quad (8)$$

Reflected secondary voltage and switched-capacitor voltage are given as

$$V_{s\_\rm on} = V_{\rm Cf2} = NV_{p\_\rm on} = NV_{\rm in} \quad (9)$$

$$V_{\rm Cf1} = V_{s\_\rm on} + V_{\rm Cc} = NV_{\rm in} + V_{\rm Cc} \quad (10)$$

where $N = n_2/n_1$ is the turns ratio of the coupled inductor.

When switch S is turned OFF, the magnetizing inductance L_m is discharged, as shown in Fig. 4(d). In addition, switched capacitors C_{f1} and C_{f2} work as a dc source with constant voltage. The formulas are yielded as

$$V_{\rm Cc} = V_{\rm in} + V_{p\_\rm off} \quad (11)$$

$$V_{\rm in} + (N+1)V_{p\_\rm off} + V_{\rm Cf1} + V_{\rm Cf2} = V_o. \quad (12)$$

By applying the voltage-second balance principle to the magnetizing inductance L_m, the voltage gain of the proposed converter is given by

$$M_{\rm ideal} = \frac{V_o}{V_{\rm in}} = \frac{2N+2-ND}{1-D} \quad (13)$$

where D is the duty cycle of main switch.

Actually, the leakage inductance L_k cannot be zero in the practical prototype. Considering the effect of the leakage inductance, the output voltage gain M could be given as

$$M = \frac{V_o}{V_{\rm in}} = \frac{2N+2-ND}{1-D} \cdot \frac{1}{1+\frac{4N^2k_m}{D^2}+\frac{4N^2k_m}{D^2(1-D)}} \quad (14)$$

where $k_m = L_k f_s/R_o$, with f_s being the switching frequency and R_o represents the load resistor.

From formula (14), it is obvious that a high voltage gain could be obtained under a low duty cycle only if the turns ratio of the coupled inductor is set to be a reasonable value, which makes the proposed converter suitable for high step-up applications. The

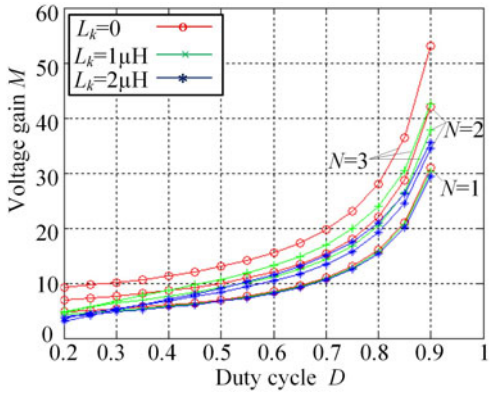

Fig. 5. Voltage gain versus duty cycle under various turns ratios and leakage inductances.

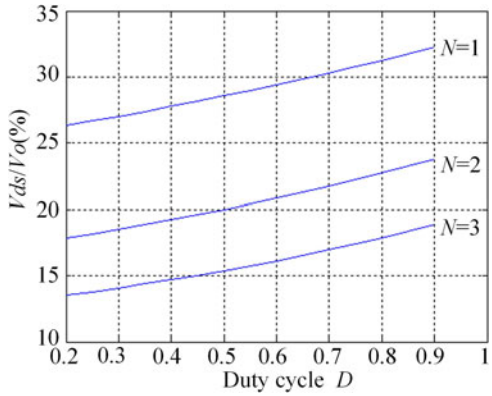

Fig. 6. Voltage stress of main switch versus duty cycle under various turns ratios.

relationship between voltage gain and duty cycle of different leakage inductances and turns ratios is shown in Fig. 5. As the duty cycle and turns ratio increase, the voltage gain rises significantly. Not to be ignored, the leakage inductance exerts some effect on the voltage gain of the proposed converter. As the leakage inductance increases, the voltage gain decreases.

B. Voltage and Current Stress Across Power Devices

As shown in Fig. 4, the voltage stress of main switch S and auxiliary switch $S_{\rm au}$ both equal to $V_{\rm cc}$. Hence, the voltage stress on both switches can be obtained as

$$V_{\rm ds\_}S = V_{\rm ds\_}S_{\rm au} = V_{\rm Cc} = \frac{1}{1-D}V_{\rm in} = \frac{1}{2N+2-ND}V_o. \tag{15}$$

It can be seen that, from formula (15), the voltage stress on main switch S and auxiliary switch $S_{\rm au}$ has been reduced to be much lower than output voltage. The relationship between voltage stress and duty cycle of different turns ratios is shown in Fig. 6. As the turns ratio increases, the voltage stress decreases significantly, meanwhile, the voltage stress increases slowly with duty cycle rising. Therefore, switches with low rated-voltage and low on-resistance can be utilized in high step-up and high output-voltage applications to reduce the conduction losses.

The voltage stress of output diodes can be derived as

$$V_{\rm Do} = \frac{N+1}{2N+2-ND}V_o. \tag{16}$$

From formula (16), it is worth mentioning that even though the voltage stress of the output diodes rises with the turns ratio, it is always less than the output voltage. The minimum voltage stress of the output diode halves the output voltage.

Analogously, the voltage stress of the feedforward diodes could be calculated as

$$V_{\rm Df1} = \frac{N+1}{2N+2-ND}V_o \tag{17}$$

$$V_{\rm Df2} = \frac{N}{2N+2-ND}V_o. \tag{18}$$

According to the ampere-second balance principle, the average current of output capacitor will be zero in whole switching period. Thus, the average current of output diode D_o equals to output current I_o.

Consequently, the peak value of the output diode current could be derived as

$$i_{D_o\,(\rm peak)} = \frac{2I_o}{1-D}. \tag{19}$$

Similarly, the peak value of feedforward diodes is given as

$$i_{D_{f1}\,(\rm peak)} = i_{D_{f2}\,(\rm peak)} = i_{S_{\rm au}\,(\rm peak)} = \frac{2I_o}{D}. \tag{20}$$

The peak value of main switch S can be expressed as

$$i_{S\,(\rm peak)} = MI_o + Ni_{D_{f2}\,(\rm peak)} + i_{D_{f1}\,(\rm peak)}. \tag{21}$$

By substituting (20) into (21), the peak value of main switch can be given out

$$i_{S\,(\rm peak)} = \left(M + \frac{2N+2}{D}\right)I_o. \tag{22}$$

C. Design of Coupled-Inductor and Capacitors

The coupled-inductor design should make sure the converter work in the continuous current mode. The peak current of magnetizing inductance at the boundary current mode (BCM) could be given by

$$i_{L_m\,(\rm peak)} = \frac{V_{\rm in}D}{L_m f_s}. \tag{23}$$

Correspondingly, at the BCM mode, the average current of magnetizing inductance is obtained as

$$i_{L_m\,(\rm ave)} = \frac{i_{L_m\,(\rm peak)}}{2} = \frac{(N+1)I_o}{(1-D)}. \tag{24}$$

Thus, considering formulas (13), (23), and (24), the boundary magnetizing inductance can be derived out

$$L_m = \frac{R_o D(1-D)^2}{2f_s(N+1)(2N+2-ND)}. \tag{25}$$

Finally, a toroidal sendust cores with 37 turns in the primary winding, and 37 turns in the second winding is utilized for the proposed converter in the prototype.

TABLE I
CONVERTER PERFORMANCE COMPARISON

	Converter in [27]	Converter in [32]	Proposed Converter
MOSFETs	2	2	2
Diode,	3	3	3
Voltage gain	$\frac{2N+2-(N+1)D}{1-D}$	$\frac{2N+1-ND}{1-D}$	$\frac{2N+2-ND}{1-D}$
Voltage stress on MOSFETs	$\frac{V_o}{2N+2-(N+1)D}$	$\frac{V_o}{2N+1-ND}$	$\frac{V_o}{2N+2-ND}$
Voltage stress on output diode	$\frac{(N+1)V_o}{2N+2-(N+1)D}$	$\frac{(N+1)V_o}{2N+1-ND}$	$\frac{(N+1)V_o}{2N+2-ND}$
Soft switching	Hard switching	ZVS	ZVS

Depending on switching frequency f_s and their voltage ripple, the value of capacitors C_{f1}, C_{f2}, and C_o is designed. The corresponding equations are given by

$$C_{f1} \geq \frac{I_o(1-D)}{f_s \Delta V_{\mathrm{Cf1}}} \tag{26}$$

$$C_{f2} \geq \frac{I_o(1-D)}{f_s \Delta V_{\mathrm{Cf2}}} \tag{27}$$

$$C_o \geq \frac{I_o D}{f_s \Delta V_o} \tag{28}$$

where ΔV_{Cf1}, ΔV_{Cf2}, and ΔV_{Co} are the voltage ripple of capacitors C_{f1}, C_{f2}, and C_o, respectively. Generally speaking, a large capacitor could reduce the voltage ripple; however, bulky size and expensive cost may be inevitable. Hence, the tradeoff should be considered when selecting a capacitor.

In order to achieve ZVS for main switch *S*, the turn-off interval of the main switch S should be shorter than the half of resonant period, which is determined by leakage inductance and clamped capacitor. The corresponding equation could be yielded as

$$C_c \geq \frac{(1-D_{\min})^2}{\pi^2 L_k {f_s}^2} \tag{29}$$

where $D_{\min}$ is the minimum value of duty cycle.

D. Performance Comparison

The performance comparison among the converters is presented in [27] and [32], and the proposed converter is summarized in Table I. The voltage gain comparison of these converters at turns ratio $N = 1$ is given in Fig. 7. It can be concluded that the proposed converter could achieve higher voltage gain than converters presented in [27] and [32], given the same duty cycle and turns ratio. Meanwhile, as turns ratio increases, the gain advantage will become more obvious. Voltage stress on MOSFETs comparison of these converters at duty cycle D of 0.5 is given in Fig. 8. It is evident that the switches in the proposed converter suffer from lower voltage stress than the converters presented in [27] and [32], which makes low-voltage MOSFETs with low $R_{\mathrm{DS\_ON}}$ available in high step-up applications. Also, the voltage stress on the output diode of the proposed converter is lower than other converters, as shown in Fig. 9. Compared with the converter in [27], the proposed converter can achieve ZVS operation, which brings about reduced switching loss and improved efficiency.

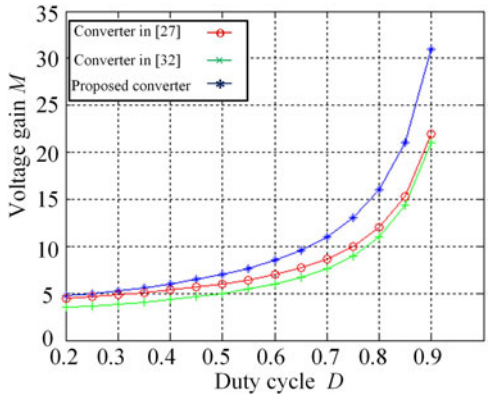

Fig. 7. Comparison of voltage gain versus duty cycle when $N = 1$.

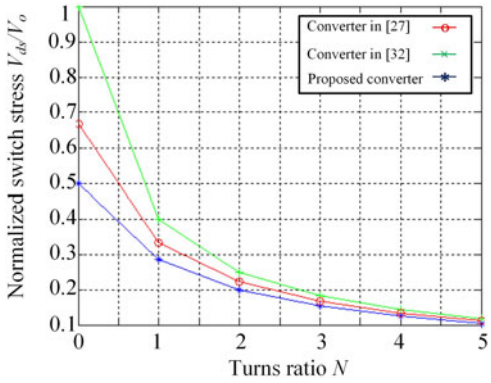

Fig. 8. Comparison of voltage stress on MOSFETs versus turns ratio when $D = 0.5$.

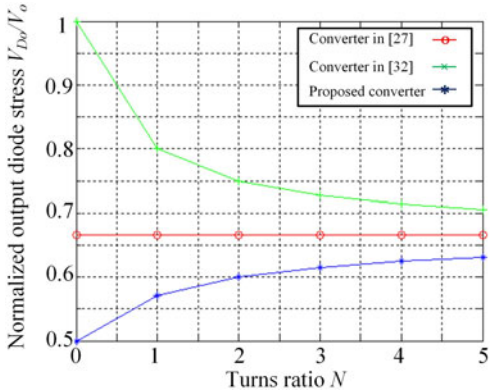

Fig. 9. Comparison of voltage stress on output diodes versus turns ratio when $D = 0.5$.

IV. ZVS OPERATION ANALYSIS

When the switch *S* is turned OFF under ZVS condition due to the parasitic capacitor, the energy stored in leakage inductance will be transferred to the clamped capacitor through the antiparallel body diode of auxiliary switch S_{au}, which creates ZVS turn-on condition for auxiliary switch S_{au}. Voltage across

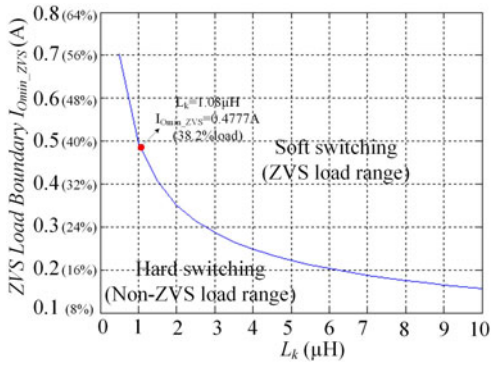

Fig. 10. ZVS load boundary according to leakage inductance.

parasitic capacitor of main switch S equals to voltage across clamped capacitor when $S_{\rm au}$ is turned ON. Therefore, $S_{\rm au}$ can be turned OFF under ZVS condition. At this instant, when $S_{\rm au}$ has been turned OFF, a new resonant loop composed of input power source, leakage inductance, and parasitic capacitor C_r will form. Then, when the parasitic capacitor is discharged by leakage inductance completely, the ZVS turn-on condition will be produced for main switch S because it's antiparallel body diode has conducted.

Based on the above-mentioned analysis, in order to realize soft switching, there are some constraint conditions to be considered. First, the auxiliary switch $S_{\rm au}$ needs to be turned ON after its antiparallel body diode conducts, as shown in Fig. 4 (c). Second, $S_{\rm au}$ should be turned OFF timely to make sure that the interval of modes 6 and 7 is shorter than the half of resonant period, which is determined by leakage inductance and parasitic capacitor, as shown in Fig. 4(f) and Fig. 14(g), respectively. The responding equations are given by

$$t_l = t_7 - t_5 \le \frac{\pi}{\omega_3} \tag{30}$$

where t_l is interval time between falling edge of gate signal for $S_{\rm au}$ and rising edge of gate signal for S.

Finally, the parasitic capacitor should be discharged completely by leakage inductance to guarantee conduction for antiparallel body diode of main switch S, as shown in (7). The current of leakage inductance at t_5 can be obtain as

$$i_{\rm Lk}(t_5) = \left(M - \frac{2N}{1-D}\right) I_o. \tag{31}$$

Thus, the ZVS boundary current of load $I_{O\min\_ZVS}$ can be derived from formulas (7), (15), and (31), it is expressed as

$$I_{o\min\_ZVS} = \sqrt{\frac{C_r}{L_k}} \frac{1-D}{(2-ND)(2N+2-ND)} V_o. \tag{32}$$

From (32), it is obvious that the ZVS turn-on condition for main switch S in the proposed converter is dependent on L_k rather than load. The boundary cure between ZVS and non-ZVS range against L_k is shown in Fig. 10. Considering the parameters used in the experiment, the ZVS load boundary $I_{O\min\_ZVS}$ is 0.4777 A, as the red point shown in the curve. It means that the ZVS turn-on condition can be guaranteed from a 38.2% load to a full load. On the other hand, the ZVS will be lost below a 38.2% load condition. Thus, it seems that a large leakage inductance is preferable to a wide ZVS range. However, large leakage inductance will make voltage gain decay, as shown in Fig. 5, so that the duty ratio D should be increased for compensation, unfortunately, which will cause the increase in the peak and rms values of the primary leakage current. Therefore, L_k should be designed reasonably.

TABLE II
PARAMETERS AND SPECIFICATIONS OF THE PROTOTYPE

Components	Specifications
Input voltage	40 V
Output voltage	400 V
Power	500 W
MOSFETs	IRFP250N
Diodes	RHR1560
Switching frequency	50 kHz
Duty cycle of S	70%
Duty cycle of $S_{\rm au}$	22%
t,	600 ns
Turns ratio	37/37
Leakage inductance	1.08 μpH
Magnetizing inductance	220 μH
Switched capacitor	4.7 μF/ 250 V
Clamped capacitor	1.5 μF/ 250 V
Output capacitor	470 μF/450 V

V. EXPERIMENTAL RESULTS

To validate the performance of the proposed converter, a simulation with the same specifications as prototype has done based on SABER software before a 500-W prototype is implemented in the laboratory. Specifications of the prototype are listed in Table II. From the simulation results, as shown in Fig. 11, the waveforms are basically in line with the above-mentioned analysis. The prototype bock diagram is shown in Fig. 12. Notice that the converter is operated in an open loop and the driving signal is generated based on DSP TMS320F28335.

The experimental waveforms of the main switch S and auxiliary switch $S_{\rm au}$ are shown in Fig. 13. It can be seen from Fig. 13(a) that the drain–source voltage across main switch $V_{\rm ds}$ has fell down to zero before it is turned ON, and its ZVS operation is realized completely. Also, $V_{\rm ds}$ will rise gradually for ZVS operation when it is turned OFF. Due to the clamped capacitor, there is only a small voltage spike, and voltage stress across main switch approaches about 120 V, far less than the output voltage of 400 V. From Fig. 13(b), it can be observed that auxiliary switch $S_{\rm au}$ becomes on-state after its antiparallel body diode is forward biased. Meanwhile, the rising rate of drain–source voltage across auxiliary switch $S_{\rm au}$ is relative small when $S_{\rm au}$ is turned OFF. Thus, auxiliary switch $S_{\rm au}$ has achieved ZVS operation at turn-on or turn-off operation.

The current through leakage inductance is shown in Fig. 14(a), which is basically identical with theoretical analysis. The current through diodes D_{f1} and D_{f2} is shown in Fig. 14(b). The current falling rate of diodes D_{f1} and D_{f2} is controlled effectively. Thus, the reverse-recovery problem of

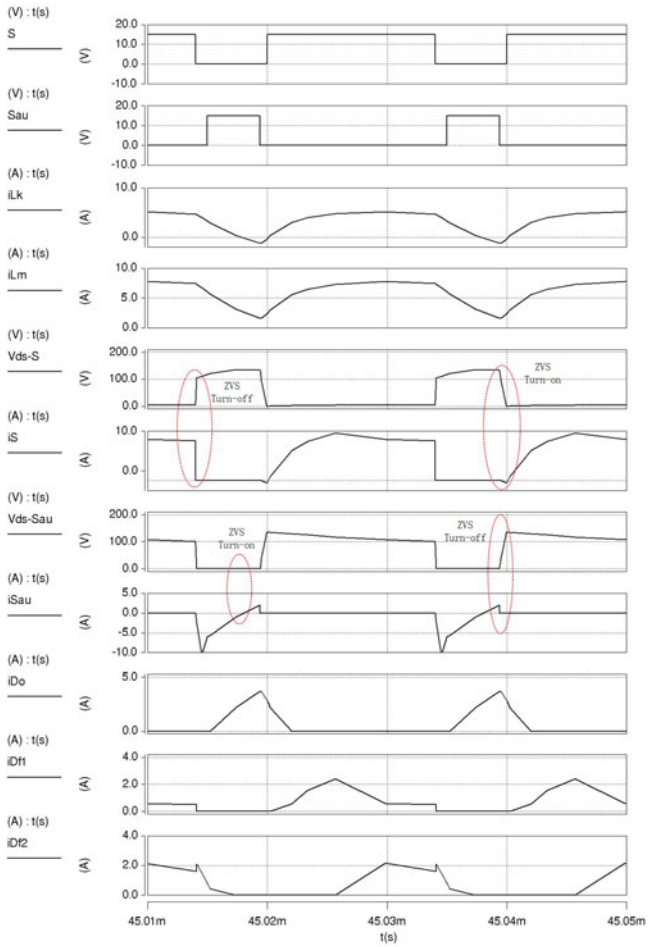

Fig. 11. Simulation results.

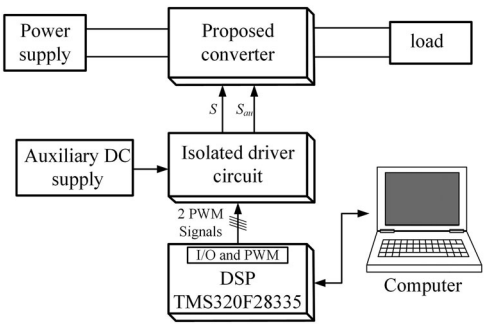

Fig. 12. Prototype block diagram.

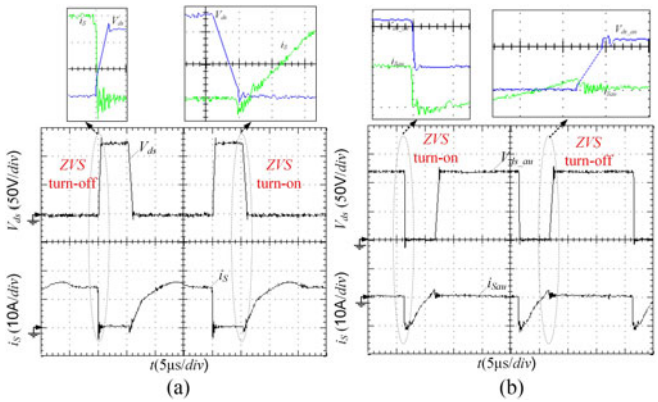

Fig. 13. ZVS operation waveforms. (a) Drain–source voltage across main switch $(V_{\rm ds})$ and main switch current (i_s). (b) Drain–source voltage across auxiliary switch $(V_{\rm ds})$ and auxiliary switch current (i_s).

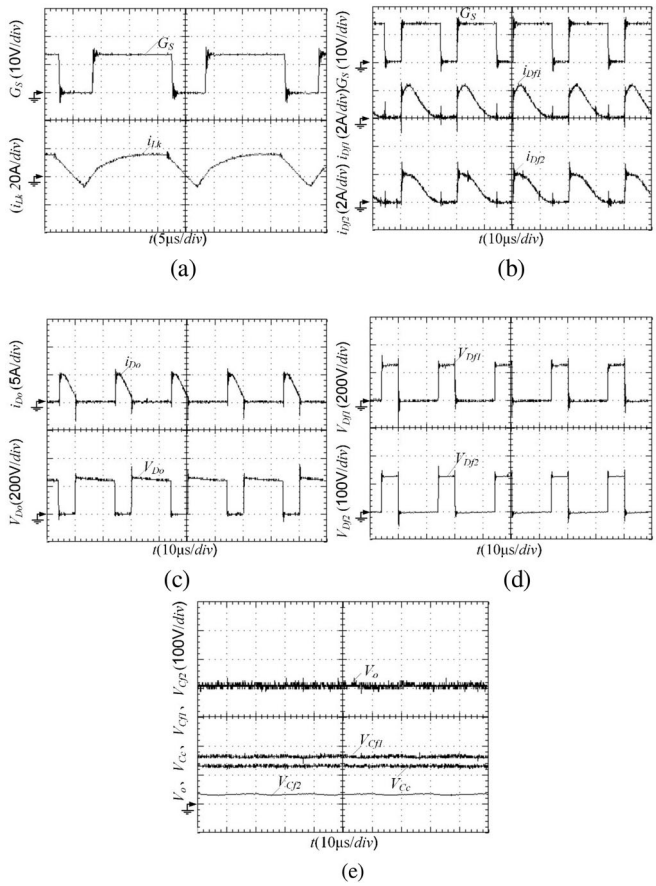

Fig. 14. Typical waveforms. (a) $i_{\rm Lk}$ and G_S. (b) $i_{\rm Df1}, i_{\rm Df2}$, and G_S. (c) $G_S, i_{\rm Df1}$, and $i_{\rm Df2}$. (d) $V_{\rm Df1}$ and $V_{\rm Df2}$. (e) $V_o, V_{\rm Cc}, V_{\rm Cf1}$, and $V_{\rm Cf2}$.

diodes D_{f1} and D_{f2} is alleviated. The current through output diode and its voltage stress is shown in Fig. 14(c). Similarly, the current falling rate of the output diode is controlled effectively to approximately 1.25 A/μs. The reverse-recovery problem of the output diode is also alleviated distinctly. From Fig. 14(c) and (d), it is seen that voltage stress of diodes D_{f1}, D_{f2}, and D_o is reduced, which is far smaller than the output voltage. It is worth noting that due to oscillation caused by their parasitic capacitance, there are some small voltage ripples across diodes. The waveforms of voltage across capacitors and output voltage are shown in Fig. 14(e). When output voltage has value of 400 V, voltage of clamped capacitor $V_{\rm Cc}$, switched capacitors V_{f1} and V_{f2} are about 120, 160, and 40 V, respectively, which is consistent with theoretical analysis as well. The gain of 10 in experimental results has a little smaller than the theoretical voltage gain of 10.2 according to formula (14), because there is voltage drop in switch device, inductor, and line resistor out of theoretical calculation.

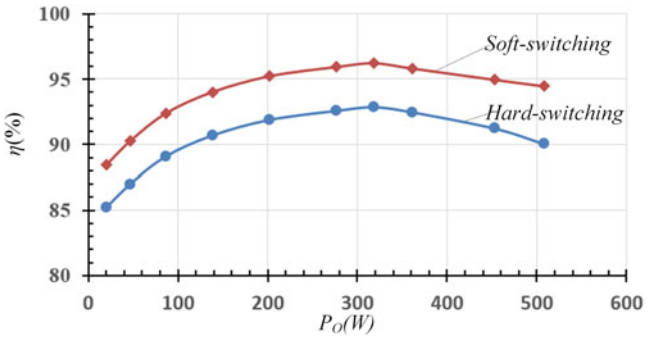

Fig. 15. Efficiency of the proposed converter against output power.

The conversion efficiency against output power between the proposed converter and its own hard-switching counterpart is shown in Fig. 15, the maximum efficiency of the proposed converter reaches up to 96.2% and the full-load efficiency is approximately 94.4%. An average improvement of approximately 3% in the conversion efficiency is provided by the proposed converter compared with its own hard-switching counterpart. Importantly, the converter could work under high efficiency in wide load range.

V. Conclusion

The paper has developed a compact high step-up dc–dc converter with relative small components and a simply control strategy to achieve extreme gain with soft operation and active clamping. The feature of the proposed converter can be summed up as follows.

1) Wide input operation range and high voltage gain without an extreme duty cycle can be achieved.
2) Voltage stress on power devices are reduced greatly and low on-resistance MOSFET can be employed for conduction loss reducing.
3) The reverse recovery problem of the output diode is alleviated due to leakage inductance.
4) Voltage spike on the main switch is effectively clamped by the active clamp circuit.
5) Active clamped-circuit takes the role of resonance as well, achieving soft-switching for main switch and auxiliary switch in wide load range, and reaching high efficiency in wide load range.
6) Active clamped-circuit participates in gain enhancement.

Therefore, the proposed converter can obtain high gain with high efficiency, which can be effectively used in renewable energy systems as the front-end converters.

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