Fully Soft-Switched Dual-Active-Bridge Series-Resonant Converter With Switched-Impedance-Based Power Control

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***Abstract*—Both conduction loss and switching loss can contribute significantly to the overall power loss of an isolated bidirectional dual-active-bridge series-resonant dc–dc converter (DABSRC) operating at high frequency. To achieve soft switching and minimum-tank-current operation under wide-range variations in output voltage and current, a switched-impedance-based DABSRC is proposed. Minimum-tank-current operation aims to reduce conduction loss arising from circulating current at the low voltage, high-current side of DABSRC. Full-range soft switching is achieved in all switches, thus, switching loss is significantly reduced. With this new topology, power control is achieved by controlling a switch-controlled capacitor in the series resonant tank while ensuring minimum-tank-current operation and soft switching in all switches. The proposed topology and modulation scheme are validated by means of a 1-kW experimental prototype of DABSRC operating at 100 kHz designed to interface a 250-V dc bus to a supercapacitor with a rated output voltage of 48 V. The effectiveness of the proposed topology for charging/discharging a supercapacitor at a maximum rated power of 1 kW is verified by simulations and experimental results with a maximum efficiency of 97.5%.**

***Index Terms*—Dual-active-bridge (DAB) converter, minimum-tank-current operation, soft switching, supercapacitor, switch-controlled capacitor (SSC).**

I. Introduction

With an increased penetration of renewable energy generation into power grid, rise in conventional fuel prices and new legislations requiring low carbon emissions, the automotive companies were led to focus on power-efficient fuel cell vehicles (FCVs), electric vehicles (EVs), and hybrid EVs [1]. Efficiency enhancement is one of the main challenges toward the development of these vehicles. A typical power system architecture of FCVs or EVs is shown in Fig. 1. In the first half of the past century, 6-V dc bus which later increased to 12 V served the purpose of powering all the electric load demands in automobile systems . But nowadays, with a shift toward the production of more EVs, this bus voltage level is forecasted to stand between 240 to 450 V [2], [3]. With this rise in voltage level, it becomes essential to use high-power dc–ac inverters for supplying power to traction motors and bidirectional dc–dc converters to charge/discharge auxiliary energy storages attached to the main dc bus [4]. These auxiliary energy storages, which include low-voltage supercapacitors, help to improve the dynamic response and performance of vehicles by providing startup power and absorbing regenerative brake energy [5]. Bidirectional dc–dc power converters can be used to integrate these auxiliary storage devices to the main dc bus, and in this context dual-active-bridge (DAB) converter has shown many advantages over its counterpart topologies in terms of device stress, ease of control, galvanic isolation, and power density [6].

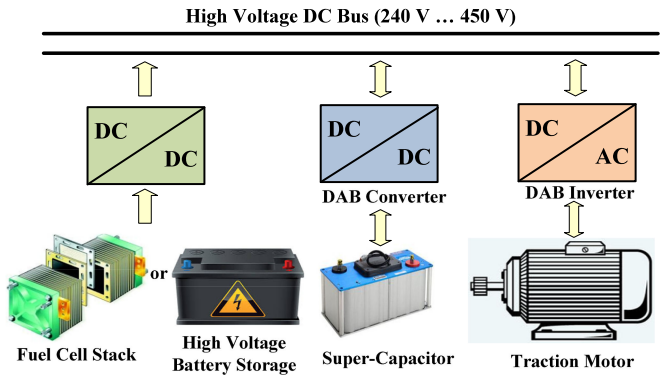

Fig. 1. Typical power system architecture of EVs.

Recently, due to the advancements in power electronic devices, DAB converter is gaining more attention for its use in bidirectional power flow in medium-voltage power architectures [7]–[10]. A conventional LC-type DAB series-resonant converter (DABSRC) is designed and analyzed in [11]. However, under wide-range variations in output voltage and current, this topology undergoes switching and conduction losses in certain operating regions that deteriorate converter's performance in terms of efficiency and semiconductor device's stress. Circulating current and hard switching in conventional DAB converter are mainly due to the out-of-phase relationship between the tank current and bridge voltages [12], [13]. These two phenomena can cause excessive conduction loss and switching loss in high-frequency operation. Several modulation schemes

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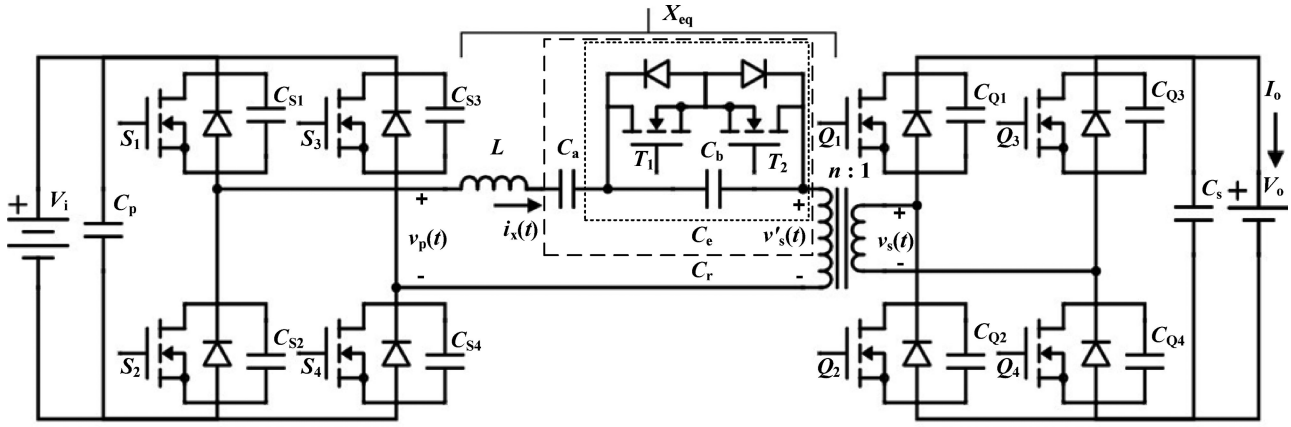


Fig. 2. Proposed DABSRC topology incorporating SCC.

and topologies of DAB converter have been proposed to reduce conduction loss (due to circulating current) and switching loss (due to hard switching) but they cover only certain operating regions. Single-phase-shift (SPS) modulation uses one degree of freedom to modulate power but it fails to provide wide-range soft switching particularly under light-load condition and nonunity voltage gain [11]. To reduce circulating current and achieve soft switching, extended-phase-shift (EPS) [14], [15], dual-phase-shift (DPS) [16]–[20], and triple-phase-shift [21]–[23] modulation methods were proposed, which adds one or two extra degrees of freedom in power modulation by introducing internal phase shift within the primary and secondary bridges in addition to the traditional external phase shift between the primary and secondary bridges. However, in these complex modulation schemes, soft switching can be achieved for certain operating regions only. Modulation schemes based on fundamental component analysis (FCA) were proposed in [24], [25] to reduce circulating current as well as computational complexities involving online and offline calculations. These modulation schemes also fail to achieve soft switching in all switches under wide-range variations in output current and voltage. Several topologies with tuned LCL, CLC, $CLLC$ were proposed in [26]–[29]. EPS and DPS are used to control power for DAB topologies based on LCL and CLC, but under wide-range variation in power, these topologies also encounter hard switching. $CLLC$-based topology utilizes a complex modulation scheme to achieve soft switching at the primary bridge only, while the output rectifier operates with soft commutation. The application of switched-impedance-based resonant topologies were investigated in [30]–[32], but only unidirectional power transfer is achieved by these topologies.

In this paper, a switched-impedance-based DABSRC incorporating switch-controlled capacitor (SCC) is proposed to achieve both soft switching and minimum circulating current over wide-range variations in output voltage and current. The proposed topology and modulation scheme enables the realization of zero-voltage switching (ZVS) at the primary high voltage and secondary low voltage bridges. In both buck and boost operations, minimum-tank-current operation ensures an in-phase relationship between tank current and bridge voltage on either side of the high-frequency transformer of DABSRC to avoid excessive ringing and current stress due to circulating current [13], [33]. In Section II, the conditions required for achieving soft switching, minimum-tank-current operation, and the required dead-time intervals are identified for DABSRC, and to meet these conditions a modified DABSRC based on switched impedance is proposed and its operating principles are explained. The design of experimental prototype, simulation, and experimental results for charging/discharging a supercapacitor module are presented in Section III. Finally, concluding remarks are given in Section IV.

II. Proposed Topology Based on Switched Impedance

Fig. 2 shows the schematic diagram of the proposed DABSRC based on switched impedance with input dc-bus voltage $V_{\rm i}$, input filter capacitor $C_{\rm p}$, primary-side switches S_1–S_4, secondary-side switches Q_1–Q_4, output filter capacitor $C_{\rm s}$, and output voltage $V_{\rm o}$. It can be seen that the switches S_1–S_4 form the primary-side full bridge are modulated to generate $v_{\rm p}(t)$ (with a dc value of $V_{\rm p} = V_{\rm i}$). The secondary-side full bridge of the converter consists of Q_1–Q_4, which are modulated to generate a phase-shifted voltage $v_{\rm s}(t)$ (with a dc value of $V_{\rm s} = V_{\rm o}$) or primary-reflected $v'_{\rm s}(t)$, where the phase shift θ between $v_{\rm p}(t)$ and $v'_{\rm s}(t)$ determines the direction and magnitude of power flow. Since power is mainly transferred by the fundamental components of the resonant tank current and bridge voltages, FCA is adopted, which leads to simplified analytical expressions of the key equations [24], [34], [35]. Under the assumption of FCA, the equivalent circuit of DABSRC converter and the phasor diagrams showing the soft switching and hard switching conditions of the primary-side and secondary-side switches are shown in Fig. 3.

In the following analysis, normalized variables (i.e., per-unit values) are used so that generalized results are obtained and applicable to all power levels. To perform FCA in normalized form, the following base values are selected: $V_{\rm B} = V_{\rm p}$, $Z_{\rm B} = \frac{n^2 V_{\rm o}^2}{P_{\rm o,max}}$, and $I_{\rm B} = V_{\rm B}/Z_{\rm B}$. The normalized bridge voltages and primary-reflected resonant tank current are given as

$$v_{\rm p,p.u}(t) = \frac{4}{\pi}\sin\omega t \tag{1}$$

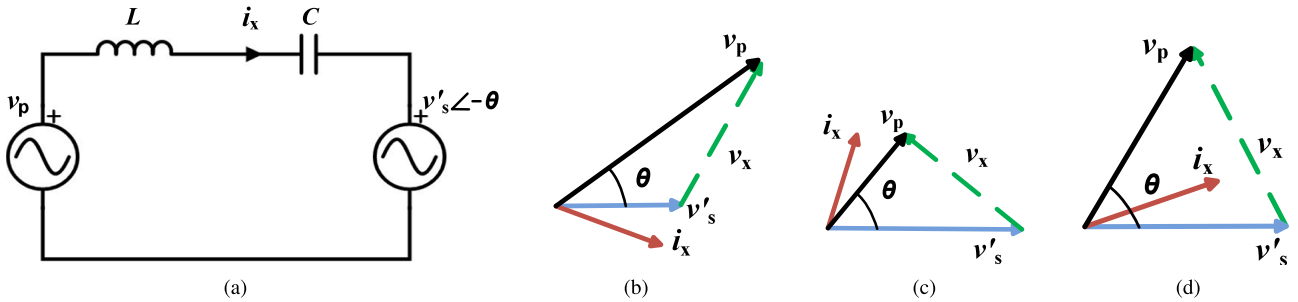


Fig. 3. (a) Equivalent circuit of DABSRC. (b) Phasor representation depicting hard switching of secondary-side switches. (c) Phasor representation depicting hard switching of primary-side switches. (d) Phasor representation depicting ZVS operation of all switches of DABSRC.

$$v'_{\mathrm{s,p.u}}(t) = \frac{4M}{\pi}\sin(\omega t - \theta) \tag{2}$$

$$i_{\mathrm{x,p.u}}(t) = \frac{4}{\pi X_{\mathrm{eq,p.u}}}(-\cos\omega t + M\cos(\omega t - \theta)) \tag{3}$$

where $M = \frac{nV_{\mathrm{s}}}{V_{\mathrm{p}}}$, θ is the phase shift between $v_{\mathrm{p}}(t)$ and $v'_{\mathrm{s}}(t)$, n is the transformer's turn-ratio, and $X_{\mathrm{eq,p.u}} = (\omega L - \frac{1}{\omega C_{\mathrm{r}}})/Z_{\mathrm{B}}$ is the normalized resonant tank impedance.

From (3), the root-mean-square (rms) value of the resonant tank current $i_{\mathrm{x,p.u}}(t)$ is given as

$$I_{\mathrm{x,rms,p.u}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}[i_{\mathrm{x,p.u}}(t)]^2 d\omega t} = \frac{2\sqrt{2}}{\pi X_{\mathrm{eq,p.u}}}\sqrt{1 + M^2 - 2M\cos\theta}. \tag{4}$$

The average power transferred between the primary side and secondary side of the DABSRC can be evaluated using either the primary-side voltage $v_{\mathrm{p}}(t)$ or the secondary-side voltage $v'_{\mathrm{s}}(t)$ in conjunction with the tank current $i_{\mathrm{x,p.u}}(t)$, both approaches lead to the same expression. It can be seen from (5) that the maximum power is transferred when the phase shift θ between $v_{\mathrm{p}}(t)$ and $v'_{\mathrm{s}}(t)$ is 90°

$$P_{\mathrm{o,p.u}} = \frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{p,p.u}}(t) i_{\mathrm{x,p.u}}(t) dt = \frac{8M}{\pi^2 X_{\mathrm{eq,p.u}}}\sin\theta. \tag{5}$$

A. Required Soft-Switching Conditions

It can be seen from Fig. 2 that in order to achieve ZVS operation in the primary-side switches, $i_{\mathrm{x}}(t)$ should be negative at the turn-on instances of S_1 and S_4 (i.e., turn-off instances of S_2 and S_3). A negative $i_{\mathrm{x}}(t)$ is required to discharge the parasitic capacitances C_{S1} and C_{S4} (and to charge C_{S2} and C_{S3}) so that their body diodes will conduct before the turn-on gate signals are applied to S_1 and S_4. As for the secondary side, $i_{\mathrm{x}}(t)$ is required to be positive to achieve ZVS turn-on of Q_1 and Q_4. Similarly, it can be deduced that $i_{\mathrm{x}}(t)$ should be positive for ZVS turn-on of S_2 and S_3 and negative for Q_2 and Q_3.

Thus, by evaluating (3) at $\omega t = 0$ (i.e., when S_1 and S_4 are turned ON) and θ (i.e., when Q_1 and Q_4 are turned ON), the required conditions for achieving ZVS in the primary-side and secondary-side switches can be derived as given by (6) and (7), respectively

$$i_{\mathrm{x,p.u}}(0) = \frac{4}{\pi X_{\mathrm{eq,p.u}}}(-1 + M\cos\theta) < 0 \Rightarrow \theta \le \cos^{-1}\frac{1}{M} \tag{6}$$

$$i_{\mathrm{x,p.u}}\left(\frac{\theta}{\omega}\right) = \frac{4}{\pi X_{\mathrm{eq,p.u}}}(-\cos\theta + M) \ge 0 \Rightarrow \theta \ge \cos^{-1} M. \tag{7}$$

The phasor representation and operating waveforms corresponding to different cases of hard switching and soft switching of DABSRC are shown in Figs. 3 and 4. Plotting (6) and (7) with respect to θ at various values of M leads to the soft-switching boundaries of DABSRC depicted in Fig. 5. Fig. 5(a) shows that, for primary-side switches, the required condition can be met for all $M \le 1$ by ensuring $\frac{nV_{\mathrm{s(max)}}}{V_{\mathrm{p}}} \le 1$, but for $M > 1$ primary-side switches will experience hard switching in region B. For secondary-side switches, Fig. 5(b) shows that they will experience hard switching in region B when $M < 1$. In summary, DABSRC cannot achieve full-range soft switching under variations in primary-to-secondary voltage ratio and load (i.e., phase shift angle) due to the contradictory requirements of (6) and (7), i.e., (6) and (7) cannot be satisfied simultaneously. This limitation will be addressed by a new method proposed in Section II-D.

B. Minimum-Tank-Current Operation

The per-unit output current $I_{\mathrm{o,p.u}}$ can be obtained from (5) by dividing the per-unit average output power by the per-unit output voltage and result is given as

$$I_{\mathrm{o,p.u}} = \frac{8}{\pi^2 X_{\mathrm{eq,p.u}}}\sin\theta. \tag{8}$$

The per-unit rms tank current $I_{\mathrm{x,rms,p.u}}$ is further normalized with respect to $I_{\mathrm{o,p.u}}$ to obtain a load independent, and hence a generalized, expression for tank current by eliminating $X_{\mathrm{eq,p.u}}$ from (8) and (4). Equation (9) shows that the normalized tank current is a function of M and θ only

$$\frac{I_{\mathrm{x,rms,p.u}}}{I_{\mathrm{o,p.u}}} = \frac{\pi\sqrt{2}}{4\sin\theta}\sqrt{1 + M^2 - 2M\cos\theta}. \tag{9}$$

In order to achieve minimum-tank-current operation, the minimum value of $\frac{I_{\mathrm{x,rms,p.u}}}{I_{\mathrm{o,p.u}}}$ is found by setting its first derivative with respect to θ to zero. Equation (10) gives the required

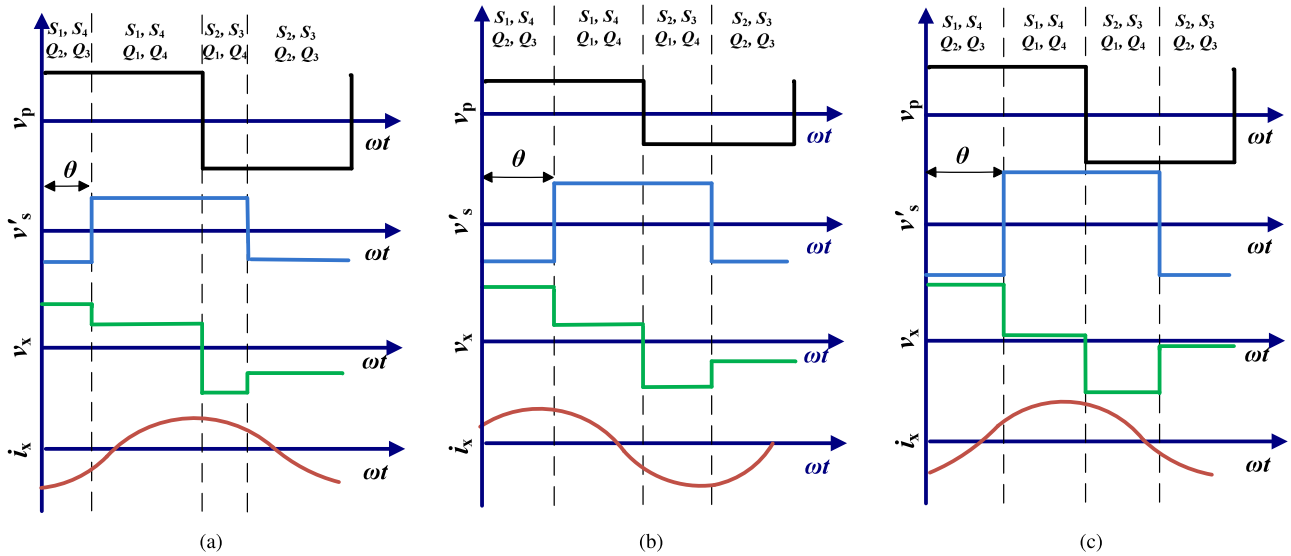


Fig. 4. Operating waveforms of the DABSRC (a) Hard switching of secondary-side switches. (b) Hard switching of primary-side switches of the DABSRC. (c) ZVS operation of all switches of DABSRC.

conditions for minimum tank current for the cases of $M \leq 1$ and $M > 1$. By substituting (10) into (6) and (7) for the case of $M \leq 1$ and $M > 1$, respectively, it can be verified that $i_{\mathrm{x,p.u}}(0) = 0$ and $i_{\mathrm{x,p.u}}(\frac{\theta}{\omega}) = 0$ for $M \leq 1$ and $M > 1$, indicating that under these conditions, the tank current $i_{\mathrm{x}}(t)$ becomes in phase with the primary-bridge voltage $v_{\mathrm{p,p.u}}(t)$ when $M > 1$ and in phase with the secondary-bridge voltage $v'_{\mathrm{s,p.u}}(t)$ when $M \leq 1$

$$\frac{\mathrm{d}}{\mathrm{d}\theta}(I_{\mathrm{x,rms,p.u}}) = 0 \Rightarrow \theta = \begin{cases} \cos^{-1}(M) & M \leq 1 \\ \cos^{-1}\left(\frac{1}{M}\right) & M > 1 \end{cases}. \tag{10}$$

Hence, (5) and (8) can be rewritten as

$$P_{\mathrm{o,p.u}} = \begin{cases} \frac{8M}{\pi^2 X_{\mathrm{eq,p.u}}} \sin\left(\cos^{-1}(M)\right) & M \leq 1 \\ \frac{8M}{\pi^2 X_{\mathrm{eq,p.u}}} \sin\left(\cos^{-1}\left(\frac{1}{M}\right)\right) & M > 1 \end{cases} \tag{11}$$

$$I_{\mathrm{o,p.u}} = \begin{cases} \frac{8}{\pi^2 X_{\mathrm{eq,p.u}}} \sin\left(\cos^{-1}(M)\right) & M \leq 1 \\ \frac{8}{\pi^2 X_{\mathrm{eq,p.u}}} \sin\left(\cos^{-1}\left(\frac{1}{M}\right)\right) & M > 1 \end{cases}. \tag{12}$$

By imposing the desired conditions (10), it can be seen from (11) and (12) that the output power $P_{\mathrm{o,p.u}}$ and output current $I_{\mathrm{o,p.u}}$ can only be adjusted by varying M for a given resonant tank design. In other words, the dependence of $P_{\mathrm{o,p.u}}$ on M has limited the flexibility of power control in DABSRC operating with minimum tank current, as M cannot be varied arbitrarily. Therefore, a modified DABSRC topology based on switched impedance is proposed to overcome this limitation.

C. Minimum Dead Time to Achieve Soft Switching and Minimum-Tank-Current Operation

To avoid incomplete soft-switching transitions in all switches, it is necessary to charge/discharge the parasitic capacitances within the dead-time interval of two complimentary switches as shown in Fig. 6. The minimum required tank current to charge/discharge these capacitances is given as

$$\int_{t_{\mathrm{off}}}^{t_{\mathrm{on}}} i_{\mathrm{x,min}}(t)dt \geq Q_{\mathrm{C,max}}(V_{\mathrm{max}}) \tag{13}$$

where $i_{\mathrm{x,min}}(t)$ is the tank current within the dead-time interval and $Q_{\mathrm{C,max}}(V_{\mathrm{max}}) = 2V_{\mathrm{max}}C(V_{\mathrm{max}})$ is the maximum accumulated charge within the parasitic capacitances of the two complimentary switches on both sides of DABSRC. A large dead-time interval is required to satisfy (13) at low-power transfer and maximum bridge voltages $V_{\mathrm{p,max}}$ and $V_{\mathrm{s,max}}$ as the tank current $i_{\mathrm{x}}(t)$ is small and the accumulated charge $Q_{\mathrm{C,max}}(V_{\mathrm{max}})$ is high. Hence, for full-range soft switching, the tank impedance $X_{\mathrm{p.u}}$ should be chosen to satisfy (13), i.e., to provide the required $i_{\mathrm{x,min}}(t)$ at the specified minimum power transfer $P_{\mathrm{o,p.u,min}}$.

It can be seen from Fig. 6(b) that for $M > 1$, the minimum dead-time interval for achieving complete soft-switching transitions in the primary-side switches is defined at the minimum power level $P_{\mathrm{o,p.u,min}}$, and the maximum primary-bridge voltage $V_{\mathrm{p,max}}$, i.e., at the instance of minimum tank current $i_{\mathrm{x,min}}(t)$ and maximum accumulated charge $Q_{\mathrm{CS,max}}(V_{\mathrm{p,max}})$ within the parasitic capacitances. Hence, the required dead-time interval can be found as

$$\int_{0}^{\frac{\theta_{\mathrm{dp}}}{\omega}} i_{\mathrm{x,min}}(t)dt = Q_{\mathrm{CS,max}}(V_{\mathrm{p,max}}) \tag{14}$$

where $\frac{\theta_{\mathrm{dp}}}{\omega}$ is the required dead-time interval for the primary-side switches. Similarly, from Fig. 6(a) for $M \leq 1$, the required dead-time for the secondary-side switches is given by (15) at the minimum power level $P_{\mathrm{o,p.u,min}}$ and maximum maximum secondary-bridge voltage $V_{\mathrm{s,max}}$

$$\int_{\frac{\theta}{\omega}}^{\frac{\theta}{\omega}+\frac{\theta_{\mathrm{ds}}}{\omega}} n i_{\mathrm{x,min}}(t)dt = Q_{\mathrm{CQ,max}}(V_{\mathrm{s,max}}) \tag{15}$$

where $\frac{\theta_{\mathrm{ds}}}{\omega}$ is the required minimum dead-time interval for the secondary-side switches.

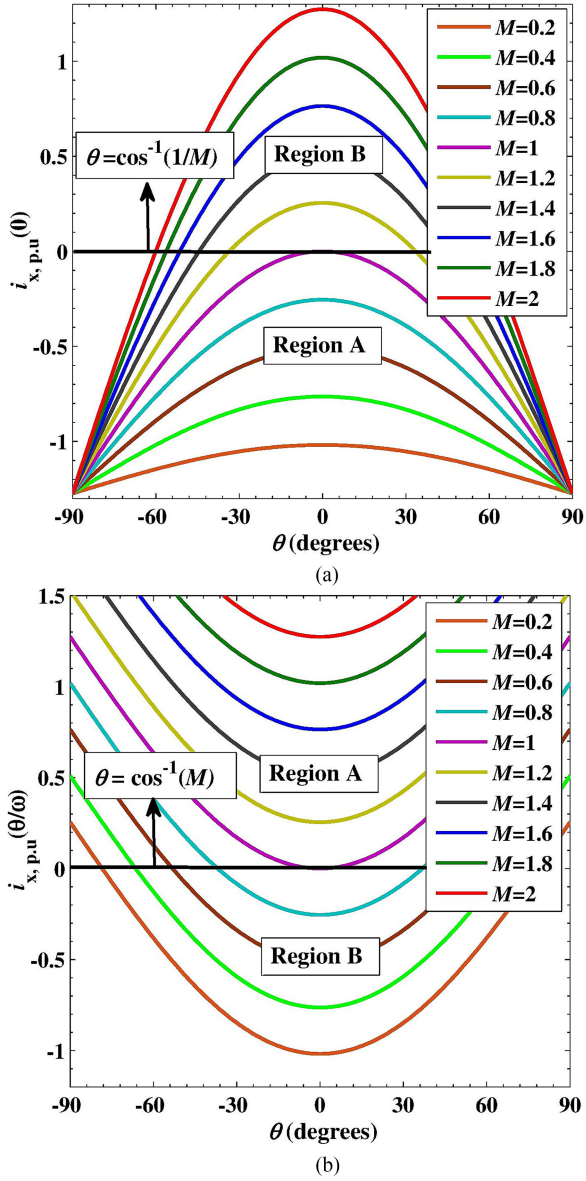


Fig. 5. Soft-switching regions of primary- and secondary-side switches under variations in M and θ. (a) Primary side. (b) Secondary side.

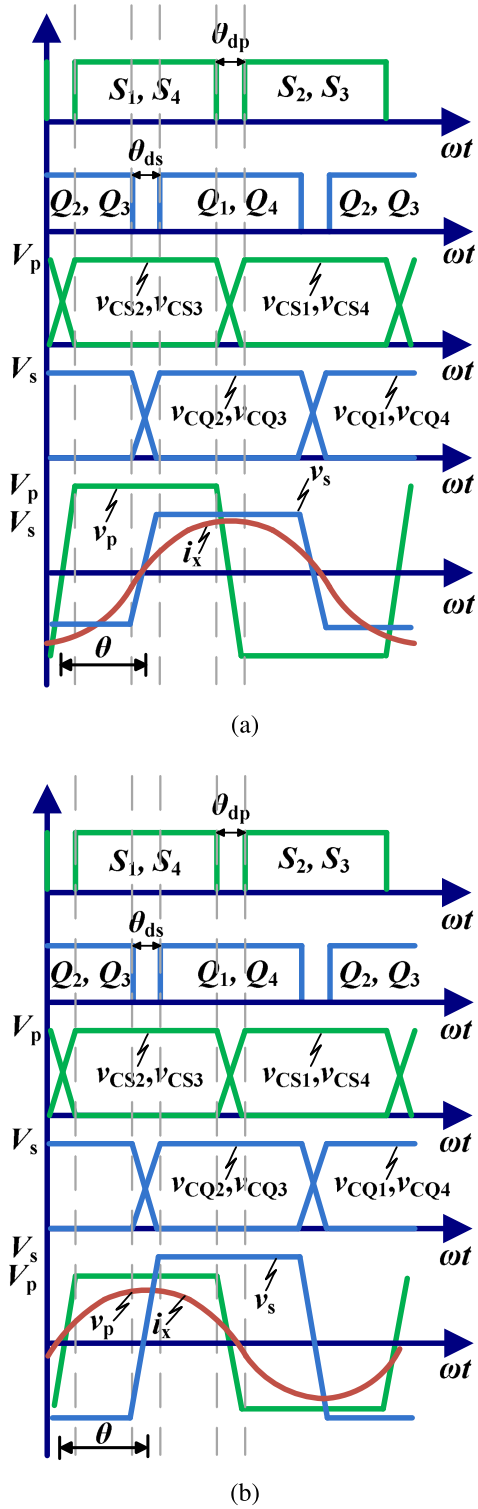
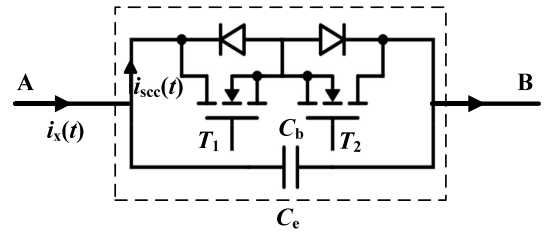


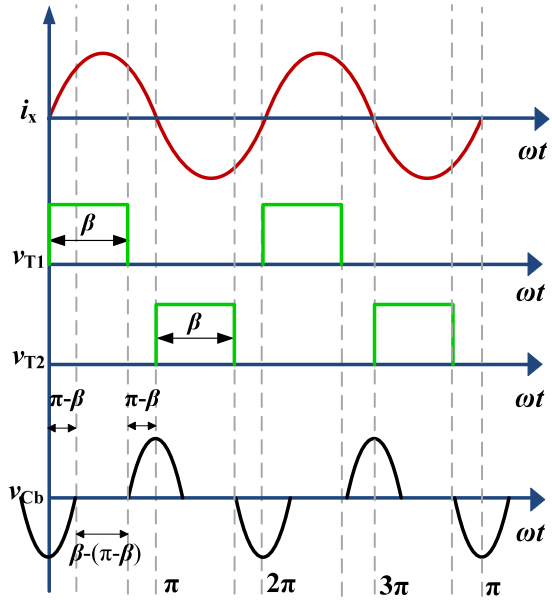
Fig. 6. Operating waveforms of DABSRC with complete soft-switching transitions and minimum-tank-current operation. (a) $M \leq 1$. (b) $M > 1$.

D. Design and Analysis of the Switched-Controlled Capacitor

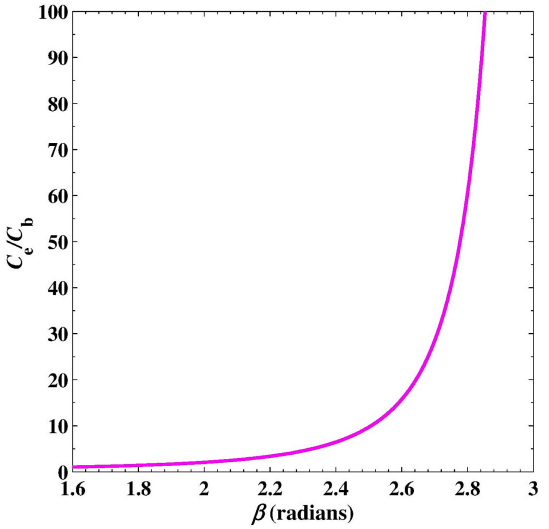
The proposed DABSRC topology based on switched impedance is shown in Fig. 2. It can be seen that SCC is inserted in DABSRC to realize a tunable resonant tank at the primary side and in doing so $X_{\rm eq} = X_{\rm eq,p.u} Z_{\rm B}$ can be utilized for power control in order to eliminate the restriction imposed by the minimum-tank-current conditions (10) on power variation. SCC allows the effective value of the resonant capacitor $C_{\rm r}$ of the resonant tank to be varied electronically so that the required variation in $P_{\rm o,p.u}$ can be achieved while θ is controlled to track the minimum-tank-current conditions (10). The schematic diagram of SCC is shown in Fig. 7(a), which is composed of two switches (i.e., T_1, T_2) in parallel with a base capacitor $C_{\rm b}$ [36]. In Fig. 7(b), consider a sinusoidal input current $i_{\rm x}(t)$ flowing from A to B, and the SCC switches are turned ON at the zero-crossings of $i_{\rm x}(t)$ for a duration of $\frac{\beta T}{2\pi}$. When the current passes through zero from negative to positive, T_1 is turned ON, whereas T_2 is turned ON at the zero crossings of $i_{\rm x}(t)$ from positive to negative. At the instance when the voltage $v_{\rm Cb}(t)$ across $C_{\rm b}$ is zero and T_1 conducts, the current flows from A to



(a)



(b)



(c)

Fig. 7. (a) Schematic diagram of SCC. (b) Operating waveforms of SCC. (c) Ratio of effective resonant capacitance C_e to base capacitance C_b with respect to control angle β.

B through T_1 and the body diode of T_2. At β, T_1 is turned OFf and C_b is charged by positive $i_x(t)$ and at the next zero crossing (i.e., positive to negative) T_2 is turned ON and C_b is discharged. When $v_{Cb}(t)$ is zero and T_2 conducts, $i_x(t)$ flows from B to A

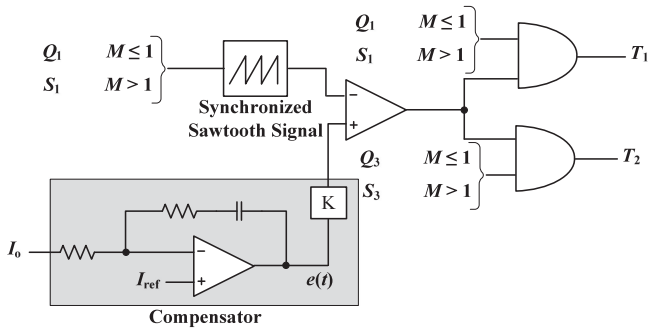


Fig. 8. Block diagram of SCC control.

through T_2 and the body diode of T_1 until T_2 is turned OFFat $\beta + \pi$ and C_b is charged by the negative flowing $i_x(t)$.

Furthermore, it can be seen that both T_1 and T_2 turn ON at zero current (due to zero i_x) and turn OFFat zero voltage (due to zero v_{Cb}). Hence, both T_1 and T_2 are soft switched with very small switching loss. On the other hand, the total conduction loss in SCC is derived and given as

$$P_{scc} = I_{scc,rms}^2 R_{DS(on)} + V_f I_{scc,rms} \tag{16}$$

where $R_{DS(on)}$ is on-resistance of MOSFETs, V_f is the forward-voltage drop of the body diode. From Figs. 6 and 7(b), the rms current $I_{scc,rms}$ flowing through T_1 and T_2 is given as

$$I_{scc,rms} = \sqrt{\frac{1}{\pi}\int_{\pi-\beta}^{\beta} [i_x(t)]^2 d\omega t}. \tag{17}$$

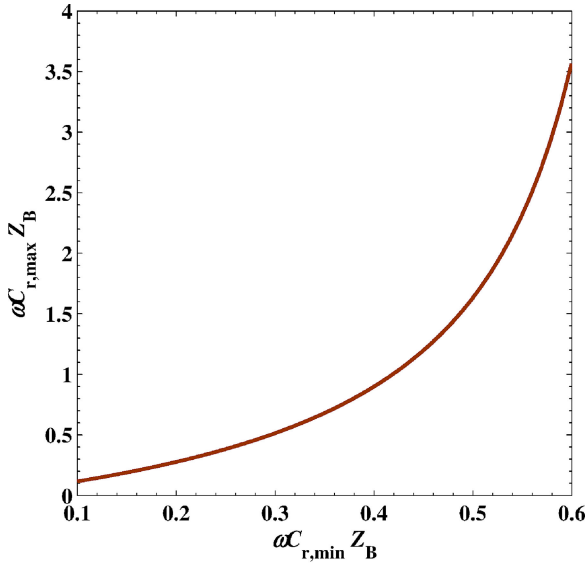
It can be seen from Fig. 7(b) that as β increases, the available charging time for capacitor C_b, i.e., $(\pi - \beta)$, decreases, resulting in a smaller peak and rms value of $v_{Cb}(t)$. Consequently, for a given $i_x(t)$, the control angle β provides a means of varying $v_{Cb}(t)$ and the amplitude of its fundamental component. The expression for the effective capacitance C_e is derived by considering the fundamental component of $v_{Cb}(t)$ and the result is given as [36]

$$C_e = \frac{C_b}{2 - (2\beta - \sin 2\beta)/\pi}. \tag{18}$$

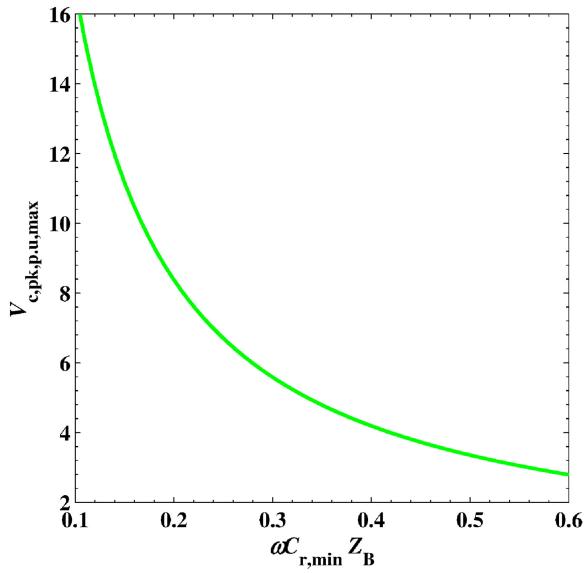
The ratio of the effective capacitance C_e to the base capacitor C_b is plotted against β in Fig. 7(c), which shows that C_e/C_b can in theory be varied from $0 \rightarrow \infty$ by adjusting $\frac{\pi}{2} \le \beta \le \pi$.

E. Realization of Switched-Impedance Network X_{eq} Using SCC

The tunable resonant tank is realized by incorporating SCC in the DABSRC as shown in Fig. 2. The overall impedance network X_{eq} is composed of a fixed resonant inductor L and a tunable resonant capacitor C_r. The effective value of the resonant capacitance C_r can be varied by choosing an appropriate value of control angle β; at $\beta = \pi$, C_r is equal to its maximum value C_a, and its minimum value $C_a//C_b$ is obtained at $\beta = \frac{\pi}{2}$. In practice, the required range of variation in C_r is limited to between $\frac{\pi}{2} \le \beta < \pi$. From Fig. 7(c) there is an exponential increase in C_e/C_b as $\beta \rightarrow \pi$, hence β is chosen to be 0.9π (i.e., 2.82) to avoid the case of $C_e = \infty$.



(a)



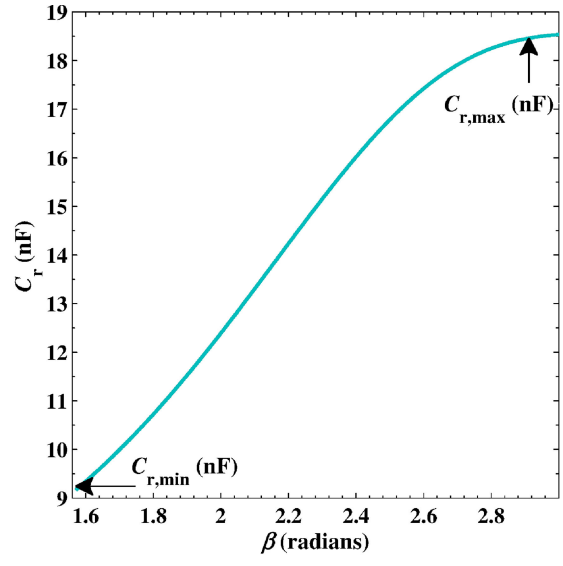
(b)

Fig. 9. (a) Variation of $C_{\mathrm{r,max}}$ against $C_{\mathrm{r,min}}$. (b) Change in $V_{\mathrm{c,pk,max}}$ at different values of $C_{\mathrm{r,min}}$.

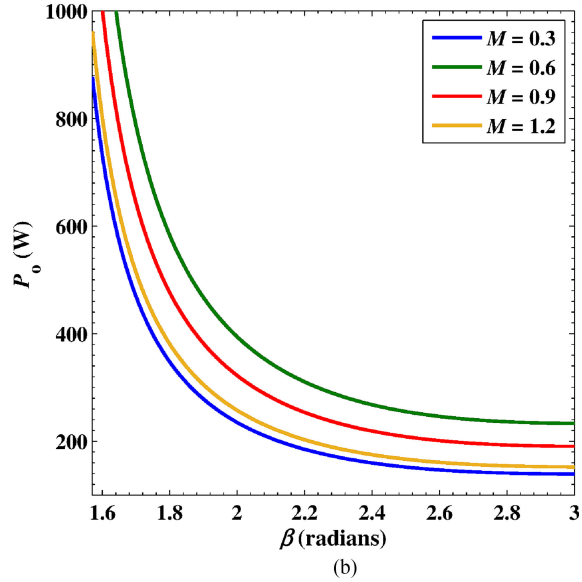
The maximum and minimum values of C_{r} are given by (20) and (21) and the corresponding values of C_{a} and C_{b} are determined by solving (20) and (21) simultaneously and the results are given by (22) and (23)

$$C_{\mathrm{r}} = \frac{C_{\mathrm{a}}C_{\mathrm{e}}}{C_{\mathrm{a}}+C_{\mathrm{e}}} = \frac{\pi C_{\mathrm{a}}C_{\mathrm{b}}}{\pi C_{\mathrm{b}}+C_{\mathrm{a}}\left(2\pi-2\beta+\sin 2\beta\right)} \tag{19}$$

$$C_{\mathrm{r,max}} = C_{\mathrm{r}}\mid_{\beta=0.9\pi} = \frac{\pi C_{\mathrm{a}}C_{\mathrm{b}}}{\pi C_{\mathrm{b}}+C_{\mathrm{a}}\left(2\pi-2\left(0.9\pi\right)+\sin(2\times 0.9\pi)\right)} \approx C_{\mathrm{a}} \tag{20}$$



(a)



(b)

Fig. 10. (a) Variation of C_{r} with respect to control angle β. (b) Variation in output power P_{o} with respect to control angle β for various values of M.

$$C_{\mathrm{r,min}} = C_{\mathrm{r}}\mid_{\beta=\frac{\pi}{2}} = \frac{C_{\mathrm{a}}C_{\mathrm{b}}}{C_{\mathrm{a}}+C_{\mathrm{b}}} \tag{21}$$

$$C_{\mathrm{a}} = \frac{C_{\mathrm{r,max}}C_{\mathrm{r,min}}\left[\pi-2\left(0.9\pi\right)+\sin\left(2\times 0.9\pi\right)\right]}{C_{\mathrm{r,max}}\left[2\pi-2\left(0.9\pi\right)+\sin\left(2\times 0.9\pi\right)\right]-\pi C_{\mathrm{r,min}}} \tag{22}$$

$$C_{\mathrm{b}} = \frac{C_{\mathrm{r,min}}C_{\mathrm{a}}}{C_{\mathrm{a}}-C_{\mathrm{r,min}}}. \tag{23}$$

The per-unit output power with the proposed DABSRC topology can be rewritten as

$$P_{\mathrm{o,p.u}} = \begin{cases} \frac{8M}{\pi^2 X_{\mathrm{eq,p.u}}}\sin(\cos^{-1}(M)) & M\le 1 \\ \frac{8M}{\pi^2 X_{\mathrm{eq,p.u}}}\sin\left(\cos^{-1}\left(\frac{1}{M}\right)\right) & M>1 \end{cases} \tag{24}$$

where $X_{\mathrm{eq,p.u}} = (\omega L - \frac{1}{\omega C_{\mathrm{r}}})/Z_{\mathrm{B}}$.

TABLE I
SPECIFICATIONS OF CONVERTER PROTOTYPE

Maximum input voltage $V_{\mathrm{i,max}}$	250 V
Maximum output voltage $V_{\mathrm{o,max}}$	48 V
Transformer ratio n	5.21
Proposed resonant tank (L, C_{a}, and C_{b})	Calculated (302.6 μH, 18.1 nF, and 18.5 nF)
	Experimental (300 μH, 18 nF, and 18.5 nF)
Maximum rated output power $P_{\mathrm{avg,o}}$	1 kW
Primary side MOSFETs	UJC06505K (650 V, 36.5 A, 35 mΩ)
Secondary side MOSFETs	CSD18535KCS (60 V, 279 A, 1.6 mΩ)
SCC MOSFETs	UJC06505K (650 V, 36.5 A, 35 mΩ)
Gate drivers	Infineon 2ED020I12-F2
Inductor's core shape and material	FC3 Ferrite (ETD-49 Core)
Transformer's core shape and material	FC3 Ferrite (ETD-49 Core)
Supercapacitor	Maxwell Technologies (48 V, 83 F)
Controller	32-bit ARM Cortex-M3 PSoC 5LP by Cypress Semiconductor
Voltage and current sensors	LEM Sensors (LV25-P and LA55-P)

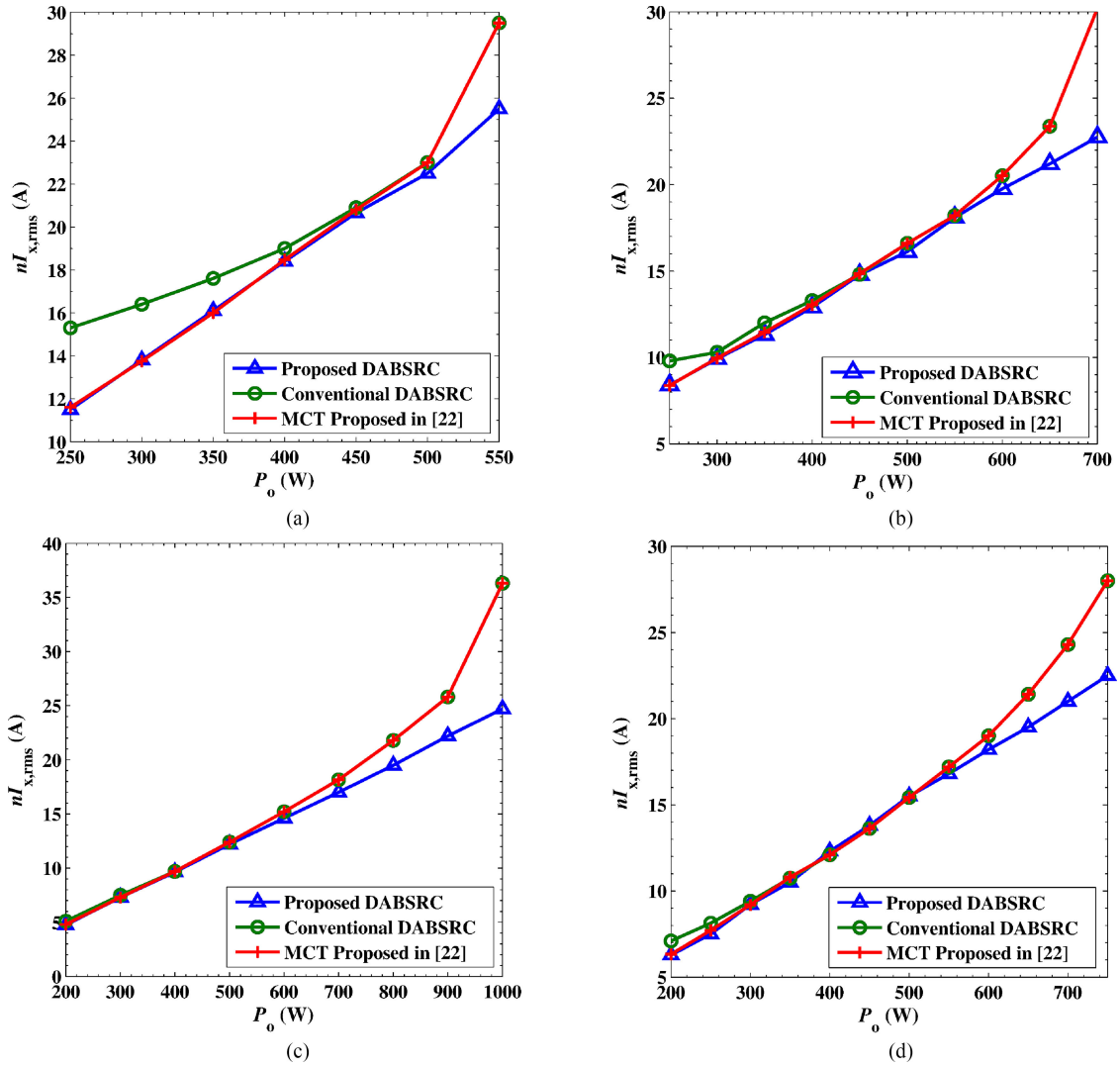


Fig. 11. Secondary reflected tank current $nI_{\mathrm{x,rms}}$ of DABSRC under the proposed, conventional, and MCT modulation methods. (a) $M = 0.5$. (b) $M = 0.7$. (c) $M = 0.94$. (d) $M = 1.2$.

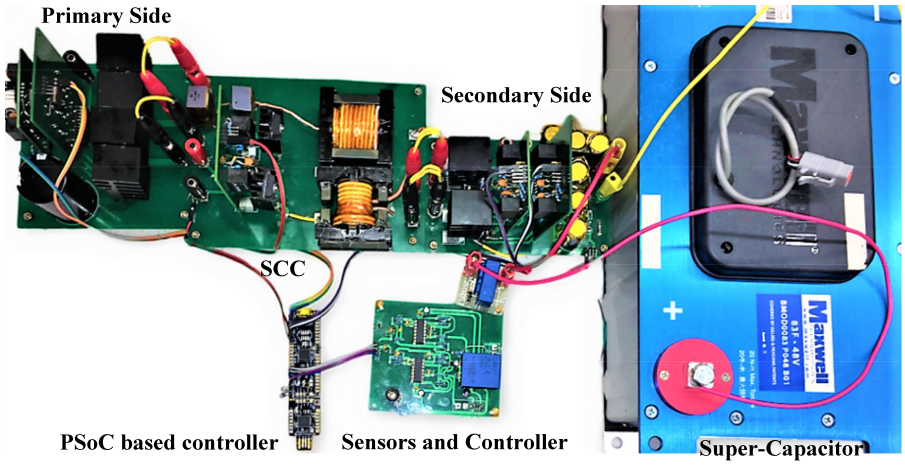


Fig. 12. Hardware realization of the proposed DABSRC topology.

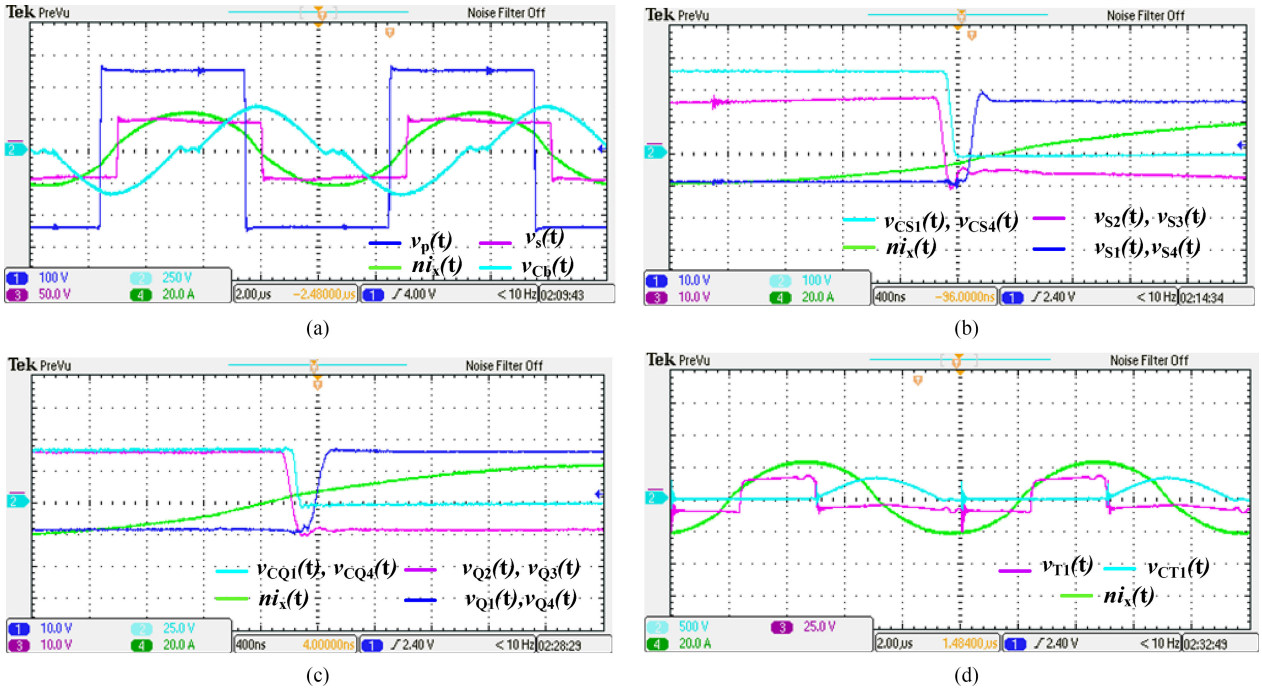


Fig. 13. Experimental waveforms. (a) Charging supercapacitor with $V_{\rm p} = 250$ V (100 V/div), $V_{\rm s} = 45$ V (50 V/div), $nI_{\rm x,rms} = 19.8$A (20 A/div), $I_{\rm o} = 17.7$ A, $M = 0.94$, $V_{\rm Cb,rms} = 279$ V (500 V/div), $P_{\rm o} = 800$ W, conduction loss due to SCC $P_{\rm scc} = 1$ W and efficiency $= 94.7\%$. (b) ZVS operation of S_1 and S_4. (c) ZVS operation of Q_1 and Q_4. (d) ZVS operation of T_1.

Fig. 8 illustrates the block diagram of the output current regulator. S_1, S_3, Q_1, Q_3, T_1, and T_2 are the pulse width modulation (PWM) signals to control the primary-side, secondary-side, and SCC MOSFETs. In order to generate the required control angle β for the SCC, a sawtooth voltage is synchronized with the tank current $i_{\rm x}(t)$ (or equivalently, with the secondary-side voltage $v_{\rm s}(t)$ for $M \leq 1$ and with the primary-side voltage $v_{\rm p}(t)$ for $M > 1$) and compared with the error voltage $e(t)$ generated by the compensator.

III. Simulation and Experimental Results

To validate the proposed DABSRC, a switched impedance $X_{\rm eq,p.u}$ is designed for M with a minimum value of 0.2 and in order to avoid the need of generating excessively large dead-time intervals as suggested by (13), the per-unit power variation $P_{\rm o,p.u}$ is limited to between 0.1 and 1. By analyzing (24), the maximum value of the switched impedance $X_{\rm eq,p.u,max}$ is determined by the required minimum output power $P_{\rm o,p.u,min} = 0.1$ at $M = 0.2$, because under minimum-tank-current operation, θ is large for small M according to (10). At $M = 1$, (10) gives $\theta = 0^{\rm o}$ which according to (13) does not provide the required tank current to charge/discharge parasitic capacitances for complete soft-switching transitions. Hence, for practical design purpose and to provide sufficient current to achieve soft switching, $M = 0.94$ (i.e., $\theta = 20^{\rm o}$) is chosen to provide required maximum output power $P_{\rm o,p.u,max} = 1$ at $X_{\rm eq,p.u,min}$. According to the aforementioned design considerations and by the use of (24), the expressions for $X_{\rm eq,p.u,max}$ and $X_{\rm eq,p.u,min}$ are given

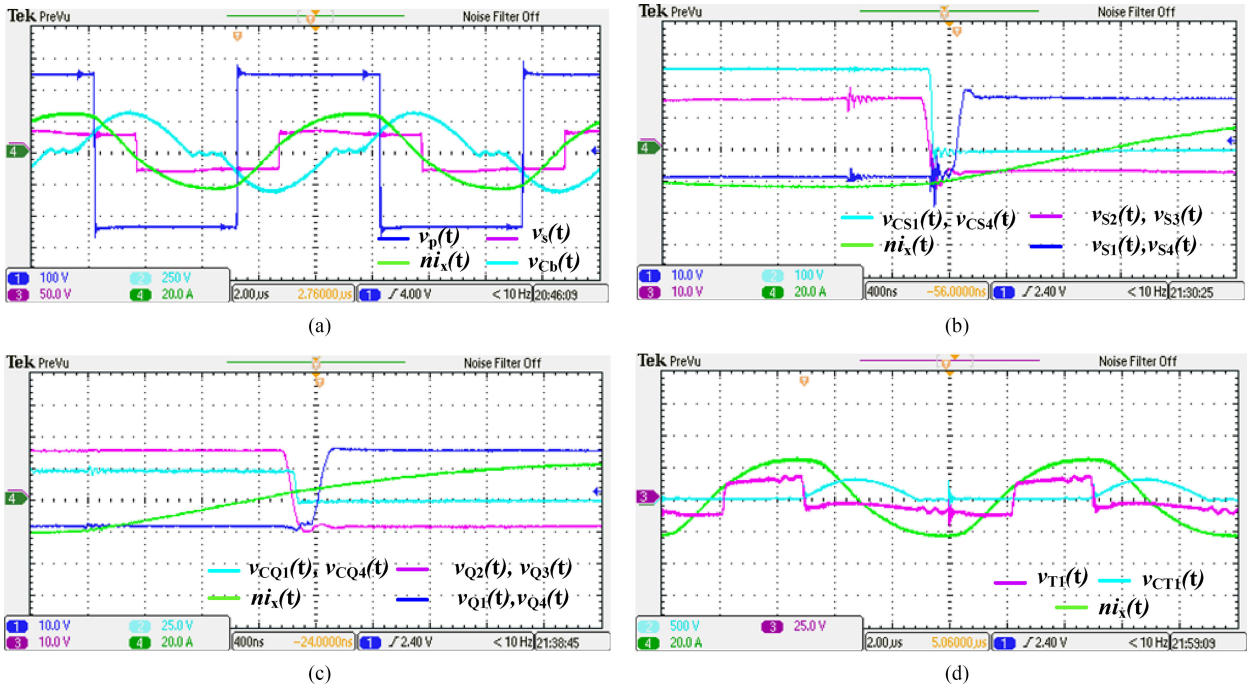


Fig. 14. Experimental waveforms. (a) Charging supercapacitor with $V_{\rm p} = 250$ V (100 V/div), $V_{\rm s} = 29$ V (50 V/div), $nI_{\rm x,rms} = 19.3$ A (20 A/div), $I_{\rm o} = 17.4$ A, $M = 0.6$, $V_{\rm Cb,rms} = 226$ V (500 V/div), $P_{\rm o} = 500$ W, conduction loss due to SCC $P_{\rm scc} = 2.8$ W and efficiency $= 91.2\%$. (b) ZVS operation of S_1 and Q_1. (c) ZVS operation of Q_1 and Q_4. (d) ZVS operation of T_1.

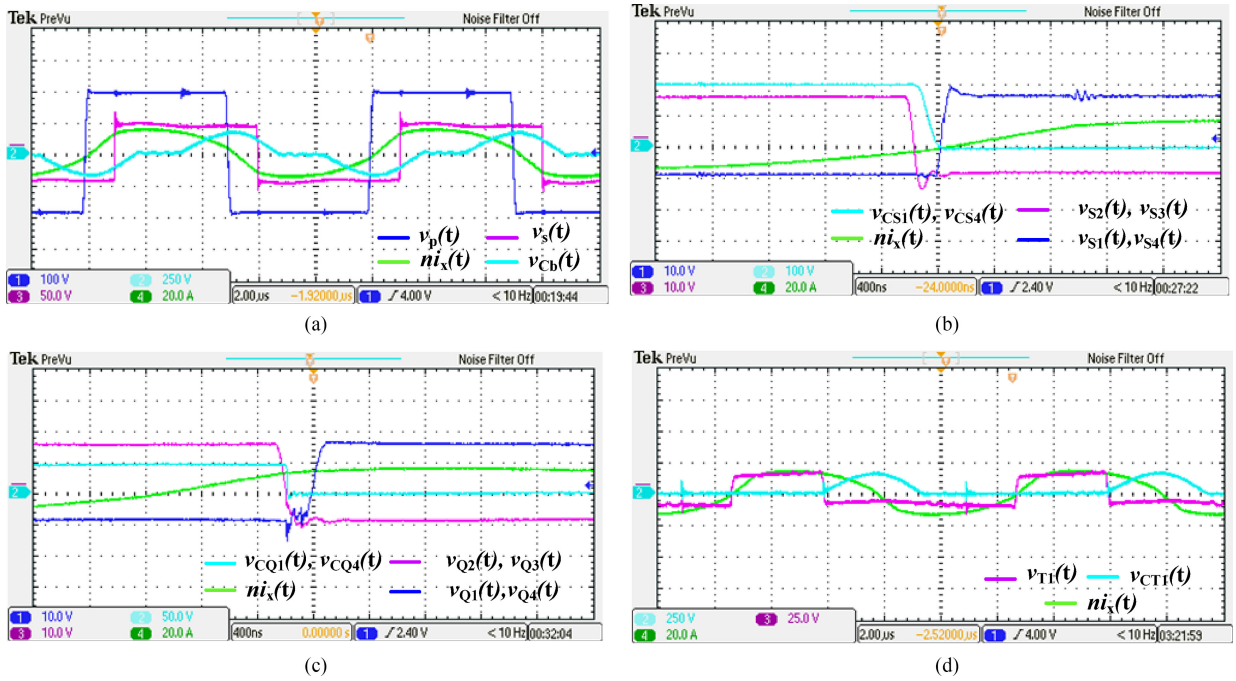


Fig. 15. Experimental waveforms. (a) Charging supercapacitor with $V_{\rm p} = 195$ V (100 V/div), $V_{\rm s} = 45$ V (50 V/div), $nI_{\rm x,rms} = 12.6$ A (20 A/div), $I_{\rm o} = 9$ A, $M = 1.2$, $V_{\rm Cb,rms} = 113$ V (250 V/div), $P_{\rm o} = 400$ W, conduction loss due to SCC $P_{\rm scc} = 1.8$ W, and efficiency $= 95\%$. (b) ZVS operation of S_1 and S_4. (c) ZVS operation of Q_1 and Q_4. (d) ZVS operation of T_1.

by (25) and (26), respectively

$$\frac{\omega L}{Z_{\rm B}} - \frac{1}{\omega C_{\rm r,max} Z_{\rm B}} = X_{\rm eq,p.u,max} = 1.65 \qquad (25)$$

$$\frac{\omega L}{Z_{\rm B}} - \frac{1}{\omega C_{\rm r,min} Z_{\rm B}} = X_{\rm eq,p.u,min} = 0.26. \qquad (26)$$

The range of variation of C_r is defined by $\omega C_{\rm r,max} Z_{\rm B}$ and $\omega C_{\rm r,min} Z_{\rm B}$, which are related by solving (25) and (26) simultaneously. The result is given by (27) and plotted in Fig. 9(a). Another important design parameter is the maximum peak voltage $V_{\rm c,pk,p.u,max}$ across $C_{\rm r}$, given by (28), which is determined by the value of $\omega C_{\rm r,min} Z_{\rm B}$ at $M = 0.94$ and $P_{\rm o,p.u,max} = 1$

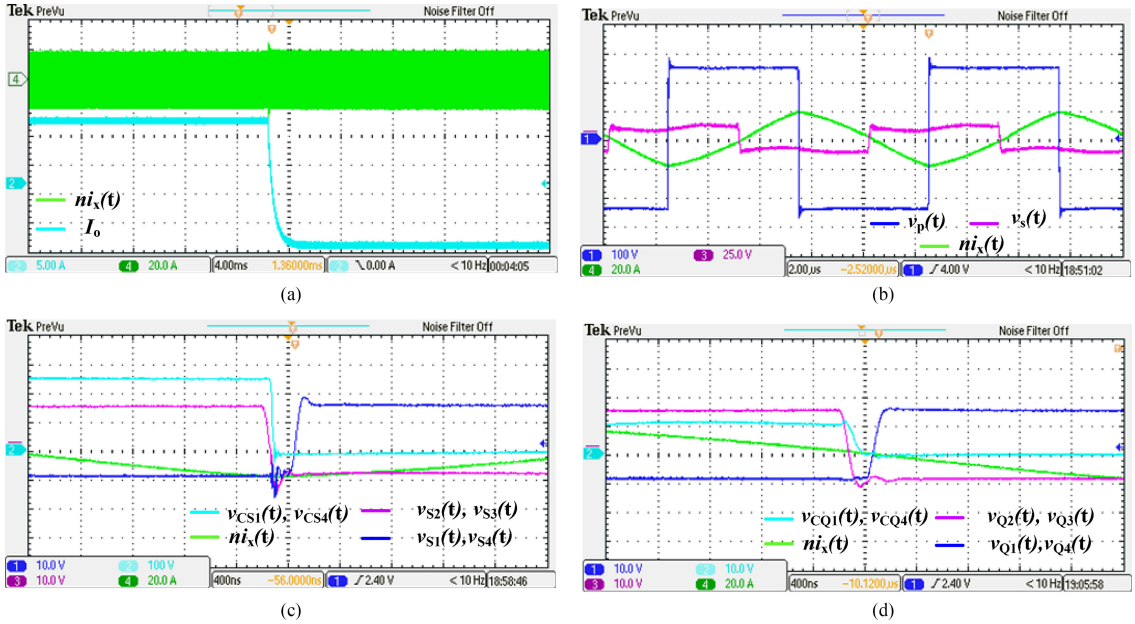


Fig. 16. Experimental waveforms. (a) Transition between charging (forward power flow) and discharging (backward power flow) mode for the change in output current I_o of 22 A (+11 A to −11 A) (b) Discharging mode (backward power flow) with $V_p = 250$ V (100 V/div), $V_s = 10$ V (25 V/div), $nI_{x,rms} = 12.1$ A (20 A/div), $I_o = 11$ A, $M = 0.2$, $P_o = 110$ W, conduction loss due to SCC $P_{scc} = 2.6$ W and efficiency $= 88.5\%$. (c) ZVS operation of S_1 and S_4. (d) ZVS operation of Q_1 and Q_4.

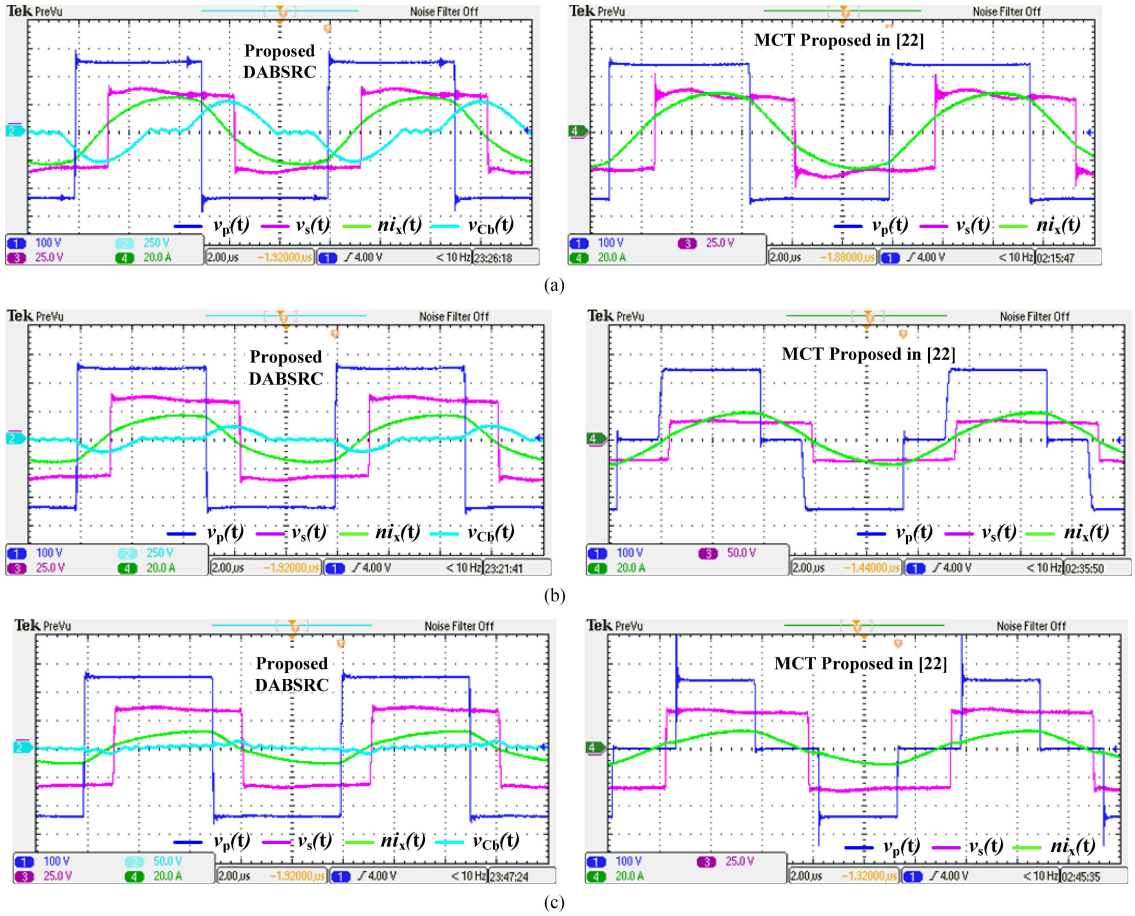


Fig. 17. Experimental waveforms with $V_p = 250$ V, $V_s = 33.6$ V, and $M = 0.7$ (a) Proposed modulation method with $nI_{x,rms} = 18.2$A, $P_o = 600$ W, and efficiency $= 91.3\%$. MCT with $nI_{x,rms} = 19.5$ A, $P_o = 600$ W, and efficiency $= 90\%$. (b) Proposed modulation method with $nI_{x,rms} = 12.8$ A, $P_o = 400$ W, and efficiency $= 93.6\%$. MCT with $nI_{x,rms} = 12.7$ A, $P_o = 400$ W, and efficiency $= 93.7\%$. (c) Proposed modulation method with $nI_{x,rms} = 8.28$ A, $P_o = 250$ W, and efficiency $= 95\%$. MCT with $nI_{x,rms} = 8.2$ A, $P_o = 250$ W, and efficiency $= 93.5\%$.

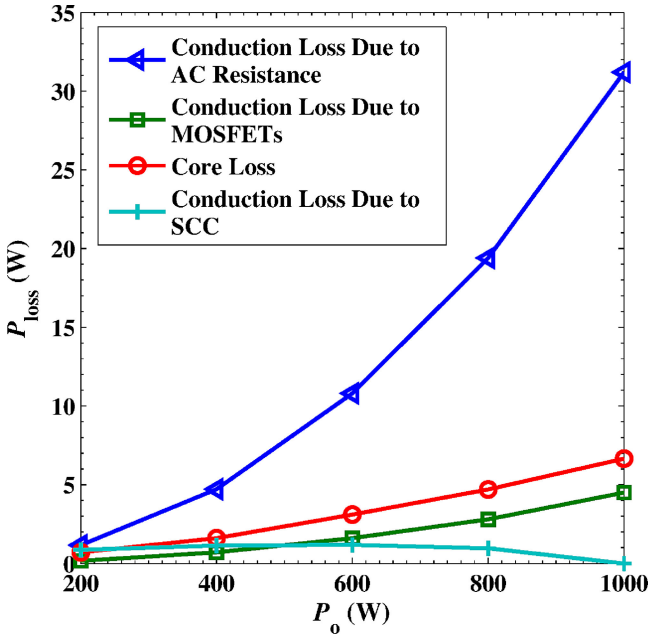


Fig. 18. Breakdown of power losses $P_{\rm loss}$ at the nominal operating point.

$$\omega C_{\rm r,max} Z_{\rm B} = \frac{1}{\frac{1}{\omega C_{\rm r,min} Z_{\rm B}} - 1.38} \tag{27}$$

$$V_{\rm c,pk,p.u,max} = \frac{\sqrt{2} \times I_{\rm x,rms,p.u,max}}{\omega C_{\rm r,min} Z_{\rm B}}. \tag{28}$$

Fig. 9(b) shows the variation of $V_{\rm c,pk,p.u,max}$ against $\omega C_{\rm r,min} Z_{\rm B}$ and it can be seen that in order to reduce the voltage stress across $C_{\rm r}$, a higher value of $C_{\rm r,min}$ is preferred. However, Fig. 9(a) shows that $C_{\rm r,max}$ increases exponentially with increasing $C_{\rm r,min}$. The large difference between $C_{\rm r,max}$ and $C_{\rm r,min}$ at high value of $C_{\rm r,min}$ in turn causes $C_{\rm r}$ to be a steep function of the control angle β [(c.f., Fig. 10(a)], which degrades the noise susceptibility of the converter at high $C_{\rm r,min}$. Therefore, bearing in mind this tradeoff, a mid-range value of $\omega C_{\rm r,min} Z_{\rm B} = 0.36$ is chosen and $\omega C_{\rm r,max} Z_{\rm B} = 0.72$ is found from (27).

A. Simulation Results

The proposed DABSRC is designed for a rated power of 1 kW to charge/discharge a supercapacitor with a terminal voltage variation of 10 to 45 V, switching frequency of 100 kHz, and an input dc bus of maximum 250 V. The base resistance for the rated power of 1 kW can be found as $Z_{\rm B} = \frac{n^2 V_{\rm o,max}^2}{P_{\rm o,max}} = 62.5\,\Omega$. The values of other components (L, $C_{\rm a}$, and $C_{\rm b}$) are calculated using (22), (23), (25), and (26) and listed in Table I. The variation of $C_{\rm r}$ for the proposed design with respect to the control angle β is plotted in Fig. 10(a) using (19), and by the use of (24) the converter's output power $P_{\rm o}$ is plotted as a function of the control angle β at various values of M and is shown in Fig. 10(b).

The tank currents under three modulation methods, i.e., conventional (SPS), proposed, and minimum current trajectory (MCT) based modulation method proposed in [22], are simulated for different power levels and the results are plotted in Fig. 11(a)–(d). It can be seen that both MCT and the proposed method result in similar rms tank current at low to medium power levels, i.e., $|P_{\rm o}/P_{\rm o,max}| \leq \sqrt{1-M^2}$ for $M \leq 1$ or $\sqrt{1-(1/M)^2}$ for $M > 1$. However, as power level increases to $|P_{\rm o}/P_{\rm o,max}| \geq \sqrt{1-M^2}$ for $M \leq 1$ or $\sqrt{1-(1/M)^2}$ for $M > 1$, MCT follows the conventional method and, therefore, results in higher rms tank current than the proposed method. Furthermore, while the proposed method ensures full-range soft switching, two primary-side switches of DABSRC modulated with MCT encounter hard switching when power level decreases to $|P_{\rm o}/P_{\rm o,max}| \leq \sqrt{M-M^2}$ for $M \leq 1$ or $\sqrt{1/M-(1/M)^2}$ for $M > 1$.

B. Experimental Results

The experimental prototype of the proposed DABSRC topology with the specifications given by Table I is shown in Fig. 12. MOSFETs are used to realize all primary-side, SCC, and secondary-side switches. A programmable system-on-chip (PSoC) is used to generate the required PWM signals for all switches, adjust the phase-shift θ based on the sensed output voltage to ensure minimum-tank-current operation, and generate the synchronized sawtooth waveform for the production of control angle β of SCC by sensing the output current.

The measured waveforms of $v_{\rm p}(t)$, $v_{\rm s}(t)$, $ni_{\rm x}(t)$, $v_{\rm Cb}(t)$, $v_{\rm CS1}(t)$, $v_{\rm CS4}(t)$, $v_{\rm CQ1}(t)$, $v_{\rm CQ4}(t)$, and $v_{\rm T1}(t)$ are analyzed to validate the proposed DABSRC topology. Fig. 13(a)–(d) depict the case of charging supercapacitor at output power $P_{\rm o} = 800$ W, output current $I_{\rm o} = 17.7$ A, and $M = 0.94$ ($V_{\rm i} = 250$ V and $V_{\rm o} = 45$ V). Fig. 13(b) and (c) shows that ZVS operation is achieved for all primary-side and secondary-side switches by charging and discharging parasitic capacitances within the designed dead-time interval. As for the SCC, both T_1 and T_2 undergo soft switching inherently, as shown in Fig. 13(d), at the switching instances of T_1. A case of lower output power $P_{\rm o} = 500$ W, output current $I_{\rm o} = 17.2$ A, and $M = 0.6$ ($V_{\rm i} = 250$ V and $V_{\rm o} = 29$ V) is shown in Fig. 14(a)–(d) and it can be seen that ZVS operation is achieved for all switches. The proposed DABSRC is also verified for the case of $M = 1.2$ ($V_{\rm i} = 195$ V and $V_{\rm o} = 45$ V) at $P_{\rm o} = 400$ W with experimental waveforms shown in Fig. 15(a)–(d). The cases depicting the transition from charging to discharging mode of the supercapacitor and backward power flow are captured in Fig. 16(a)–(d), which shows the effectiveness of the proposed topology for reverse power flow as well. Moreover, minimum-tank-current operation is achieved by keeping an in-phase relationship between the tank current and secondary-side voltage for $M \leq 1$ and with primary-side voltage for $M > 1$ by satisfying the condition (10) for the purpose of reducing circulating current and parasitic-induced ringing [37].

To compare the proposed modulation method to MCT, a prototype that operates with MCT is built and tested. Fig. 17(a)–(c) depicts the experimental waveforms for three power levels. For $P_{\rm o} = 600$ W, i.e. $|P_{\rm o}/P_{\rm o,max}| \geq \sqrt{1-M^2}$, Fig. 17(a) shows that the proposed method results in a higher efficiency (91.3% compared to 90% with MCT) due to a lower tank current (18.2 A compared to 19.5 A with MCT). As the power level is reduced to $P_{\rm o} = 400$ W, i.e. $|P_{\rm o}/P_{\rm o,max}| \leq \sqrt{1-M^2}$, as shown

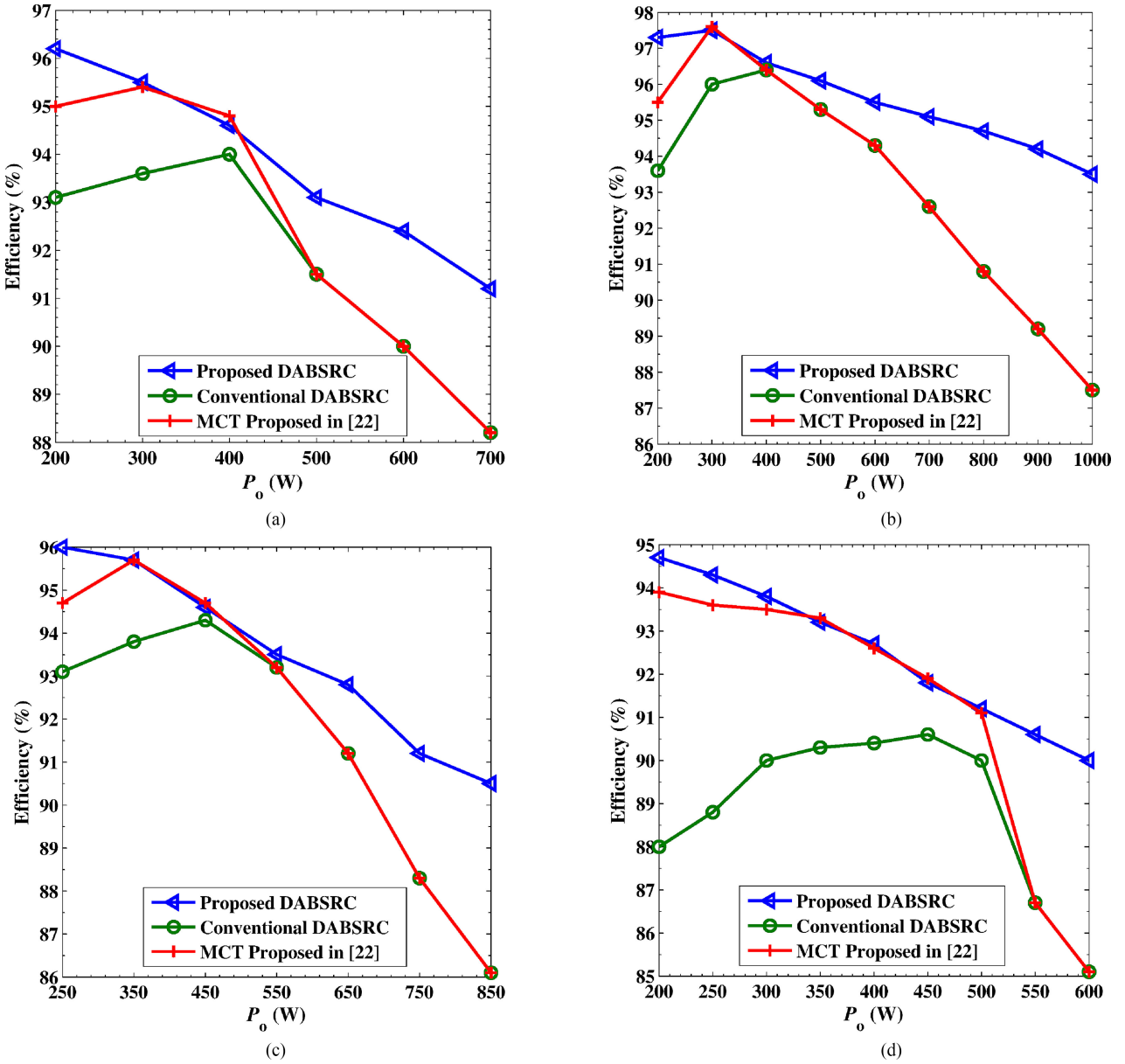


Fig. 19. Measured efficiencies of DABSRC for various values of M and P_o. (a) $M = 1.2$. (b) $M = 0.94$. (c) $M = 0.8$. (d) $M = 0.6$.

in Fig. 17(b), both methods result in similar efficiency and tank current magnitude. However, as the power level is further reduced to $|P_o/P_{o,max}| \leq \sqrt{M - M^2}$, Fig. 17(c) shows that for $P_o = 250$ W two primary-side switches in DABSRC modulated with MCT encounter hard switching (as evident from the severe ringing at the primary bridge voltages rising edges) while soft switching is maintained by the proposed method for all switches. As a result of the incurred switching loss, MCT results in a lower efficiency (93.5% compared to 95% with the proposed method).

The measured efficiencies of the proposed, conventional, and MCT-based DABSRC under various P_o and M are plotted in Fig. 19(a)–(d), which show that the proposed DABSRC topology and modulation method outperforms the conventional and MCT-based DABSRC under wide variation in output power P_o. Fig. 18 shows the loss break down at the nominal operating point and it can be observed that the conduction loss incurred in SCC is not significant when compared with the switching and conduction losses resulting (c.f., Fig. 19) from the conventional and MCT modulation methods, as they remain outperformed by the proposed method in terms of efficiency. The increase in efficiency with increasing M can be explained by the fact that, at lower M, and hence lower output power, the conduction loss resulting from the parasitic resistance of semiconductor devices, windings resistance, forward voltage drop of the body diodes of MOSFETs, and PCB traces are constant for a given output current and poses more weight in efficiency as compared to the cases of higher M. Also, according to (10), at lower values of M, a large phase shift θ is necessary to maintain minimum-tank-current operation that will lead to a larger circulating power and hence a larger conduction loss at the primary side of the DABSRC [35], [38], [39].

IV. Conclusion

An efficient operation of DABSRC in high-power applications requires the minimization of both conduction loss and switching loss. To achieve these aims, a modified series resonant topology of DABSRC is proposed to achieve soft switching and minimum-tank-current operation over wide-range variations in output current and voltage. The proposed topology utilizes SCC to realize a switched-impedance-based series resonant tank, where the control angle β of an SCC is utilized for power control. To verify the feasibility and effectiveness of the proposed DABSRC topology and power modulation method, simulation and experimental results under different values of supercapacitor's output voltages, and charging/discharging currents are presented. A maximum efficiency of 97.5% is obtained from experimental prototype.

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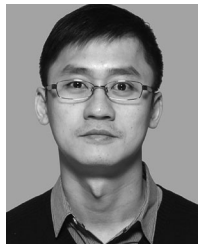

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