Dual-Buck AC–AC Converter With Inverting and Non-Inverting Operations

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***Abstract*—In this paper, a novel buck–boost ac–ac converter is proposed. The basic switching unit of the proposed converter is a unidirectional buck circuit; therefore, it has no shoot-through worries. It can achieve safe commutation without using *RC* snubbers or soft commutation strategies. It can be implemented with power MOSFETs without their body diodes conducting and, for current freewheeling external diodes, can be used to minimize the reverse recovery issues and related loss. It has a bipolar voltage gain with both inverting and non-inverting operations. The non-inverting operation can be used to compensate voltage sag, and inverting operation can be used to compensate voltage swell. Therefore, the proposed converter as a dynamic voltage restorer is capable of compensating for both voltage sag and swell in a wide range. The detailed theoretical analysis followed by detailed experimental results of a 300-W prototype converter is provided.**

***Index Terms*—AC–AC converter, bipolar voltage gain, commutation, dual-buck, dynamic voltage restorer (DVR), MOSFET, reliability.**

Nomenclature

DVR	Dynamic voltage restorer.
VSI	Voltage-source inverter.
PWM	Pulse width modulation.
RMS	Root mean square.
NIB	Non-inverting buck.
IBB	Inverting buck–boost.
INIBB	Inverting and non-inverting buck–boost.
IBu	Inverting buck.
IBo	Inverting boost.
PI	Proportional–integral.

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I. Introduction

DUE to variation in load condition and supply-side disturbance, the voltage available to consumers is exposed to problems of power quality. The sag and swell in the supply voltage are the main power quality problems. They can damage or shut down the sensitive equipment. Voltage sag happens when the supply voltage dropped between 10% and 90% of the RMS voltage [1], [2], and voltage swell happens when the supply voltage suddenly increased up 110–180% of the RMS voltage [3]. The static synchronous series compensator (SSSC) and the DVR are commonly employed to mitigate the power quality problems. The SSSC is used at the higher voltage level [4] and the DVR is preferred at the lower voltage level [5].

A DVR can be designed with a VSI [6] or a direct PWM ac–ac converter [7]. A DVR based on the VSI is shown in Fig. 1. It compensates both voltage sag and swell and also stores energy in batteries for voltage compensation. However, it requires an additional ac–dc power processing stage with bulky dc-link capacitors and batteries, which makes this solution cumbersome. Fig. 2 shows the DVRs implemented with an ac–ac converter [7]. The DVR based on a direct ac–ac converter saves the bulky dc-link capacitors and the additional ac–dc power-processing stage.

Among the direct PWM ac–ac converters, the traditional buck, IBB, non-inverting buck–boost, and Cuk converters [8]–[12] are the common topologies. However, they have unipolar voltage gains and can compensate either voltage sag or swell. The ac–ac converters with a bipolar voltage gain can compensate both voltage sag and swell. The Z-source ac–ac converters [13]–[16] have bipolar voltage gains; however, the sharp rise and fall in its gain during the NIB operation are quite challenging for the controller. In addition, the high voltage and current stresses of the switches degrade its efficiency. The ac–ac converters in [17] and [18] have bipolar voltage gains; however, they have complex operational modes. The aforementioned ac–ac converters [13]–[18] have shoot-through and/or dead-time problems, which are major reliability issues. To avoid shoot-through and dead-time problems, they use either *RC* snubbers or soft commutation strategies [19], [20]; however, these techniques have some serious drawbacks [21], [22].

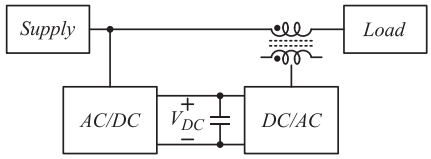

Fig. 1. DVR using a VSI [6].

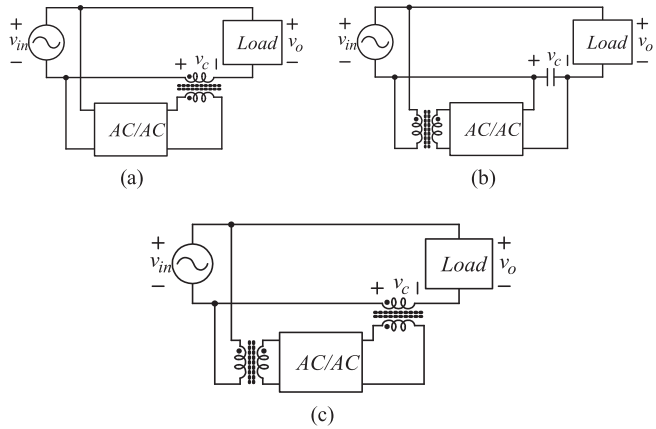

Fig. 2. Single-phase DVRs using a direct PWM ac–ac converter [7].

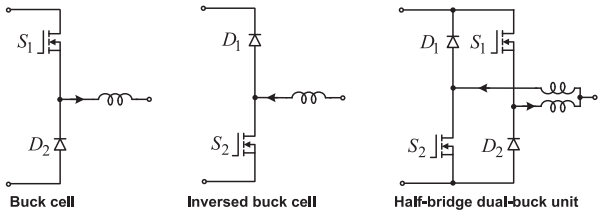

Fig. 3. Dual-buck structure [35].

The first dual-buck converter was proposed in [35]. Its basic switching unit consists of two buck cells connected in parallel, as shown in Fig. 3. In each buck cell, an external diode is connected in series with a MOSFET; therefore, no shoot-through is possible. In Fig. 3, instead of body diodes, external diodes of good reverse recovery features freewheel the current; therefore, the reverse recovery issues can be decreased.

Recently, new type single-phase [21] and three-phase [22] ac–ac converters using the dual-buck structure [35] are proposed. They do not have short-circuit and open-circuit issues, and they do not require *RC* snubbers and soft commutation strategies. Furthermore, they can use MOSFETs without their body diodes conducting. However, they generate circulating currents, and to limit their circulating currents, they require coupled inductors. To decrease the magnetic volume of the coupled inductors in [21], the separate coupled inductors are integrated into one core in [12]. To further decrease the magnetic volume, the filter inductor in [12] is eliminated by utilizing the leakage inductance of the integrated coupled inductor in [23]. In [25], a cascaded multilevel converter based on the single-phase converter [21] is proposed. The converters in [12], [21]–[23], and [25] generate circulating currents, and to eliminate their circulating currents, modified ac–ac converters using separate filter inductors are proposed in [11], [24], and [36]. However, all of these converters have unipolar voltage gains and can compensate either voltage sag or swell in a DVR. In [26], a high-frequency isolated double step-down ac–ac converter is proposed. It has a buck function with a bipolar voltage gain. However, its output peak voltage cannot exceed half of the input peak voltage; therefore, its range to compensate voltage sag or swell is limited. Furthermore, it is associated with the circulating current of [21], which decreases the efficiency.

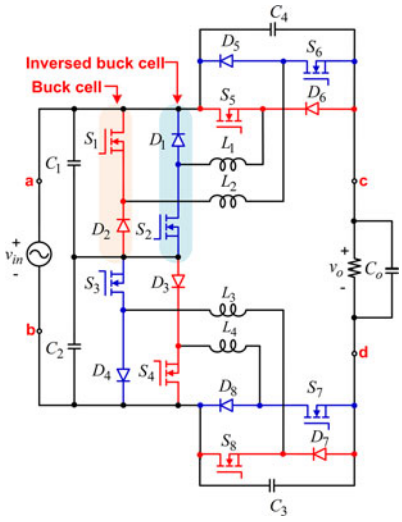

Fig. 4. Proposed ac–ac converter.

Similar to the aforementioned dual-buck-type ac–ac converters, single-stage buck–boost inverters [27], [28], buck inverters [29]–[32], and multilevel converters [33], [34] are proposed with the dual-buck structure to avoid shoot-through and to improve efficiency by utilizing MOSFETs without the reverse recovery issues of their body diodes.

In this paper, a dual-buck-type buck–boost ac–ac converter with a bipolar voltage gain is proposed. It compensates both voltage sag and swell in a wide range when used as a DVR. The proposed converter can operate as a conventional NIB converter and an IBB converter with voltage gains D and $-D/(1-D)$, respectively, where D is the duty cycle of the converter [39]. In addition, it can be operated with the voltage gain $(2D-1)/D$, with the NIB operation for $0.5 < D < 1$, the IBu operation for $0.33 < D < 0.5$, and the IBo operation for $0 < D < 0.33$. The proposed converter has no short-circuit and open-circuit issues, and it can achieve safe commutation without requiring *RC* snubbers and soft commutation techniques.

II. Proposed Converter

Fig. 4 shows the schematic diagram of the proposed converter. Its basic switching unit is a buck cell. In each buck cell and inversed buck cell, a MOSFET is connected in series with an external diode, and each cell is connected to a separate inductor. Therefore, the proposed converter has no shoot-through issues.

Inductors $(L_1$–$L_4)$ store energy, oppose shoot-through, and avoid current flow through the body diodes of MOSFETs $(S_1$–$S_8)$. The current freewheeling external diodes $(D_1$–$D_8)$ of good reverse recovery features can be used, ow-

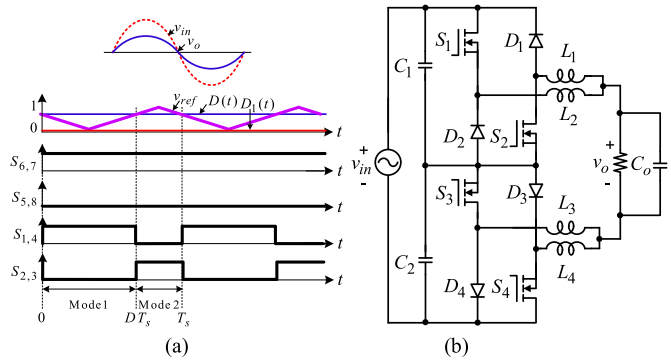

Fig. 5. NIB operation. (a) Gate signal generation. (b) Equivalent circuit.

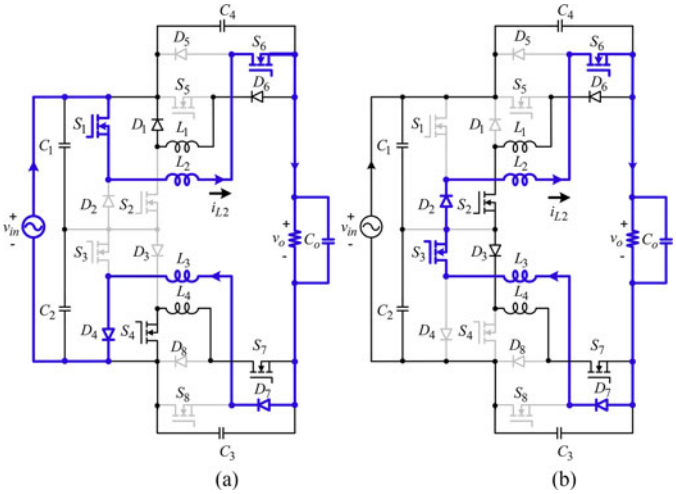

Fig. 6. Operational modes in NIB operation. (a) Mode 1. (b) Mode 2.

ing to which the reverse recovery loss and issues can be minimized.

As aforementioned, the proposed ac–ac converter has no shoot-through concerns; therefore, large dead-time in the gating signals and *RC* snubbers are not required. C_1–C_4 are attached to avoid voltage spikes in unwanted dead-times between the switches. They also serve as filtering capacitors. In this paper, L_1–L_4 are assumed to have the identical inductance L, and the operating modes are shown only for $v_o > 0$.

III. NIB Operation

As shown in Fig. 5(a), in NIB operation, S_6 and S_7 are always ON, and S_5 and S_8 are always OFF. The equivalent circuit in the NIB operation is shown in Fig. 5(b). In this operation, $v_o \leq v_{\text{in}}$ and v_o is in phase with v_{in}.

A. Mode 1 $[0 - DT_s]$

D is defined in Fig. 5(a). As shown in Fig. 6(a), S_1 and S_4 are ON, and S_2 and S_3 are OFF

$$\frac{di_{L2}}{dt} = \frac{v_{\text{in}} - v_o}{2L}. \tag{1}$$

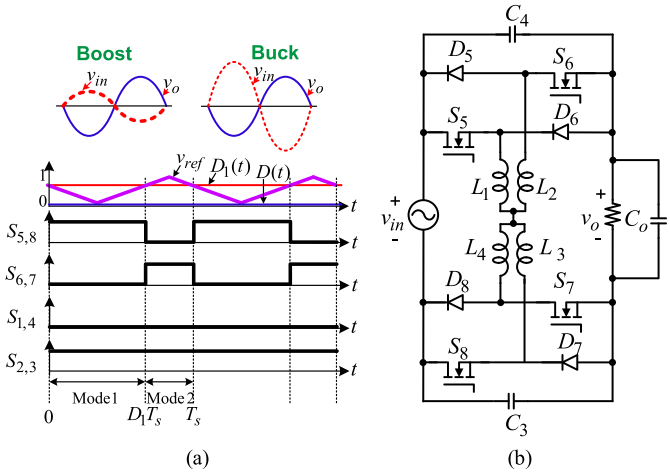

Fig. 7. IBB operation. (a) Gate-signal generation. (b) Equivalent circuit.

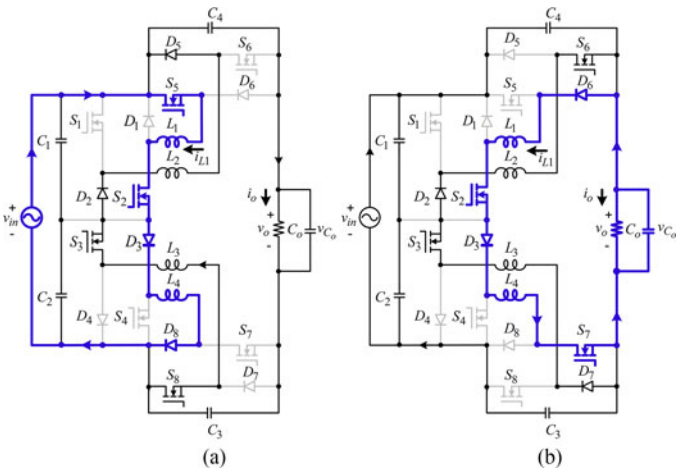

Fig. 8. Operational modes in IBB operation. (a) Mode 1. (b) Mode 2.

B. Mode 2 $[DT_s - T_s]$

As shown in Fig. 6(b), S_1 and S_4 are OFF, and S_2 and S_3 are ON

$$\frac{di_{L2}}{dt} = -\frac{v_o}{2L}. \tag{2}$$

Using (1) and (2), and the volt–second balance condition on L_2 and L_3, the voltage gain (M_A) in NIB is obtained as

$$M_A = \frac{v_o}{v_{\text{in}}} = D. \tag{3}$$

IV. IBB Operation

As shown in Fig. 7, in an IBB operation, S_2 and S_3 are always ON, and S_1 and S_4 are always OFF. In this operation, v_o can be obtained both greater and lower than v_{in}.

A. Mode 1 $[0 - D_1T_s]$

D_1 is defined in Fig. 7(a). As shown in Fig. 8(a). S_5 and S_8 are ON, while S_6 and S_7 are OFF

$$\frac{di_{L2}}{dt} = \frac{v_{\text{in}}}{2L}, \quad \frac{dv_{C_o}}{dt} = -\frac{i_o}{C}. \tag{4}$$

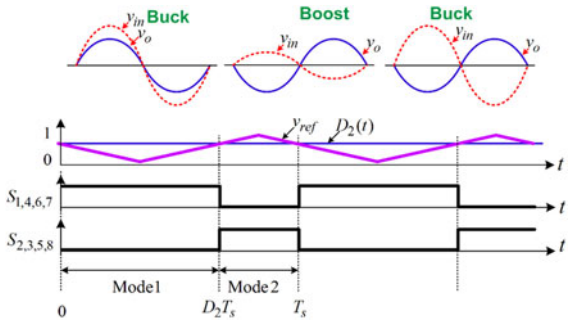

Fig. 9. Gate-signal generation in INIBB operation.

B. Mode 2 $[D_1T_s - T_s]$

As shown in Fig. 8(b), S_5 and S_8 are OFF, while S_6 and S_7 are ON

$$\frac{di_{L2}}{dt} = \frac{v_o}{2L}, \quad \frac{dv_{C_o}}{dt} = -\frac{-i_{L1} - i_o}{C}. \tag{5}$$

The voltage gain (M_B) in an IBB operation is obtained as

$$M_B = \frac{v_o}{v_{\text{in}}} = -\frac{D_1}{1 - D_1}. \tag{6}$$

The negative sign in (6) shows that v_{in} and v_o are out of phase by 180°. Using the ampere–second balance condition on the output capacitor C_o, we obtain

$$i_{L2} = -\frac{i_o}{1 - D}. \tag{7}$$

V. INIBB Operation

The gate-signal generation in an INIBB operation is shown in Fig. 9, where D_2T_s is the ON time of S_1, S_4, S_6, and S_7 in one switching cycle. All the switches are switched at a high frequency. In this operation, an output voltage greater or lower than the input voltage and in phase or out of phase to the input voltage can be obtained. In this operation, the converter has two operating modes in a switching cycle.

A. Mode 1 $[0 - D_2T_s]$

As shown in Fig. 10(a), S_1, S_4, S_6, S_7 are ON, and S_2, S_3, S_5, S_8 are OFF

$$\frac{di_{L2}}{dt} = \frac{v_{\text{in}} - v_o}{2L}, \quad \frac{dv_{C_o}}{dt} = -\frac{i_{L2} - i_o}{C}. \tag{8}$$

B. Mode 2 $[D_2T_s - T_s]$

As shown in Fig. 10(b), S_1, S_4, S_6, S_7 are OFF, and S_2, S_3, S_5, S_8 are ON

$$\frac{di_{L2}}{dt} = -\frac{v_{\text{in}}}{2L}, \quad \frac{dv_{C_o}}{dt} = -\frac{i_o}{C}. \tag{9}$$

The voltage gain (M_C) in an INIBB operation can be obtained as

$$M_C = \frac{v_o}{v_{\text{in}}} = \frac{2D_2 - 1}{D_2}. \tag{10}$$

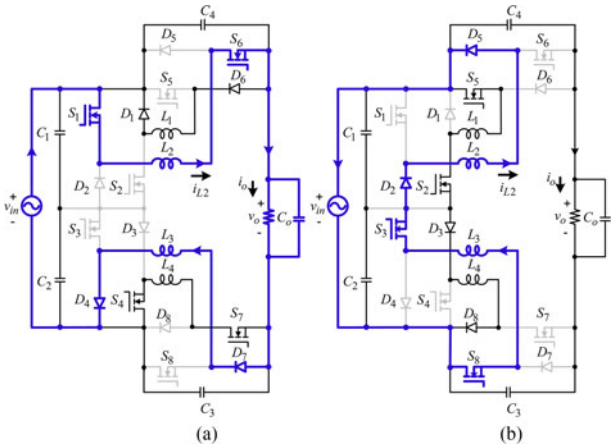

Fig. 10. Operational modes in INIBB. (a) Mode 1. (b) Mode 2.

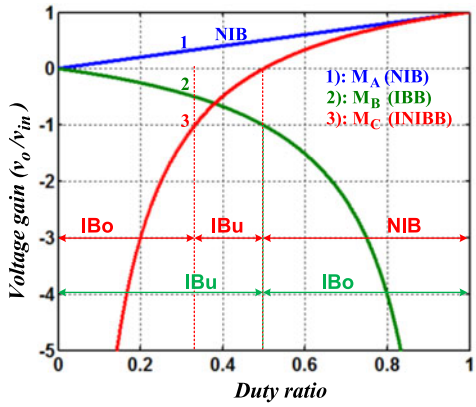

Fig. 11. Voltage gains of the proposed converter.

Using (8) and (9), and the ampere–second balance condition on C_o, we obtain

$$i_{L2} = \frac{i_o}{D_2}. \tag{11}$$

The voltage gains in (3), (7), and (10) are plotted in Fig. 11.

VI. Switch Voltage and Current Stresses

In this section, the voltage and current stresses of the switches are normalized to V_o and I_o, respectively, and the results are expressed in terms of voltage gain (G).

A. NIB Operation

1) Voltage stress

$$\begin{cases} \frac{V^{\text{nib}}_{\text{stress}(S_{1-4})}}{V_o} = \frac{1}{G}, \ \frac{V^{\text{nib}}_{\text{stress}(S_{5,8})}}{V_o} \\ = \frac{1}{G} - 1, \frac{V^{\text{nib}}_{\text{stress}(S_{6,7})}}{V_o} = 0 \end{cases}. \tag{12}$$

2) Current stress

$$\left\{ \frac{I^{\text{nib}}_{\text{stress}(S_{1-4,6,7})}}{I_o} = 1, \ \frac{I^{\text{nib}}_{\text{stress}(S_{5,8})}}{I_o} = 0 \right. . \tag{13}$$

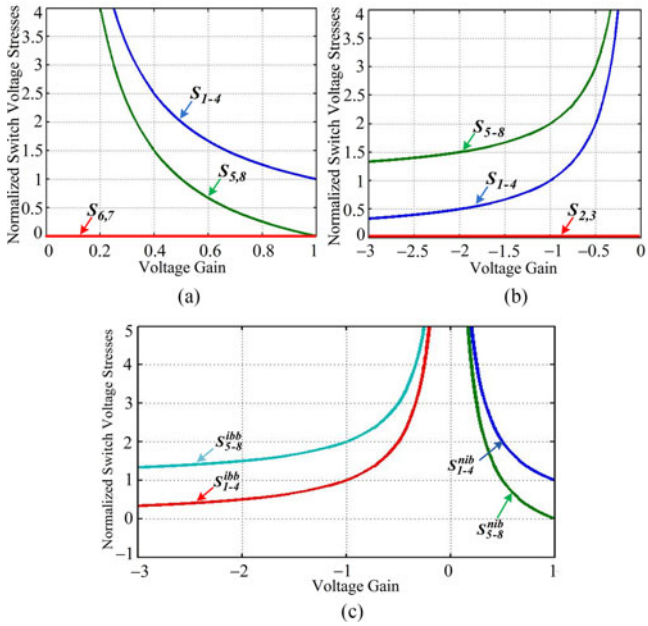

Fig. 12. Normalized switch voltage stresses. (a) NIB operation. (b) IBB operation. (c) INIBB operation.

B. IBB Operation

1) Voltage stress

$$\begin{cases} \frac{V^{\text{ibb}}_{\text{stress}(S_{1,4})}}{V_o} = -\frac{1}{G}, & \frac{V^{\text{ibb}}_{\text{stress}(S_{2,3})}}{V_o} = 0, \\ \frac{V^{\text{ibb}}_{\text{stress}(S_{5-8})}}{V_o} = -\frac{1}{G} + 1. \end{cases} \tag{14}$$

2) Current stress

$$\left\{ \frac{I^{\text{ibb}}_{\text{stress}(S_{2,3,5-8})}}{I_o} = 1 - G, \quad \frac{I^{\text{ibb}}_{\text{stress}(S_{1,4})}}{I_o} = 0 \cdot \right. \tag{15}$$

C. INIBB Operation

1) Voltage stress: The INIBB has NIB and IBB operations. In the NIB operation, the normalized voltage stresses are obtained as

$$\left\{ \frac{V^{\text{inibb(nib)}}_{\text{stress}(S_{1-4})}}{V_o} = \frac{1}{G}, \quad \frac{V^{\text{inibb(nib)}}_{\text{stress}(S_{5-8})}}{V_o} = \frac{1}{G} - 1 \right. . \tag{16}$$

In an IBB operation, G is negative. Thus, by inputting negative G in (16), the normalized voltage stresses are obtained as

$$\begin{cases} \frac{V^{\text{inibb(ibb)}}_{\text{stress}(S_{1-4})}}{V_o} = -\frac{1}{G} \\ \frac{V^{\text{inibb(ibb)}}_{\text{stress}(S_{5-8})}}{V_o} = -\frac{1}{G} + 1. \end{cases} \tag{17}$$

The normalized voltage stresses in (12) and (14) are plotted in Fig. 12(a) and (b), respectively, and the normalized voltage stresses in (16) and (17) are plotted in Fig. 12(c).

1) Current stress

$$\frac{I^{\text{inibb}}_{\text{stress}(S_{1-8})}}{I_o} = 2 - G. \tag{18}$$

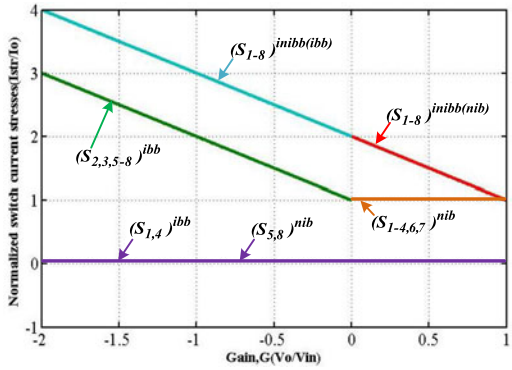

Fig. 13. Normalized switch current stresses.

The normalized switch current stresses in (13), (15), and (18) are plotted in Fig. 13.

Table I compares the NIB, IBB, and INIBB operations.

VII. Parameter Design

In this section, the guidelines for the parameter selection are given.

1) As given in Table II, the peak input voltage $V_{\text{in}} = [110\text{–}200]$ V, the peak output voltage $V_o = 155.5$ V, and the switching frequency $f_{\text{sw}} = 50$ kHz. In the buck operation, $V_{\text{in.max}} = 200$ V, and in the boost operation, $V_{\text{in.min}} = 110$ V.
2) The maximum voltage stress of $S_1 - S_4$ is $V_{\text{in.max}}$, and that of $S_5 - S_8$ is $V_{\text{in.max}} + V_o = 355.5$ V.
3) To obtain the same $V_o = 155.5$ V in various operations, the duty ratios can be obtained as

$$\begin{cases} D_{\min} = \frac{V_o}{V_{\text{in.max}}} = 0.78 \\ D_{1.\min} = \frac{1}{1+\left(\frac{V_{\text{in.max}}}{V_o}\right)} = 0.44 \\ D_{1.\max} = \frac{1}{1+\left(\frac{V_{\text{in.min}}}{V_o}\right)} = 0.58 \\ D_2^{\text{nib}} = \frac{1}{2-\left(\frac{V_o}{V_{\text{in.max}}}\right)} = 0.82 \\ D_2^{\text{ibu}} = \frac{1}{2-\left(-\frac{V_o}{V_{\text{in.max}}}\right)} = 0.36 \\ D_2^{\text{ibo}} = \frac{1}{2-\left(-\frac{V_o}{V_{\text{in.min}}}\right)} = 0.29. \end{cases} \tag{19}$$

4) The peak output current is obtained as

$$I_o = \frac{2P_o}{V_o} = 3.86\,\text{A}. \tag{20}$$

5) Using (19) and (20), the inductor currents in various operations can be obtained as

$$\begin{cases} I_{\text{nib}} = I_o = 3.86\text{ A}, & I^{\text{bu}}_{\text{ibb}} = \frac{I_o}{1-D_{1.\min}} = 6.9\text{ A} \\ I^{\text{bo}}_{\text{ibb}} = \frac{I_o}{1-D_{1.\max}} = 9.2\text{ A}, & I^{\text{nib}}_{\text{inibb}} = \frac{I_o}{D_2^{\text{nib}}} = 4.7\text{ A} \\ I^{\text{ibu}}_{\text{inibb}} = \frac{I_o}{D_2^{\text{ibu}}} = 10.7\text{ A}, & I^{\text{ibo}}_{\text{inibb}} = \frac{I_o}{D_2^{\text{ibo}}} = 13.3\text{ A}. \end{cases} \tag{21}$$

Thus, the maximum current stress is 13.3 A in the IBo mode of an INIBB operation.

6) By considering inductor current ripple $k_i = 25\%$ of the currents in (21), and using (2), (5), (9), (19), and (21), the

TABLE I
COMPARISON OF OPERATION MODES

	Non-inverting buck (NIB)		Inverting buck-boost (IBB)		Inverting and non-inverting buck-boost (INIBB)			
Voltage gain	$M_A = D$		$M_B = -\frac{D}{1-D}$		$M_C = \frac{2D-1}{D}$			
					NIB		IBB	
Voltage stress	$S_1 - S_4$	V_{in}	S_1, S_4	V_{in}	$S_1 - S_4$	V_{in}	$S_1 - S_4$	V_{in}
	S_5, S_8	$V_{in} - V_o$	S_2, S_3	0	$S_5 - S_8$	$V_{in} - V_o$	$S_5 - S_8$	$V_{in} + V_o$
	S_6, S_7	0	$S_5 - S_8$	$V_{in} + V_o$				
Current stress	$S_1 - S_4$, S_6, S_7	I_o	S_2, S_3 $S_5 - S_8$	$\frac{I_o}{1-D_1}$	$S_1 - S_8$	$\frac{I_o(3D_2-1)}{D_2}$	$S_1 - S_8$	$\frac{I_o(1-D_2)}{D_2}$
	S_5, S_8	0	S_1, S_4	0				
Inductor design	$L_{nib} = \frac{V_o \cdot (1 - D_{min})}{2 \cdot f_{sw} \cdot k_i \cdot I_{nib}}$		$L_{ibb}^{bu} = \frac{V_o \cdot (1 - D_{1.min})}{2 \cdot f_{sw} \cdot k_i \cdot I_{ibb}^{bu}}$		$L_{inibb}^{nib} = \frac{V_{in.max} \times \left(1 - D_2^{nib}\right)}{2 \times f_{sw} \times k_i \times I_{inbb}^{nib}}$		$L_{inibb}^{ibu} = \frac{V_{in.max} \times \left(1 - D_2^{ibu}\right)}{2 \times f_{sw} \times k_i \times I_{inbb}^{ibu}}$	
			$L_{ibb}^{bo} = \frac{V_o \times (1 - D_{1.max})}{2 \times f_{sw} \times k_i \times I_{ibb}^{bo}}$				$L_{inibb}^{ibo} = \frac{V_{in.min} \times \left(1 - D_2^{ibo}\right)}{2 \times f_{sw} \times k_i \times I_{inibb}^{ibo}}$	
Capacitor design	$C_{ibb}^{bu} = \frac{I_o \times D_{min}}{f_{sw} \times k_v \times V_o}$		$C_{ibb}^{bu} = \frac{I_o \times D_{1.min}}{f_{sw} \times k_v \times V_o}$		$C_{inibb}^{nib} = \frac{I_o \times \left(1 - D_2^{nib}\right)}{f_{sw} \times k_v \times V_o}$		$C_{inibb}^{ibu} = \frac{I_o \times \left(1 - D_2^{ibu}\right)}{f_{sw} \times k_v \times V_o}$	
			$C_{ibb}^{bo} = \frac{I_o \times D_{1.max}}{f_{sw} \times k_v \times V_o}$				$C_{inibb}^{ibo} = \frac{I_o \times \left(1 - D_2^{ibo}\right)}{f_{sw} \times k_v \times V_o}$	

TABLE II
ELECTRICAL SPECIFICATIONS

Output voltage	155 V_{peak}/ 60 Hz
Input voltage	110–200 V_{peak}/ 60 Hz
Output power	300 W
Switching frequency	50 kHz
MOSFET S_1–S_8	47N60CFD
Diode D_1–D_8	RHRG3060
Inductor L_1–L_4	0.5 mH
Capacitors C_1-C_4	2.2 μF
Output capacitor C_o	6.8 μF
Controller	TMS320F28335

inductances can be obtained as

$$\begin{cases} L_{\rm nib} = \frac{V_o \cdot (1 - D_{\rm min})}{2 \cdot f_{\rm sw} \cdot k_i \cdot I_{\rm nib}} = 0.353 \text{ mH} \\ L_{\rm ibb}^{\rm bu} = \frac{V_o \cdot (1 - D_{1.\rm min})}{2 \cdot f_{\rm sw} \cdot k_i \cdot I_{\rm ibb}^{bu}} = 0.503 \text{ mH} \\ L_{\rm ibb}^{\rm bo} = \frac{V_o \cdot (1 - D_{1.\rm max})}{2 \cdot f_{\rm sw} \cdot k_i \cdot I_{\rm ibb}^{bo}} = 0.283 \text{ mH} \\ L_{\rm inibb}^{\rm nib} = \frac{V_{\rm in.max} \cdot \left(1 - D_2^{\rm nib}\right)}{2 \cdot f_{\rm sw} \cdot k_i \cdot I_{\rm inbb}^{\rm nib}} = 0.306 \text{ mH} \\ L_{\rm inibb}^{\rm ibu} = \frac{V_{\rm in.max} \cdot \left(1 - D_2^{\rm ibu}\right)}{2 \cdot f_{\rm sw} \cdot k_i \cdot I_{\rm inbb}^{\rm ibu}} = 0.478 \text{ mH} \\ L_{\rm inibb}^{\rm ibo} = \frac{V_{\rm in.min} \cdot \left(1 - D_2^{\rm ibo}\right)}{2 \cdot f_{\rm sw} \cdot k_i \cdot I_{\rm inibb}^{\rm ibo}} = 0.235 \text{ mH}. \end{cases} \tag{22}$$

The maximum required inductance is 0.503 mH in the buck mode of an IBB operation.

7) The capacitance of C_o to maintain an output voltage ripple $k_v = 6\%$ of v_o in various operating modes can be obtained as

$$\begin{cases} C_{\rm ibb}^{\rm bu} = \frac{I_o \cdot D_{1.\rm min}}{f_{\rm sw} \cdot k_v \cdot V_o} = 3.65 \ \mu\text{F} \\ C_{\rm ibb}^{\rm bo} = \frac{I_o \cdot D_{1.\rm max}}{f_{\rm sw} \cdot k_v \cdot V_o} = 4.81 \ \mu\text{F} \\ C_{\rm inibb}^{\rm nib} = \frac{I_o \cdot \left(1 - D_2^{\rm nib}\right)}{f_{\rm sw} \cdot k_v \cdot V_o} = 1.49 \ \mu\text{F} \\ C_{\rm inibb}^{\rm ibu} = \frac{I_o \cdot \left(1 - D_2^{\rm ibu}\right)}{f_{\rm sw} \cdot k_v \cdot V_o} = 5.31 \ \mu\text{F} \\ C_{\rm inibb}^{\rm ibo} = \frac{I_o \cdot \left(1 - D_2^{\rm ibo}\right)}{f_{\rm sw} \cdot k_v \cdot V_o} = 5.89 \ \mu\text{F}. \end{cases} \tag{23}$$

The maximum required capacitance is 5.89 μF in the boost mode of an IBB operation. Therefore, the inductance of each inductor is chosen as 0.5 mH, and the capacitance of the output capacitor is chosen as 6.8 μF.

VIII. DVR

Fig. 14(a) shows the proposed DVR, and Fig. 14(b) shows the vectors associated with the voltages. In Fig. 14(a), v_L is the load voltage, $v_{\rm in}$ is the input voltage, v_c is the output voltage of the converter, and V_L, $V_{\rm in}$, and V_c are their peak values. As shown, when $V_{\rm in} < V_L$, the converter generates a positive $V_c = V_L - V_{\rm in}$, which is then added to $V_{\rm in}$ to compensate voltage sag. Similarly, when $V_{\rm in} > V_L$, the converter generates a negative V_c, which is then added to $V_{\rm in}$ to compensate voltage swell. From Fig. 14(a), we obtain

$$v_L = v_{\rm in} + v_C. \tag{24}$$

The output voltages of the converters ($v_o = v_c$) in the NIB, IBB, and INIBB operations are given in (3), (6), and (10), respectively. By using $v_o = v_c$ from these equations in (24), the

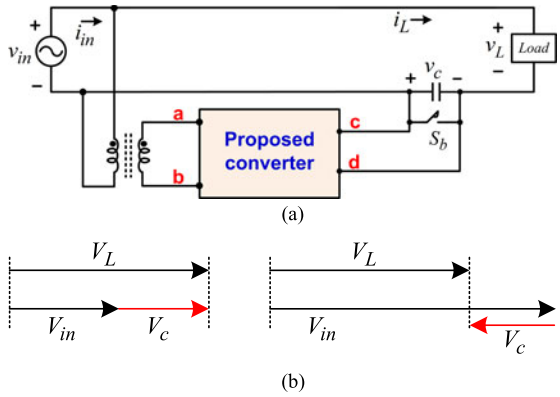

Fig. 14. (a) Proposed DVR. (b) Vectors associated with $V_{\rm in}$, V_c, and V_L.

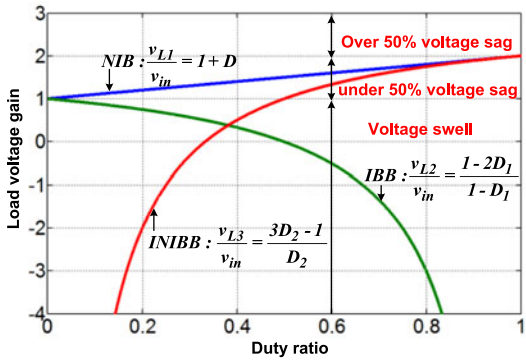

Fig. 15. Load voltage gain versus duty ratio.

load voltage can be obtained as

$$\begin{cases} v_{L1} = (1+D)\cdot v_{\rm in} & \text{(NIB)} \\ v_{L2} = \left(1-\frac{D_1}{1-D_1}\right)\cdot v_{\rm in} & \text{(IBB)} \\ v_{L3} = \left(1+\frac{2D_2-1}{D_2}\right)\cdot v_{\rm in} & \text{(INIBB)}\,. \end{cases} \tag{25}$$

The load voltage gain ($v_L/v_{\rm in}$) from (25) is plotted in Fig. 15. In the NIB operation, only the voltage sag can be compensated, and a maximum of 50% voltage sag can be compensated. In an IBB operation, only the voltage swell can be compensated, and ideally, 100% voltage swell can be compensated. In an INIBB operation, the voltage sag can be compensated for $D_2 > 0.5$, and the voltage swell can be compensated for $D_2 < 0.5$. Ideally, in an INIBB operation, 50% voltage sag and 100% voltage swell can be compensated.

Thus, to compensate both the input voltage sag and swell, two operations can be used: 1) INIBB operation with one control variable D_2, and 2) combined NIB and IBB operation, with two control variables D and D_1.

A. Bypass Mode

In practice, when $V_{\rm in} = 0.9\,V_{\rm ref} - 1.1\,V_{\rm ref}$, the input voltage is considered in the nominal range, and the bypass mode is activated. In the bypass mode, switch S_b in Fig. 14(a) is turned ON and the switches of the converter do not need to be actively controlled. Thus, the gate lock operation is implemented and all

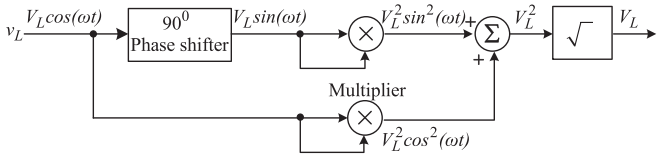

Fig. 16. Peak voltage detector [37].

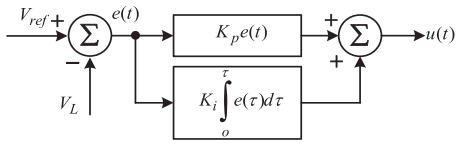

Fig. 17. Block diagram of the PI controller.

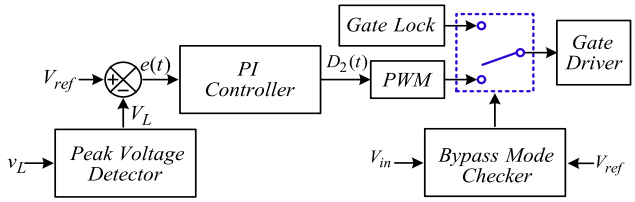

Fig. 18. Block diagram of the closed-loop control in INIBB operation for the DVR.

the converter switches are turned OFF. When $V_{\rm in}$ is not in the range $(0.9\,V_{\rm ref} - 1.1\,V_{\rm ref})$, S_b is turned OFF and the converter is activated and controlled by a closed-loop controller. In closed-loop control, V_L is compared with $V_{\rm ref}$. To obtain V_L from v_L, the widely used peak voltage detector [37] shown in Fig. 16 is used. As shown in Fig. 17, V_L is then compared with $V_{\rm ref}$ to obtain an error signal $e(t)$, which is given into a PI controller. The PI controller compensates $e(t)$ and a control signal $u(t)$ is generated. K_p and K_i are the proportional and integral gains of the PI controller, respectively.

B. INIBB Operation

The control block diagram in an INIBB operation is shown in Fig. 18. V_L is compared with $V_{\rm ref}$ and an error signal $e(t)$ is obtained, which is given into the PI controller. The PI controller compensates the $e(t)$ as shown in Fig. 17, and the control signal $D_2(t)$ is generated. $D_2(t)$ is compared with a carrier signal (see Fig. 9) to obtain the switching signals.

C. NIB and IBB Operations

The control block diagram of NIB and IBB operations is shown in Fig. 19.

1) *Voltage sag compensation:* When $V_{\rm in} < 0.9\,V_{\rm ref}$, the input voltage has a sag. To compensate voltage sag, the controller activates the converter in the NIB operation. In the NIB mode, $D_1(t) = 0$ and $D(t)$ are determined by the PI controller.
2) *Voltage swell compensation:* When $V_{\rm in} > 1.1\,V_{\rm ref}$, the input voltage has a swell. To compensate voltage swell, the controller activates the converter in the IBB mode. In the IBB mode, $D(t) = 1$ and $D_1(t)$ is determined by the PI controller.

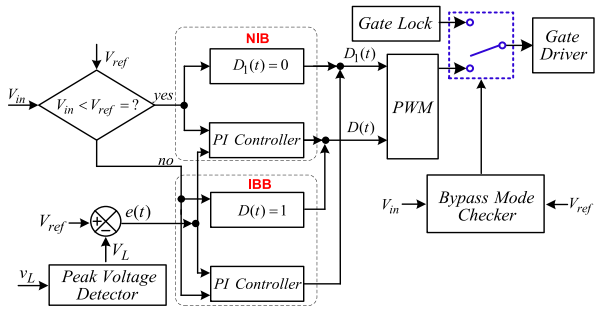

Fig. 19. Block diagram of the closed-loop control in NIB and IBB operations for the DVR.

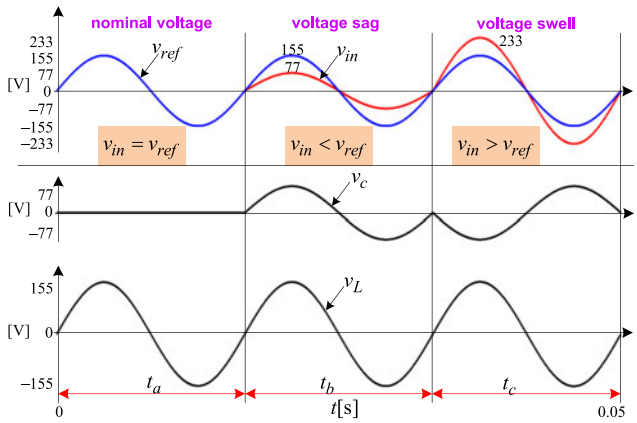

Fig. 20. Simulation results of the DVR.

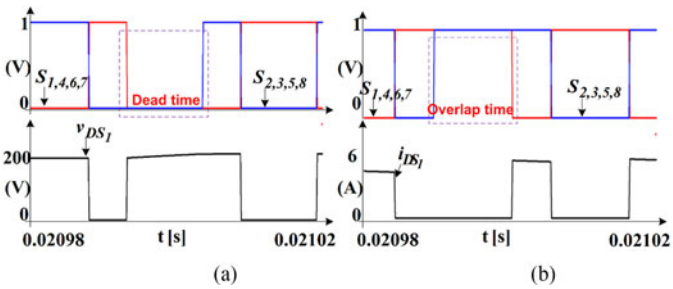

Fig. 21. Simulation results of the proposed converter. (a) Dead-time. (b) Overlap time.

D. Simulation Results of the DVR

Fig. 20 shows the simulation results of the DVR in the INIBB operation. V_{ref} is 155.5 V_{pk}. In t_a, the input voltage is the nominal value; therefore, the bypass mode is activated and $v_c = 0$. In t_b, a voltage sag of 77 V occurs. To compensate the voltage sag, the converter generates $v_c = 77$ V. In t_c, a voltage swell of 77 V occurs. To compensate the voltage swell, the converter generates $v_c = -77$ V.

The load voltage (v_L) is regulated at 155.5 V_{pk}. The simulation results of the proposed converter with dead and overlap times are shown in Fig. 21. As discussed in Section II, the proposed converter has no problem with dead and overlap times in gate signals and, therefore, has no commutation problem.

Table III compares the bipolar voltage gain ac–ac converters.

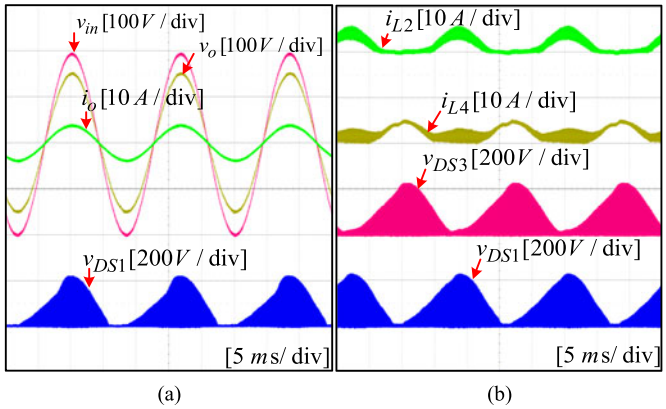

Fig. 22. NIB operation. (a) Input and output voltages, output current and switch voltage. (b) Inductor currents and switch voltages.

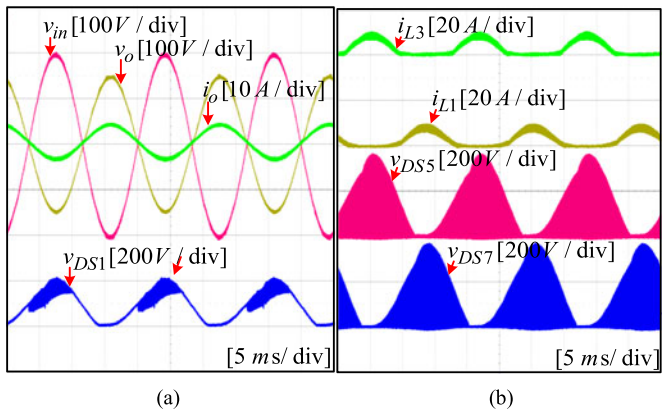

Fig. 23. IBB operation (IBu). (a) Input and output voltages, output current and switch voltage. (b) Inductor currents and switch voltages.

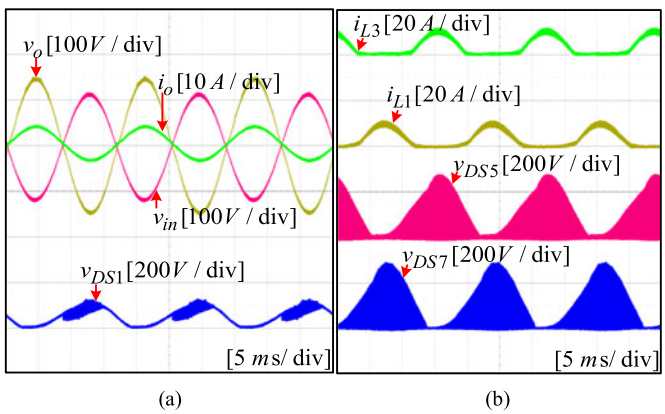

Fig. 24. IBB operation (IBo). (a) Input and output voltages, output current and switch voltage. (b) Inductor currents and switch voltages.

IX. Experimental Results

A 300-W laboratory prototype is fabricated and tested successfully. The design specifications are given in Table I. During the experiments, safe commutation is achieved without using soft commutation techniques and lossy snubbers. The experimental results in Figs. 22–27 are obtained with resistive loads.

TABLE III
COMPARISON BETWEEN THE PROPOSED AND CONVENTIONAL BIPOLAR VOLTAGE GAIN AC–AC CONVERTERS

	Proposed converter (INIBB operation)	[17] IBB operation	[18]	[26]	[14], [15], [38]
Operation	Buck–boost	Buck–boost	Buck–boost	Buck	Buck–boost
Number of switches	8	6	8	6	4
Voltage gain	$\frac{2D_2-1}{D_2}$	$\frac{D}{1-D}$	$\frac{D_1-D_3}{1-D_3}$	$\pm\frac{1}{2}nD$	$\frac{1-D}{1-2D}$
Switch voltage stress	$V_{S1-S4}=V_{\rm in}$, $V_{S5-S8}=$ $\begin{cases} V_{\rm in}-V_o & \text{(NIB)} \\ V_{\rm in}+V_o & \text{(IBB)} \end{cases}$	$V_{S1,S2}=V_{\rm in}$, $V_{S3,S4}=V_{\rm in}+V_o$ $V_{S5,S6}=V_o$	$V_{S1-S4}=V_{\rm in}$, $V_{S5-S8}=V_{\rm in}\times\frac{1-D_1}{1-D_3}$	$V_{S1-S4}=V_{\rm in}$, $V_{S5-S6}=V_o$,	$V_{S1-S4}=\frac{V_{\rm in}}{1-2D}$
Switch current stress	$\begin{cases} \frac{I_o(3D_2-1)}{D_2} & \text{(NIB)} \\ \frac{I_o(1-D_2)}{D_2} & \text{(IBB)} \end{cases}$	$\frac{I_o}{1-D}$	$I_o\times\frac{1-D_1}{1-D_3}$	$I_{S1-S4}=I_{cm}+nI_o$, $I_{S5-S6}=I_s+I_o$	$\frac{I_o}{1-2D}$
Reverse recovery issues of body diode?	no	no	yes	no	yes
Dead or overlap time problem?	no	yes	yes	no	yes
Commutation problem?	no	no	yes	no	yes
Recommended device for switching	MOSFET	MOSFET with series diode	IGBT	MOSFET	IGBT
Power	Suitable for both low and high powers owing to inductive power transfer	Suitable for both low and high powers owing to inductive power transfer	Suitable for both low and high powers owing to inductive power transfer	Suitable for low power owing to capacitive power transfer	Suitable for low power owing to capacitive power transfer

$I_{\rm cm}$ is the circulating current and I_s is the current through the capacitor C_s defined in [26].

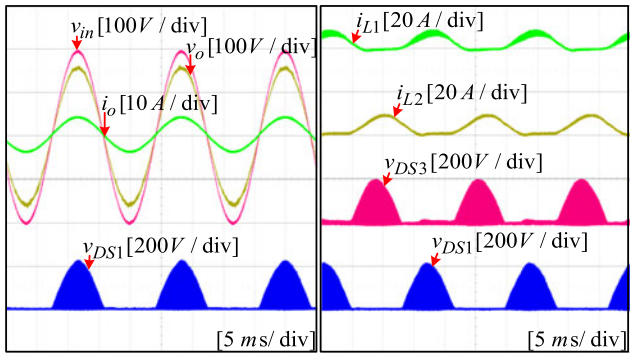

Fig. 25. INIBB operation (NIB). (a) Input and output voltages, output current and switch voltage. (b) Inductor currents and switch voltages.

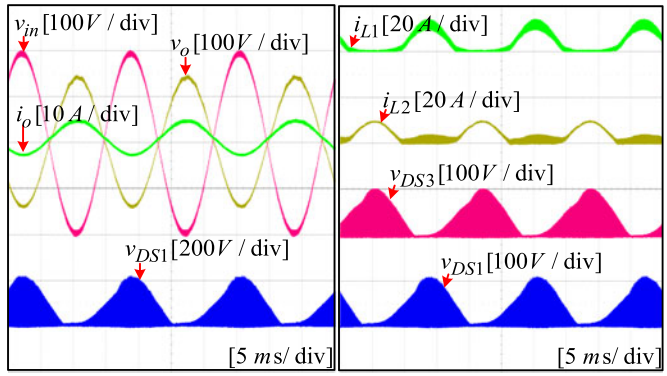

Fig. 26. INIBB operation (IBu). (a) Input and output voltages, output current and switch voltage. (b) Inductor currents and switch voltages.

A. NIB Operation

Fig. 22 shows the waveforms in the NIB operation, when $V_{\rm in}=198\ V_{\rm pk}$, $V_o=155.5\ V_{\rm pk}$, and $D=0.785$. Fig. 22(a) shows the waveforms of the input voltage $v_{\rm in}$, output voltage v_o, output current i_o, and drain–source voltage $v_{\rm DS1}$ of switch S_1. Fig. 22(b) shows the currents i_{L2} and i_{L4} of inductors L_2 and L_4, respectively, and the drain–source voltages $v_{\rm DS1}$ and $v_{\rm DS3}$.

B. IBB Operation

1) *Inverting-buck mode:* Fig. 23 shows the results in the buck mode when $V_{\rm in}=198\ V_{\rm pk}$, $V_o=155.5\ V_{\rm pk}$, and $D_1=0.44$.

2) *Inverting-boost mode:* Fig. 24 shows the results in the boost mode when $V_{\rm in}=113\ V_{\rm pk}$, $V_o=155.5\ V_{\rm pk}$, and $D_1=0.58$.

C. INIBB Operation

1) *NIB mode:* Fig. 25 shows the results in the NIB mode when $V_{\rm in}=198\ V_{\rm pk}$, $V_o=155.5\ V_{\rm pk}$, and $D_2=0.825$.
2) *IBu mode:* Fig. 26 shows the results in the IBu mode when $V_{\rm in}=198\ V_{\rm pk}$, $V_o=155.5\ V_{\rm pk}$, and $D_2=0.3589$.
3) *IBo mode:* Fig. 27 shows the results in the IBo mode when $V_{\rm in}=113\ V_{\rm pk}$, $V_o=155.5\ V_{\rm pk}$, and $D_2=0.296$.

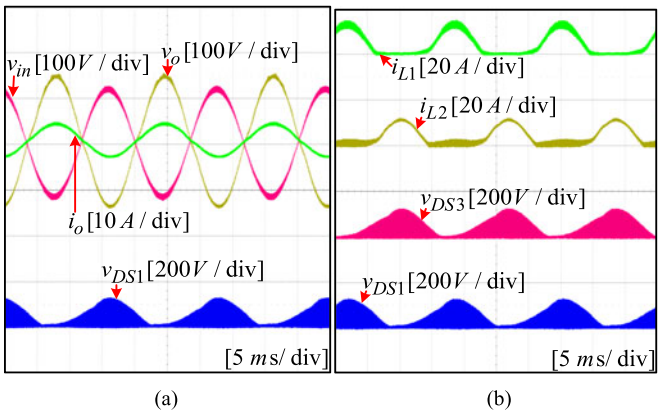

Fig. 27. INIBB operation (IBo). (a) Input and output voltages, output current and switch voltage. (b) Inductor currents and switch voltages.

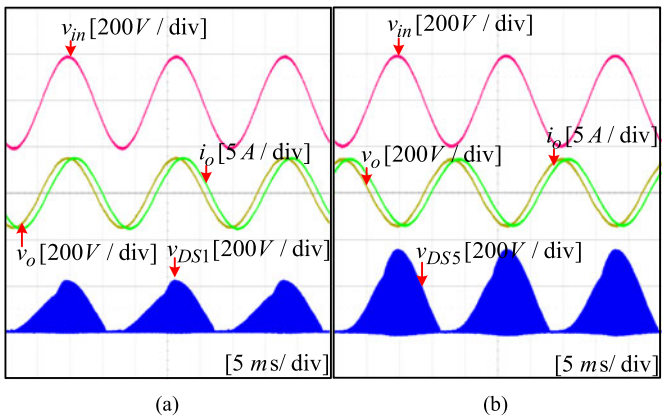

Fig. 28. Experimental results with partially inductive load. (a) NIB operation. (b) IBB operation.

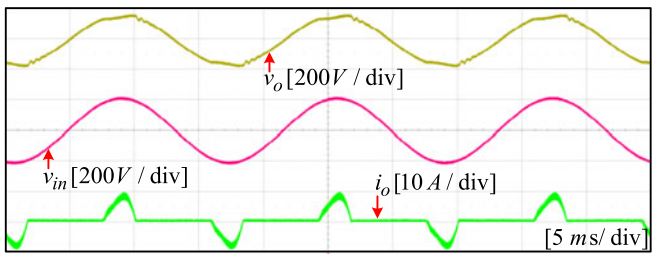

Fig. 29. Experimental results with nonlinear load in NIB operation.

Fig. 28(a) and (b) shows the experimental results with partially inductive load ($R_L = 40\,\Omega$, $L_L = 50$ mH) in NIB and IBB operations, respectively. Fig. 29 shows the experimental results with the nonlinear load in the NIB operation. The nonlinear load consists of a full-wave diode rectifier followed by a dc-link capacitor of 470 μF.

To verify the operation of the proposed DVR, the experimental results under the input voltage swell, voltage sag, and nominal voltage are provided in Fig. 30. The load voltage v_L is regulated at 155 $V_{\rm pk}$.

1) *Voltage swell:* In Fig. 30(a), $(V_{\rm in} = 233\ V_{\rm pk}) > (V_L = 155\ V_{\rm pk})$, and $V_{\rm in}$ has a voltage swell of 78 $V_{\rm pk}$. To compensate voltage swell, the converter is activated in the inverting operation and switch (S_b) in Fig. 14(a) is turned OFF. The converter produces the inverted $V_c = 78\ V_{\rm pk}$, which is then added to $V_{\rm in} = 233\ V_{\rm pk}$, and $V_L = 155\ V_{\rm pk}$ is obtained.
2) *Voltage sag:* In Fig. 30(b), $(V_{\rm in} = 77\ V_{\rm pk}) < (V_L = 155\ V_{\rm pk})$, and $V_{\rm in}$ has a voltage sag of 78 $V_{\rm pk}$. To compensate the voltage sag, the converter produces a non-inverted $V_c = 77\,V_{\rm pk}$, which is then added to $V_{\rm in} = 77\ V_{\rm pk}$, and V_L is regulated at 155 $V_{\rm pk}$.
3) *Nominal voltage:* As shown in Fig. 30(c), when $V_{\rm in} = 155\ V_{\rm pk}$ (nominal value), switches $(S_1$–$S_8)$ are turned OFF, and S_b is turned ON to bypass $v_{\rm in}$ to v_L.

As shown in Fig. 30, for all the three cases, V_L is regulated at 155 $V_{\rm pk}$, which verifies the operation of the proposed DVR.

Fig. 31 shows the measured efficiencies, and Fig. 32 shows the measured total harmonic distortion (THD) of the output voltage.

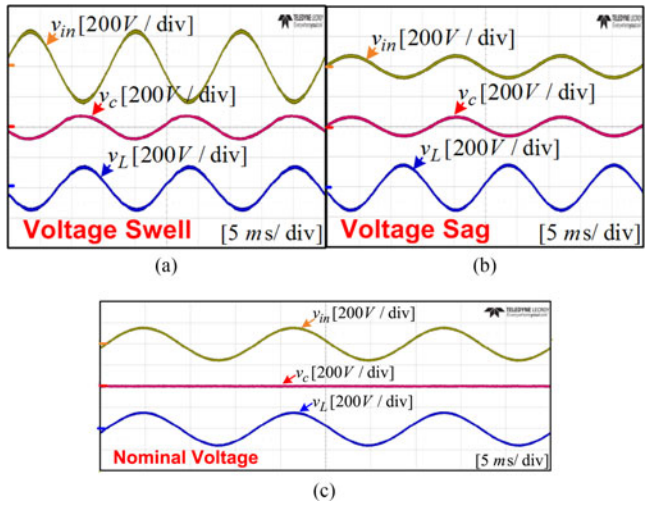

Fig. 30. Experimental results of the proposed DVR.

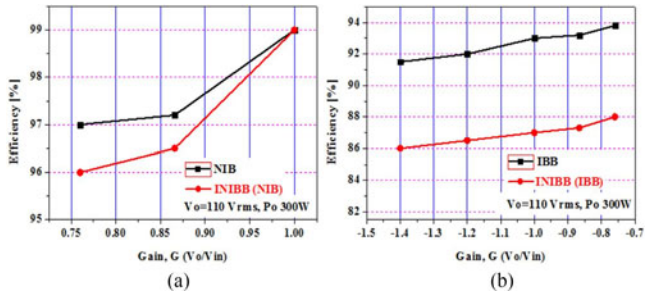

Fig. 31. Measured efficiencies. (a) Positive G. (b) Negative G.

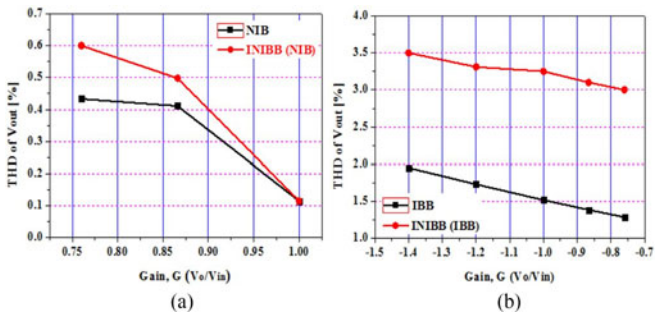

Fig. 32. Measured THD of the output voltage. (a) Positive G. (b) Negative G.

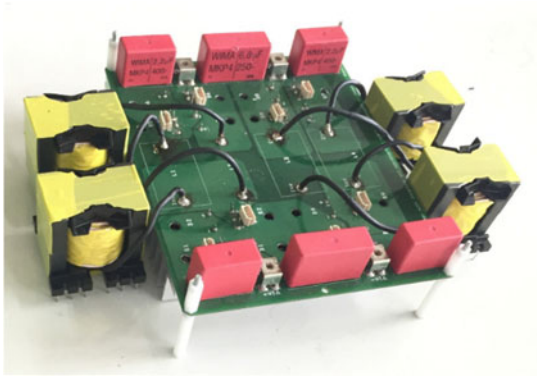

Fig. 33. Prototype photo.

The photo of the hardware prototype is shown in Fig. 33. In all the experimental results, the inductor currents are unidirectional, which confirmed that the body diodes are disabled to conduct.

X. Conclusion

In this paper, a novel buck–boost ac–ac converter is proposed. It combined the operations of NIB and IBB converters in one structure. Similar to the buck converter, it has a NIB operation, and similar to an IBB converter, it has an IBB operation. In addition, it has an extra operation, in which the output voltage higher or lower than the input voltage that is in phase or out of phase with the input voltage can be obtained. Thus, the proposed converter can compensate both voltage sag and swell when used in a DVR.

The basic unit of the proposed converter is a unidirectional buck circuit; therefore, it has no short-circuit and open-circuit problems. It has no commutation problems and does not require lossy snubbers and/or soft commutation strategies for operation. Furthermore, it can utilize MOSFETs without their body diodes conducting and without reverse recovery issues and relevant losses. A detailed analysis of the proposed converter and the DVR has been presented and validated by experimental results.

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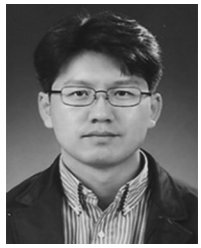

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