Active Cancelation of Equivalent Grid Impedance for Improving Stability and Injected Power Quality of Grid-Connected Inverter Under Variable Grid Condition

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***Abstract*—An active grid impedance cancelator using the concept of series active filter to suppress the effect of the grid disturbance and stabilize the single-phase grid-connected inverters with an inductive–capacitive–inductive filter operating under variable grid condition is presented. Harmonic interaction between the inverter and the grid is thereby avoided owing to the cancelation of equivalent grid impedance. More importantly, the impedance cancelator offers an active damping function to ease the heavy burden of the inverter control, such as power control, phase locked loop, current regulation, impedance shaping, etc. The impedance cancelator is a full-bridge dc–ac converter having no passive inductive–capacitive filter. It is connected in series with the inverter output and is operated as a negative virtual grid impedance. As the volt-ampere rating of the impedance cancelator is low, the efficiency of the entire system is not sacrificed. Starting with the impedance-based analytical modeling method, the basic principle of equivalent grid impedance cancelator is derived and studied. Then, the digital control strategy and the modeling of equivalent grid impedance cancelator are examined. The experimental results of a prototype cancellator for a single-phase inverter are favorably compared with theoretical predictions.**

***Index Terms*—Grid impedance cancelator, impedance-based stability criterion, inductive–capacitive–inductive (*LCL*) filter, negative virtual grid impedance, single-phase inverters, weak grid.**

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I. Introduction

To offer a high degree of modularity, scalability, adaptability, maintainability, and autonomic behaviors, large number of distributed power generation (DPG) units have been expected to deliver energy to the distributed network via multiple parallel-connected dc–ac converters [1]–[3]. A simplified single-phase photovoltaic (PV) DPG architecture is shown in Fig. 1, where equivalent grid impedance mainly consists of line impedance and power transformer leakage impedance. The equivalent grid impedance viewed by single inverter will vary widely as the number of grid-connected inverters at the point-of-common-coupling (PCC) changes [4], [5].

Grid-connected inverters are generally voltage source converters with an output power filter. Among various types of filters, third-order inductive–capacitive–inductive (*LCL*) filter has become popular, as it requires smaller reactive elements than the classical inductive (*L*) and inductive–capacitive (*LC*) filters [6], [7]. For these types of inverters, the ac output current regulation faces a critical challenge of filter resonance. Thus, many prior arts, such as passive and active damping techniques, have been proposed to tackle filter resonance. Among them, active damping techniques are preferable, as they do not cause extra power dissipation and can achieve resonance suppression flexibly. Active damping performance strictly relies on the ratio between the filter resonant frequency and the sampling frequency due to the digital delay in the digitally-controlled inverter [8], [9]. As the filter resonant frequency will vary with the changes of the equivalent grid impedance, it would give challenges to develop an effective active damping function that can ensure the operational stability of the inverter both in stiff- and weak-grid conditions. Continuous research efforts have been made to alleviate the impact of equivalent grid impedance variation and the digital delay on the system performance. Many improved damping methods have been developed to increase the robustness of current controlled inverters, such as hybrid damping [10], [11], damping function with reduced digital delay [8], [12], adaptive cascaded notch filter [13], active damper connected in shunt at the PCC [14], fast boundary control with inherent damping property [15], [16], etc. Alternatively, grid-voltage feedforward mechanism is popularly integrated into the inverter control function so as to

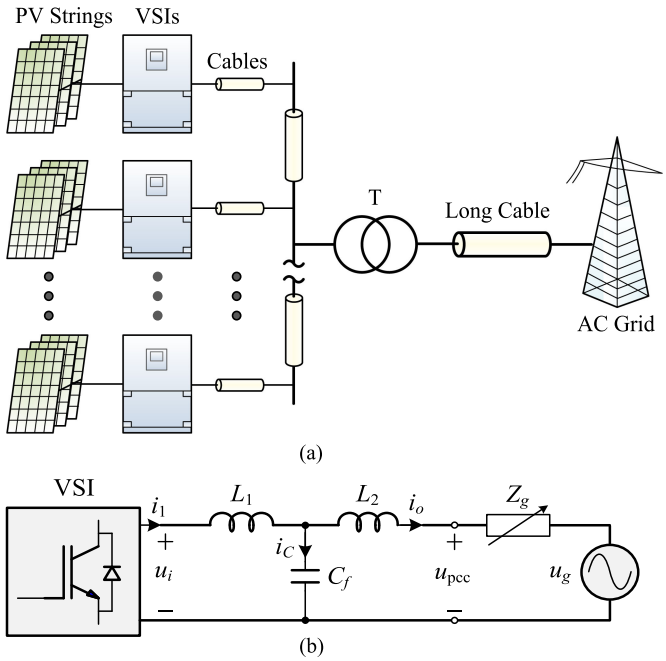

Fig. 1. Typical single-phase PV DPG system. (a) System configuration. (b) Equivalent single inverter.

alleviate the effect of variable grid impedance and suppress grid harmonic distortion [17], [18]. Due to the effect of the digital delay and the noise amplification of the differentiator, previous work has already shown that grid voltage feedforward would diverse the system stability with the increase in the equivalent grid impedance. In principle, good system performance can be assured as long as the equivalent grid impedance can be accurately estimated [4]. However, its accuracy is inevitably affected by the harmonics generated from other inverters at the PCC [15].

On the other hand, a more complicated aspect is that DPG inverters installed at the same PCC are coupled with each other due to the grid impedance and would lead to harmonic interaction and current circulation among them [5], [19], [20]. Moreover, multiple reactive elements in the inverter output filters, such as filtering capacitive and inductive components, as shown in Fig. 1(b), could also exhibit multiple resonant frequencies. It is due to the existence of the grid impedance. Thus, the system stability will be subject to multiple resonant behavior rather than the single resonance caused by the local filter. Such phenomenon has already been reported in [19]. It reveals that, due to harmonic interaction among multiple DPG inverters and possible mismatch among the output impedances of DPG inverters and the equivalent grid impedance, the DPG system could be dynamically unstable. It is, therefore, vital to develop effective modeling and analysis on the harmonic stability problem of the DPG system. A well-established technique to analyze such harmonic stability problem is by the impedance-based stability criterion: The ratio of the inverter output impedance to the load input impedance must satisfy Nyquist stability criterion in order for the DPG system to be stable [21]. The conceptual scenario is to represent the inverter by a Norton's equivalent circuit in the form of a stable equivalent current source in parallel with an output impedance, while the grid can be represented by its input impedance [22]. In [20], the output and input impedance at each node of the feeder in a trunk-based network is calculated to explore the quasi-resonance among numerous DPG inverters and the grid. The design constraints to mitigate harmonic interaction can be guided as the impedance limits at each node of the feeder. In [23], multiple resonance problem in a parallel-inverter-based microgrid is studied with Norton's equivalent circuit. The multiple resonances are identified as internal resonance caused by the local filter, parallel resonance with other paralleled inverters, and series resonance with the grid. In addition, Agorreta *et al*. [5] proposes an equivalent impedance model to incorporate numerous DPG inverters into a single unit based on the hypothesis that all paralleled inverters are assumed to be equal. Recently, Lu *et al*. [24] specifies that the modeling and analysis methods are based on current separation scheme. It can characterize the interactive current between DPG inverters and common current to the grid on the assumption that all the inverter parameters are identical.

The paper presents an *LCL* filter-based single-phase grid-connected inverter with active cancelation of equivalent grid impedance based on the concept of series active filter. The cancelator consists of a bidirectional dc–ac converter and has the following features:

1) no need to use extra passive *LC* filtering elements;
2) cancelation of the effect of grid impedance;
3) strong harmonic suppression against grid disturbance; and
4) active damping function to ease the burden of the inverter current control.

The reshaped inverter with an *LCL* filter appears as a well-damped one without equivalent grid impedance. This paper is organized as follows. In Section II, based on the concept of impedance-based stability criterion, the basic principle of the grid impedance cancelator is introduced. Then, the proposed system configuration is described in Section III. The control strategy and the modeling of the grid impedance cancelator are examined carefully in Section IV-A prototype cancelator for a single-phase inverter has been built and evaluated. Its steady-state and transient behaviors under different grid conditions are discussed in Section V. The conclusion follows in Section VI.

II. Principle of the Grid Impedance Cancelator

Impedance-based stability analysis has been becoming popular to assess the small-signal stability of the DPG inverter system. In this section, detailed description of the impedance-based stability method for current-controlled single-phase grid-connected inverters will be reviewed. Then, the basic principle of the grid impedance cancelator will be derived and studied.

A. Overview of the Impedance-Based Stability Criterion

Based on the impedance-based stability criterion, the current-controlled inverter in Fig. 1(b) is represented as an small-signal current source ΔI_s in parallel with the output impedance Z_o, and the grid appears as a voltage source ΔU_g in series with the equivalent grid impedance Z_g, as shown in Fig. 2. The equivalent grid impedance mainly consists of line impedance, local load,

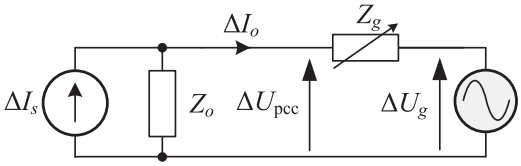

Fig. 2. Small-signal representation of a grid-connected inverter system.

and power transformer leakage impedance and will vary widely as the number of grid-connected inverters connected to the PCC changes.

Assuming that both the grid voltage source u_g and the equivalent inverter current source i_s are stable, the injected current i_o is then expressed as [22]

$$\Delta I_o(s) = \left[\Delta I_s(s) - \frac{\Delta U_g(s)}{Z_o(s)}\right] \cdot \frac{1}{1 + Z_g(s)/Z_o(s)} \quad (1)$$

where only if the ratio of the equivalent grid impedance (Z_g) to the inverter output impedance (Z_o), $Z_g(s)/Z_o(s)$, meets the Nyquist stability criterion [21], the current-controlled grid-connected inverter becomes stable. As the bandwidth of the phase locked loop (PLL, typically less than 50 Hz) is significantly lower than the bandwidth of the inner current loop (typically higher than 1 kHz), the PLL effect on the inverter output impedance is commonly neglected in grid-connected inverter [25]. Considering that the grid impedance is unknown and variable, the inverter output impedance is usually considered to be an important index for controlling the inverters. Thus, extensive research efforts have been made to enhance the output impedance in the inverter controller designs [26], [27]. Nevertheless, the inverter output impedance is still subject to the output power filter design and the control bandwidth of the inverter.

B. Principle of the Grid Impedance Cancelator

To counteract the effect of the grid impedance on the injected current based on (1) and the assumption stated before, it is known that either infinite increase in the inverter output impedance (Z_o), as shown in Fig. 3(a), or cancelation of equivalent grid impedance (Z_g), as presented in Fig. 3(b), would make the Nyquist stability criterion always satisfy and keep the system stable regardless of the grid impedance. Thus, with infinite increase in the inverter output impedance, the reshaped grid

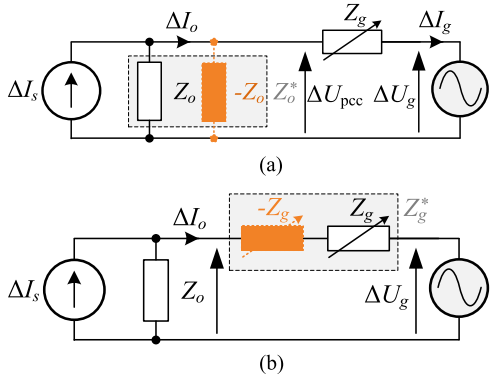

Fig. 3. Illustration of the interactive decoupling between the inverter and the grid. (a) Infinite increase of the inverter output impedance. (b) Cancelation of equivalent grid impedance.

current i_g is modified into

$$\Delta i_g(s)|_{Z_o^*(s)\to\infty} = \left[\Delta I_s(s) - \frac{\Delta U_g(s)}{Z_o^*(s)}\right] \cdot \frac{1}{1 + Z_g(s)/Z_o^*(s)} = \Delta I_s(s). \quad (2)$$

With the cancelation of equivalent grid impedance, the reshaped injected current i_o is

$$\Delta i_o(s)|_{Z_g^*(s)\to 0} = \left[\Delta I_s(s) - \frac{\Delta U_g(s)}{Z_o(s)}\right] \cdot \frac{1}{1 + \frac{Z_g^*(s)}{Z_o(s)}} = \Delta I_s(s) - \frac{\Delta U_g(s)}{Z_o(s)}. \quad (3)$$

Then, the effect of the grid impedance has been decoupled as described both in (2) and (3).

Taking the single loop direct control strategy for the single-phase grid-connected inverter with an *LCL* filter for instance, the corresponding control block diagrams in (2) and (3) can be drawn, as shown in Fig. 4, in which the original inverter output impedance Z_o is calculated as Eq. (4) shown at the bottom of this page, and the considered stable current source i_s given in (2) and (3) is written as Eq. (5) shown at the bottom of this page, where Z_1, Z_2, and Z_C represent the inverter-side inductor, grid-side inductor, and filter capacitor of the *LCL* filter, respectively, G_C and G_d are the digital current controller and the digital delay, and $\Delta I_{\rm ref}$ is the reference command.

Detailed derivation of Fig. 4(a) is given in the Appendix A. By converting the impedance insertion of Fig. 4 into equivalent active circuits, both infinite increase in the output impedance and

$$Z_o(s)|_{\Delta I_s(s)=0,\ Z_g(s)=0} = \left.\frac{\Delta U_g(s)}{\Delta I_o(s)}\right|_{\Delta I_s(s)=0,\ Z_g(s)=0} = \frac{Z_1(s)Z_2(s) + Z_1(s)Z_C(s) + Z_2(s)Z_C(s) + Z_C(s)G_C(s)G_d(s)}{Z_1(s) + Z_C(s)} \quad (4)$$

$$\Delta I_s(s) = \frac{Z_C(s)G_C(s)G_d(s)}{Z_1(s)Z_2(s) + Z_1(s)Z_C(s) + Z_2(s)Z_C(s) + Z_C(s)G_C(s)G_d(s)}\Delta I_{\rm ref}(s) \quad (5)$$

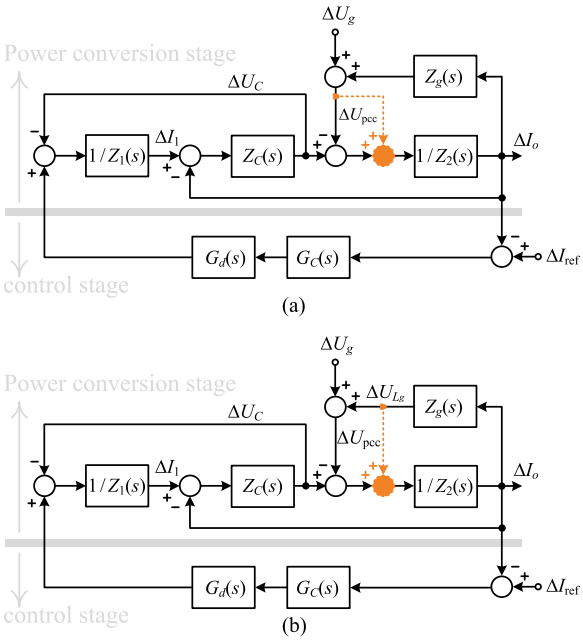

Fig. 4. Block diagram of the decoupled *LCL* filter-based grid-connected inverter. (a) Infinite increase of the inverter output impedance. (b) Cancelation of equivalent grid impedance.

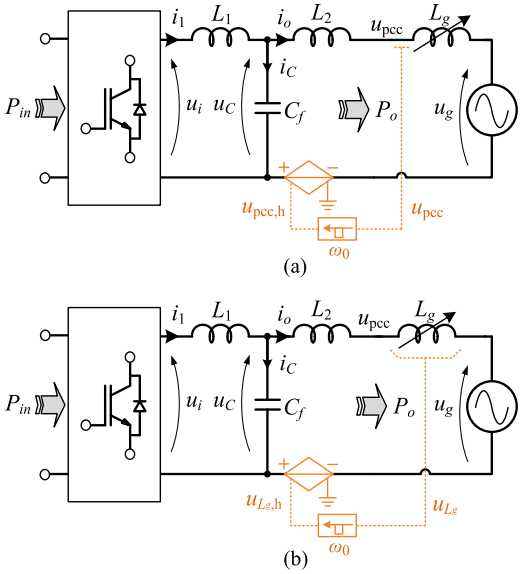

Fig. 5. Illustration of the grid decoupling mechanism. (a) Infinite increase of the inverter output impedance. (b) Cancelation of equivalent grid impedance.

cancelation of equivalent grid impedance, as shown in Fig. 3, could be achieved by the voltage-controlled voltage source in series at the inverter output, as shown in Fig. 5, where the notch filter with the center frequency ω_0 is used to eliminate the dominant line frequency (ω_0) component in practical implementation, and $u_{\mathrm{pcc},h}$ and $u_{L_g,h}$ represent the harmonic voltage at the PCC and across the equivalent grid impedance, respectively. To simulate the worst case scenario and simplify the analysis, the resistive part at the power filter and the grid impedance is neglected in Fig. 5 and in the following sections. As the voltage across the equivalent grid impedance u_{L_g} is not measurable, the

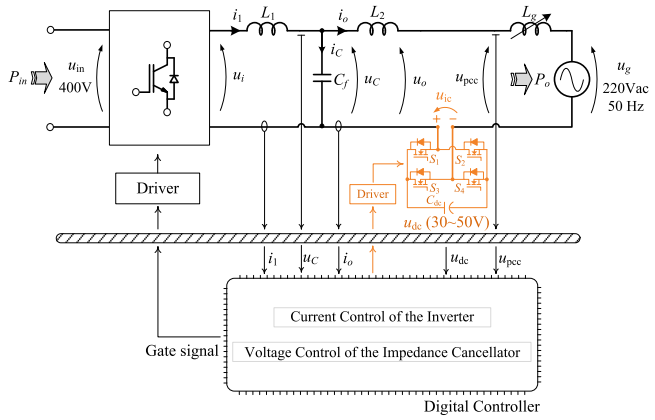

Fig. 6. Proposed single-phase inverter system configuration with the grid impedance cancelator.

cancelation of equivalent grid impedance cannot be achieved directly, as shown in Fig. 5(b).

The only difference between Fig. 5(a) and (b) is found to reshape the impedance by locating different measured voltages u_{pcc} and u_{L_g} in which

$$\Delta U_{\mathrm{pcc}}(s) = \Delta U_{L_g}(s) + \Delta U_g(s) \tag{6}$$

where the pure grid voltage source ΔU_g has no effect on the inverter stability. Thus, infinite increase in the inverter output impedance can be considered as the cancelation of equivalent grid impedance plus the harmonic suppression at the grid voltage source u_g, which can be observed by comparing (2) and (3). Furthermore, from a stability point of view, both of them can be achieved based on the same equivalent active circuit in Fig. 5(a). Because the unity-gain PCC voltage is feedforwarded to realize grid decoupling function, as shown in Fig. 5(a), the cancelation of grid impedance is independent on the circuit parameters of the inverter.

III. System Configuration With the Grid Impedance Cancelator

The *LCL* filter-based current-controlled single-phase grid-connected inverter with the proposed grid impedance cancelator for typical PV application is shown in Fig. 6, where the dc bus voltage of the full-bridge inverter is about 400 V, if the inverter is connected to a 220 Vac/50 Hz power grid. The grid impedance cancelator, implemented by a full bridge dc–ac converter without passive filtering elements, is connected in series at the inverter output, which aims to cancel the grid impedance and eliminate the harmonic voltage at the inverter output voltage u_o as analyzed in Section II. Although four switching devices are used in the impedance cancelator, each switching device only needs to sustain a very low dc capacitor voltage u_{dc} ranging around 30–50 V. That is because the mean output voltage of the impedance cancelator is the small harmonic voltage at the PCC, $u_{\mathrm{pcc},h}$, as described in Section II.

Some issues related to the implementation of the cancelation are addressed. First, the required voltage rating of the switching devices used in the cancelator is much lower than that in the in-

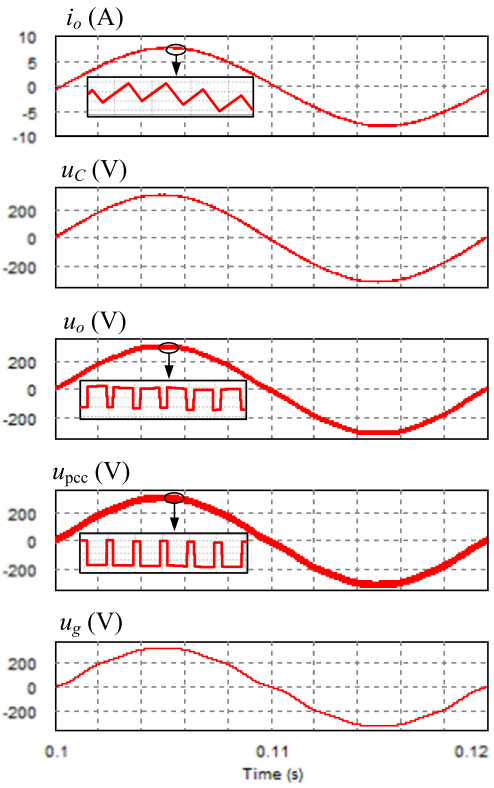

Fig. 7. Key waveforms of the proposed inverter system.

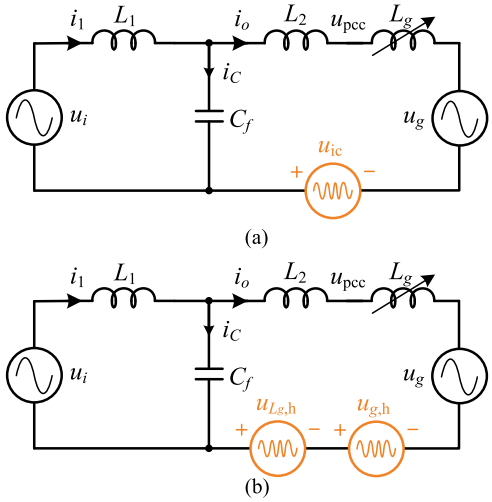

Fig. 8. Simplified equivalent circuit of the inverter-grid system.

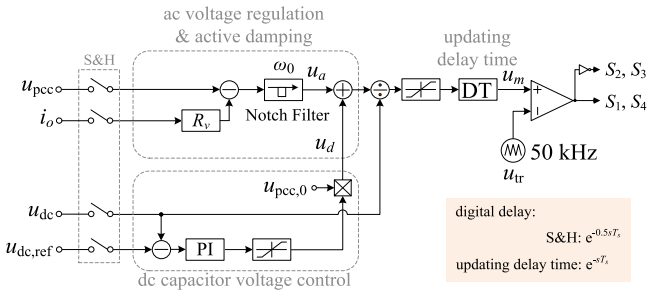

Fig. 9. Control block diagram of the grid impedance cancelator.

verter. As the on-state resistance of MOSFETs increases with the increase in the blocking voltage rating [28], low-voltage MOSFETs of low on-state resistance used in the cancelator result in small conduction loss. The switching loss of low-voltage MOSFETs is also small. Second, the core loss of the grid-side filtering inductor L_2 brought in by the much higher frequency switching operation of MOSFETs $S_1 \sim S_4$ than the dominant inverter switching components, can be neglected because of very low switching ripple current overlaid at the injected current i_o, as shown in Fig. 7. Fig. 7 shows the key waveforms of the proposed inverter system with the grid impedance cancelator.

The simplified equivalent circuit of the proposed inverter system is shown in Fig. 8(a), where the output voltage of the impedance cancelator $u_{\rm ic}$ equals the harmonic voltage at the PCC $u_{{\rm pcc},h}$ at the steady state. u_{ic} is composed of harmonic voltage of the grid voltage $u_{g,\rm h}$ and that across the equivalent grid impedance $u_{L_g,\rm h}$, as shown in Fig. 8(b), in which the injected harmonic voltage $-u_{L_g,\rm h}$ is used to cancel the effect of equivalent grid impedance and suppressing harmonic disturbances from other local DPG systems at the PCC.

IV. Digital Control Strategy of the Grid Impedance Cancelator

A. AC Voltage Regulation

Since the compensated ac voltage u_{ic} is the direct output voltage of the dc–ac converter with no attenuation of passive *LC* filter, as shown in Fig. 6, the unity gain-based harmonic voltage at the PCC is directly feedforwarded into the modulator so as to generate equivalent ac output voltage, as presented in Fig. 9, where the notch filter with the center frequency ω_0 is used to eliminate the dominant line frequency component of the PCC voltage, and T_S is the sampling cycle in synchronous with the switching operation.

B. Active Damping Function

As shown in Fig. 8(a), three equivalent voltage sources are combined together through the third-order filter cascading with the equivalent grid impedance. To suppress the effect of the filter resonance on the inverter performance, active damping function is usually integrated into the current control loop of the inverter, which is restricted by the dominant digital delay and interacts with the inverter current control loop. Considering that the digital delay in the impedance cancelator is significantly decreased due to a much higher sampling rate than that in the inverter control, active damping function can also be integrated into the impedance cancelator to widen its effective range and ease the burden of the inverter current control. The implementation of active damping function can be realized through simple proportional harmonic injected current feedback, as shown in Fig. 9, where R_v represents the gain of the active damping function or the virtual resistance.

The expected value of virtual resistance R_v can be designed as

$$R_v = \frac{\omega_{r\_up} L_2 + \omega_{r\_down} (L_1 + L_2)}{2} \tag{7}$$

where $\omega_{r\_down} = \sqrt{\frac{1}{L_1 C_f}}$ and $\omega_{r\_up} = \sqrt{\frac{L_1+L_2}{L_1 L_2 C_f}}$.

Detailed derivation of (7) is given in the Appendix B.

C. DC Capacitor Voltage Control

In the former discussion, the dc capacitor voltage of the cancelator is assumed to be constant. In practice, the dc capacitor voltage should be regulated at a reference value (i.e., $u_{dc,ref} = 30$ V) with a closed-loop feedback control [29]. As shown in Fig. 9, the dc capacitor voltage is subtracted with the reference value $u_{dc,ref}$, and the error is fed into a proportional-integral (PI) controller. The output signal of the PI controller u_d is then multiplied with a sinusoidal signal in phase with the line voltage, and the generated signal is added to the modulating information. Thus, the dc capacitor voltage will be regulated by changing the real power flowing into the capacitor. The sinusoidal signal in Fig. 9 is obtained through the PLL in the inverter controller.

As the dc–ac converter is bidirectional, it absorbs high-frequency components to emulate the resistive component R_v and counteract the effects of the grid impedance on the current-controlled inverter. The absorbed high-frequency power is then transformed to low-frequency one by forming a voltage in phase with the line voltage, as shown in Fig. 9, so as to sustain the voltage u_{dc} across the capacitor C_{dc} at the reference one, $u_{dc,ref}$. The absorbed real power is to compensate the power dissipation of the entire system and emulate the resistive component R_v.

D. System Modeling

By combining the ac voltage regulation and the active damping function, as shown in Fig. 9, the corresponding generated output information u_a will be

$$\Delta U_a(s) = G_{NF}(s)\, e^{-0.5sT_S} \left[\Delta U_{pcc}(s) - R_v\, \Delta I_o(s)\right] \tag{8}$$

where $e^{-0.5sT_S}$ is the transfer function of the sampling-and-holding unit, and $G_{NF}(s)$ represents the notch filter written as

$$G_{NF}(s) = \frac{s^2 + \omega_0^2}{s^2 + 2\omega_b s + \omega_0^2} \tag{9}$$

in which the center line frequency ω_0 is generated from the PLL in the inverter controller and the band ω_b determines the response time of the filter. The generated output signal based on the dc capacitor voltage feedback loop is calculated as

$$\Delta U_d(s) = \Delta U_{pcc,0}(s)\, G_{PI}(s)\, e^{-0.5sT_S} \times \left[\Delta U_{dc}(s) - \Delta U_{dc,ref}(s)\right] \tag{10}$$

where $G_{PI}(s)$ is the transfer function of PI controller and the sinusoidal signal $\Delta U_{pcc,0}$ is used to force the dominant line-frequency component at the ΔU_d. Thus, the cutoff frequency of PI controller should be designed to be much lower than the line frequency.

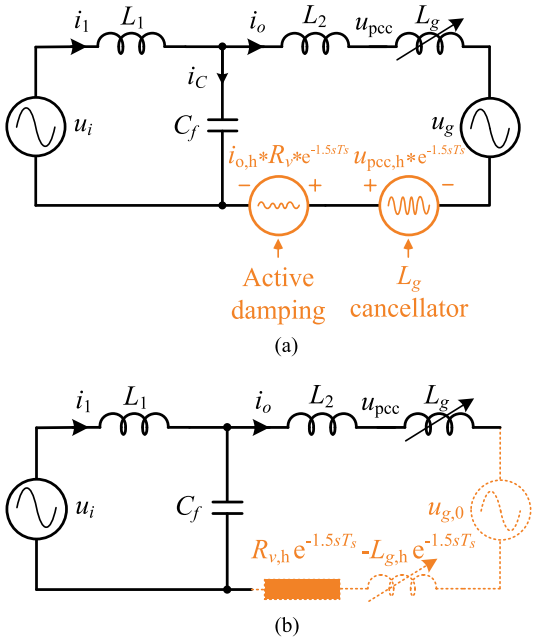

Fig. 10. Equivalent circuit of the grid impedance cancelator. (a) Equivalent voltage source. (b) Equivalent impedance.

By integrating (8) and (10), the modulating signal ΔU_m is derived as

$$\Delta U_m(s) = \frac{\Delta U_a(s) + \Delta U_d(s)}{U_{dc}} e^{-sT_S}. \tag{11}$$

Thus, the converter output voltage of the impedance cancelator is

$$\Delta U_{ic}(s) = \left[\Delta U_a(s) + \Delta U_d(s)\right] e^{-sT_S}. \tag{12}$$

Considering that the control bandwidth of the dc capacitor voltage feedback loop is designed to be much lower because the line frequency, ΔU_d can be neglected and (12) is simplified into

$$\begin{aligned} \Delta U_{ic}(s)|_{\Delta U_d(s)\cong 0} &= \Delta U_a(s)\, e^{-sT_S} \\ &= G_{NF}(s)\, e^{-1.5sT_S} \left[\Delta U_{pcc}(s) - R_v\, \Delta I_o(s)\right] \\ &= e^{-1.5sT_S} \left[\Delta U_{pcc,h}(s) - R_v\, \Delta I_{o,h}(s)\right]. \end{aligned} \tag{13}$$

Based on (13), the equivalent circuit is obtained by separating the ac voltage regulation (or the equivalent grid impedance cancelation) and the active damping function, as presented in Fig. 10(a). Then, the corresponding physical meaning can be represented by the equivalent impedance, as shown in Fig. 10(b), in which $u_{pcc,0}$ represents the line-frequency component of the grid voltage, the virtual resistance, $R_{v,h} = R_v e^{-1.5sT_S}$, is brought in by the active damping function, and the negative grid impedance, $L_{g,h} = L_g\ e^{-1.5sT_S}$, is formed by the unity gain-based PCC harmonic voltage feedforward.

As shown in Fig. 10, both of the virtual resistance and the negative grid impedance are relevant with the digital delay term, $e^{-1.5sT_S}$. To examine the effect of the digital delay on them, the mathematical model of the original *LCL* filter and the reshaped one in regard of the grid impedance can be derived and evaluated

TABLE I
VALUES OF THE COMPONENTS USED IN THE INVERTER PROTOTYPE

	LCL filter			Grid inductance	DC capacitor	Switching frequency		DC input voltage	DC capacitor voltage	PCC voltage
System Parameter	L_1	L_2	C_f	L_g	C_{dc}	$f_{sw\text{-}1}$ (Inverter)	$f_{sw\text{-}2}$ (Cancellator)	u_{in}	u_{dc}	u_{pcc}
Value	2mH	1mH	4.3μF	0~7.2mH	4×680μF	20kHz	50kHz	220V	30V	125V

comparatively. Following Fig. 1(b), the open-loop transfer function of the original *LCL* filter with respect to the grid impedance is expressed as

$$G_{o,o}(s) = \frac{\Delta I_o(s)}{\Delta U_i(s)} = \frac{Z_C(s)}{Z_1(s)[Z_2(s)+Z_g(s)]+Z_1(s)Z_C(s)+[Z_2(s)+Z_g(s)]Z_C(s)}. \quad (14)$$

After reshaping the impedance, the inserted series impedance by the grid impedance cancelator is

$$Z_{ic}(s) = G_{\mathrm{NF}}(s)\left(R_v e^{-1.5sT_S} - L_g e^{-1.5sT_S}\right) \quad (15)$$

and thereby the open-loop transfer function of the reshaped "*LCL* filter" is expressed as Eq. (16) shown at the bottom of this page.

By replacing the filter parameters with the value tabulated in Table I, (14) and (16) are plotted as shown in Fig. 11, in which a set of frequency response of the reshaped "*LCL* filter" with the grid impedance cancelation is overlaid with each other. It indicates the following:

1) without the grid impedance cancelation, the filter resonant frequency varies widely with the variation of equivalent grid impedance;
2) with the grid impedance cancelation, the effect of equivalent grid impedance is eliminated;
3) with the active damping function, the filter resonance is well damped; and
4) the digital delay leads to minor impact on the impedance reshaping within the filter resonant frequency, as presented in Fig. 11(b).

Therefore, by neglecting the effect of minor digital delay, the reshaped grid-connected inverter with an *LCL* filter behaves as a well-damped one with the cancelation of equivalent grid impedance, as revealed in Fig. 12.

V. EXPERIMENTAL VALIDATION

A 125 V, 50-Hz single-phase inverter prototype with the proposed grid impedance cancelator has been built and evaluated

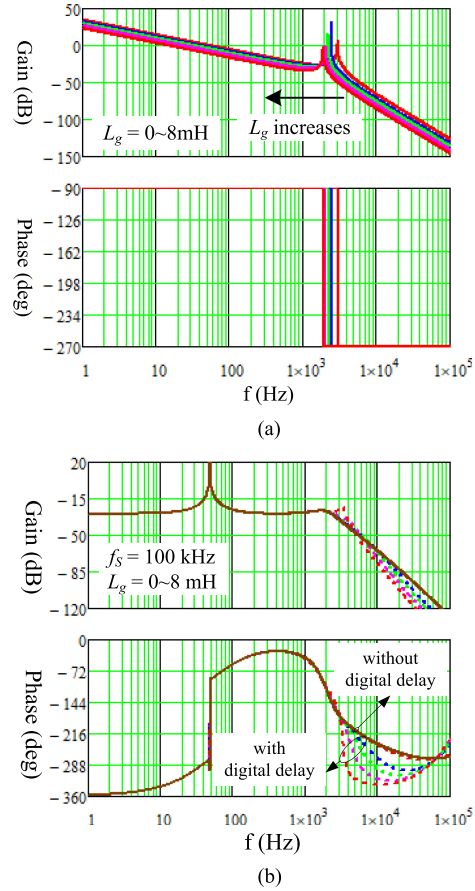

Fig. 11. Open-loop transfer functions of the original *LCL* filter and the reshaped one with variable grid impedance. (a) Original *LCL* filter. (b) Reshaped "*LCL* filter."

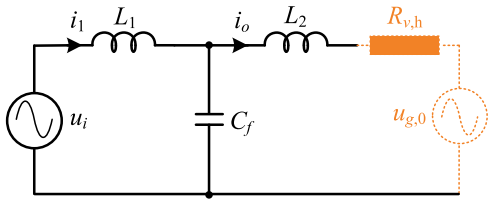

Fig. 12. Reshaped well-damped grid-connected inverter with the cancelation of L_g.

$$G_{o,ic}(s) = \frac{\Delta I_o(s)}{\Delta U_i(s)} = \frac{Z_C(s)}{Z_1(s)[Z_2(s)+Z_{ic}(s)+Z_g(s)]+Z_1(s)Z_C(s)+[Z_2(s)+Z_{ic}(s)+Z_g(s)]Z_C(s)}. \quad (16)$$

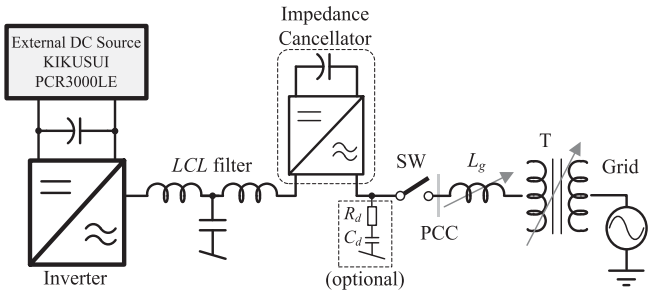

Fig. 13. Experimental inverter setup with variable grid inductance.

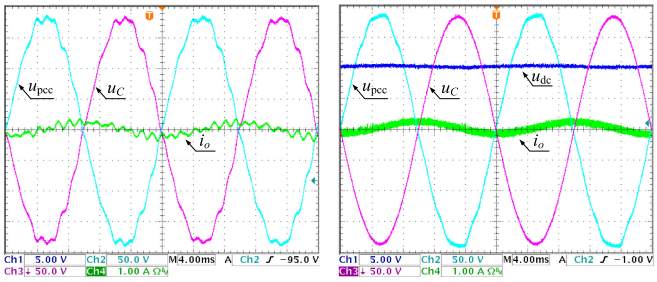

Fig. 14. Key waveforms with the inverter disabled. (a) Cancelator disabled. (b) Cancelator enabled.

for demonstration purpose. The design parameters are given in Table I. The prototype is supplied by an external dc power supply KIKUSUI PCR3000LE. The digital controller is Texas Instruments TMS320F2808. The experimental inverter setup with variable grid inductance and the impedance cancelator is presented in Fig. 13 and the inverter prototype is connected to a 220 V, 50-Hz power grid through an isolator, of which the leakage inductance is 0.8 mH. Electrical parameters of the cancelator are selected based on its operating volt-ampere (VA) rating. For instance, the current rating of the switching devices and the dc capacitors is selected based on the inverter output current, while the voltage rating is determined on the maximum harmonic PCC voltage under the worst case condition (e.g., vTHD $<$ 5%). To avoid square pulse voltage overlaid at the PCC voltage, as shown in Fig. 7, an optional $R_d - C_d$ branch with small value can be connected in shunt at the PCC. In the following tests, the inverter is regulated using proportional-resonant-plus-harmonic-compensation based current control strategy with unity gain-based filter capacitor voltage feedforward [18].

A. Key Waveforms With the Inverter Disabled

Fig. 14 presents the key waveforms when the grid-connected inverter is disabled. As seen in Fig. 14(a), due to the standby *LC* resonant tank at the grid side of the inverter, the oscillation appears at the grid current and the PCC voltage when the grid impedance cancelator is disabled. With the insertion of the grid impedance cancelator, the oscillation disappears, as shown in Fig. 14(b), because of the inserted active damping function or virtual resistance, as introduced in Section IV. Moreover, it prevents the voltage at the inverter output from the harmonic one at the PCC successfully. Improvements of the inverter stability

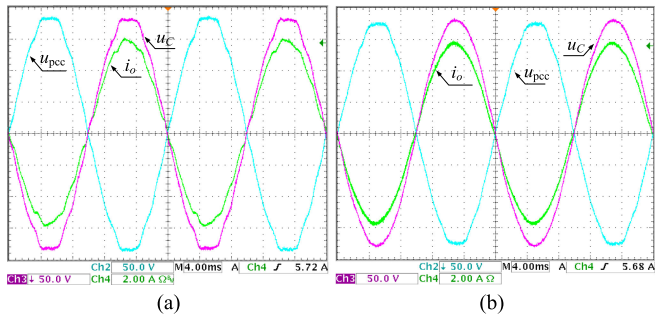

Fig. 15. Steady-state waveforms of the inverter outputs when $L_g = 0$. (a) Cancelator disabled. (b) Cancelator enabled.

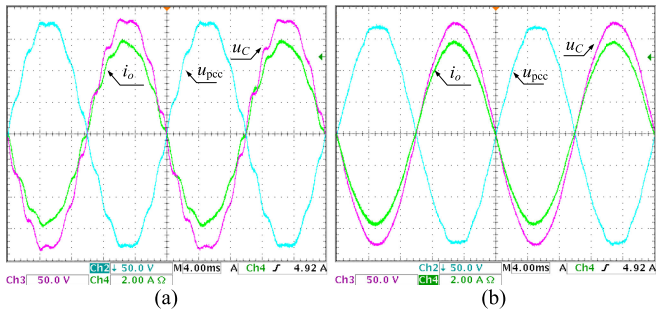

Fig. 16. Steady-state waveforms of the inverter outputs when $L_g = 2$ mH. (a) Cancelator disabled. (b) Cancelator enabled.

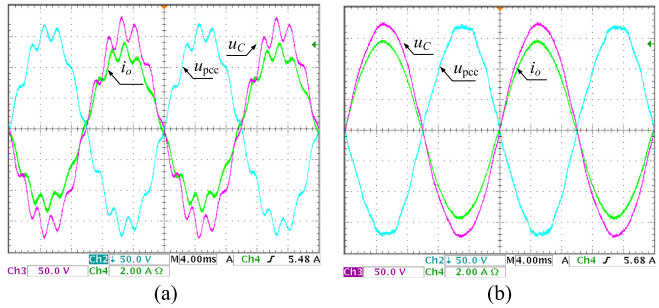

Fig. 17. Steady-state waveforms of the inverter outputs when $L_g = 7.2$ mH. (a) Cancelator disabled. (b) Cancelator enabled.

and harmonic rejection with the grid impedance cancelator will be validated in the following parts when the inverter is enabled.

B. Steady State Waveforms

Figs. 15–17 show the steady-state waveforms of the inverter outputs with and without the grid impedance cancelator under different grid conditions. It can be seen that the grid impedance cancelator enhances the harmonic rejection capability of the inverter against the grid voltage distortion and improves the power quality of the injected current a lot.

Without the grid impedance cancelator, the inverter stability becomes poor as the equivalent grid inductance L_g increases from 0 to 7.2 mH, as shown in Figs. 15(a)–17(a). The measured total-harmonic-distortion (THD) of the injected current increases from 1.7%, 2.7%, to 6.6%. Fig. 18 presents the corresponding frequency spectrum of the oscillating injected current with $L_g = 7.2$ mH, where the oscillation around 0.7 kHz is

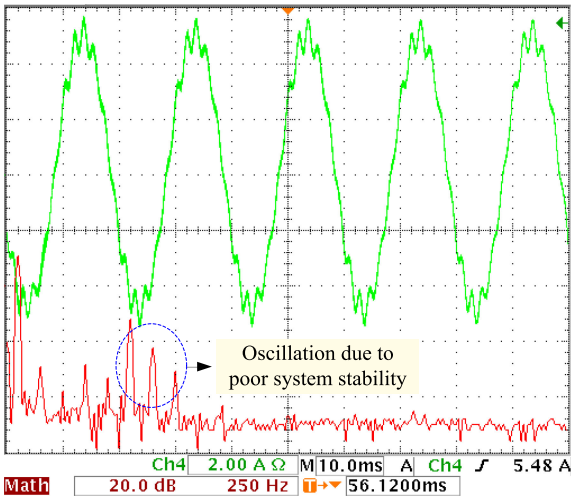

Fig. 18. Frequency spectrum of the injected current.

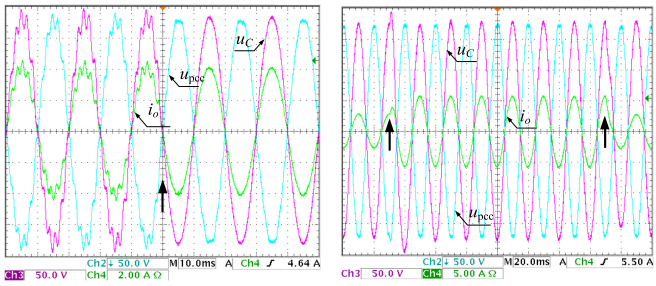

Fig. 19. Dynamic behaviors of the grid-connected inverter when $L_g = 7.2$ mH. (a) Cancelator from disabled to enabled. (b) Injected power transients.

caused by the poor stability margin, matching with the theoretical stability analysis in [18].

With the grid impedance cancelator, the inverter is maintained stable even under wide variation of equivalent grid impedance, as shown in Figs. 15(b)–17(b), because of elimination of equivalent grid impedance and the insertion of virtual resistance at the grid side, as shown in Fig. 12. The measured THD of the injected current is sustained at 0.9%, 1.0%, and 0.8%, respectively.

C. Dynamic Behavior

The dynamic behavior of the grid impedance cancelator is investigated under different grid inductances when the impedance cancelator is engaged, and the power rating is suddenly changed from half to full power and vice versa. The corresponding experimental results waveforms are shown in Fig. 19. It shows that the waveforms upon the transition when the cancelator is engaged. Fig. 19(b) indicates that the inverter operates well with the power transients. The amplitude variation of the filter capacitor voltage during transient state is brought in by the notch filter as shown in Fig. 9.

D. Power Consumption of the Cancelator

Considering the extreme low dc capacitor voltage, switching devices of the impedance cancelator are MOSFET FDD86110 (100 V, 50 A) with on-state resistance of 10.2 mΩ. Based on that, Fig. 20 shows the power consumption of the cancelator

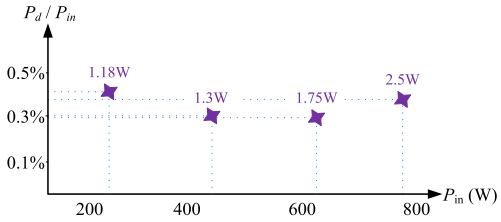

Fig. 20. Power loss of the cancelator as a function of the inverter input power.

(P_d) measured by universal power analyzer, Voltech PM6000, as a function of the inverter input power ($P_{\rm in}$), in which the power loss of the cancelator is mainly composed of switching devices and dc capacitors, and accounts for lower than 0.5% of the inverter input power. Thus, the efficiency of the entire system is not sacrificed owing to extreme low VA rating of the impedance cancelator.

VI. Conclusion

Active cancelation of equivalent grid impedance based on a full-bridge dc–ac converter has been presented. Its basic principle is derived based on the impedance-based stability criterion and has been proven to exhibit similar characteristics with the infinite increase in the inverter output impedance by introducing a negative virtual grid impedance. The grid impedance cancelator features the following:

1) no need to use extra passive *LC* filtering elements;
2) cancelation of equivalent grid impedance;
3) strong harmonic suppression against grid disturbance; and
4) active damping function to ease the burden of the inverter controller.

A single-phase inverter prototype has been built to verify the feasibility of the cancelator successfully. It shows that the inverter stability and injected power quality even under wide variation of grid conditions have been improved. Compared with the traditional grid-connected inverter with an *LCL* filter, the reshaped inverter with the grid impedance cancelator performs as a well-damped one without equivalent grid impedance. Further research will be dedicated to using such single-phase cancelator for three-phase inverter systems.

Appendix

A. Derivation of Fig. 4(a)

Infinite increase in the inverter output impedance in Fig. 3(a) can be transformed into the block diagram, as shown in Fig. 21(a), where the dotted lines represent the corresponding current insertion related to the PCC voltage and the inverter output impedance Z_o.

Considering the complicated calculation of Z_o expressed in (4), it is necessary to simplify the current insertion. Thus, a series of equivalent transformations for the system block diagram with infinite increase of the inverter output impedance is presented in Fig. 21, where the light dash lines represent the original status, and the dark solid lines means the current status. First, moving the feedback signal $\Delta U_C(s)$ right to the input of $Z_C(s)$, and calculating the corresponding closed-loop gain, an equivalent block diagram is obtained, as shown in Fig. 21(b).

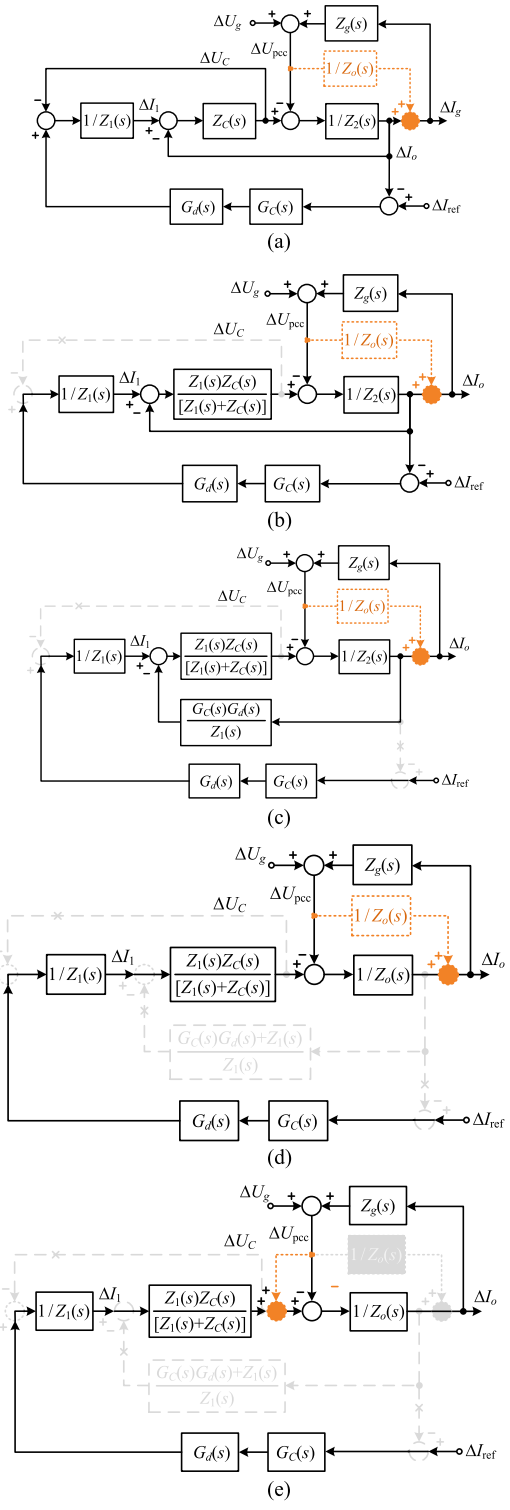

Fig. 21. Equivalent transformation for the system block diagram. (a) Step 1. (b) Step 2. (c) Step 3. (d) Step 4. (e) Step 5.

Second, moving the feedback signal $\Delta I_o(s)$ in the control stage to the node of inverter-side current $\Delta I_1(s)$, and combining it with the feedback branch of $\Delta I_o(s)$ in the power conversion stage, the equivalent block diagram is updated, as shown in Fig. 21(c). Then, moving it right to the input of $1/Z_2(s)$, and finishing the calculation of the corresponding closed-loop gain,

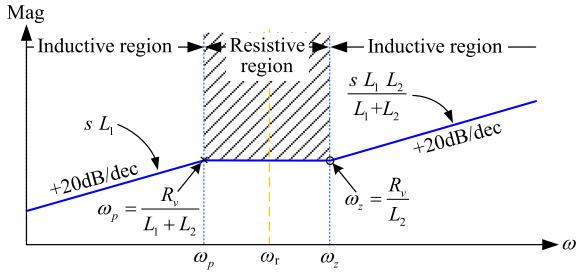

Fig. 22. Impedance feature of L_1 and branch $L_2 - R_v$.

the simplified block diagram is presented in Fig. 21(d). Finally, moving the current insertion point left to the input of $1/Z_o(s)$, the current insertion becomes an unity gain-based feedforward of the PCC voltage as indicated in Fig. 21(e).

Therefore, infinite increase of the inverter output impedance can be realized simply through the block diagram, as shown in Fig. 4(a), after recovering the transformation of remained parts mentioned before.

B. Derivation of (7)

Based on Fig. 12, the characteristic resonant frequency of the filter is changeable with different R_v. For example, in Fig. 12, if $R_v = 0\,\Omega$

$$\omega_{r\_\mathrm{up}} = \sqrt{\frac{L_1 + L_2}{L_1\, L_2\, C_f}} \tag{A1}$$

where ω_{r_up} is the possible maximum characteristic resonant frequency, while if $R_v = \infty\,\Omega$, then

$$\omega_{r\_\mathrm{down}} = \sqrt{\frac{1}{L_1\, C_f}} \tag{A2}$$

where ω_{r_down} is the possible minimum characteristic resonant frequency.

Second, the impedance of L_1 and branch $L_2 - R_v$, is calculated as

$$Z_{L(\mathrm{LCL})} = sL_1 \frac{sL_2 + R_v}{s\,(L_1 + L_2) + R_v} \tag{A3}$$

with the impedance feature as shown in Fig. 21.

To find out the optimized quality factor (Q-factor), the range of changeable characteristic resonant frequency between (A1) and (A2) should fall into the shadow areas, as shown in Fig. 22, which is the resistive region of L_1 and $L_2 - R_v$ branch [7]. Accordingly, based on (A3), the virtual resistance is limited with the range of

$$\frac{R_v}{L_1 + L_2} \le \omega_r \le \frac{R_v}{L_2}. \tag{A4}$$

Supposing that the virtual resistance R_v changes from 0 Ω to ∞ Ω, it is deduced that

$$\omega_{r\_\mathrm{down}} \le \omega_r \le \omega_{r\_\mathrm{up}}. \tag{A5}$$

Combining (A4) and (A5), the selection criterion of the apparent virtual resistance is derived as

$$\begin{cases} \frac{R_v}{L_1+L_2} \le \omega_{r\_\mathrm{down}} \\ \frac{R_v}{L_2} \ge \omega_{r\_\mathrm{up}} \end{cases} \tag{A6}$$

of which the optimized value of R_v is given as (7).

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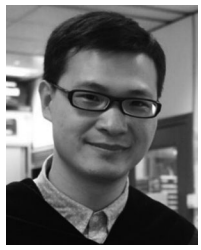

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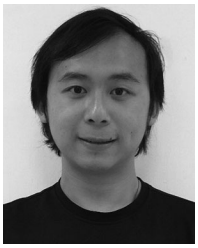

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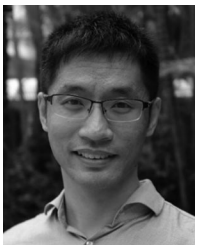

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