A Simple SR Gate Driving Circuit With Reduced Gate Driving Loss for Phase-Shifted Full-Bridge Converter

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***Abstract*—The phase-shifted full-bridge (PSFB) converter with synchronous rectifier (SR) is one of the most attractive dc–dc converters for the server power supply due to its high power capability and small secondary ripple current with the output inductor. Moreover, it can more reduce the secondary conduction loss by using parallel-connected MOSFETs in SR. However, due to large input capacitance of the parallel-connected MOSFETs in SR, the PSFB converter has large SR gate driving loss, which particularly degrades the light load efficiency. Thus, in this paper, one additional resistor is added to the conventional SR gate driving circuit to recycle the gate driving energy. As a result, the proposed circuit can improve the light load efficiency of the PSFB converter without operation mode change, additional controls, and complex circuits. The most advantage of the proposed circuit is that it is very simple and available to any other SR gate driver IC. The validity of the proposed circuit is confirmed by experimental results from a prototype with 340–400 V input and 12 V/66.66 A output.**

***Index Terms*—Gate driving circuit, light load efficiency, phase-shifted full-bridge (PSFB) converter, server power supply, synchronous rectifier (SR).**

I. Introduction

RECENTLY, as the information technology (IT) market has grown, the number of data centers has been increased. Accordingly, the server power supply has been consistently and actively developed. In general, the server power supply requires high efficiency at the heavy load condition because it operates under heavy load condition at daytime. Moreover, since the sever power supply runs under light load condition at night and dawn, the light load efficiency has also become important in the market of the server power supply. This tendency is confirmed by the 80 PLUS incentive program [1] requiring high efficiency from 10% to 100% load conditions. Furthermore, many manufacturers of the server power supply tend to require high efficiency even below 5% load condition, which exceeds the latest Energy Star specifications [2], [3].

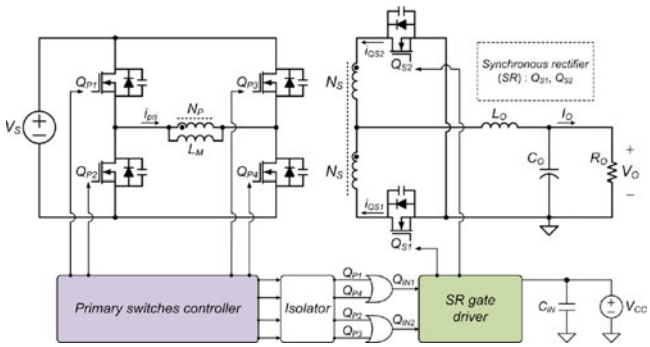

Fig. 1. Circuit diagram of conventional PSFB converter with SR.

For obtaining high efficiency at the heavy load condition, it is important to reduce the secondary conduction loss due to low output voltage and high output current specifications of the server power supply. Thus, a phase-shifted full-bridge (PSFB) converter with synchronous rectifier (SR), as shown in Fig. 1, has been widely used in the dc/dc stage of the server power supply [3]–[6]. From this figure, the PSFB converter can have small secondary ripple current with the output inductor (L_O), which reduces the secondary RMS current. Moreover, it can generally achieve higher heavy load efficiency by adopting parallel-connected MOSFETs with small on-resistance in SR.

However, since a MOSFET with small on-resistance typically has large input capacitance, parallel-connected MOSFETs in SR cause large gate driving loss. Thus, despite of high efficiency at the heavy load condition, the PSFB with SR has low efficiency at the light load condition where the gate driving loss is dominant, i.e., below 10% load condition. As a result, it is required to reduce the SR gate driving loss for improving the light load efficiency of the PSFB converter with SR.

To reduce the gate driving loss, many methods have been proposed [7]–[13]. First, resonant gate driving methods are presented in [7]–[10]. These methods can reduce the gate driving loss by recycling the gate driving energy. However, due to

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complex circuits including additional large inductors, it is difficult to be applied to the server power supply requiring high power density. Second, adaptive gate driving (AGD) methods are presented in [11]–[13]. In these methods, the gate driving voltage is adjusted according to the load condition so the AGD methods can reduce the gate driving loss by decreasing the gate driving voltage at the light load condition. However, these methods also require additional active and passive components as well as control techniques to adjust the gate driving voltage. Finally, to eliminate the SR gate driving loss, the SR can be turned off at the light load condition, which is called the discontinuous conduction mode (DCM) control [5], [14], [15]. In addition, since the PSFB converter has higher voltage gain under the DCM operation than under the continuous conduction mode (CCM) operation, this method can also reduce the transformer core loss with the reduced effective duty ratio. However, the DCM control method causes large conduction loss on the body diode of MOSFETs in SR. Moreover, provided that large magnetizing inductance is used to improve the efficiency at the heavy load condition, the switching loss of the primary MOSFETs can be increased due to the reduced effective duty ratio under very light load condition [5], [15]. Furthermore, the SR on/off operation results in poor dynamic performance because of the different voltage gain between DCM and CCM operations. As a result, it is required to reduce the SR gate driving loss of the PSFB converter without degradation of the dynamic performance, additional complex circuits, and additional control schemes.

In this paper, a simple SR gate driving circuit is proposed to improve the light load efficiency of the PSFB converter with SR. The proposed circuit adds only one resistor in the conventional SR gate driving circuit to recycle the gate driving energy. Thus, it can reduce the gate driving voltage at the turn-off instance, which results in small turn-off gate driving loss. Moreover, since the proposed circuit does not require operation mode change as well as additional complex circuits and control schemes, it can achieve good dynamic performance and high power density compared to the conventional methods.

This paper is an improved version of the paper reported in [16]. Compared to the previous paper, the analysis and experimental results are newly added, and the overall contents were improved.

II. Concept of Proposed SR Gate Driving Circuit

A. Concept of Proposed Control Method

The SR in the PSFB converter is typically controlled by OR-gated signals, i.e., $Q_{S1} = Q_{P1} + Q_{P4}$ and $Q_{S2} = Q_{P2} + Q_{P3}$, to reduce the secondary conduction loss during the freewheeling period and to avoid the shoot through problem, as shown in Fig. 2. Thus, the overlap interval occurs between Q_{S1} and Q_{S2} signals. It implies the possibility that the turn-on operation of a switch can affect the turn-off operation of the other switch, which is the starting point of the proposed circuit.

Fig. 3 shows the concept of the conventional SR gate driving circuit during the overlap interval, i.e., $t_C \sim t_D$ in Fig. 2. When Q_{S1} is turned on at t_C, only $V_{\rm CC}$ begins to charge the input capacitance of Q_{S1} ($C_{\rm iss-QS1}$), as shown in Fig. 3(a). And then, when Q_{S2} is turned off at t_D, all stored energy in the input capacitance of Q_{S2} ($C_{\rm iss-QS2}$) is discharged to the ground.

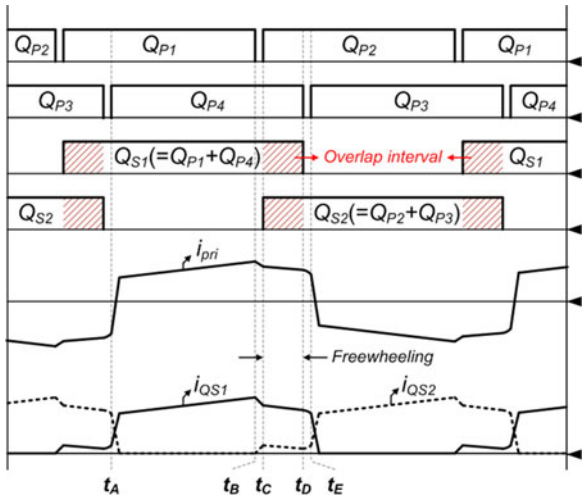

Fig. 2. Simplified key waveforms of conventional PSFB converter with SR.

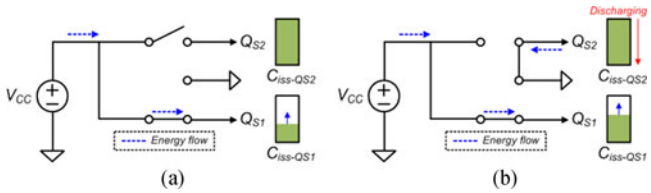

Fig. 3. Concept of conventional SR gate driving circuit. (a) Turn-on of Q_{S1} ($t_C \sim$). (b) Turn-off of Q_{S2} (t_D)

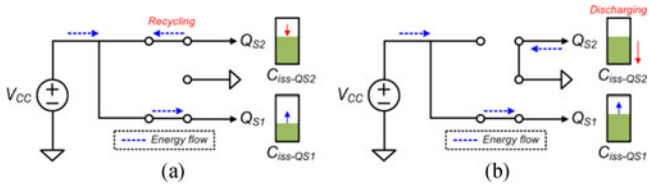

Fig. 4. Concept of proposed SR gate driving circuit. (a) Turn-on of Q_{S1} ($t_C \sim$). (b) Turn-off of Q_{S2} (t_D).

On the other hand, the concept of the proposed SR gate driving circuit can be depicted as shown in Fig. 4. Unlike the conventional circuit, when Q_{S1} is turned on, not only $V_{\rm CC}$ but also the energy recycled by $C_{\rm iss-QS2}$ is used to charge $C_{\rm iss-QS1}$, as shown in Fig. 4(a). Thus, as shown in Fig. 4(b), when Q_{S2} is turned off, the wasted energy of $C_{\rm iss-QS2}$ can be reduced, which results in small turn-off gate driving loss. Detailed explanations of the proposed circuit such as operation principles and design consideration are discussed in the following sections.

III. Operational Principles

A. Operational Principles of Conventional Circuit

Fig. 5(a) shows the conventional SR gate driving circuit. From this figure, $C_{\rm IN}$ is the input capacitor of the SR gate driver, $Q_{\rm IN1}$ and $Q_{\rm IN2}$ are input signals of the SR gate driver, R_{ON1} and R_{ON2} are turn-on gate resistors, $D_{\rm OFF1}$ and $D_{\rm OFF2}$ are

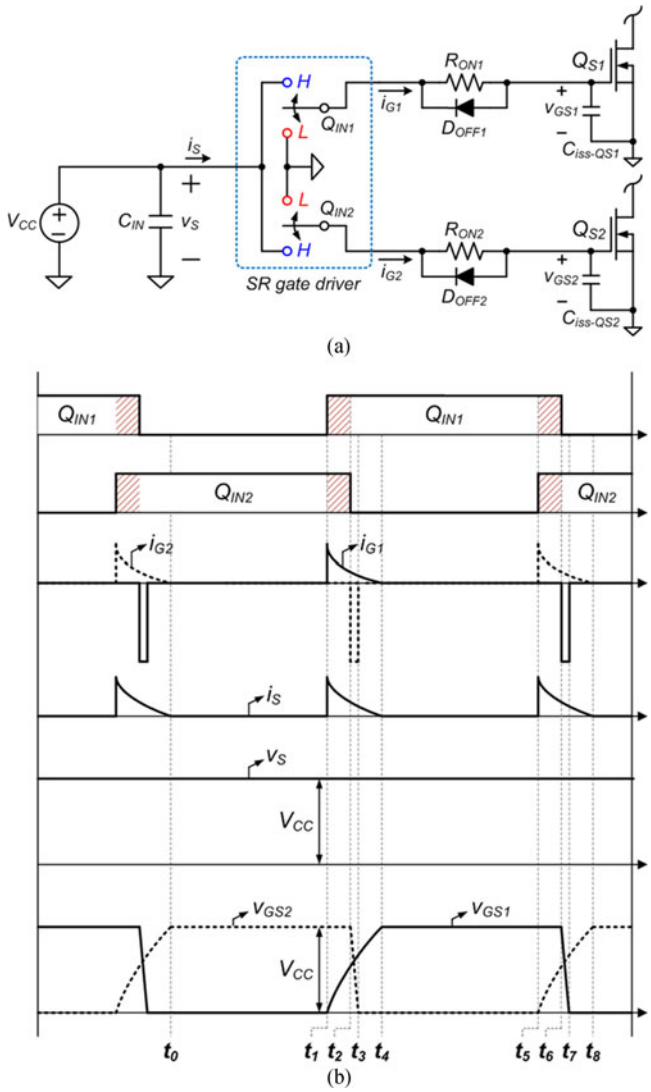

Fig. 5. Conventional SR gate driving circuit. (a) Circuit diagram. (b) Operational key waveforms.

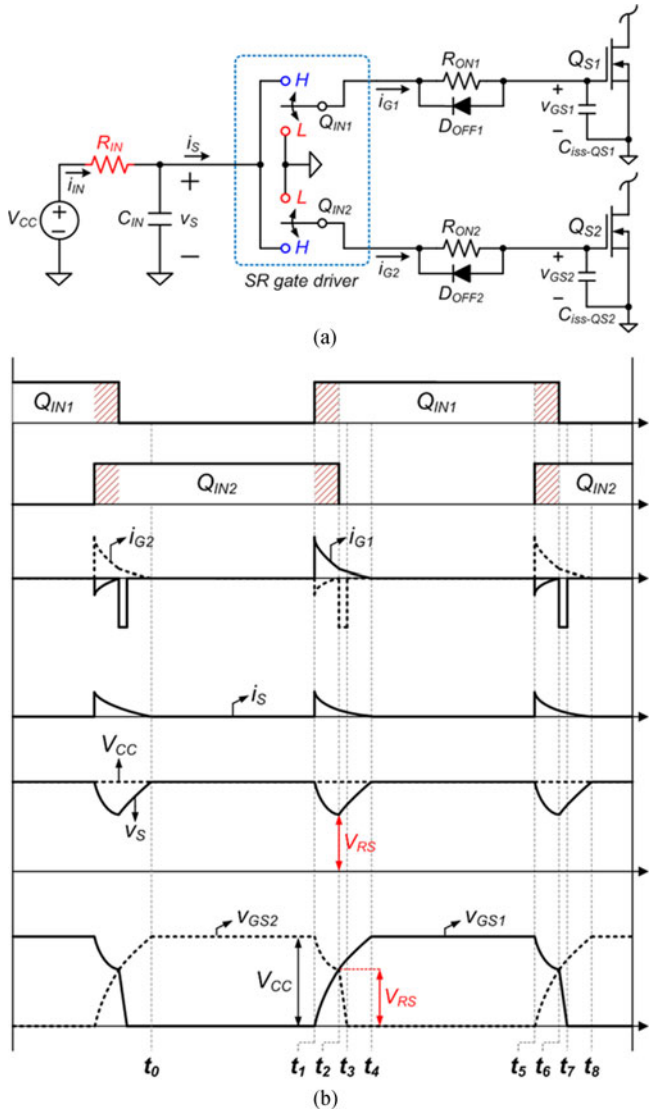

Fig. 6. Proposed SR gate driving circuit. (a) Circuit diagram. (b) Operational key waveforms.

turn-off diodes, and the supply voltage of the SR gate driver (v_S) is maintained as $V_{\rm CC}$. Each switching period is divided into two cycles, t_0–t_4 and t_4–t_8. Because of the symmetric operation, the first cycle is only explained. Fig. 5(b) shows the operational key waveforms of the conventional SR gate driving circuit.

Mode1[t_0–t_1]: When the gate-source voltage of Q_{S2} ($v_{\rm GS2}$) reaches v_S at t_0, the gate current of Q_{S2} (i_{G2}) and supply current of the SR gate driver (i_S) become zero. Thus, $v_{\rm GS2}$ keeps its value as $V_{\rm CC}$.

Mode2[t_1–t_2]: When $Q_{\rm IN1}$ is high at t_1, the gate current of Q_{S1} (i_{G1}) begins to charge $C_{\rm iss-QS1}$ through $R_{\rm ON1}$. Thus, the gate-source voltage of Q_{S1} ($v_{\rm GS1}$) is increased as follows:

$$v_{\rm GS1}(t) = V_{\rm CC}(1 - e^{-(t-t_1)/\tau_{\rm SR}}) \tag{1}$$

where $\tau_{\rm SR} = C_{\rm iss-QS1}R_{\rm ON1} = C_{\rm iss-QS2}R_{\rm ON2}$.

Mode3[t_2–t_3]: When $Q_{\rm IN2}$ is low to turn off Q_{S2} at t_2, the energy stored in $C_{\rm iss-QS2}$ is discharged to the ground through $D_{\rm OFF2}$. Thus, $v_{\rm GS2}$ becomes zero. On the other hand, $v_{\rm GS1}$ continues to be increased with $\tau_{\rm SR}$ as in (1). In this mode, it is noted that $v_{\rm GS2}$ is decreased from $V_{\rm CC}$ to zero resulting in large turn-off gate driving loss.

Mode4[t_3–t_4]: At time t_3, $v_{\rm GS2}$ reaches zero and this mode starts. During this mode, $v_{\rm GS2}$ remains as zero, and $v_{\rm GS1}$ reaches $V_{\rm CC}$ at the end of this mode.

B. Operational Principles of Proposed Circuit

Fig. 6 shows the proposed SR gate driving circuit. From this figure, the proposed circuit adds one resistor ($R_{\rm IN}$) between $V_{\rm CC}$ and $C_{\rm IN}$, which makes v_S be lower than $V_{\rm CC}$ by restricting the input current ($i_{\rm IN}$) during the overlap interval. Therefore, the proposed circuit can recycle the energy stored in the input capacitance of MOSFETs, which reduces the SR gate driving loss. Followings are operation explanations of the proposed circuit.

Mode1[t_0–t_1]: When v_S and $v_{\rm GS2}$ reach $V_{\rm CC}$ at t_0, i_{G2}, and i_S become zero like *Mode 1* in the conventional circuit, as shown in Fig. 6(b). As a result, during this mode, v_S and $v_{\rm GS2}$ maintain their value as $V_{\rm CC}$.

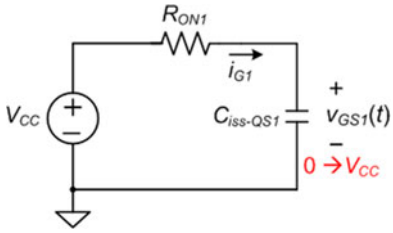

Fig. 7. Conventional equivalent circuit during turn-on operation of Q_{S1}.

Mode2[t_1–t_2]: At time t_1, Q_{IN1} is high to turn on Q_{S1}, and then i_{G1} begins to charge $C_{\mathrm{iss-QS1}}$ like the conventional circuit. Thus, v_{GS1} is increased as in (1). However, since R_{IN} can restrict the charging current of C_{IN}, i.e., i_{IN}, v_S can be considerably reduced by i_{G1}, as shown in Fig. 6(b).

During this interval, v_{GS2} is also decreased with v_{S} through D_{OFF2} because Q_{IN2} is high. Therefore, not only V_{CC} but also $C_{\mathrm{iss-QS2}}$ can be the gate charging source for $C_{\mathrm{iss-QS1}}$. Meanwhile, v_S and v_{GS2} can be expressed as follows:

$$v_S(t) = V_{\mathrm{CC}} - \frac{1}{C_{\mathrm{IN}}}\left[C_{\mathrm{iss1}} v_{\mathrm{GS1}}(t) - \int_{t_1}^{t} i_{\mathrm{IN}}(\tau)d\tau\right] \quad (2)$$

$$v_{\mathrm{GS2}}(t) = v_S(t) + V_{F-D2} \quad (3)$$

where $i_{\mathrm{IN}}(t) = (V_{\mathrm{CC}} - v_S(t))/R_{\mathrm{IN}}$, V_{F-D2} is the forward voltage drop of D_{OFF2}. From (3), if V_{F-D2} is negligible, v_{GS2} is equal to v_S.

Mode3[t_2–t_3]: When Q_{IN2} is low to turn off Q_{S2} at t_2, the energy stored in $C_{\mathrm{iss-QS2}}$ is dissipated to the ground through D_{OFF2} like the conventional circuit. However, unlike the conventional circuit, since v_{GS2} is turned off from not V_{CC} but the reduced supply voltage (V_{RS}), the proposed circuit can achieve smaller turn-off gate driving loss than the conventional circuit. Meanwhile, v_S and v_{GS1} are increased with τ_{IN}, and v_S can be expressed as follows:

$$v_S(t) = V_{\mathrm{CC}} + (V_{\mathrm{RS}} - V_{\mathrm{CC}})\exp\left[-(t-t_2)/\tau_{\mathrm{IN}}\right] \quad (4)$$

where $\tau_{\mathrm{IN}} = C_{\mathrm{OSS-QS2}}(R_{\mathrm{IN}} + R_{\mathrm{ON2}}) = C_{\mathrm{OSS-QS1}}(R_{\mathrm{IN}} + R_{\mathrm{ON1}})$.

Mode4[t_3–t_4]: During this mode, v_{GS2} remains as zero, and v_S and v_{GS1} reach V_{CC} at the end of this mode.

IV. Analysis of Proposed SR Gate Driving Circuit

A. SR Gate Driving Loss

The SR gate driving loss (P_G) occurs at MOSFETs in SR during their turn-on and turn-off operations. Thus, in this section, P_G is discussed considering the turn on/off operations of MOSFETs in the conventional and proposed SR gate driving circuits. Moreover, due to the symmetric operation of Q_{S1} and Q_{S2}, the gate driving loss of Q_{S1} is only explained.

1) Conventional SR Gate Driving Loss: In the conventional circuit, when Q_{IN1} is high to turn on Q_{S1}, V_{CC} only provides the gate driving energy for $C_{\mathrm{iss-QS1}}$ as shown in Fig. 7. From this figure, while charging $C_{\mathrm{iss-QS1}}$ from zero to V_{CC}, the turn-on energy loss of Q_{S1} in the conventional circuit ($E_{\mathrm{ON-Loss-Conv}}$) occurs at R_{ON1}, and it can be calculated by using the ordinary differential equation as follows:

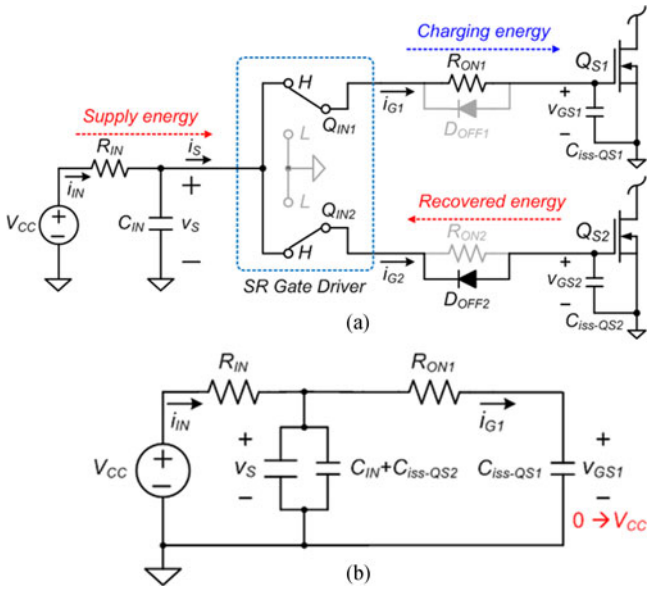

Fig. 8. Proposed circuit during turn-on operation of Q_{S1}. (a) Operation circuit. (b) Equivalent circuit.

$$E_{\mathrm{ON-Loss-Conv}} = \int R_{\mathrm{ON1}} i_{G1}^2(t)dt = \frac{1}{2}C_{\mathrm{iss-QS1}}V_{\mathrm{CC}}^2 \quad (5)$$

$$i_{G1}(t) = \frac{V_{\mathrm{CC}}}{R_{\mathrm{ON1}}} e^{\frac{-t}{\tau_{\mathrm{SR}}}}. \quad (6)$$

Meanwhile, during the turn-off operation of Q_{S1}, since Q_{S1} is turned off at V_{CC}, the turn-off energy loss of Q_{S1} ($E_{\mathrm{OFF-Loss-Conv}}$) is given by (7). As a result, including both Q_{S1} and Q_{S2}, the total SR gate driving loss of the conventional circuit ($P_{G-\mathrm{Conv}}$) can be expressed as in (8)

$$E_{\mathrm{OFF-Loss-Conv}} = \frac{1}{2}C_{\mathrm{iss-QS1}}V_{\mathrm{CC}}^2 \quad (7)$$

$$P_{G-\mathrm{Conv}} = 2C_{\mathrm{iss}}V_{\mathrm{CC}}^2 f_S \quad (8)$$

where f_S is the switching frequency and $C_{\mathrm{iss}} = C_{\mathrm{iss-QS1}} = C_{\mathrm{iss-QS2}}$.

2) Proposed SR Gate Driving Loss: When Q_{IN1} is high to turn on Q_{S1} in the proposed circuit, not only V_{CC} but also $C_{\mathrm{iss-QS2}}$ can provide the gate driving energy for $C_{\mathrm{iss-QS1}}$ as shown in Fig. 8(a). Provided that V_{F-D2} is negligible, the equivalent circuit of Fig. 8(a) can be depicted like Fig. 8(b). From this figure, the turn-on energy loss of Q_{S1} ($E_{\mathrm{ON-Loss-Pro}}$) in the proposed circuit can be calculated by finding each energy loss of R_{ON1} and R_{IN}, which are obtained in the same manner with the conventional circuit as follows:

$$E_{\mathrm{RIN}} = \frac{C_{\mathrm{iss-QS1}}^2 R_{\mathrm{IN}}}{2(C_{\mathrm{iss-QS1}}R_{\mathrm{IN}} + C_{\mathrm{eq}}R_{\mathrm{IN}} + C_{\mathrm{eq}}R_{\mathrm{ON1}})}V_{\mathrm{CC}}^2 \quad (9)$$

$$E_{\mathrm{RON1}} = \frac{C_{\mathrm{eq}}C_{\mathrm{iss-QS1}}R_{\mathrm{IN}} + C_{\mathrm{iss-QS1}}^2 R_{\mathrm{ON1}}}{2(C_{\mathrm{iss-QS1}}R_{\mathrm{IN}} + C_{\mathrm{eq}}R_{\mathrm{IN}} + C_{\mathrm{eq}}R_{\mathrm{ON1}})}V_{\mathrm{CC}}^2 \quad (10)$$

$$E_{\mathrm{ON-Loss-Pro}} = E_{\mathrm{RIN}} + E_{\mathrm{RON1}} = \frac{1}{2}C_{\mathrm{iss-QS1}}V_{\mathrm{CC}}^2 \quad (11)$$

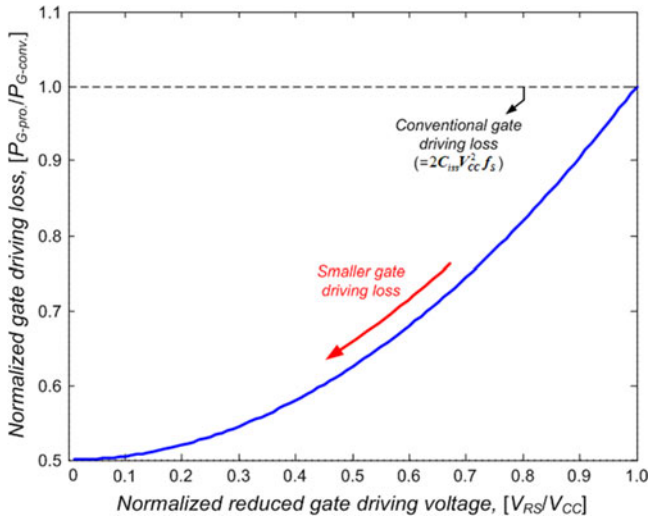

Fig. 9. Normalized gate driving loss of proposed circuit according to $V_{\rm RS}$.

TABLE I
DESIGN SPECIFICATION AND PARAMETER OF PSFB CONVERTER

Items	Parameters
Input voltage, V_S	300—400 V (Nominal: 400 V)
Output voltage, V_O	12 V
Switching frequency, f_S	100 kHz
Nominal duty ratio, $D_{\rm nom}$	0.405
Transformer	Core: EE3531
	L_M : 2.6 mH, L_{lkg} : 11.4 μH
	N_P :N_S :N_S = 27 : 1 : 1
Output inductor, L_O	Core: AMP27P90
	L_O : 2 μH, Turn: 3turns
Primary switches, Q_{P1} ~ Q_{P4}	Q_{P1} & Q_{P2} (Leading Lag): TK25V60X
	Q_{P3} & Q_{P4} (Lagging Lag): TK12V60W
Secondary switches, Q_{S1} & Q_{S2}	IPT007N06N ($C_{\rm iss}$ = 16 nF), 3EA
PSFB controller	UCC3895
SR gate driver	2EDN7524R

where $C_{\rm eq}$ is the sum of $C_{\rm IN}$ and $C_{\rm iss-QS2}$. From (5) and (11), although the proposed circuit has one additional resistor ($R_{\rm IN}$), it has the same turn-on energy loss with the conventional circuit.

Meanwhile, the turn-off energy loss of Q_{S1} in the proposed circuit ($E_{\rm OFF-Loss-Pro}$) can be calculated by considering the energy recycling operation of Q_{S1} during the turn-on operation of Q_{S2}. When Q_{S2} is turned on in the proposed circuit, the energy stored in $C_{\rm iss-QS1}$ is also used to charge $C_{\rm iss-QS2}$ like the abovementioned energy recycling operation of Q_{S2}. Thus, the gate-source voltage of Q_{S1} can be reduced as much as the recycled energy of $C_{\rm iss-QS1}$ for $C_{\rm iss-QS2}$, which is determined by the value of $C_{\rm IN}$ and $R_{\rm IN}$. Provided that the reduced gate-source voltage of Q_{S1} is $V_{\rm RS}$, $E_{\rm OFF-Loss-Pro}$ can be given by

$$E_{\rm OFF-Loss-Pro} = \frac{1}{2}C_{\rm iss-QS1}V_{\rm RS}^2 \tag{12}$$

Based on (11) and (12), the total SR gate driving loss of the proposed circuit ($P_{G-\rm Pro}$), including both Q_{S1} and Q_{S2}, can be expressed as follows:

$$P_{G-\rm Pro} = C_{\rm iss}(V_{\rm CC}^2 + V_{\rm RS}^2)f_S. \tag{13}$$

From (8) and (13), the proposed circuit can achieve smaller gate driving loss than the conventional circuit by decreasing $V_{\rm RS}$. Fig. 9 shows the normalized gate driving loss of the proposed circuit according to $V_{\rm RS}$. From this figure, as $V_{\rm RS}$ is decreased, the proposed circuit can obtain smaller gate driving loss compared to the conventional circuit. However, too small $V_{\rm RS}$ can cause side effects such as under voltage lockout protection of the SR gate driver. Therefore, $V_{\rm RS}$ should be carefully designed considering gate driving loss and normal operation, which is discussed next part.

In addition to the SR gate driving loss, the proposed circuit can increase the conduction loss of turn-off diodes ($D_{\rm OFF1}$ and $D_{\rm OFF2}$) and MOSFETs in SR. However, the quantity of the increased loss is negligible compared to the reduced gate driving loss because the average current of turn-off diodes and increased on-resistance of MOSFETs in SR are very small. As a result, the proposed SR gate driving circuit can improve the efficiency of the PSFB converter by reducing the SR gate driving loss, especially under light load condition.

B. Design Consideration of Proposed Circuit ($C_{\rm IN}$ and $R_{\rm IN}$)

To illustrate simple design procedure of the propose circuit, a design example is presented, and its specifications and design parameters are shown in Table I. From this table, the proposed circuit should be designed to improve the efficiency at the nominal input voltage (V_S = 400 V) where the converter operates mostly. In order to use the proposed circuit effectively, followings should be considered: 1) the minimum operating voltage of the SR gate driver and 2) rising time of the gate-source voltage ($v_{\rm GS}$).

First, as mentioned previously, the proposed circuit can more reduce the SR gate driving loss by decreasing $V_{\rm RS}$. However, provided that $V_{\rm RS}$ is lower than the minimum operating voltage of the SR gate driver ($V_{\rm DD-min}$), not only the SR gate driver is turned off due to the under voltage lock out protection, but also normal operations cannot be guaranteed. Thus, $V_{\rm RS}$ should be higher than $V_{\rm DD-min}$. To satisfy this condition, $C_{\rm IN}$ should have larger energy than the required energy for charging the input capacitance of MOSFETs. Therefore, considering the charging and discharging energy for $C_{\rm IN}$, the minimum $C_{\rm IN}$ can be obtained as in (14) shown at the bottom of this page.

Second, the rising time of $v_{\rm GS}$ should be considered. A MOSFET typically has larger on-resistance as $v_{\rm GS}$ is decreased. Thus, to avoid large conduction loss under heavy load condition, $v_{\rm GS}$

$$C_{\rm IN} \geq \frac{C_{\rm iss}R_{\rm IN}(3V_{\rm DD-min}^2 - V_{\rm CC}^2) + (0.5 - D_{\rm nom})(0.1V_{\rm DD-min} - 0.1V_{\rm CC})T_SV_{\rm CC}}{R_{\rm IN}(V_{\rm CC}^2 - V_{\rm DD-min}^2)}. \tag{14}$$

TABLE II
DETAILED DESIGN PARAMETER OF CONVENTIONAL AND PROPOSED CIRCUITS

Parameters	Conventional	Proposed
Supply voltage, V_{CC}	V_O (= 12 V)	
Turn-off diode, D_{OFF1} & D_{OFF2}	M1FM3	
Turn-on gate resistor, R_{ON1} & R_{ON2}	10 Ω	1.8 Ω
Input capacitor of SR gate driver, C_{IN}	4.7 μF	22 nF
Input resistor of SR gate driver, R_{IN}	–	8.2 Ω

has to reach V_{CC} as fast as possible. As a result, the proposed circuit should have similar rising time of v_{GS} with that of the conventional circuit. Considering this requirement, an additional resistor (R_{IN}) of the proposed circuit has to meet the following condition:

$$R_{IN} = R_{ON-conv} - R_{ON-pro} \tag{15}$$

where $R_{ON-conv}$ and R_{ON-pro} are the turn-on gate resistor of MOSFETs in conventional and proposed circuits, respectively.

V. EXPERIMENTAL RESULTS

To verify the validity of the proposed circuit, the conventional and proposed SR gate driving circuits were applied to an 800 W prototype PSFB converter with the specifications of Table I. Moreover, in the prototype PSFB converter, V_O is used as the supply voltage of the secondary ICs (V_{CC}) to reduce the loss of the standby converter.

In the proposed circuit, C_{IN} and R_{IN} were designed considering the minimum operating voltage of the SR gate driver with 100% voltage margin and rising time of the gate-source voltage of the conventional circuit. Thus, by using (14) and (15), C_{IN} and R_{IN} were selected as 22 nF and 8.2 Ω, respectively. On the other hand, C_{IN} of the conventional circuit is 4.7 μF to obtain constant supply voltage of the SR gate driver, i.e., $v_S = V_{CC}$. Detailed design parameters are shown in Table II.

Figs. 10 and 11 show experimental waveforms of the PSFB converter with conventional and proposed SR gate driving circuits at 100% and 1% load conditions. In the conventional SR gate driving circuit, the supply voltage of the SR gate driver (v_S) is maintained as V_{CC} regardless of load conditions, as shown in Fig. 10. Thus, Q_{S1} and Q_{S2} are turned off at $v_{GS1} = v_{GS2} = 12$ V, which causes large turn-off gate driving loss in the PSFB converter with the conventional SR gate driving circuit. On the other hand, in the proposed circuit, v_S is decreased when Q_{S1} and Q_{S2} are turned on, as shown in Fig. 11. Therefore, the energy stored in the input capacitance of Q_{S1} and Q_{S2} can be recycled. For this reason, Q_{S1} and Q_{S2} are turned off at $v_{GS1} = v_{GS2} = 8$ V, which enables the PSFB converter with proposed SR gate driving circuit to reduce its SR gate driving loss by 28% compared to the conventional one.

Fig. 12 shows experimental waveforms while the output load current is changed from 1 A to 41 A (60% load change) and from 41 A to 1 A. To verify the dynamic performance of the proposed SR gate driving circuit, not only the conventional SR gate driving circuit but also the DCM control method which turns off the SR under 10% load conditions is tested. As shown in Fig. 12(a), the conventional SR gate driving circuit has 600 mV (±2.5%)

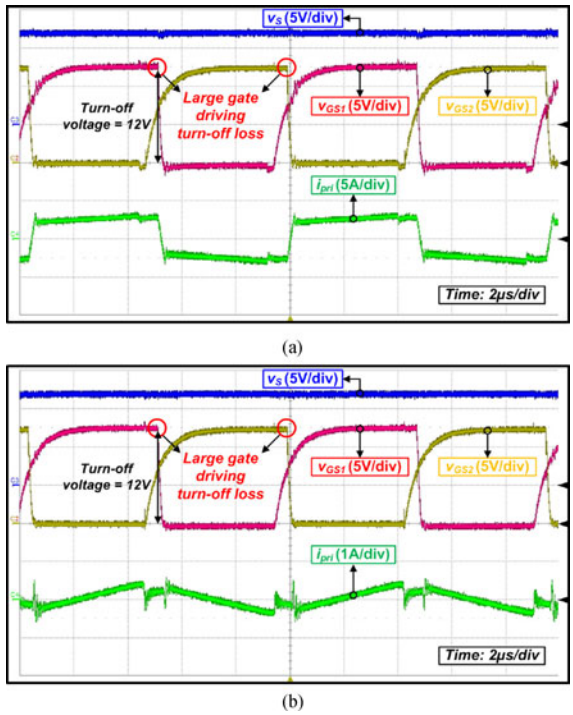

Fig. 10. Experimental waveforms with conventional SR gate driving circuit. (a) 100% load condition. (b) 1% load condition.

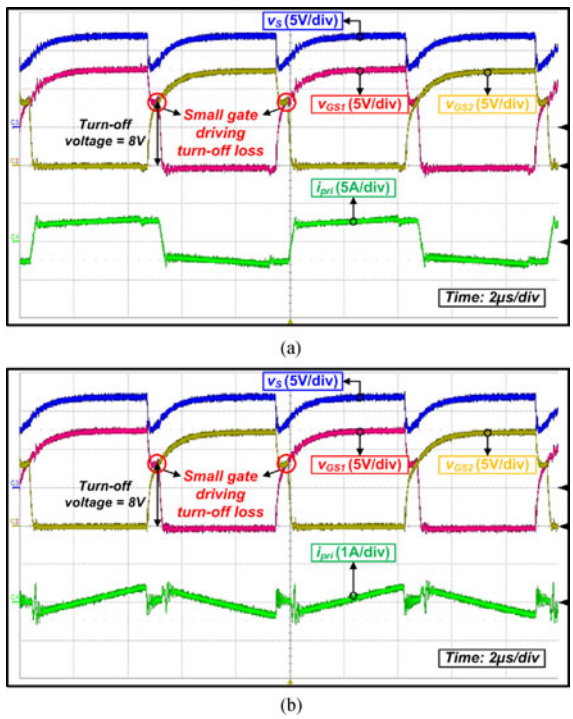

Fig. 11. Experimental waveforms with proposed SR gate driving circuit. (a) 100% load condition. (b) 1% load condition.

maximum output ripple voltage (ΔV_{O-max}) during 60% load change. However, from Fig. 12(b), the DCM control method degrades the dynamic performance due to the different voltage gain between DCM and CCM operations of the PSFB converter. In case of the proposed circuit, as shown in Fig. 12(c),

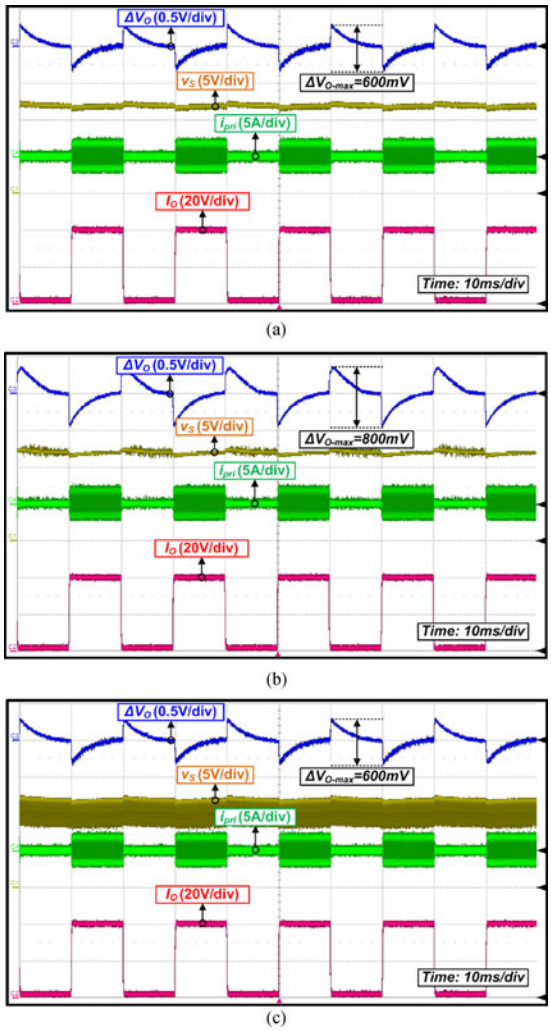

Fig. 12. Experimental waveforms during 60% load change (1 A ↔ 41 A). (a) Conventional circuit. (b) DCM control (SR on/off). (c) Proposed circuit.

the proposed circuit has the same maximum output ripple voltage ($\Delta V_{O-\max}$) with the conventional circuit, which is about 600 mV ($\pm 2.5\%$) during 60% load change. Therefore, the proposed circuit has good dynamic performance like the conventional circuit.

Fig. 13 shows the measured efficiency of the PSFB converter with conventional SR gate driving circuit, DCM control turning off SR under 10% load condition, and proposed SR gate driving circuit at the nominal input voltage ($V_S = 400$ V). The efficiency was measured with a power analyzer, i.e., Yokogawa WT1600. As shown in Fig. 13, the PSFB converter with the proposed circuit has similar efficiency to the PSFB converter with the convention SR gate driving circuit over 20% load conditions because the gate driving loss occupies small portion of total loss. On the other hand, the PSFB converter with proposed circuit has higher efficiency than the conventional circuit lower than or equal to 20% load conditions where the portion of the gate driving loss becomes dominant. The difference of efficiency is increased as the load current is decreased. Meanwhile, although the DCM control method can eliminate the gate driving loss

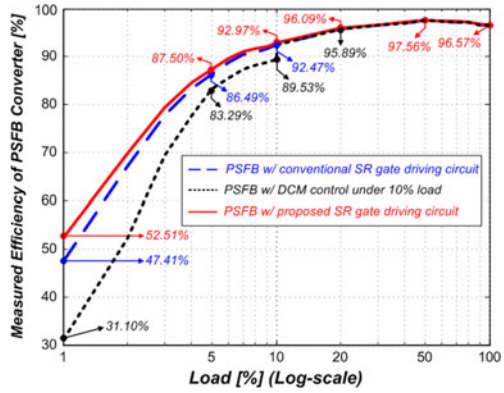

Fig. 13. Measured efficiency of PSFB converter in 1%–100% load condition at $V_S = 400$ V.

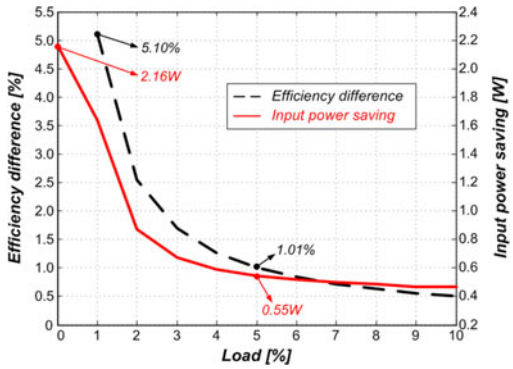

Fig. 14. Efficiency and input power comparison between PSFB converter with conventional and proposed circuits in 1%–10% load conditions.

and reduce the transformer core loss, the PSFB converter with the DCM control method has the lowest efficiency under 10% load conditions due to large conduction loss resulting from the body diode of the MOSFETs in SR. Moreover, it has very low efficiency under 5% load conditions because of large primary switching loss.

Fig. 14 shows the efficiency and input power comparison between the conventional and proposed circuits in 1%–10% load conditions. As expected from the efficiency graphs and (16), the input power saving of the proposed circuit is increased when the output load is getting lower. Especially, since the proposed circuit saves 2.16 W at no load condition, it directly reduces the idle mode power consumption

$$P_{\mathrm{IN-Pro.}} - P_{\mathrm{IN-Conv.}} = P_O \left(\frac{1}{\eta_{\mathrm{Pro.}}} - \frac{1}{\eta_{\mathrm{Conv.}}} \right) \tag{16}$$

where $P_{\mathrm{IN-pro.}}$, $P_{\mathrm{IN-conv}}$, $\eta_{\mathrm{pro.}}$, and $\eta_{\mathrm{conv.}}$ are the input power and efficiency of the PSFB converter with the proposed and conventional circuits, respectively.

VI. Conclusion

This paper presents a simple SR gate driving circuit to improve the light load efficiency of the PSFB converter with SR.

In the proposed circuit, one resistor ($R_{\rm IN}$) is added between $V_{\rm CC}$ and the input capacitor of the SR gate driver ($C_{\rm IN}$). Thus, the gate driving energy can be recycled during the turn-on operation of MOSFETs in SR, which reduces the SR gate driving loss. Moreover, the proposed circuit can adjust the reduced supply voltage ($V_{\rm RS}$) by designing $R_{\rm IN}$ and $C_{\rm IN}$. Furthermore, the proposed circuit can have good dynamic performance because it has no operation mode change. As a result, the proposed circuit can improve the light load efficiency without degradation of the dynamic performance, additional complex circuits, and additional control schemes. In summary, the proposed circuit is suitable for the practical server power supply using the PSFB converter with SR. In particular, the proposed circuit can be more promising in higher switching frequency conditions.

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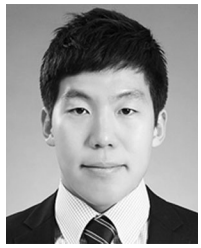

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