A New PWM and Commutation Scheme for One Phase Loss Operation of Three-Phase Isolated Buck Matrix-Type Rectifier

Jahangir Afsharian, Dewei Xu, *Member, IEEE*, Bin Wu, *Fellow, IEEE*, Bing Gong, and Zhihua Yang

***Abstract*—In this paper, a new pulse width modulation (PWM) scheme and commutation method is presented for one phase loss operation of three-phase isolated buck matrix-type rectifier. With the proposed PWM scheme, the maximum allowable voltage gain for one phase loss operation can be achieved, which permits the continuous operation of the converter to deliver two-third of the rated power and regulate the output voltage with maximum output voltage drop less than 5% of nominal output voltage. In addition, with the proposed commutation method, a safe transition from one phase loss operation to normal operation and vice versa can occur with minimum commutation steps (two-step) under zero-voltage switching condition. The performance of the proposed PWM scheme and commutation schemes with one phase loss operation is evaluated and verified by simulations and experiments on a 5 kW prototype.**

***Index Terms*—Buck rectifier, commutation, high frequency, isolated, matrix converter, MOSFET, one phase loss, pulse width modulation (PWM), three-phase, zero-voltage switching (ZVS).**

I. Introduction

IT IS shown that buck matrix-type power factor correction (PFC) rectifier topologies, as shown in Fig. 1, offer the advantage of performing PFC functionality and galvanic isolation in a single-stage conversion [1]–[7]. High conversion efficiency and compact construction stemming from the nonexistence of an intermediated dc-link capacitors and the second stage dc–dc conversion can be attributed to this family of converters. The three-phase buck matrix-type rectifier is a zero-voltage switching (ZVS) converter and the isolated ZVS rectifier is an excellent candidate for the applications in which the SiC MOSFETS are the most favorable device choice. It should be noted that ZVS here refers to zero voltage turn-ON and is used to reduce the switching losses only at turn-ON [4]. Due to the fact that SiC MOSFET tends to have low turn-OFF loss but high turn-ON loss, SiC MOSFET operating at ZVS can achieve much lower switching losses while it switches at high frequency. The significant benefits of using SiC MOSFET in matrix converters and others are also well proven in [8]–[10], and all these benefits cannot be obtained with the use of Si insulated gate bipolar transistor (IGBT) devices instead. The three-phase buck-type rectifiers provide a wide output-voltage control range down to low voltages while maintaining PFC capability at the input. However, despite of good efficiency and power density, the matrix converters are still not widely used in industry. One possible reason for their limited utilization is the complex modulation scheme required simultaneously to perform PFC and isolated dc–dc conversion over the entire load and input range especially under abnormal grid conditions. The main objective of this paper thus lies in the analysis and performance evaluation of the three-phase buck matrix-type rectifier for one phase loss operation (one of the three-phase inputs is shorted or disconnected).

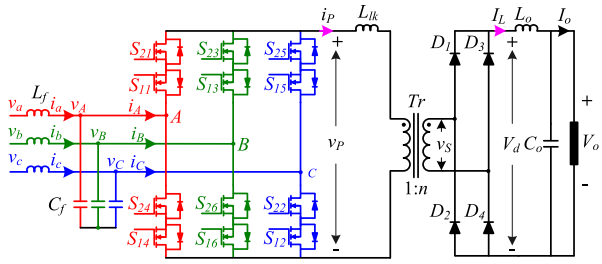

Fig. 1. ZVS three-phase PWM rectifier.

The three-phase buck matrix-type rectifier design concept is not limited to applications in the 380 V dc data centers and 48 V dc Telecom market. It can be also leveraged to other types of applications, e.g., electric vehicle (EV) charging stations and on board three-phase EV charger, where the output voltage needs to be changed widely (200 to 450 V dc) [11], [12]. However, in here, the example of power supply operation in data center and telecom are chosen because of the stringent requirement of delivering two-third of the rated power to the output load during one phase loss operation.

This specification requirement can be easily fulfilled with two-stage power supply due to the large storage energy on the output of first-stage ac–dc and second-stage dc–dc converter for isolation and tight output voltage regulation. The significant advantage of two-stage power conversion that should be

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highlighted in here is the capability of delivering two-third of the rated power to the load with tight output voltage regulation during fault condition of one phase loss operation [13]–[15]. Though, all the functions realized in the two-stage scheme can be also achieved in a single-stage converter without performance compromise as reported in [16]. However, with a matrix-type rectifier, it is challenge to satisfy this requirement due to the lack of intermediate storage energy. The major challenge for matrix-type rectifier is delivering output power and regulating output voltage simultaneously during one phase loss operation. The traditional pulse width modulation (PWM) schemes which are derived for matrix-type rectifier and summarized in [17] cannot be directly applied for one phase loss operation. Therefore, the main focus of this paper is on developing a viable PWM scheme to maintain proper operation of the converter during one phase loss condition as well as to provide smooth transitions between the one phase loss and normal modes. Since it is a big challenge for the single-stage buck matrix-type converter to maintain proper output voltage under this faulty mode and guarantee safe operation during the transitions, this paper aims to provide solutions to these issues.

The rest of this paper is organized as follows. Operation principle and the proposed PWM scheme for one phase loss operation is provided in Section II. The analysis of transition from one phase loss to normal operation and vice versa and commutation method is described in Section III. Simulated and experimental results are presented in Sections IV and V, respectively, followed by the conclusion in Section VI.

II. Operation Principle and the Proposed PWM Scheme for One Phase Loss Operation

The converter topology and modulation scheme for normal operation (all the three phases are operating) is derived and explained in [17]. However, none of the PWMs in [17] can be directly applied for one phase loss operation. With them, the converter cannot regulate the output voltage even with very large value of output storage energy. In addition, the possibility of converter switches failure is high due to shoot through between switching actions during the transition from one phase loss to normal operation. Therefore, deriving a new PWM and commutation scheme is indispensable for safe operation of converter during one phase loss operation. The proposed PWM and commutation scheme works under ZVS condition while the converter can deliver two-third of the rated power to the load and regulate the output voltage with maximum voltage drop less than 5% of nominal output voltage simultaneously.

A. Operation Principle of Isolated Buck Matrix-Type Rectifier During One Phase Loss

The converter switches are operated according to the space vector modulation presented in [18] during normal operation. Within any 30° interval between two successive zero crossings of input phase voltage, there are two line voltages that do not change sign as shown in Fig. 2. For example, during interval of $-30° < \theta < 30°$ (shaded area), the line voltages $v_{AB} = v_A - v_B$ and $v_{AC} = v_A - v_C$ are positive, and they both attain their maximum in this interval. Since the switching frequency of the converter is much higher than the line frequency, the two line voltages can be treated as slow-varying dc voltages. Therefore, the three-phase converter can be redrawn as two full-bridge phase-shifted (FB-PS) converter. For example, in sector I, the three-phase converter can be redrawn as "bridge *x*" and "bridge *y*" as shown in Fig. 3(a). Operation of "bridge *x*" and "bridge *y*" is similar to (FB-PS) converter [19]. When one phase is lost ("phase *C*" is lost for all the analysis in this paper), the bridge connected to this phase has to stop operation since no power can be delivered from this bridge. Otherwise, this may cause severe damage to the converter switches due to high switching stress. Therefore, the control scheme of the converter needs to be adapted to allow the other bridge continuous operating. As shown in Fig. 3(b), when "phase *C*" is lost, "bridge *y*" (in dashed line) will stop working and "bridge *x*" continue operating in the same way as an FB-PS. The circuit principal waveforms within one gird side cycle with excessively increased switching period of PWM when phase voltage v_c is shorted can be observed in Fig. 4, where v_P is the transformer primary voltage, V_d is the transformer secondary rectified voltage, I_L is the output inductor current, and i_a, i_b, i_c are grid side currents. Since v_{AB}, the input voltage of "bridge *x*", is slow varying, the duty cycle of the transformer voltage v_P or V_d needs to be adjusted accordingly in order to regulate the output voltage. However, when the magnitude of v_{AB} becomes low such that the magnitude of V_d is lower than V_o as shown in Fig. 4(c), the duty cycle reaches to maximum and V_o starts losing regulation. In this case, the converter should stop gating to reduce the gating losses and other associated losses. It is important to be noted that a large output ripple may be gen-

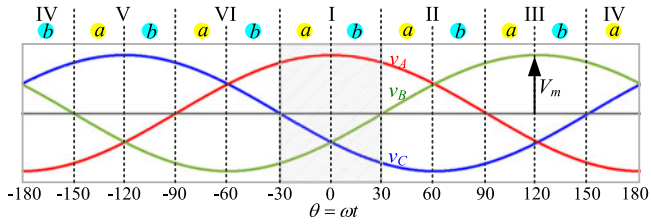

Fig. 2. Input phase voltages with sector division corresponding to [18, Fig. 4].

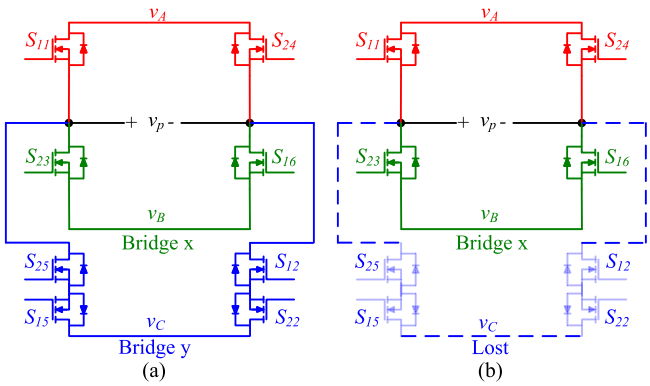

Fig. 3. Three-phase converter redrawn as: (a) two ZVS full-bridge dc-dc converters when the three phases are connected (b) a ZVS full-bridge dc-dc converters when one phase is lost ("phase *C*").

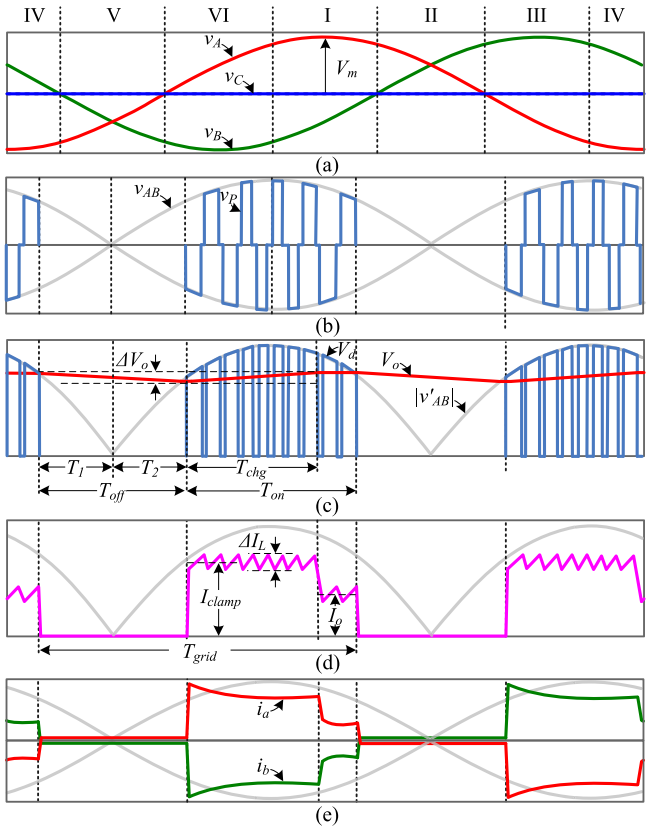

Fig. 4. Three-phase converter operation with "phase *C*" is shorted.

erated since the output voltage is only sustained by the output capacitors during the interval of $T_{\rm off}$. The ripple voltage ΔV_o is the function of $T_{\rm off}$, output capacitance C_o, and load current I_o, and can be derived as follows:

$$\Delta V_o = \frac{I_o T_{\rm off}}{C_o}. \tag{1}$$

The envelope of V_d is the absolute value of v_{AB} with respect to the secondary side and can be expressed as $|v'_{AB}| = n\sqrt{3}V_m \sin(\omega t)$, where n is the transformer turns ratio. The output voltage can be expressed as $V_o = \frac{3}{2} n V_m m_a$ where m_a is the modulation index [17]. Assuming the duty cycle loss of the buck converter is very small and can be neglected, $T_{\rm off}$ is the distance between the two adjacent crossing points when $|v'_{AB}|$ is lower than V_o. It is also assumed $T_1 = T_2$, since the ripple voltage ΔV_o is relatively small as compared to V_o. The location of these two adjacent crossing points can be found by equaling $|v'_{AB}|$ and V_o. Then, the $T_{\rm off}$ can be estimated by the following:

$$T_{\rm off} = \frac{\sin^{-1}\left(\frac{\sqrt{3}}{2} m_a\right)}{\pi f_{\rm grid}} \tag{2}$$

where $f_{\rm grid}$ is the grid frequency.

By combining (1) and (2), the ripple voltage ΔV_o is described as follows:

$$\Delta V_o = \frac{I_o \sin^{-1}\left(\frac{\sqrt{3}}{2} m_a\right)}{C_o \pi f_{\rm grid}}. \tag{3}$$

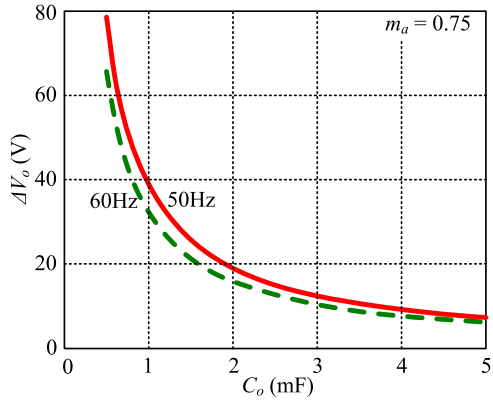

Fig. 5. Output voltage drop ΔV_o versus output capacitance C_o for one phase loss operation at $2/3 P_{o\_\max}$.

When one phase is lost, the output power is reduced to two-third of the rated power in order to limit the "rms" value of phase currents $i_{a,b,c}$ to 1.2 times of the rated phase currents.

The output voltage drop ΔV_o versus output storage energy C_o at $m_a = 0.75$ (the nominal input line to line voltage, $v_{LL} = 480$ V) when one phase is lost can be drawn as shown in Fig. 5 for 380 V output voltage. The output voltage drop is inversely proportional to the output capacitance of C_o. The m_a and grid frequency are also important in determining the voltage drop. Either higher m_a or lower grid frequency will result in higher voltage drop.

One of the criteria of selecting capacitance of C_o is that the resultant maximum output voltage drop ΔV_o should be smaller than the difference between the set point of output voltage and the set point of the battery voltage such that to avoid the battery engagement during one phase loss operation. For example, if the battery voltage set point is 360 V, the maximum of ΔV_o should be smaller than 20 V.

A reasonable value of 2.0 mF for the output capacitance is selected as a compromise between the output voltage ripple and power density of the converter.

Current stress is another important consideration when the converter is operating during one phase loss. As shown in Fig. 4(d), the output inductor current ramps up very fast and reaches to the maximum value of $I_{\rm clamp}$ due to the fast response of the current control loop and large voltage error at the beginning of $T_{\rm on}$. $I_{\rm clamp}$ is the upper clamping value for the current control loop. During the interval of $T_{\rm chg}$, the output capacitor is charged by the current of $(I_{\rm clamp} - I_o)$, and the output voltage rises up until it reaches to the set point (380 V). During the interval when the output voltage is regulated at the set point, the inductor current equal to the load current and no charging and discharging currents go through the output capacitor (neglecting the inductor current switching ripple). Since the output capacitor is discharged by I_o during $T_{\rm off}$ and based on the current-second balance of the output capacitor, the relationship between $I_{\rm clamp}$ and I_o can be derived as follows:

$$(I_{\rm clamp} - I_o)\, T_{\rm chg} = I_o T_{\rm off}. \tag{4}$$

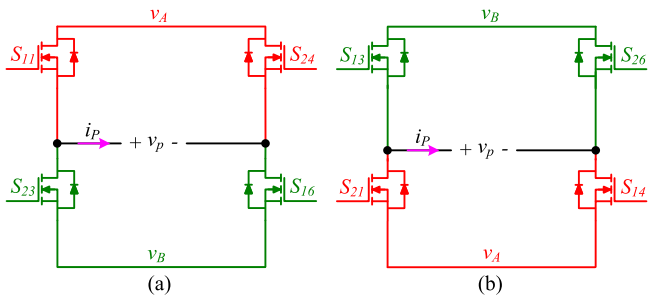

Fig. 6. Three-phase converter equivalent circuit with assumption phase leg *C* lost (a) during interval $v_A > v_B$ (b) during interval $v_A < v_B$.

Since $T_{\rm chg} \le T_{\rm on}$, the minimum value of $I_{\rm clamp}$ is derived at $T_{\rm chg} = T_{\rm on}$ as shown in the following equation:

$$I_{\rm clamp\_min} = \frac{I_o\,(T_{\rm off} + T_{\rm on})}{T_{\rm on}} = \frac{I_o T_{\rm grid}}{T_{\rm grid} - T_{\rm off}} \tag{5}$$

where $T_{\rm grid} = 1/(2f_{\rm grid})$is the grid half-cycle duration.

Considering the maximum load current of one phase loss operation $I_o = 2/3 I_{\rm rated}$ and substituting $T_{\rm off}$ with (2) and $T_{\rm grid}$ with $1/(2f_{\rm grid})$ into (5), $I_{\rm clamp\_min}$ can be described as follows:

$$I_{\rm clamp\_min} = \frac{\frac{2}{3} I_{\rm rated}}{1 - \frac{2}{\pi}\sin^{-1}\left(\frac{\sqrt{3}}{2} m_a\right)}. \tag{6}$$

Reduced $I_{\rm clamp}$ can reduce the current stress of the converter during one phase loss operation and the output inductor can be designed with smaller size and lower cost. However, $I_{\rm clamp}$ should be higher than $I_{\rm clamp\_min}$ in order to deliver $2/3\,P_{o\_\max}$ during one phase loss operation. Considering $m_a = 0.75$, the minimum value of $I_{\rm clamp}$ should be 1.2 times of the rated output load current. For the worst case at $m_a = 1$, the minimum value of $I_{\rm clamp}$ should be 2 times of the rated output load current.

B. Proposed PWM Scheme for One Phase Loss Operation

Within every 180° interval, the three-phase converter is operated as a ZVS FB-PS PWM dc–dc converter [4] as shown in Fig. 6. To achieve ZVS, the two legs of the bridge are operated with a phase shift [19]. The zero-voltage turn-ON is achieved by using the energy stored in the leakage inductance of the transformer to discharge the output capacitance of the switches before turning them ON. During every 180° interval, 8 of the 12 switches are involved and the switches connected to the leg with phase loss are not operating. All the switches of the converter turned ON under ZVS condition and turned OFF with hard switching. Among these eight switches, four switches operate as active switches and the other four switches operate as synchronous rectification switches to reduce the conduction losses. For example, during the 180° interval where the voltage potential v_A is higher than v_B $(v_A > v_B)$, the switches S_{14}, S_{21}, S_{13}, and S_{26} of bridge are synchronous rectification switches and can be kept ON all the time since their body diodes are forward biased. The rest four switches $(S_{11}, S_{24}, S_{23}, S_{16})$ operate in a same manner of ZVS FB-PS converter. Similarly, during the other 180° interval, where the voltage potential v_B is higher than v_A $(v_B > v_A)$, the switches S_{23}, S_{16}, S_{11}, and S_{24} can be kept ON all the time since their body diodes are forward biased. The rest four switches $(S_{21}, S_{14}, S_{13}, S_{26})$ operate in a same manner of ZVS FB-PS converter. The corresponding switch gate signals during one switching period T_s is shown in Fig. 7. It is important to be noted that there are two possible switching patterns in each 180° interval. For example, during the 180° interval with $v_A > v_B$, there are two types of switching patterns as shown in Fig. 7(a) and (c), respectively. In each switching cycle, there are two bypassing intervals where switches of either "phase leg *A*" or "phase leg *B*" are used for bypassing ($v_P = 0$). As shown in Fig. 7(a), switches (S_{16}, S_{23}) of "phase leg *B*" are used for bypassing in the first bypassing interval and switches (S_{11}, S_{24}) of "phase leg *A*" are used in the second bypassing interval. While in the switching pattern of Fig. 7(c), switches (S_{11}, S_{24}) of "phase leg *A*" are used for bypassing in the first bypassing interval and switches (S_{16}, S_{23}) of "phase leg *B*" are used in the second bypassing interval. Identical voltage on the transformer primary side can be generated by these two switching patterns. However, the switching pattern needs to be properly selected in each sector to enable a smooth transition from one phase loss operation to normal operation (the loss phase recovered). In order to facilitate a smooth transition from one phase loss operation to normal operation, the switching state during the second bypassing interval at the end of each switching cycle must be the same as the bypassing switching state for normal operation. For normal operation, the switches of the phase leg whose voltage has the highest magnitude are used for the two bypassing (zero vector) intervals in each switching cycle [17, Fig. 3]. Both normal operation and one phase loss operation must use the same phase leg for bypassing at the end of the switching cycle. For example, in sector I and sector IV, phase voltage v_A has the highest magnitude and the switches of "phase leg *A*" are used for bypassing at end of the switching cycle as shown in Fig. 7(a) and (d). Similarly, in sector III and VI, the switches of "phase leg *B*" are used for bypassing at the end of the switching cycle as shown in Fig. 7(b) and (c). Detailed analysis of the transition from one phase loss operation to normal operation will be discussed in the next section.

III. Analysis of Transitions and the Proposed Commutation Method

A. Transition From One Phase Loss to Normal Operation and Vice Versa

As discussed in [17], two-step commutation with ZVS can be achieved for the transition from zero state to active state or from active state to zero state during normal operation. Zero state refers to the switching state of zero vectors or bypassing state, while active state refers to the switching state for active vectors. It is important to be noted that the corresponding modulation scheme is critical to facilitate this two-step commutation. Due to the inductive current on the transformer primary side, the continuity of the transformer primary current has to be ensured during the commutation. Therefore, the adjacent zero state and active state in the modulation scheme is arranged such that there is a common phase leg involved in both active state and the zero state. The same criteria can

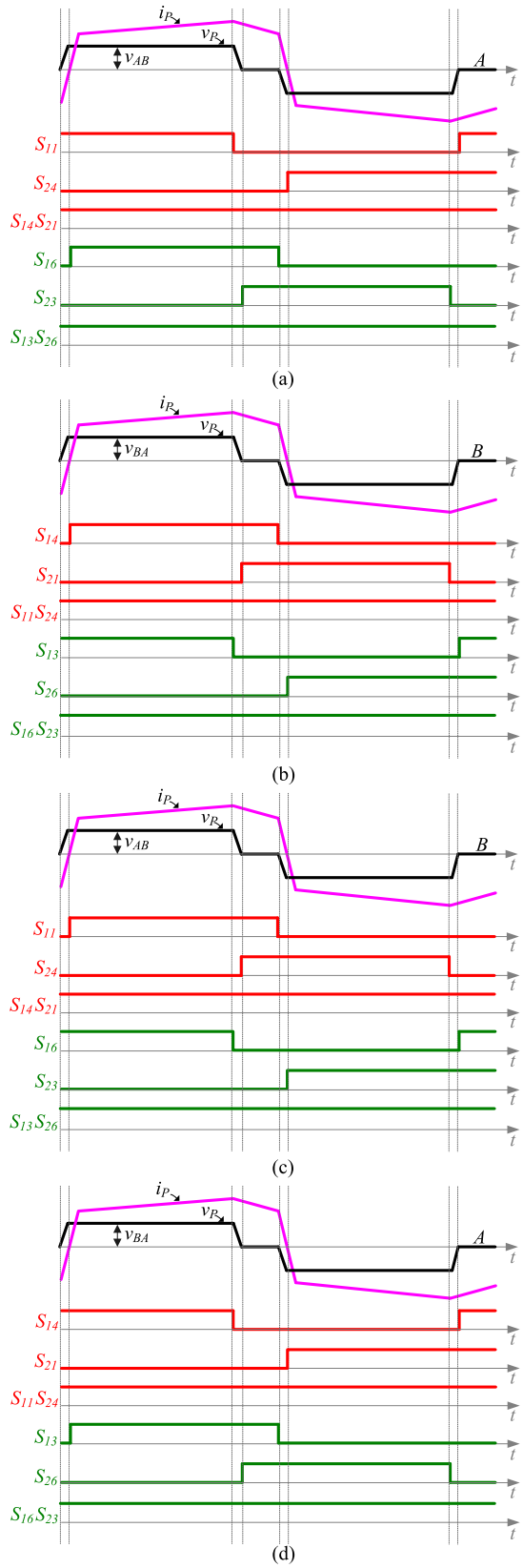

Fig. 7. Three-phase converter operation with one phase loss during interval of: (a) sector I with "phase leg *A*" for bypassing time at the end of the switching cycle, (b) sector III with "phase leg *B*" for bypassing time at the end of the switching cycle, (c) sector VI with "phase leg *B*" for bypassing time at the end of the switching cycle, (d) sector IV with "phase leg *A*" for bypassing time at the end of the switching cycle.

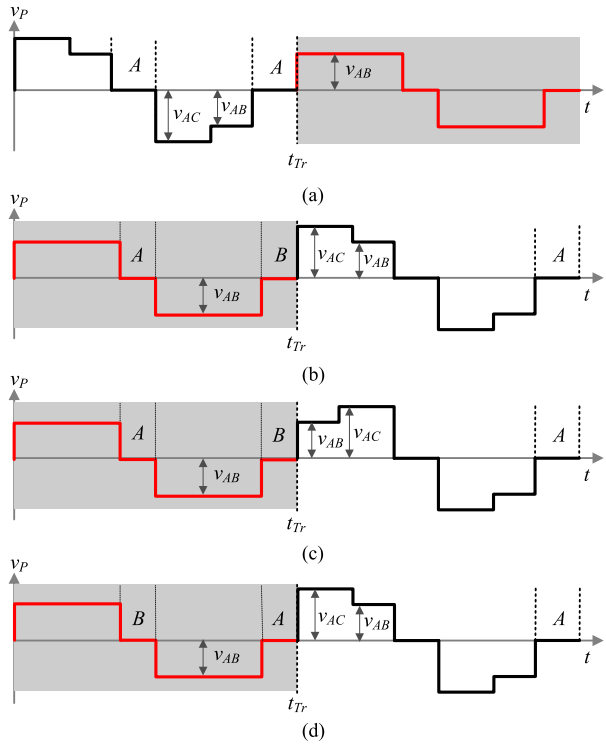

Fig. 8. Transformer primary side voltage transition in sector I (b) (shaded area represents one phase loss operation): (a) from normal operation to one phase loss operation, (b) from one phase loss operation to normal operation using "phase leg *B*" for bypassing prior to t_{Tr}, (c) from one phase loss operation to normal operation using "phase leg *B*" for bypassing prior to t_{Tr} and with modified switching sequence for first cycle of normal operation (LTH) [17], [see Fig. 4(b)], (d) from one phase loss to normal operation using "phase leg *A*" for bypassing prior to t_{Tr}.

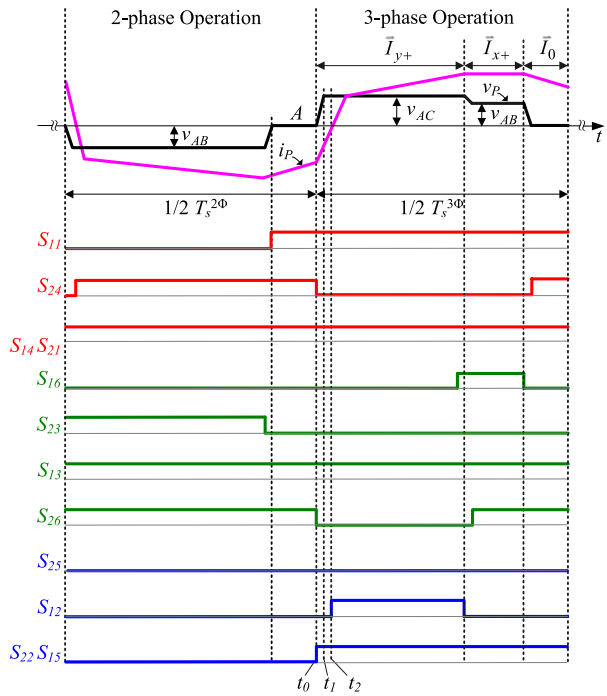

Fig. 9. Detail transition from one phase loss to normal operation of "Fig. 8(d)" in above with the waveforms of transformer primary side voltage v_P and current i_P and corresponding switch gate signals ($T_s^{2\Phi}$ is period of two-phase operation and $T_s^{3\Phi}$ period of three-phase operation).

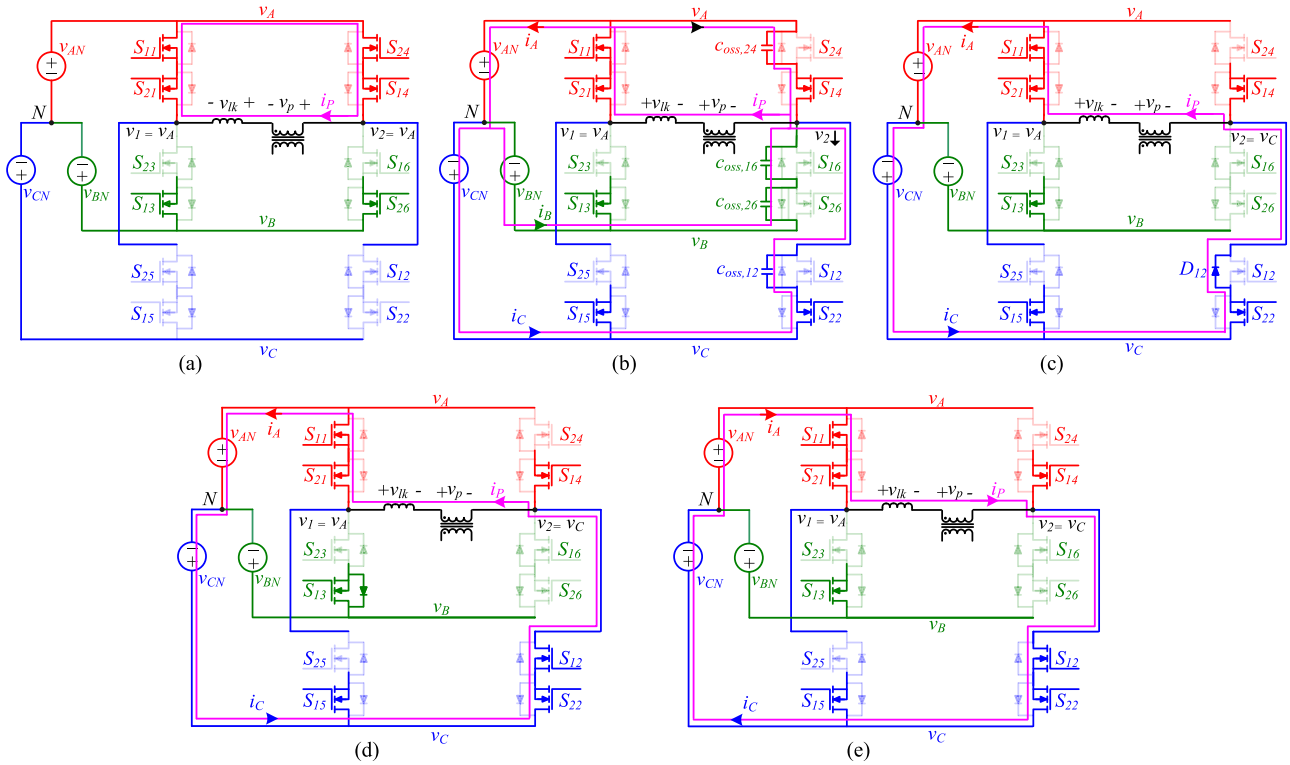

Fig. 10. Switching transitions during one phase loss operation to normal operation: (a) at t_0^-, (b) at t_0^+, (c) at t_1, (d) at t_2, (e) at t_2^+.

be used to examine the transitions from normal operation to one phase loss operation or from one phase loss operation to normal operation. As shown in Fig. 8(a), in sector I, smooth transition from normal operation to one phase loss operation (shaded area) can be achieved with two-step commutation since "phase leg *A*" is involved in both the zero state prior to the transition and the active state after the transition. Another case as shown in Fig. 8(b), there is no common phase involved in both the states. As a result, the converter primary current cannot be switched from leg *B* to leg *A* and leg *C* directly using two-step commutation, therefore, more commutation steps are required. One of the solutions is to modify the switching sequence of the first cycle for normal operation, as shown in Fig. 8(c), to have the active vector with "phase leg *B*" come first. Then, smooth transition with two-step commutation can be achieved. However, the transition between the two active vectors in the first half-cycle of the normal operation is hard switching and suffers from large diode reverse recovery of MOSFET since the switching pattern becomes low to high (LTH) as discussed in [17, Fig. 4]. This may not be a significant problem since this transition only happened once, but this solution will increase the complexity of switching scheme implementation. A better solution, as shown in Fig. 8(d), is to select the switching pattern for one phase loss operation to have the same phase leg for zero state at the end of switching cycle as that for zero state in the normal operation. Then, the criteria for two-step commutation are always satisfied.

To further facilitate the explanation of transition from one phase loss to normal operation, the commutation steps are demonstrated in Figs. 9 and 10 using an example of the transition from zero state of one phase loss operation (two-phase operation when "phase *C*" is lost) to active vector $\vec{I}_{y+}$ of normal operation (three-phase operation when "phase *C*" is recovered) in sector I (b). Fig. 9 shows the PWM gate signals and Fig. 10 shows the equivalent circuit at different stages of the transition. At t_0^-, the switching state is the zero state for "phase *C*" loss operation, where the "phase leg *A*" is used for by passing (all the switches of "phase leg *A*" are ON) and the current i_P is circulating through the primary side of transformer as shown in Fig. 10(a). The voltage across transformer v_P is zero and voltage potential at the two terminals of the transformer v_1 and v_2 is equal to v_A.

The first step of the two-step commutation is to turn ON switches S_{15}, S_{22} and turn OFF switches S_{24}, S_{26} at t_0^+. Then,

TABLE I
EXPERIMENTAL PROTOTYPE PARAMETERS

Prototype Parameter	Value
C_f	5 μF
L_f	110 μH
$v_{LL,\mathrm{rms}}$	400/480 V
f_{grid}	50/60 Hz
C_o	2.0 mF
L_o	315 μH
V_o	380 V
L_{lk}	16.5 μH
S_{11}–S_{26}	SCT3080KL
D_1–D_4	SCS215KG
N	0.86
T_r	Ferrite core (ZP47313TC)
f_{sw}	50 kHz

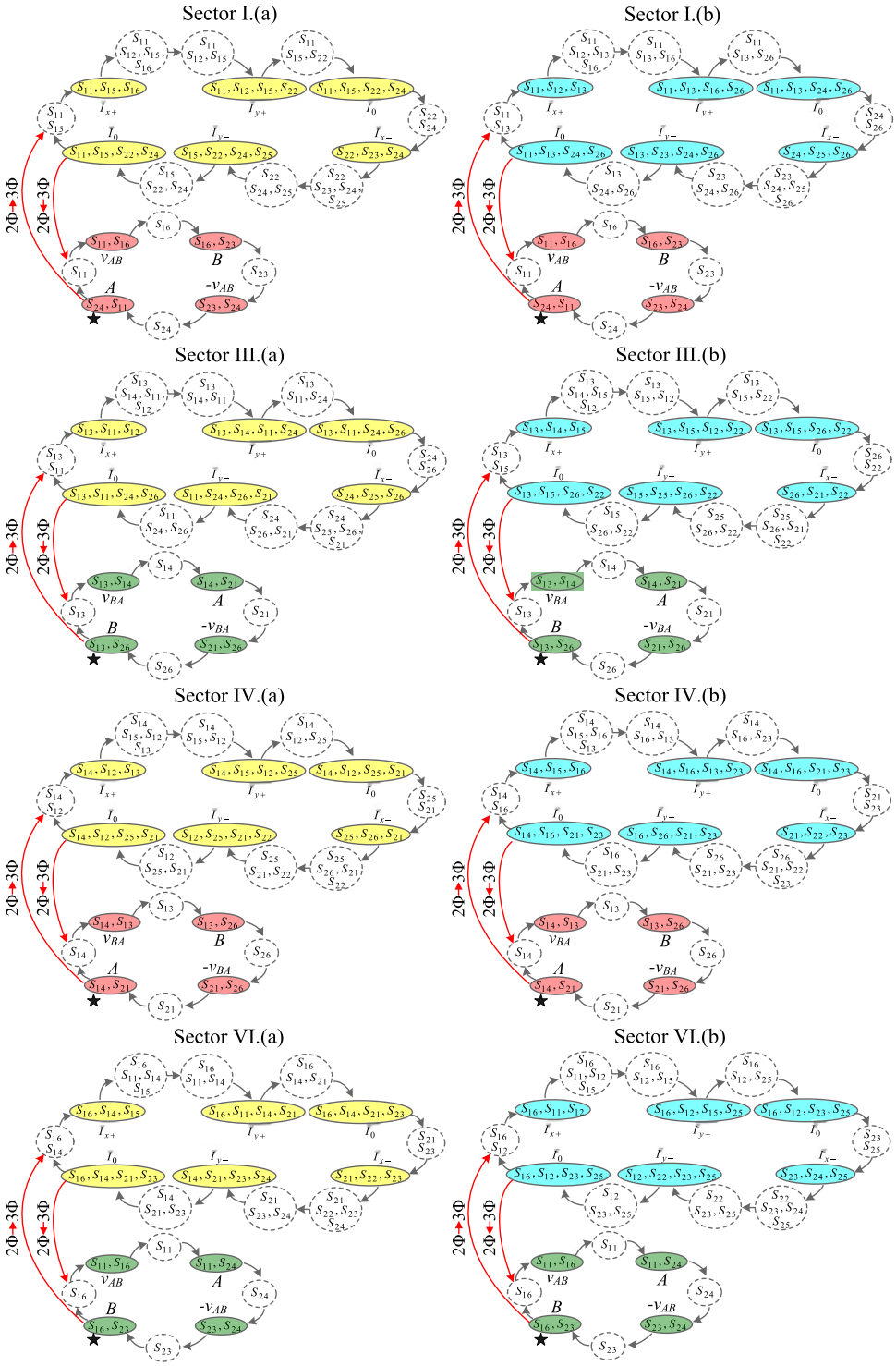

Fig. 11. Finite commutation state machine from normal operation (3Φ represents three-phase operation) to one phase loss (2Φ represents two-phase operations) and vice versa: two-step commutation realized for one phase loss operation, for the transition from one phase loss to normal operation and vice versa, for normal operation of zero vector to active vector and vice versa, three-step commutation realized for active vector to another active vector in normal operation (star represents the end of switching cycle of one phase loss operation).

the circulating path for current i_P is broken and current i_P charges or discharges the output capacitance of S_{24}, S_{16}, S_{26}, and S_{12} as shown in Fig. 10(b). As a result, the voltage v_2 is going down until, at t_1, v_2 reaches to v_C and the body diode D_{12} of switch S_{12} conducts as shown in Fig. 10(c). During this commutation step, the switches S_{15}, S_{22} are turned ON at ZVS condition for synchronous rectification since v_C has the lowest potential and their body diodes are forward biased. Switch S_{26} is turned OFF at zero current. Turning OFF S_{24} is hard switching. The second step of the two-step commutation

happens at t_2, where S_{12} is turned ON under ZVS condition before i_P change the direction as shown in Fig. 10(d). When i_P ramps up to the same value as output inductor current with respect to the primary side, the transition from zero state of one phase loss operation ("phase *C*" loss) to active vector $\vec{I}_{y+}$ of normal operation is completed. Fig. 10(e) shows the equivalent circuit of active vector $\vec{I}_{y+}$ of normal operation.

This is a smooth transition with easy implementation since no extra step is needed compared with the commutation during normal operation or during one phase loss operation.

B. Proposed Commutation Method

The corresponding switch gate signals for normal operation during one switching period T_s can be found in [17, Table I]. In [17, Table I], $\vec{I}_{x+}$ and $\vec{I}_{x-}$ represent switching states of vector $\vec{I}_x$ when $i_P > 0$ and $i_P < 0$, respectively, with equal dwell time of $T_x/2$. In addition, $\vec{I}_{y+}$ and $\vec{I}_{y-}$ represents switching states of vector $\vec{I}_y$ when $i_P > 0$ and $i_P < 0$, respectively, with equal dwell time of $T_y/2$. The finite commutation state machines within six sectors operation for normal operation are shown in [17, Fig. 9(c) and (d)].

The commutation state machines with the proposed commutation method from one phase loss operation (two-phase operation) to normal operation (three-phase operation) and vice versa are shown in Fig. 11. It is important to note that Fig. 11 illustrates the commutation state machines in sector I, III, IV, and VI except II and V since the "phase *C*" is lost (the converter switches stop gating in sectors II and V). The transition states (in dashed line) are added between main states (in shaded color) to achieve zero voltage turn-ON and synchronous rectification operation. Two-step commutation is applied for the normal operation transitions from active vector to zero vector and from zero vector to active vector, while three-step commutation is required for transitions from active vector to another active vector [17]. In different sectors, as shown in Fig. 11, different commutation state machines are applied to one phase loss operation according to the switching patterns described in Fig. 7. Therefore, two-step commutation is achieved for transition of from normal operation to one phase loss operation and vice versa.

IV. Simulation Results

To verify the proposed PWM modulation and commutation schemes for one phase loss operation, a simulation model is built and tested at $2/3P_{o\_\max} = 3.3$ kW. Fig. 12 shows the operation of one phase loss at $f_{\text{grid}} = 60$ Hz, $v_{LL} = 480$ V, $C_o = 2.0$ mF, and $m_a = 0.75$. The upper limit of the average output inductor current, I_{clamp} in one phase loss operation is set at 16 A (1.22 I_{rated}), which is higher than the minimum required inductor current at $m_a = 0.75$ as described in (6). The simulation result in here verifies the proposed PWM scheme derived for one phase loss operation and the analysis provided above. As shown in Fig. 12, at t_1, the phase is shorted and at t_2 is recovered. The maximum output voltage drop is above the battery set point to avoid the battery engagement during one phase loss.

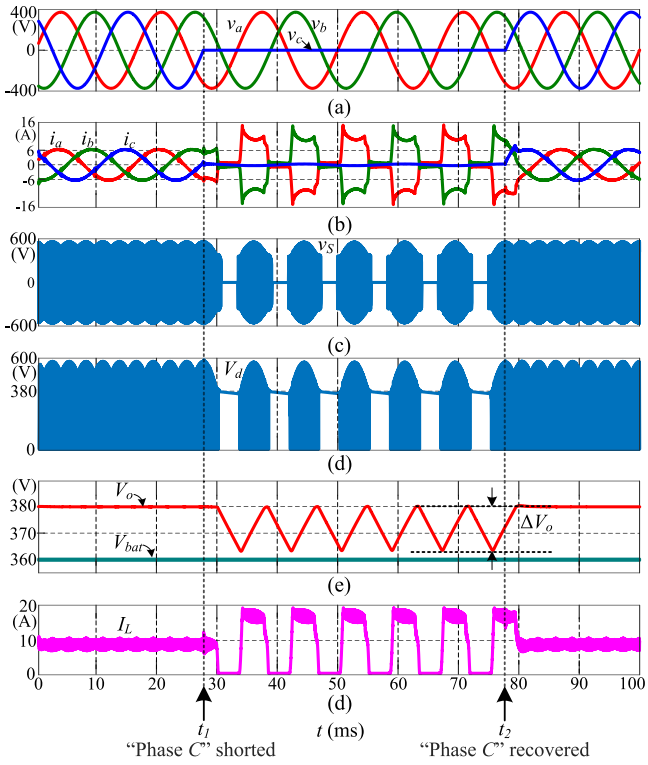

Fig. 12. Simulated waveforms for $2/3P_{O\_\max}$, $v_{LL} = 480$ V and $m_a = 0.75$ when "phase *C*" is shorted at t_1 and recovered at t_2: (a) input phase voltages, (b) input phase currents, (c) transformer secondary voltage, (d) output of bridge rectifier, (e) output voltage and battery set point, (f) output inductor current.

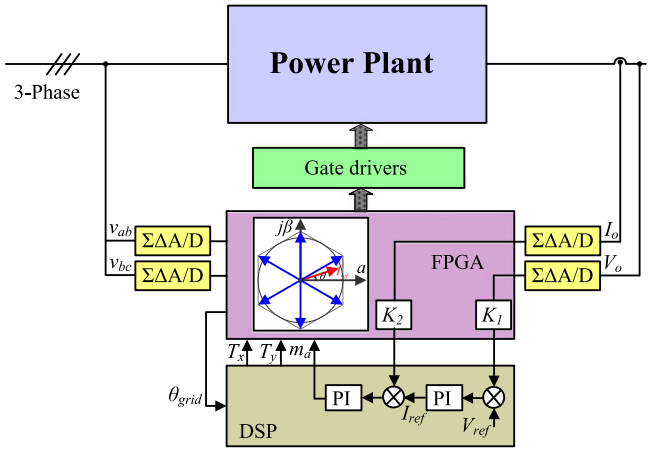

Fig. 13. Control block diagram of the converter.

V. Experimental Results

The experimental prototype is set up at the rated output power of 5 kW and regulated output voltage 380 V when all the three phases are connected. Detailed experimental system parameters are listed in Table I. The control block diagram of the converter is shown in Fig. 13.

An RCD snubber is added to the bridge rectifier in Fig. 1 to reduce the ringing and spike at the output of bridge rectifier.

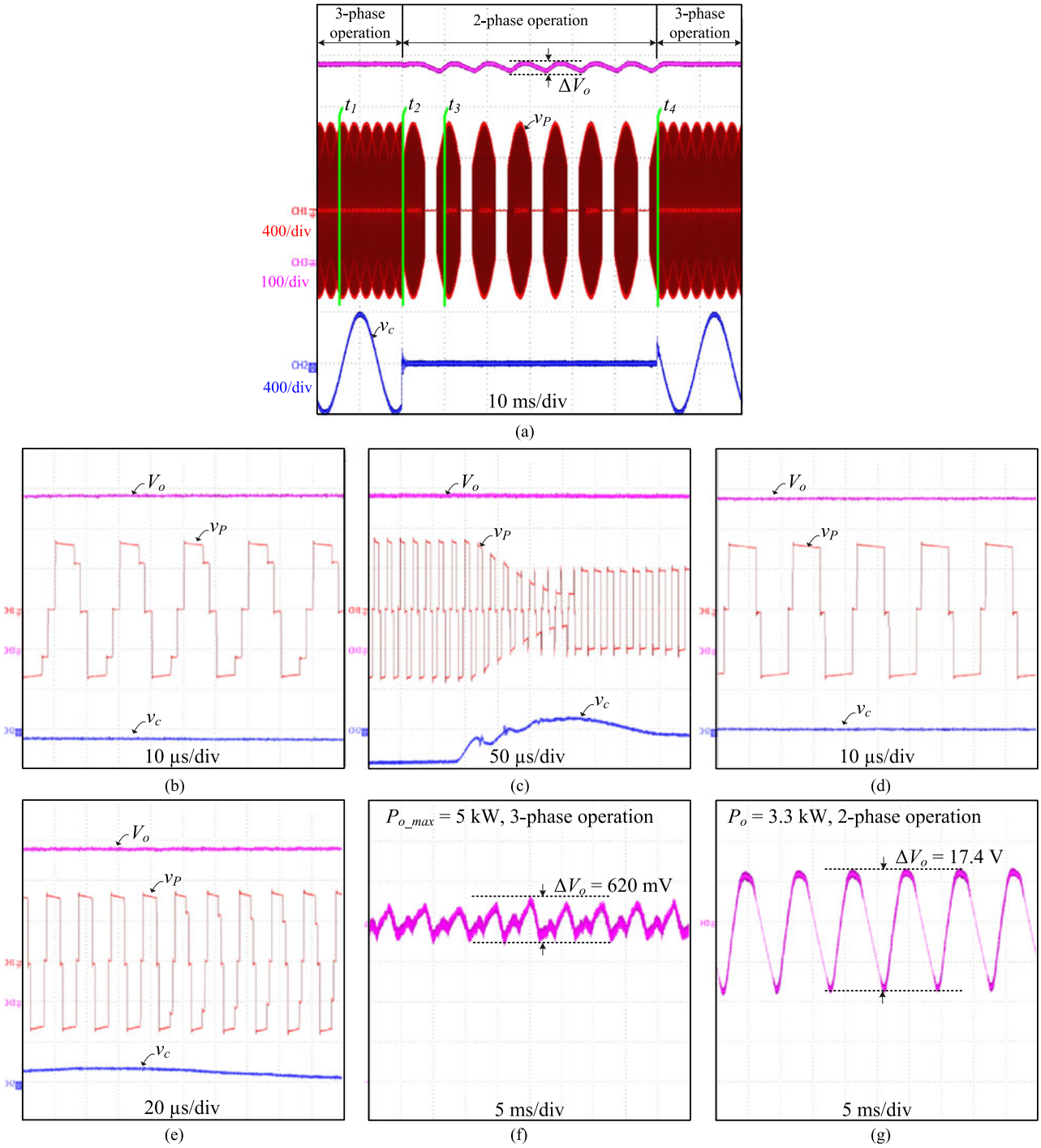

Fig. 14. Experimental waveforms for $2/3P_{o\_\max} = 3.3$ kW, $v_{LL} = 480$ V, $f_{\text{grid}} = 60$ Hz: (a) voltage waveforms of v_P, v_{LL}, V_o, (b) at t_1, normal operation (three-phase operation), (c) at t_2, instant "phase *C*" is shorted, (d) at t_3, one phase loss operation (two-phase operation), (e) at t_4, instant "phase *C*" recovered, (f) ac ripple of voltage V_o in normal operation at maximum output power $P_{o\_\max} = 5$ kW, (g) ac ripple of voltage V_o in one phase loss operation.

The experimental waveforms in Figs. 14 and 15 illustrate the operation when one phase is shorted and then recovered. For the experimental in one phase loss operation, the output power is reduced to 3.3 kW (two-third of the rated output power) in order to limit the "rms" value of phase currents $i_{a,b,c}$ to 1.2 times of the rated phase currents. As shown from transformer primary side voltage in Fig. 14(c) and (e), a smooth transition occurs at two intervals t_2 and t_4 when "phase *C*" is shorted and then recovered.

As shown in Fig. 15(b), the upper limit of the average output inductor current I_{clamp} in one phase loss operation (two-phase operation) is 16 A, which is consistent with the analysis provided in "Section II-A)" and the simulation results in Fig. 12(f). The output voltage is regulated tightly at 380 V in normal operation

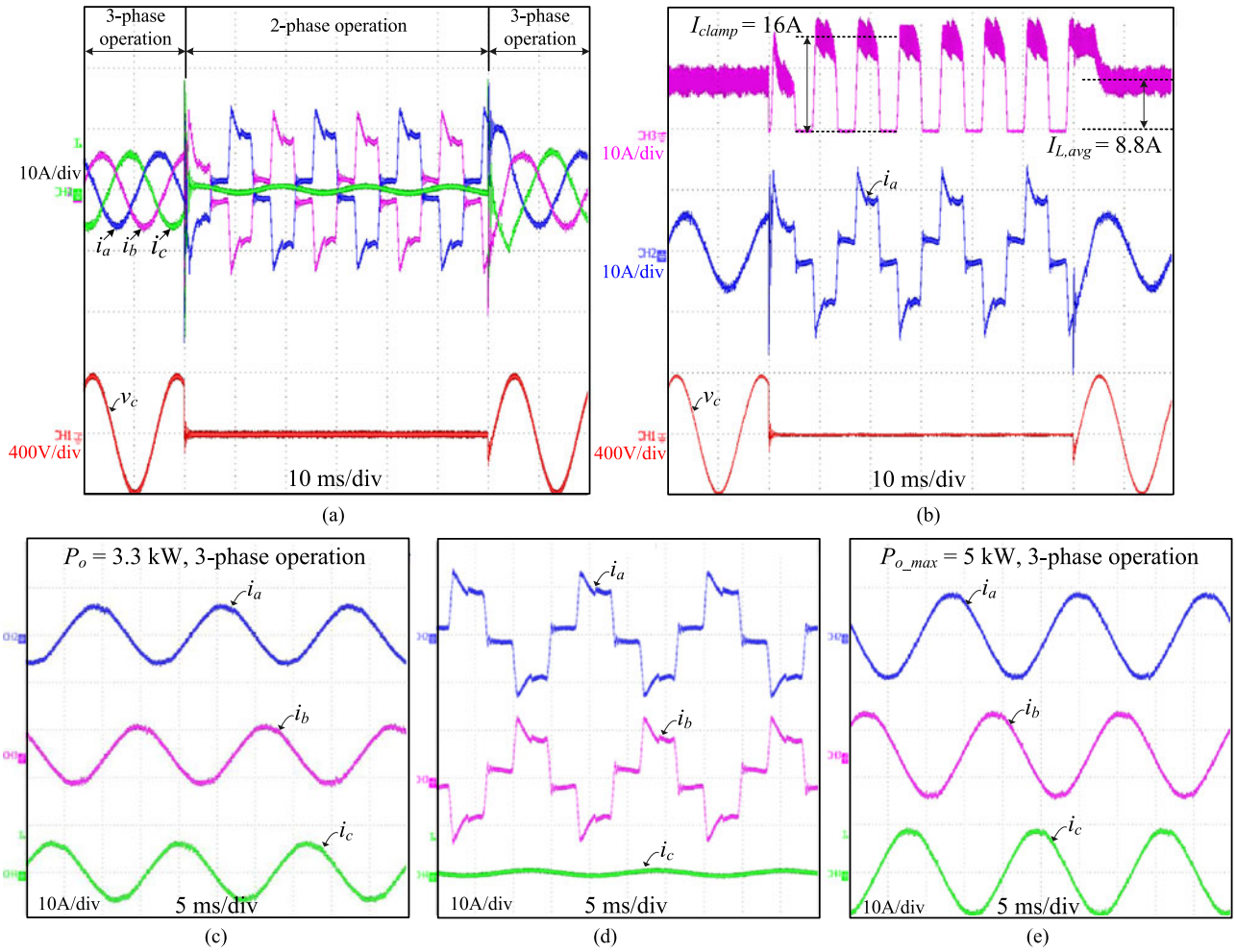

Fig. 15. Experimental waveforms for $v_{LL} = 480$ V, $f_{\text{grid}} = 60$ Hz, $m_a = 0.75$ at $2/3P_{o\_\max} = 3.3$ kW: (a) input phase currents and voltage waveforms of i_a, i_b, i_c and v_c, (b) output inductor current I_L and input phase currents and voltage, (c) normal operation (three-phase operation) (d) one phase loss operation (two-phase operation), (e) normal operation at maximum output power $P_{o\_\max} = 5$ kW.

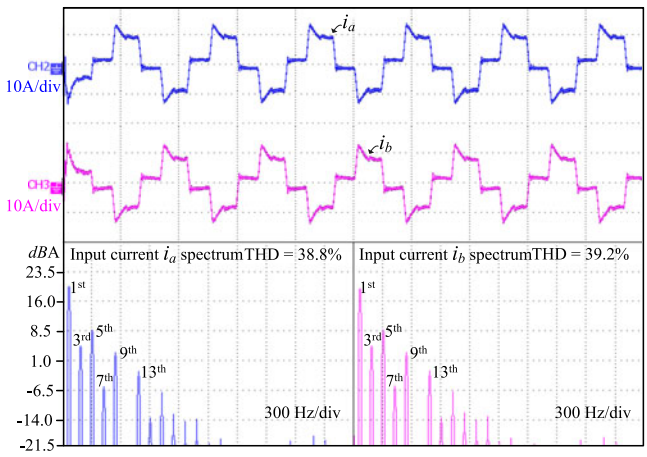

Fig. 16. Experimental spectrums of input phase currents of i_a and i_b at $2/3P_{o\_\max} = 3.3$ kW.

and ΔV_o is less than 5% of nominal output voltage in one phase loss operation as shown in Fig. 14(f) and (g), respectively. Fig. 16 shows the experimental spectrums of the input phase currents for one phase loss operation at 3.3 kW output power. The total harmonic distortion of the input phase currents is around 1.6% for normal operation and 39.2% for one phase loss operation.

A. Converter MOSFET Switching Dynamics Behavior During One Phase Loss Operation

The converter switching behavior (turn-ON and turn-OFF actions) during normal operation is analyzed and verified with experimental results in [17, Section IV-B]. Fig. 17 shows the converter turn-ON and turn-OFF actions during one phase loss operation. One of the MOSFETS that function as an active switch in the converter is selected for demonstrating the turn-ON and turn-OFF switching transitions at four locations of t_1, t_2, t_3, and t_4 (to show the entire operation mode). As shown in Fig. 17(b)–(e), drain–source voltage V_{ds} of the MOSFET tends to be zero before the gate-to-source voltage V_{gs} of the MOSFET approaches high, which indicates that the body diode is ON before the turn-ON of the switch such that ZVS is realized. As shown in Fig. 17, the transformer primary voltage v_P and the drain–source voltage V_{ds} of the MOSFET is clean and no large spike is noticeable since all the turn-ON actions are under ZVS condition. The turn-OFF actions of this MOSFET at t_1, t_2, t_3, and t_4

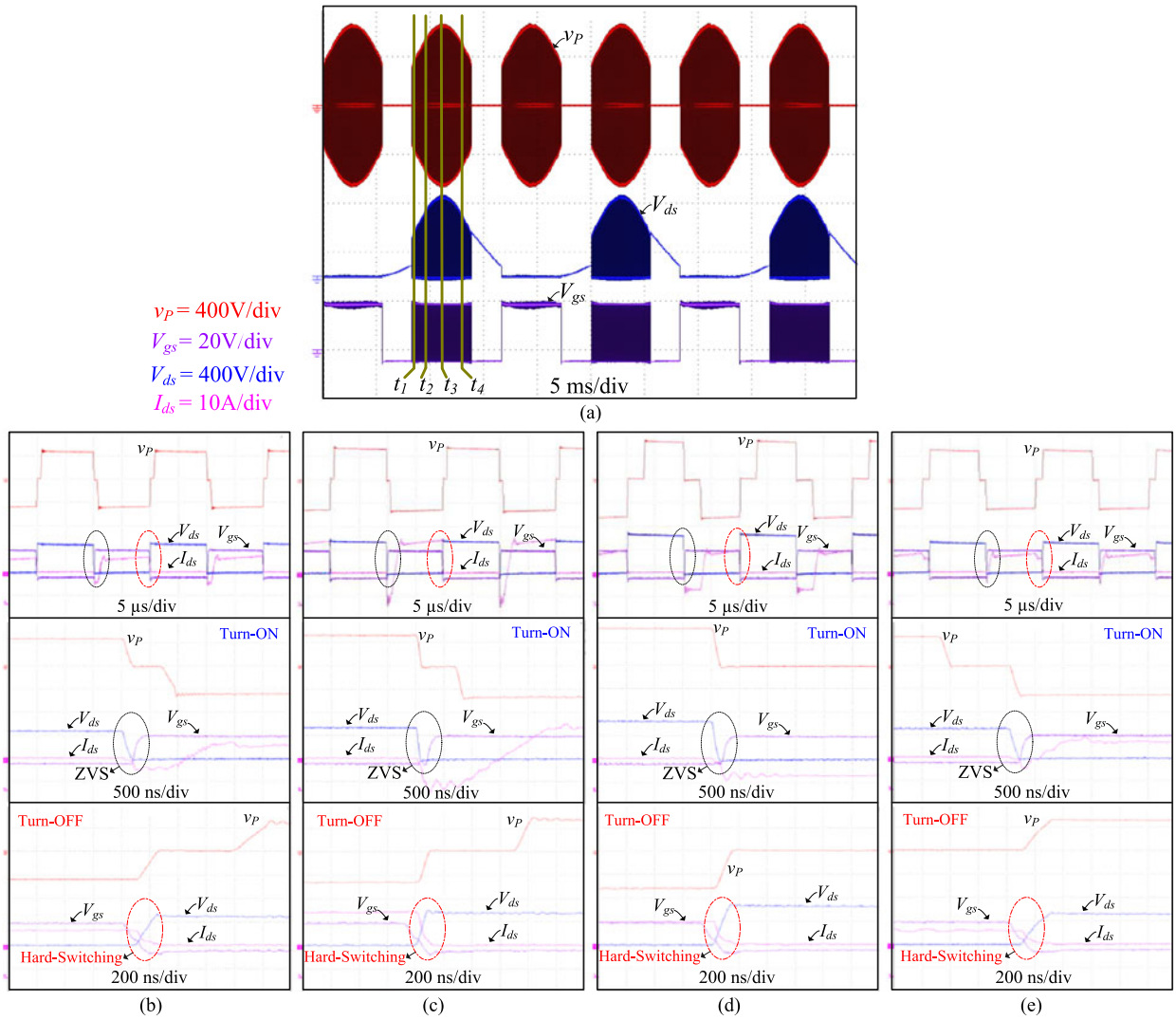

Fig. 17. Experimental waveforms for Converter MOSFETs switching behavior (turn-ON and turn-OFF actions) during one phase loss operation: (a) voltage waveforms of v_P, V_{ds} and V_{gs}, (b) at t_1 (c) at t_2, (d) at t_3, and (e) at t_4.

are all hard switching. However, these turn-OFF actions produce negligible losses since the overlapping of voltage and current is very small during the turn-OFF transition.

VI. Conclusion

In this paper, operation of the three-phase isolated buck matrix-type rectifier under one phase loss condition is described and a new PWM scheme and commutation method for the one phase loss operation is proposed. With the proposed switching scheme and commutation method, two-step commutation with ZVS (here either using ZVS or zero voltage turn-ON) can be realized for one phase loss operation and also for the transition from normal operation to one phase loss operation and from one phase loss operation to normal operation. Operation and performance of the converter with the proposed PWM and commutation method are verified with simulation and experimental results.

Based on the experimental results obtained from a 5 kW prototype, it is shown that the converter is able to deliver two-third of maximum output power to the load and regulate the output voltage with maximum voltage drop less than 5% of nominal output voltage. Current stress of the converter and input current THD and spectrum analysis are also provided in the experimental results with one phase loss operation. The relatively large THD (around 40%) is one of the drawbacks for this converter when operating under one phase loss condition.

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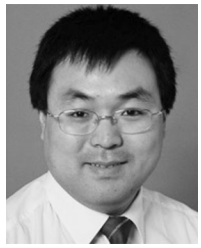

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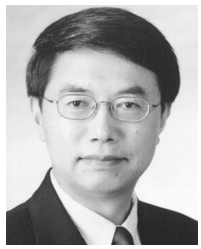

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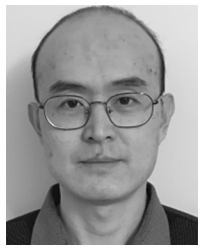

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