A 0.016 mV/mA Cross-Regulation 5-Output SIMO DC–DC Buck Converter Using Output-Voltage-Aware Charge Control Scheme

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***Abstract*—A single-inductor multiple-output (SIMO) dc–dc converter with output-voltage-aware charge control (OVACC) is presented in this paper. The OVACC scheme reduces the cross regulation by computing the total energy required by all outputs to extract exactly the same amount of energy from the input. Moreover, the proposed design also extends the load capability range of the SIMO converter by supporting the operation in both continuous conduction mode and discontinuous conduction mode while boosting the overall power efficiency. The proposed SIMO (five outputs) dc–dc converter has been implemented in a 0.18 μm 1P6M CMOS process. Measurement results show that the best cross regulation is 0.016 mV/mA when the output current of 250 mA abruptly changes. And no cross regulation is observed when the first output current changes 150 mA, the second output current changes 160 mA, the third and fourth output currents change 180 mA, and the last output current changes 250 mA. Also, the measured peak power efficiency is 86%.**

***Index Terms*—Charge control, cross regulation, ordered-power-distributive control (OPDC), single-inductor multiple-output (SIMO) converter.**

I. Introduction

MULTIPLE supply voltages are widely required in low-power systems due to the requirements of different functional blocks and dynamic voltage scaling to enhance power efficiency. Considering volume weight, component counts as well as footprint area, integration of single-inductor multiple-output (SIMO) dc–dc converters as power management circuits is highly desirable compared to multiple single-inductor single-output converters since the SIMO dc–dc converter employs only one inductor to provide the different supply voltages. However, since all the outputs share the energy from the single inductor, an abrupt change of load at any output can cause a temporary shortage or redundancy of energy provided by the inductor. Therefore, the other output voltage levels are consequently disturbed and cross regulation occurs. The cross regulation can cause noise and/or stability issues, resulting in the overall degradation of dc–dc converter performance. Hence, minimizing the cross regulation is required in SIMO dc–dc converter design while improving the power efficiency and the load delivery capability are also important criteria.

A numerous number of research works have addressed the aforementioned issues of the SIMO dc–dc converter. The control methods for SIMO dc–dc converters can be classified into two main categories: time-multiplexing control (TMC) [1]–[3] and ordered-power-distributive control (OPDC) [4]–[15]. In the TMC SIMO dc–dc converter, each output is regulated in a fixed duration of time by its own feedback. The loop control is either a voltage-mode control [1]–[3] or a current-mode control. Therefore, the charge delivered for each output is well controlled and independent of other outputs, which removes the cross regulation in TMC. However, this control method suffers from the tradeoff between the output voltage ripple and the number of outputs (or the load capability). That is, increase of the number of outputs (or larger power delivery) requires longer time to regulate and thus produces higher voltage ripple. The OPDC scheme reduces the output voltage ripple at high power delivery in the SIMO dc–dc converter [4]–[15]. For an OPDC SIMO dc–dc buck converter, all the outputs sequentially share the magnetic energy of the inductor. As depicted in Fig. 1, a charging procedure includes both charging and discharging the inductor current, where each output switch Si is turned ON at one time to share the inductor current. Since all outputs are regulated in one period, this control method can produce smaller voltage ripple for a relatively larger numbers of output channels. The control block of OPDC normally consists of two parts: the energy distributing part ensuring no voltage error compared to the reference at each output and the energy generating part extracting energy from the input to ensure no total voltage error at all outputs. The energy generating part measures the total voltage

Manuscript received April 28, 2017; revised August 28, 2017; accepted December 4, 2017. Date of publication December 21, 2017; date of current version August 7, 2018. This work was supported in part by the Ministry of Trade, Industry and Energy (MOTIE) (project number 10080622), in part by the Korea Semiconductor Research Consortium support program for the development of the future semiconductor device, and in part by the IT R&D program of MOTIE/KEIT (10054819, Development of modular wearable platform technology for the disaster and industrial site). Recommended for publication by Associate Editor Wing-Hung Ki. *(Corresponding author: Kwang-Hyun Baek.)*

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Digital Object Identifier 10.1109/TPEL.2017.2785838

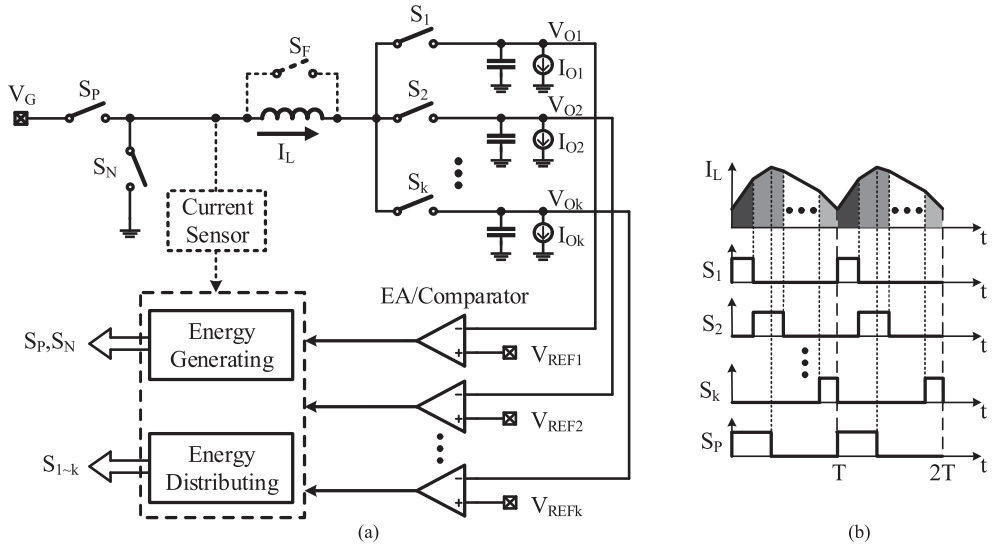

Fig. 1. (a) Overall architecture of OPDC SIMO dc–dc buck converter, and (b) timing diagram of OPDC.

error at all the outputs through a feedback loop to provide an adequate amount of energy for the inductor. Due to the speed limitation of the feedback loop, cross regulation is unavoidable when abrupt load change occurs at any output.

Many previous works have been presented to minimize the effect of the aforementioned inadequateness of energy. A well-known method is to insert a duration of a free-wheeling switch to separate the charging procedures [8]–[11]. The inserted free-wheeling switch acts as a temporal buffer of energy to compensate the energy unbalance occurred at abrupt load variations. However, inserting the free-wheeling switch requires an additional feedback loop. Furthermore, the nonzero resistance of this free-wheeling switch degrades the overall power efficiency.

To overcome the drawback of using the free-wheeling switch, a phase-locked loop based control method was proposed [12], [13]. Since the duration for the free-wheeling switch is eliminated, the charging procedure is repeated successively. The error between the duration of the charging procedure and a reference clock controls the energy generating switches. Since the charging procedure should consecutively proceed, there is no time for zero current inside the inductor. Therefore, this control method cannot be applied to a discontinuous conduction mode (DCM) and thus is not suitable for low-power applications.

If the total energy required by all outputs can be computed, only the same amount of energy is extracted from the input and thus the energy imbalance can be properly managed. This paper introduces an output-voltage-aware charge control (OVACC) method to regulate a 5-buck-output SIMO converter. The proposed control method utilizes the charge control and OPDC to independently regulate each output, so it can achieve low ripples, a wide load range because of the interoperability of both DCM and continuous conduction mode (CCM). The OVACC considers the outputs' voltages to compute the total required energy, and then maintains a precise balance of energy between the input and the outputs. This reduces the cross regulation without the need of a free-wheeling switch, thus improving the overall efficiency.

The organization of the paper is as follows. The overall architecture of the proposed converter and its operation principle are discussed in Section II. Section III describes the circuit implementation. The experimental results and comparisons are presented in Section IV. Finally, the conclusion is made in Section V.

II. Proposed Output-Voltage-Aware Charge Control (OVACC)

A. Conventional Charge Control

In energy distributing block of the OPDC method, the voltage level of each output can be regulated by comparator [10]–[13], voltage mode control [6], or charge control method [7]–[9]. The general charge control circuit for an output is depicted in Fig. 2. In the charge control method, the inductor current I_L is sensed, and then the sensed current $I_{\rm LSEN}$ charges the capacitor C_i. The ON-time duration of the output switch M_{Si} is decided by comparing the voltage of the capacitor C_i with the output of the error amplifier EA. The error amplifier EA has a function to amplify the difference between the output voltage V_{Oi} and its reference voltage $V_{{\rm REF}i}$. The energy delivered to the output in the ON-time duration of the switch M_{Si} is computed as follows:

$$E_i = \int_0^{D_i T} I_L V_{Oi} dt \tag{1}$$

where I_L is the inductor current, $D_i T$ is the ON-time duration of M_{Si}, and V_{Oi} is the voltage of output ith. The inductor current is sensed by a current sensor, which has a gain of $1/A$ to produce the sensing current $I_{\rm LSEN}$. Thus, the energy delivered to the output is rewritten as

$$E_i = \int_0^{D_i T} A I_{\rm LSEN} V_{Oi} dt. \tag{2}$$

The ON-time duration $D_i T$ of the output power switch M_{Si} corresponds to the charging time of the capacitor C_i by $I_{\rm LSEN}$. The amount of charge delivered to this capacitor in the ON-time

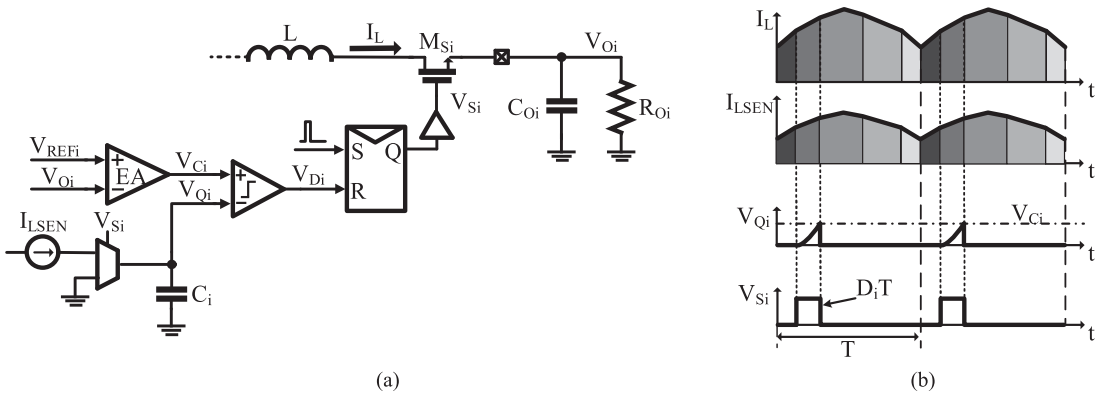

Fig. 2. (a) Charge control diagram of an output, and (b) timing diagram of charge control.

duration is calculated by the following equation:

$$Q_i = \int_0^{D_i T} I_{\mathrm{LSEN}}\, dt. \tag{3}$$

This amount of charge makes the voltage of the capacitor C_i to increase up to the output voltage V_{Ci} of the error amplifier. Thus, the output voltage V_{Ci} of the error amplifier can be calculated as follows:

$$V_{Ci} = \frac{Q_i}{C_i}. \tag{4}$$

From (2)–(4), the energy delivered to the output can be indicated by the output voltage V_{Ci} of the error amplifier as the following equation:

$$E_i = AV_{Oi}C_iV_{Ci}. \tag{5}$$

While *A* and C_i are constants, the output voltage V_{Oi} can be varied according to design requirements or load variations. So the output voltage V_{Ci} of the error amplifier cannot be used to indicate the energy delivered to the output. It is advisable to measure the energy required by each output, so that the energy-generating part can produce exactly the same amount of energy. Therefore, it is preferable to remove the output voltage V_{Oi} from (5). Note that the inductor sensing current can include the output voltage information as the following form:

$$I_{\mathrm{LSEN}} = AKV_{Oi}I_L \tag{6}$$

where *K* is a constant to represent the relative amplitude of I_{LSEN} to V_{Oi}. The final form of the energy delivered to the output can be rewritten as

$$E_i = AKC_iV_{Ci}. \tag{7}$$

Equation (7) implies that when the sensed inductor current I_{LSEN} is a proportional function of the output voltage V_{Oi}, the output voltage V_{Ci} of the error amplifier can indicate the energy transferred to the output. This is desirable because the voltage V_{Ci} can be referred when extracting the energy from the input to avoid any redundancy or shortage of energy. That is, the cross regulation can be reduced as mentioned previously.

B. Output-Voltage-Aware Charge Control

The overall architecture of the proposed SIMO converter is shown in Fig. 3. The five outputs are sequentially time-shared by the current following through the inductor by OPDC. In one period, switches M_{S1}–M_{S5} are turned ON at one time in an increasing order to charge the corresponding outputs. In [6], the last output has to compensate for the changes of energy occurred at the prior outputs. Thus, the last output is prone to cross regulation. The voltage error between the last output and its reference voltage is used as the control variable to extract a suitable amount of energy from the input. In our approach, the proposed OVACC is used to reduce the possibility of cross regulation at the last output. The main idea is that the energy distributing controller measures the energy required by all the outputs, and the energy generating controller extracts the same amount of the total energy from the input. Therefore, any change regarding the energy at the outputs is immediately compensated by the input. In other words, the required energy and the provided energy are always equal, which finally prevents the cross regulation.

To compute the energy, a full-duration inductor current sensor (output-voltage-aware current sensor) is required to provide a sensing current I_{LSEN2} for the energy distributing controller. At the same time, a generated current I_{LSEN1} by the current sensor is the input to the energy generating controller. I_{LSEN2} has the magnitude varied proportionally to the output voltages. The energy distributing controller produces the control signals for the five output switches $M_{S1} - M_{S5}$ and signals $V_{C1} - V_{C5}$, which contain the information of energy required by the five output channels. The energy-contained signals V_{C1-5} are added to produce a total required energy signal V_{CT}. This signal is the input of the energy generating controller, which controls the input power transistors M_P and M_N to extract the same amount of energy from the battery. The computation of the energy required by the outputs and generated by the input can be made by the charge control in the energy distributing and generating controllers, as shown in Figs. 4 and 5.

A detailed OVACC block is depicted in Fig. 4 and its timing diagram is provided in Fig. 5. The proposed charge control can be distinguished from the conventional charge control by the output-voltage-aware current sensor. The inductor current sensor senses the full-wave inductor current with a gain of 1/*A*

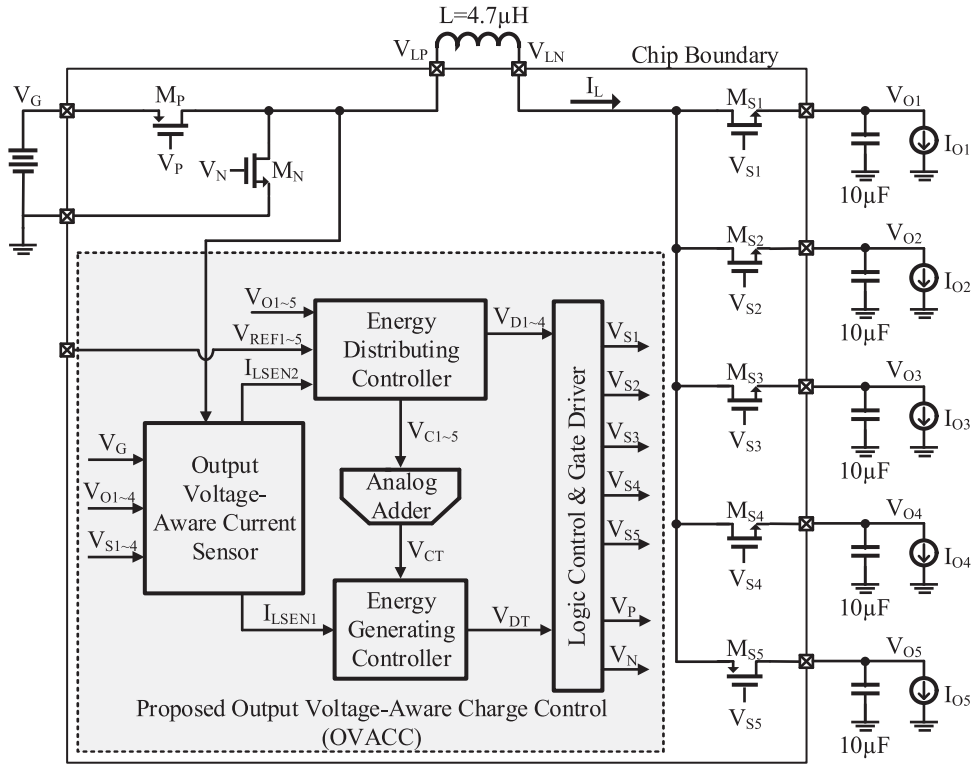

Fig. 3. Architecture of the proposed single-inductor five-output buck converter.

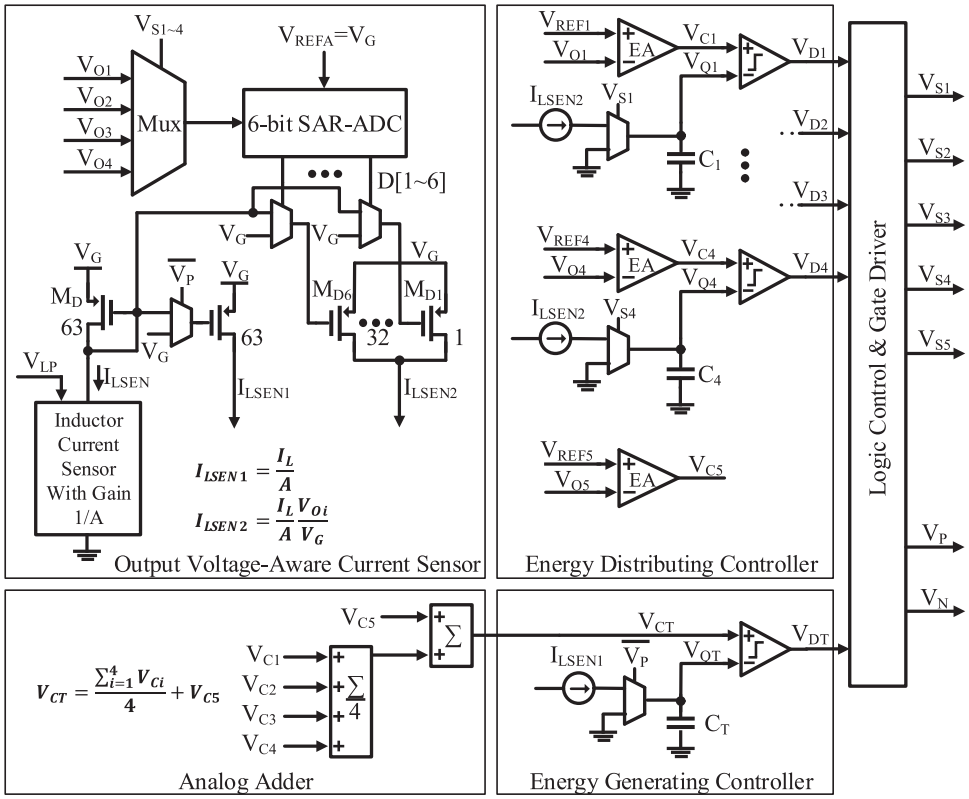

Fig. 4. Circuit implementation of the proposed OVACC block.

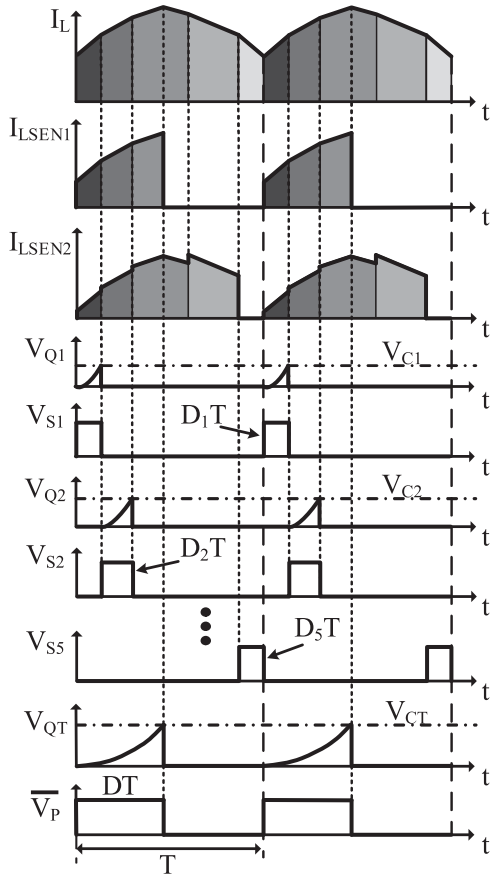

Fig. 5. Operation timing waveforms.

to make $I_{\rm LSEN}$. $I_{\rm LSEN1}$ is simply a copy of $I_{\rm LSEN}$ at the rising phase of the inductor current by a current mirror, as shown in Fig. 5. Thus, we have

$$I_{\rm LSEN1} = \frac{I_L}{A}. \tag{8}$$

This sensed current charges the capacitor C_T of the energy generating controller, which consists of a charge control loop to generate control signals V_P and V_N.

The energy extracted in one period from the input is computed as follows:

$$E_T = \int_0^{D_T T} I_L V_G dt = \int_0^{D_T T} A I_{\rm LSEN1} V_G dt \tag{9}$$

where V_G is the input voltage, and $D_T T$ is the ON-time duration of the power input switch M_P.

Similar to the charge control for a single output channel, we can calculate the charge delivered to the capacitor C_T in one period:

$$Q_T = \int_0^{D_T T} I_{\rm LSEN1} dt = C_T V_{\rm CT}. \tag{10}$$

From (9) and (10), the extracted energy in one period can be rewritten as follows:

$$E_T = A V_G C_T V_{\rm CT}. \tag{11}$$

TABLE I
CROSS REGULATION RECORDED AT OUTPUT FIFTH WHEN LOAD CURRENT OF OUTPUT FIRST ABRUPTLY DECREASES FROM 300 TO 50 MA WHILE OTHER OUTPUT LOADS ARE 50 MA

Resolution of SAR ADC	Cross regulation
4 bit	0.016 mV/mA
5 bit	0.015 mV/mA
6 bit	0.010 mV/mA
7 bit	0.013 mV/mA
8 bit	Not operating

Since A, V_G, and C_T are all constant, the extracted energy can be precisely indicated by $V_{\rm CT}$.

The generation of the second inductor-current-sensing signal $I_{\rm LSEN2}$ is more complex. Since $I_{\rm LSEN2}$ should be proportional to the output voltages when their corresponding switches are activated. In order to do that, the first four outputs one-by-one become the inputs to a 6-bit SAR ADC. This SAR ADC converts the output voltages on their charging phase to digital codes. These digital codes turn ON and OFF a binary-weighted switch array M_{D1}–M_{D6} to generate $I_{\rm LSEN2}$. This sensing current has the magnitude proportional to the output voltage on their charging phase, as depicted in Fig. 5:

$$I_{\rm LSEN2} = \frac{I_L}{A}\frac{V_{Oi}}{V_G}. \tag{12}$$

Thus, when using $I_{\rm LSEN2}$ to charge the capacitor C_i of the loop controls for those outputs, the energy delivered to each output can be calculated as follows:

$$E_i = A V_G C_i V_{Ci}. \tag{13}$$

This equation shows that the energy delivered to the output one to four is no longer dependent on the output voltages.

The last output is regulated by directly controlling the input switch M_P; thus, the energy transferred to this output is as follows:

$$E_5 = A V_G C_T V_{C5}. \tag{14}$$

If we select $C_1 = C_2 = C_3 = C_4 = \frac{C_T}{4}$ and use an analog adder to generate $V_{\rm CT}$ from V_{C1} to V_{C5}, so that

$$V_{\rm CT} = \frac{\sum_{i=1}^{4} V_{Ci}}{4} + V_{C5}. \tag{15}$$

Finally, we can achieve

$$E_T = \sum_{i=1}^{5} E_i. \tag{16}$$

This equation shows that the proposed OVACC can actually allow to compute the required energy and to extract the same amount of energy from the input.

For the selection of SAR ADC resolution, there is a trade-off between speed and accuracy. In SAR ADCs with capacitive DAC array, the operating speed becomes slower for higher resolution, because more capacitors and larger-size sampling and switching transistors are required to implement more accurate SAR ADCs (longer settling and switching times are necessary).

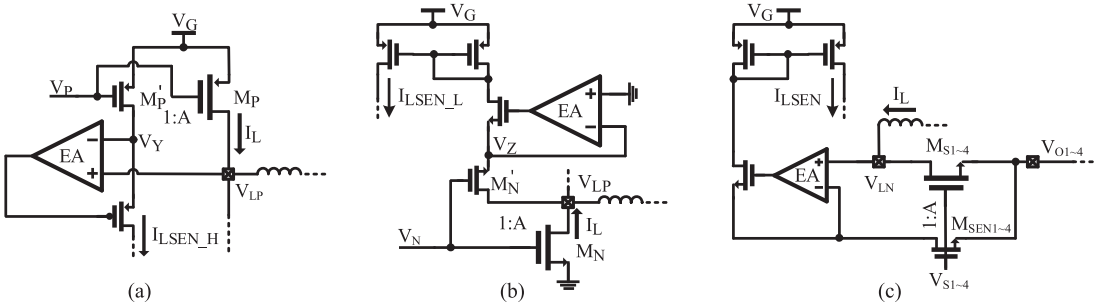

Fig. 6. Full-duration inductor current sensor: (a) Circuit to sense the rising phase of inductor current, (b) circuit to sense the falling phase of inductor current, and (c) circuit to sense inductor current by the NMOS output transistors.

With a given amount of current (I_{LSEN}) fed into "inductor current sensor" block in Fig. 4, the SAR ADC cannot be properly driven at a target operating speed beyond a certain resolution due to larger load. Although higher resolution SAR ADC can theoretically minimize cross regulation further, there is an optimum resolution with a given driving capability due to aforementioned reasons. The simulation results shown in Table I suggest that using a 6-bit SAR ADC with $''I''_{\mathrm{LSEN}} = 35\,\mu$A achieves the best compromise between the speed and the accuracy, which produces the least cross regulation. In case of the resolution of the SAR ADC larger than or equal to 8 bits, the size of transistor M_D is too large to be driven by the inductor current sensor.

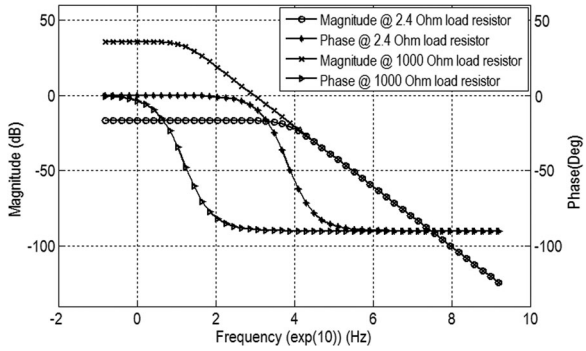

Fig. 7. Magnitude and phase of $G(s)$ when $R_{Oi} = 2.4$ and $1000\,\Omega$.

III. Circuit Implementation

A. Inductor Current Sensor

The full-duration inductor current sensor is designed to apply charge control for switching the output and the input switches. In this work, the full-duration inductor current sensor is combined with two single-phase inductor current sensors: One senses the rising phase of the inductor current, and the other senses the falling phase, as shown in Fig. 6(a) and (b).

The rising phase of the inductor current is sensed through the input transistor M_P. This current sensor works based on a current mirror technique where one very small transistor M'_P is used to mirror a very large current flowing through the power transistor M_P. In the ON-time duration of M_P, it operates in triode region, so the current equation following this switch is as follows:

$$I_L = KP_n \frac{W}{L}\left((V_{\mathrm{GS}} - V_{\mathrm{TH}})\,V_{\mathrm{GS}} - \frac{V_{\mathrm{DS}}^2}{2}\right).$$

The feedback loop consisting of a high gain Op-amp equalizes V_Y to V_{LP}. Thus, V_{GS} and V_{DS} of the both switches M_P and M'_P are equal, so the current following the two transistors follows the ratio:

$$I_{\mathrm{LSEN\_}H} : I_L = 1 : A$$

where A is the ratio between the sizes of M_P and M'_P.

By a similar technique, the falling phase of the inductor current is sensed by the circuit shown in Fig. 6(b). When the N-type metal oxide semiconductor (NMOS) switch M_N turns ON, current follows through it from the ground to the inductor, making V_{LP} lower than the ground. Due to the feedback loop made by a high gain Op-amp, V_Z is equal to V_{LP}. Thus, the current following through M'_N and M_N follows a ratio of $1{:}\,A$. As an alternative implementation, a circuit to sense the inductor current by the NMOS output transistors is shown in Fig. 6(c).

B. Charge Control

The dynamic behavior and stability of the designed charge control loop are carefully considered in this section. Because the proposed converter consists of five identical charge control loops and each loop independently operates, each loop can be represented by a general charge control loop depicted in Fig. 2(a). The difference between the output voltage V_{Oi} and its reference voltage $V_{\mathrm{REF}i}$ is amplified to achieve the control signal V_{Ci}, which determines the amount of charge delivered to the output. The sensed current I_{LSEN} (for simplicity, I_{LSEN} is used to represent for both I_{LSEN1} and I_{LSEN2}) charges the capacitor C_i in the ON-time interval of the power switch M_{Si}. This charge procedure in one period finishes when the voltage of the capacitor V_{Qi} is equal to V_{Ci}, the power switch M_{Si} is turned OFF to shut down the charge to the load. The amount of charge delivered to the output is determined V_{Ci}. If Q is the charge delivered to the output in one period T, then the average output current is

$$\bar{I} = \frac{Q}{T}. \tag{17}$$

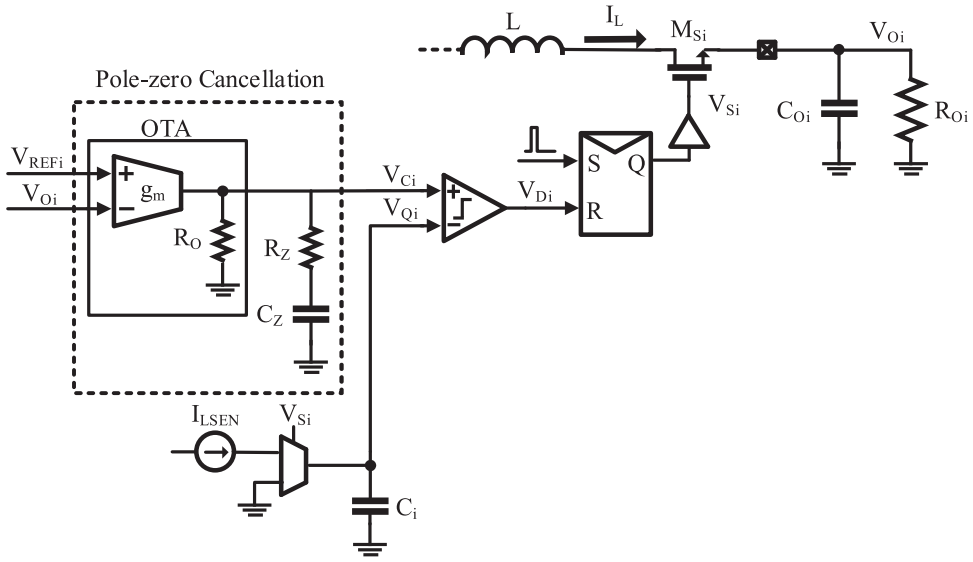

Fig. 8. Charge control diagram with a pole-zero-cancelation circuit.

The output current is also determined by the output voltage and the load as follows:

$$\bar{I} = \frac{V_{Oi}}{R_{Oi}} + sC_{Oi}V_{Oi} \tag{18}$$

where R_{Oi} is the output resistor and C_{Oi} is the output filter capacitor. The amount of charge delivered to the output can be calculated from the voltage of the capacitor C_i:

$$Q = AC_iV_{Ci} \tag{19}$$

where 1/*A* is the gain of the inductor current sensor. From (17)–(19), we can write

$$\frac{AC_iV_{Ci}}{T} = \frac{V_{Oi}}{R_{Oi}} + sC_{Oi}V_{Oi}. \tag{20}$$

Applying perturbation and linearization, the small-signal transfer function *G*(*s*) from $\hat{v}_{Ci}$ to $\hat{v}_{Oi}$ is obtained as

$$G(s) = \frac{\hat{v}_{Oi}}{\hat{v}_{Ci}} = \frac{AR_{Oi}C_i}{T(1+sR_{Oi}C_{Oi})} \tag{21}$$

where $A = 20\,000$, $C_i = 3$ pF, $T = 1\,\mu$S, $C_{Oi} = 10\,\mu$F, and the load resistor varies from 2.4 to 1 kΩ.

Fig. 7 shows the open-loop frequency response of the charge control designed for one output in this work. To boost the dc gain and achieve a better dynamic response, a pole-zero-cancelation circuit [19] is adapted, as shown in Fig. 8.

The operational transconductance amplifier (OTA) has current–voltage gain of g_m and output resistance of R_O; hence, the transfer function of the compensation circuit is given as

$$A(s) = \frac{\hat{v}_{Ci}}{\hat{v}_{Oi}} = g_mR_0\frac{1+sC_ZR_Z}{1+sC_ZR_0}. \tag{22}$$

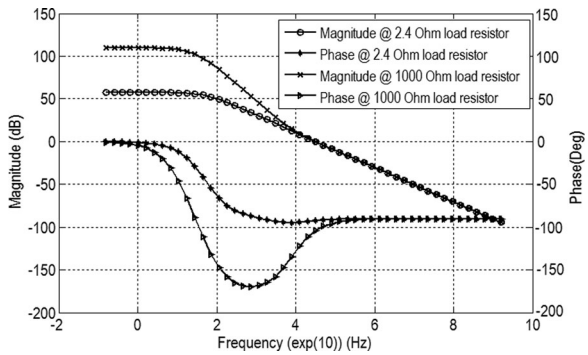

Fig. 9. Magnitude and phase of charge control with pole-zero cancelation when $R_{Oi} = 2.4$ and $1000\,\Omega$.

The total loop-gain of the charge control loop can be rewritten as

$$\begin{aligned} T(s) &= G(s)A(s) \\ &= \frac{g_mR_0AR_{Oi}C_i}{T}\frac{(1+sC_ZR_Z)}{(1+sC_ZR_0)((1+sR_{Oi}C_{Oi}))}. \end{aligned} \tag{23}$$

In this work, the specification of the pole-zero cancelation circuit is given as follows: $g_m = 0.22\,\text{mA/V}$, $\text{R}_0 = 16.2\,\text{M}\Omega$, $\text{R}_\text{Z} = 200\,\text{k}\Omega$, and $C_Z = 200$ pF.

Due to the pole-zero cancelation circuit, the charge control loop becomes always stable with a high dc gain regardless of the load resistances, as shown in Fig. 9. To design the pole-zero cancelation circuit, an external 200 kΩ resistor and an external 200 pF capacitor are required for each output channel.

IV. Measurement Results and Comparisons

The proposed SIMO dc–dc buck converter has been fabricated using a 0.18 μm 1P6M CMOS process. The chip area is 2.35 mm × 2.35 mm including pads. The micrograph is shown in Fig. 10.

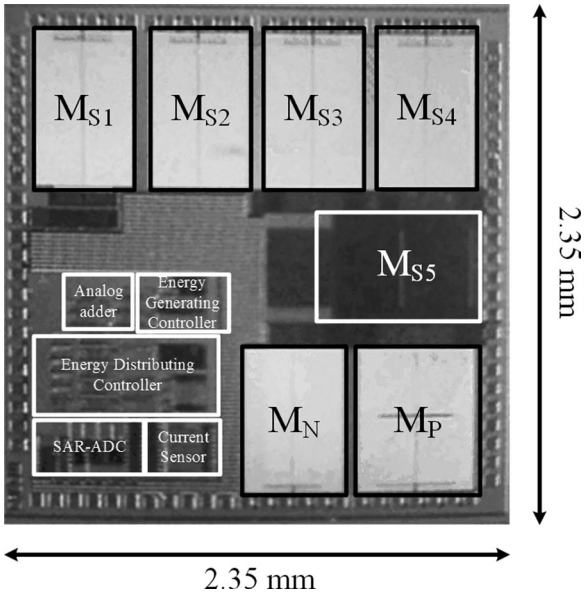

Fig. 10. Micrograph of the proposed OVACC SIMO dc–dc converter.

TABLE II
SPECIFICATIONS AND EXTERNAL COMPONENT VALUE OF THE PROPOSED CONVERTER

Input voltage	3.3–4.3 V
Output voltage	$V_{O1} = 0.9$ V, $V_{O2} = 1.2$ V, $V_{O3} = 1.5$ V, $V_{O4} = 1.8$ V, $V_{O5} = 2.2$ V
Maximum output current	$I_{O1\_MAX} = 330$ mA, $I_{O2\_MAX} = 400$ mA, $I_{O3\_MAX} = 460$ mA, $I_{O4\_MAX} = 520$ mA, $I_{O5\_MAX} = 600$ mA
Inductor and its DCR	4.7 μH and 25 mΩ
Capacitor and its ESR (each channel)	10 μF and 20 mΩ
Switching frequency	1 MHz

The control block occupies an area of 800 μm $\times$ 800 μm. Large power switches are designed and multiple metal layers are connected to reduce the parasitic resistance. By adopting the proposed control scheme instead of a free-wheeling switch, the area occupation is reduced significantly. The specifications of the dc–dc converter and the used external components are listed in Table II. The first four output voltages can range from 0 to 1.8 V. The last output should be larger than 2 V due to the use of P-type metal oxide semiconductor (PMOS) output switch. In this paper, for most of the measured experiments, the output voltages are set as follows: $V_{O1} = 0.9\,\text{V}, V_{O2} = 1.2\,\text{V}, V_{O3} = 1.5\,\text{V}, V_{O4} = 1.8\,\text{V}$, and $V_{O5} = 2.2\,\text{V}$. Only one inductor of 4.7 μH is required. Each output channel is attached with a filler capacitor of 10 μF. In Table II, the maximum output currents are measured up to when each output could not track its own reference voltage while setting currents at other outputs to a minimum value.

The steady-state operation waveform of the proposed converter is shown in Fig. 11. The figure shows the inductor current and the inductor's terminal voltages waveforms when the converter works in the CCM with $I_{O1} = 21\,\text{mA}, I_{O2} = 30\,\text{mA}, I_{O3} = 44\,\text{mA}, I_{O4} = 53\,\text{mA}$, and $I_{O5} = 63\,\text{mA}$. In one period, the five outputs are sequentially regulated by switching

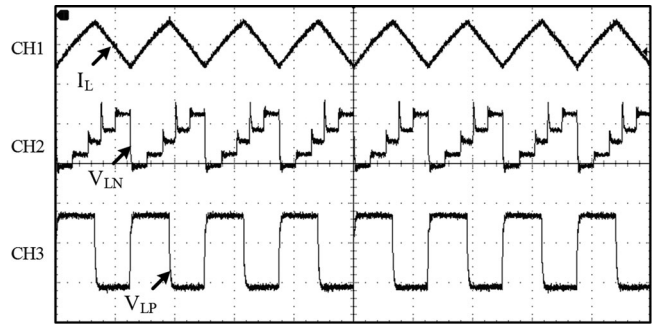

Fig. 11. Steady-state waveforms of inductor current and inductor terminal voltages where $I_{O1} = 21\,\text{mA}, I_{O2} = 30\,\text{mA}, I_{O3} = 44\,\text{mA}, I_{O4} = 53\,\text{mA}$, and $I_{O5} = 63\,\text{mA}$.

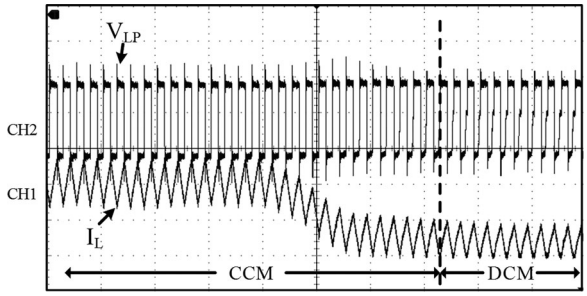

Fig. 12. Waveforms of inductor current and inductor terminal VLP when the converter changes from CCM to DCM (where $I_{O1} = 320\,\text{mA} \rightarrow 20\,\text{mA}$ and $I_{O2-5} = 20\,\text{mA}$).

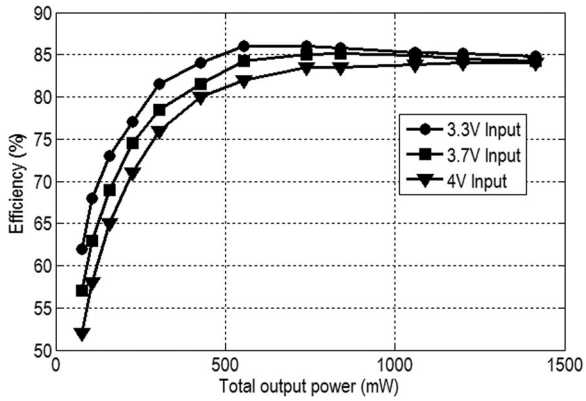

Fig. 13. Efficiency of the proposed SIMO dc–dc converter against total input power.

on their corresponding power transistors; thus, the voltage V_{LN} of the inductor steps sequentially five times in one period.

The operations of the proposed converter in both CCM and DCM are shown in Fig. 12. While the output channels from channel two to five are regulated at an output current of 20 mA, the output current of output channel one steps from 320 to 20 mA. The figure shows a smooth transition of inductor current from CCM to DCM.

The power efficiency of the proposed SIMO dc–dc converter is shown in Fig. 13, with the efficiency versus the total output power. It shows the peak efficiency of 86% when the output power is 556 mW. The efficiency significantly degrades at

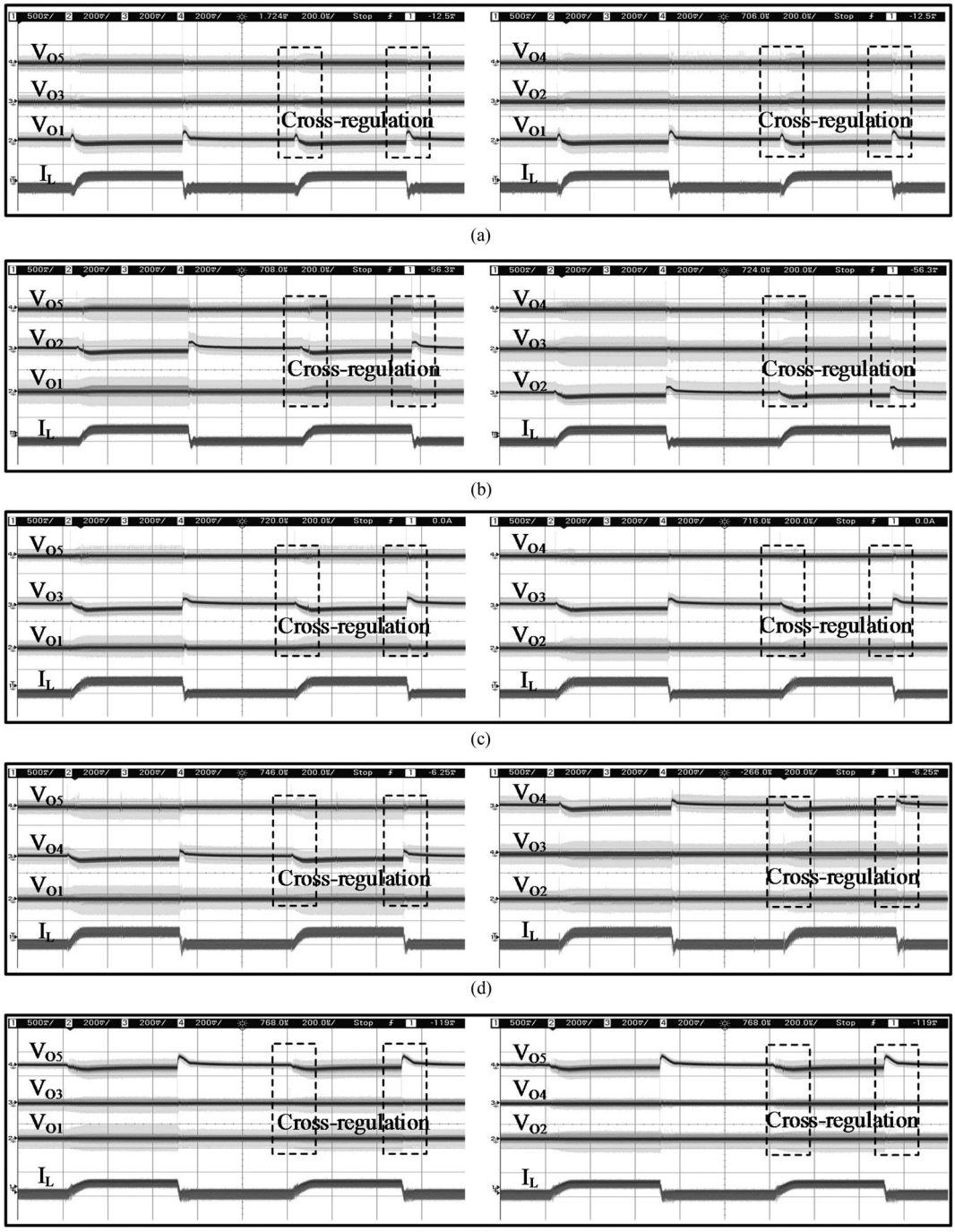

Fig. 14. Load transient responses with $V_G = 3.3\,\text{V}$ (a) at $V_{O1} = 0.9\,\text{V}$ with $\Delta I_{O1} = 250\,\text{mA}$, (b) at $V_{O2} = 1.2\,\text{V}$ with $\Delta I_{O2} = 250\,\text{mA}$, (c) at $V_{O3} = 1.5\,\text{V}$ with $\Delta I_{O3} = 250\,\text{mA}$, (d) at $V_{O4} = 1.8\,\text{V}$ with $\Delta I_{O4} = 250\,\text{mA}$, and (e) at $V_{O5} = 2.2\,\text{V}$ with $\Delta I_{O5} = 250\,\text{mA}$ (Division: 200 mV/DIV, 500 mA/DIV).

low power due to the switching power loss dominant at low power.

The load transient responses of the proposed converter are shown in Figs. 14 and 15. The cross regulations of 0.016–0.035 mV/mA are observed depending on chips and measurement methods (averaging/nonaveraging functions on oscilloscope equipment) when each output channel varies 250 mA, as shown in Fig. 14. The worst cross regulation is normally observed at the output channel five when the loads of the other outputs vary, and the cross regulation is not significant at the other outputs. When an output load changes, its voltage undergoes an overshoot less than 120 mV and can be settled after 60 μs. Fig. 15 shows that no cross regulation is observed when $\Delta I_{O1} \leq 150\,\text{mA}, \Delta I_{O2} \leq 160\,\text{mA}, \Delta I_{O3} \leq 180\,\text{mA}, \Delta I_{O4} \leq 180\,\text{mA}$, and $\Delta I_{O5} \leq 250\,\text{mA}$ (boundary cases). Note that two subfigures are shown for each output case,

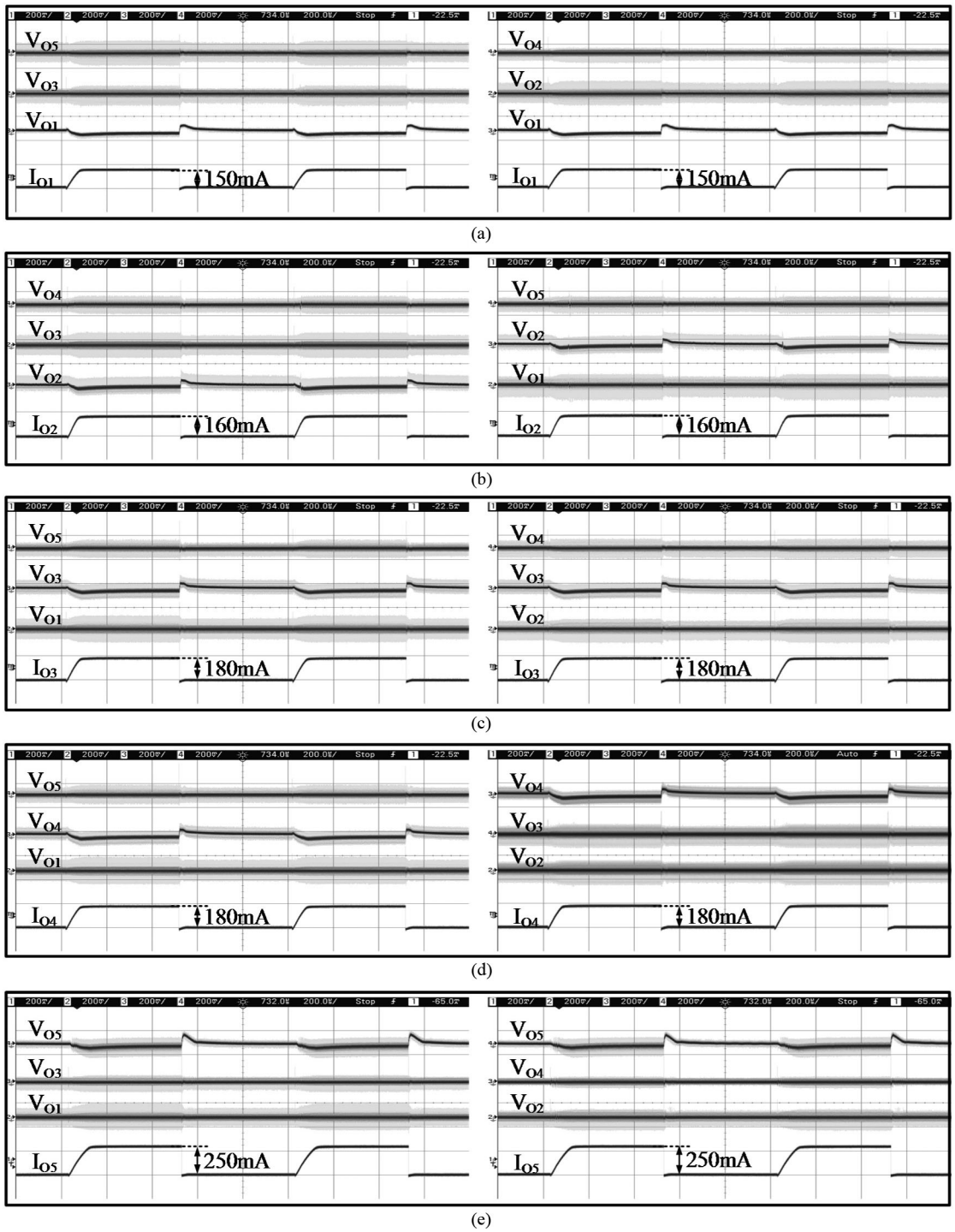

Fig. 15. Load transient responses with $V_G = 3.3$ V (a) at $V_{O1} = 0.9$ V with $\Delta I_{O1} = 150$ mA, (b) at $V_{O2} = 1.2$ V with $\Delta I_{O2} = 160$ mA, (c) at $V_{O3} = 1.5$ V with $\Delta I_{O3} = 180$ mA, (d) at $V_{O4} = 1.8$ V with $\Delta I_{O4} = 180$ mA, and (e) at $V_{O5} = 2.2$ V with $\Delta I_{O5} = 250$ mA (Division: 200 mV/DIV, 200 mA/DIV).

because an oscilloscope used for measurements has only four channels.

Table III shows a summary of the performance of the proposed converter and comparisons with state-of-the-art SIMO dc–dc converters. The proposed converter produced very small cross regulations at the large load variation of 250 mA. In addition, no cross regulation is observed at load variation smaller than 150 mA in case of output one, 160 mA in case of output two, 180 mA in case of outputs three and four, and 250 mA in case of output five. Due to the unique energy computation technique, the proposed converter can produce exact amount of energy required; thus, it excludes the requirement for a free-wheeling switch. This results in boosting the overall power efficiency and saving the chip area. Moreover, the circuit can operate in both DCM and CCM, which is preferable for wide load range applications.

TABLE III
PERFORMANCE SUMMARY AND COMPARISONS

		[12] ISSCC 2010	[9] ISSCC 2012	[13] ISSCC 2014	[15] ISSCC 2015	[8] JSSC 2016	This work
Process (CMOS)		0.35 µm	65 nm	0.35 µm	0.35 µm	65 nm	**0.18 µm**
Control Method		Comparator-based control	Charge control	RBAOT	Error-based control	Current-mode control	**OVACC**
Topology (Buck)		SIMO	SIMO	SIMO	SIMO	DF-DIMO	**SIMO**
# of Outputs		6	5	4	10	4	**5**
Supply Voltage (V)		5.0	3.4~4.3	2.7~5.0	5.0	1.6~2.0	**3.3~4**
Frequency		2 MHz (Single Frequency)	1.2 MHz (Single Frequency)	1 MHz (Single Frequency)	0.7 MHz (Single Frequency)	20 MHz (Input stage) 100 MHz (Output stage)	**1 MHz (Single Frequency)**
Output Inductor & Capacitor		4.7 µH & 10 µF	2.2 µH & 4.7 µF	4.7 µH & 10 µF	10 µH & 10 µF	2x200 nH 10 nF (on-chip)	**4.7 µH & 10 µF**
Output Ripple (mV)		<25	<40	<30	<40	<40	**<25**
Operation Mode		CCM	CCM / DCM	CCM	CCM / DCM	CCM / DCM	**CCM / DCM**
Freewheeling Switch		NO	YES	NO	NO	YES	**NO**
Load Transient Response	Load Step ΔI_L (mA)	81	150	250	99	≤125	**≤150 @ Out. 1 / ≤160 @ Out. 2 / ≤180 @ Out. 3 / ≤180 @ Out. 4 / ≤180 @ Out. 5 / 250**
	Cross-Regulation (mV/mA)	0.31	0.067	0.04	0.1	None was observed	**None was observed / 0.016 ~0.035**
Area (mm^2)		7.5	1.86	5.4	11.75	10.8	**5.52**
Max. Efficiency (%)		N/A	83.1	87	88.7	74	**86**
Max. Output Power (W)		1.2	2.232	2.16	N/A	1.2	**2.28**
Power Density @ I_{MAX} (W/mm^2)		0.16	1.2	0.4	N/A	0.11	**0.413**

V. CONCLUSION

An OPDC SIMO dc–dc converter with low cross regulation and wide load range has been reported in this paper. The proposed OVACC scheme computed the energy required by all the outputs to provide the exactly same amount of energy from the input to reduce cross regulation. Although the computation requires the use of SAR ADC, the power consumption and active area of the SAR ADC are ignorable compared to those of the entire converter. Moreover, the proposed control block eliminated the need for using a free-wheeling switch and improved the overall power efficiency. In addition, the proposed architecture supported both DCM and CCM, which is preferable for wide load range applications. The proposed design was verified by the mathematical analysis and the measurement results.

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