Three-Level Bidirectional DC–DC Converter With an Auxiliary Inductor in Adaptive Working Mode for Full-Operation Zero-Voltage Switching

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***Abstract*—This paper proposes a three-level bidirectional dc–dc converter with an auxiliary inductor for full-operation zero-voltage switching (ZVS) in high-output voltage applications. The auxiliary inductor is connected across the middle node of the split flying capacitors and the center tap of the secondary winding in the transformer. In this topology, the outer and inner switches in the three-level stage can generate two independent 50% duty-cycle square waveforms, which are used to control the current in the auxiliary inductor to extend the ZVS from no loads to full loads. Considering the phase-shift angle in three-level stage, the ZVS range of the converter is analyzed, and the modulation trajectory to maintain the full-operation ZVS range with low condition loss is proposed. A flowchart implementation can guarantee the seamless transfer in different working modes. Then, the conduction loss in the proposed converter is compared with the previous three-level bidirectional solution, which illustrates that the conduction loss in the proposed converter only increases in light loads. Finally, the experimental results verify the theoretical analyses and ZVS performance across the whole power and voltage range, and the efficiency curves demonstrate the efficiency improvement.**

***Index Terms*—Auxiliary inductor, dual active bridge (DAB), three level, zero-voltage switching (ZVS).**

I. Introduction

A DUAL active bridge (DAB), shown in Fig. 1(a), is the typical solution in bidirectional dc–dc converters [1], [2]. The DAB converter is first proposed in [3] and [4]. The two full bridges generate two 50% duty-cycle square waveforms. The bidirectional power flow can be achieved by the phase shift between the two square waveforms. When the effective voltage amplitudes of the two square waveforms are almost the same, the converter can achieve high efficiency. However, when the effective voltage conversion ratio deviates from 1, the converter may lose soft switching and large circulating current also degrades the efficiency. Therefore, researchers did not pay much attention on this converter. With developing of the energy storage system in the microgrid and battery charger in an electrical vehicle, the DAB converter is becoming a good solution for bidirectional dc–dc converters.

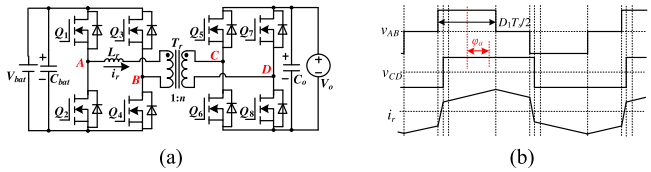

Fig. 1. (a) DAB converter. (b) EPPS modulation.

To overcome the drawbacks for large circulating current in DAB converters, a pulse width modulation (PWM) plus phase shift (PPS) is proposed for wide voltage applications [5]. Many modulations derived from PPS have been employed in DAB converters, and an extended PWM plus phase-shift (EPPS) modulation has been proposed in [6], and the typical waveforms are shown in Fig. 1(b). In Fig. 1(b), a full bridge with larger effective voltage generates a three-level voltage waveform, while the other one generates a 50% duty-cycle square voltage waveform. A minimizing conduction loss modulation [7] is also classified into EPPS. The full bridge on the larger voltage side works in PWM control, and the duty cycle is calculated by particular calculation and analysis of converter loss. A triangular current mode modulation has no circulating current in the transformer [8]. However, some switches work in zero-current switching (ZCS) instead of zero-voltage switching (ZVS). Therefore, it is not suitable for MOSFETs under high switching frequency.

To extend the soft switching, the modulations to generate two three-level voltage waveforms for two full bridges have been proposed in [9]. However, the converter suffers from high peak current. A trapezoidal modulation can maintain the converter to work in boundary current mode [10], reducing not only the root-mean-square (RMS) current in the transformer but also the peak current. An EPPS modulation by using auxiliary inductor can achieve a wide soft-switching range [11]. The full-operating range ZVS can be achieved by using commutation inductors in parallel with the active full bridges [12]. However, the commutation inductors have circulating current in all operation modes. The amount of charge that is required to charge the nonlinear parasitic output capacitances of the switches during

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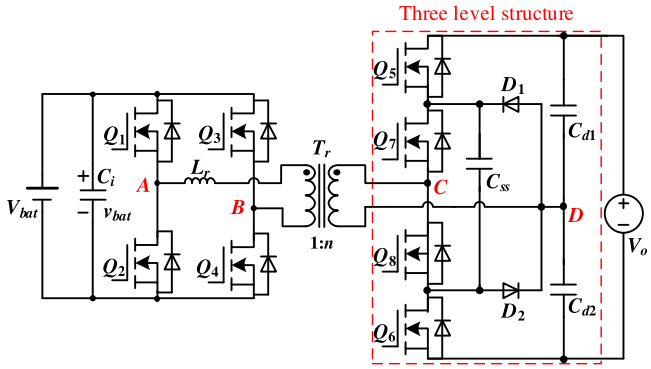


Fig. 2. Three-level bidirectional dc–dc converter.

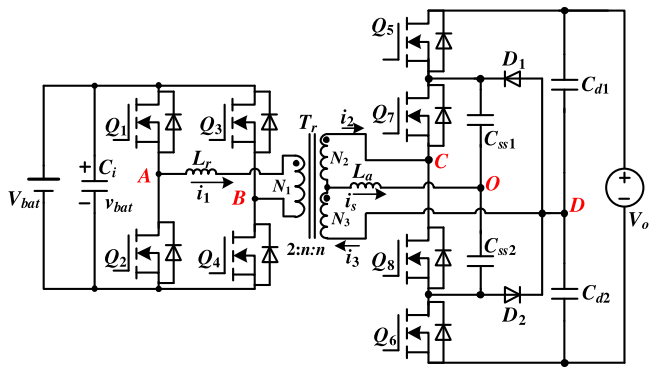


Fig. 3. Three-level bidirectional DAB converter with an auxiliary inductor.

commutation is analyzed for ZVS with nearly minimum circulating current [13]. A hybrid half bridge and full bridge to generate a four-level waveform is proposed for wide ZVS and low conduction losses [14]. The essence of these strategies is to extend more degrees of freedom for the soft switching and conduction loss reduction. The auxiliary resonant commutated pole composed of auxiliary inductor and switches can reach full ZVS capacity [15], [16]. In addition, an auxiliary commutated inductor in [17] can be extended to any full-bridge power stages for wide ZVS operation. However, the current in the auxiliary components increases the conduction loss in whole operation modes.

To simplify the conduction loss analyses of the different operation modes, a frequency-based strategy for DAB converters has been analyzed to optimize the conduction loss [18], [19]. The fundamental components in voltage and current are extracted by using Fourier transformation. The analytical methods for a sinusoidal ac grid can be used. However, it also aims to reduce the conduction loss without considering the ZVS. Furthermore, it is not accurate enough for the light-load case. Recently, the frequency-domain analyses were conducted a compromise between the conduction loss and ZVS of the switches [20], [21]. However, these did not provide the implementation in a closed-loop control.

The voltage level in the dc microgrid has reached 600–800 V or higher. Si-based MOSFETs in this voltage level have large turn-on resistance and output capacitance, which causes large conduction loss and switching loss. Insulated-gate bipolar transistors can meet this voltage level, but it does not meet high frequency requirement due to the tail-current effect. SiC-based MOSFETs can meet high switching frequency and high-voltage applications, but the cost is still very high. To meet high dc voltage applications with low cost, a three-level bidirectional dc–dc converter was proposed [22], as shown in Fig. 2. The three-level structure has been extended to current-fed bidirectional dc–dc converters [23]. By controlling the slew rate of the current in the transformer, the conduction loss is reduced. By replacing some switches with diodes, a semiactive rectifier is derived from the three-level structure for high-voltage applications [24]. Splitting the flying capacitor into two series-connected capacitors, the rectifier can achieve quadruple step-up voltage by using phase-shift control. By using split flying capacitors in the three-level stage, the outer and inner switches can generate two 50% duty-cycle square waveforms [25] in unidirectional dc–dc converters, which can reduce the circulating current.

In this paper, a three-level bidirectional dc–dc converter with an auxiliary inductor is proposed for full-operation ZVS from no loads to full loads. The auxiliary inductor is connected across the middle node of the split flying capacitors in the three-level stage and the center tap of the secondary winding in the transformer. With this topology, the outer and inner switches can generate two independent 50% duty-cycle square waveforms, which are used to control the current in the auxiliary inductor. The voltage balancing in flying capacitor is the significant issue for all the three-level structure, which reflects the voltage stress of the outer and inner switches. Whether dc–ac inverters or dc–dc converters, the three-level circuit should keep the voltage stress of the switches to be half of the dc-link voltage. However, the conventional constraint for the three-level converter is not suitable for the proposed converter. This paper investigates a new module constraint for the proposed three-level structure. In order to reduce the conduction loss caused by the auxiliary circuit, the modulation scheme in the three-level stage is designed by the boundary of the ZVS range for the full-operation ZVS.

This paper is organized as follows. The three-level bidirectional circuit and operation modes are described in Section II. The key feature and ZVS range of the converter are analyzed in Section III. According to the boundary of the ZVS range, the modulation trajectory is investigated and the adaptive modulation scheme for the ZVS from no loads to full loads is proposed. The experimental prototype is verified in Section IV. Finally, Section V provides the conclusion.

II. Proposed Three-Level Bidirectional DAB Converter

Fig. 3 shows the circuit of the three-level bidirectional DAB converter. $V_{\rm bat}$ is the battery voltage and V_o is the output voltage. On the battery side, the power stage is a full bridge. To meet high output voltage, the output-side power stage is a three-level structure. There are two series-connected windings in the secondary side of the transformer. The turns ratio of the three windings $N_1 : N_2 : N_3$ is $2 : n : n$. The auxiliary inductor is connected across the middle node of the split flying capacitors and the center tap of the secondary winding. L_r is the series

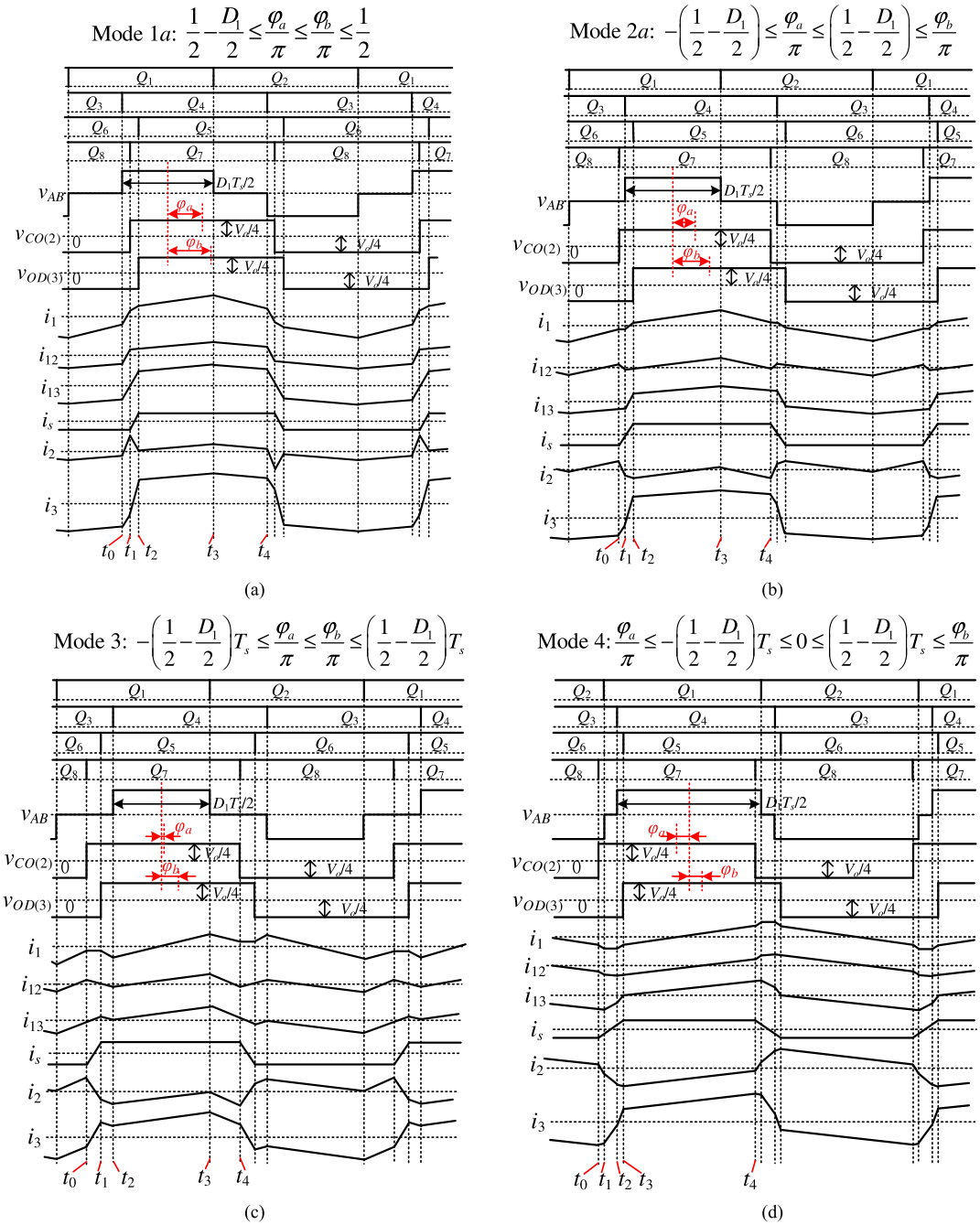


Fig. 4. Working mode in forward power flow: (a) Mode 1a: $\frac{1}{2}-\frac{D_1}{2}\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le\frac{1}{2}$. (b) Mode 2a: $-(\frac{1}{2}-\frac{D_1}{2})\le\frac{\varphi_a}{\pi}\le(\frac{1}{2}-\frac{D_1}{2})\le\frac{\varphi_b}{\pi}$. (c) Mode 3: $-(\frac{1}{2}-\frac{D_1}{2})T_s\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le(\frac{1}{2}-\frac{D_1}{2})T_s$. (d) Mode 4: $\frac{\varphi_a}{\pi}\le-(\frac{1}{2}-\frac{D_1}{2})T_s\le0\le(\frac{1}{2}-\frac{D_1}{2})T_s\le\frac{\varphi_b}{\pi}$.

inductor and L_a is the auxiliary inductor for full-operation ZVS. C_{d1} and C_{d2} are the split output filter capacitors. The output filter capacitance is large enough to regard v_{Cd1} and v_{Cd2} as constant voltage sources. The power transmitted from the battery to the output is defined as the forward power flow, and the power from the output to the battery is defined as the reverse power flow. Taking the forward power flow into consideration, the converter can work in four modes, which are shown in Fig. 4. The gate signals for Q_1-Q_8 are 50% duty cycle. $v_{\rm AB}$ is modulated by the phase shift between the two switching legs of the full bridge, and D_1 is the effective duty cycle. T_s is the switching period. φ_a is the phase shift between $v_{\rm AB}$ and $v_{\rm CO}$, and φ_b is the phase shift between $v_{\rm AB}$ and $v_{\rm OD}$. The working stages in two halves of switching period are symmetrical. One of the split output filter capacitor works in the half of the switching period, the other one works in the other half of the switching period. The output voltage of the split output filter capacitors can be naturally balanced. Therefore, the voltage across the output filter capacitors are $V_o/2$. In the three-level stage, the phase-shift angle between $v_{\rm CO}$ and $v_{\rm OD}$ is very small. Otherwise, there is large current in the auxiliary inductor. The converter cannot work normally. The full bridge in the battery side must work in

TABLE I
BOUNDARY CONDITIONS OF EACH MODE

Mode 1a	Mode 2a	Mode 3	Mode 4
$\frac{1}{2}-\frac{D_1}{2} \le \frac{\varphi_a}{\pi} \le \frac{\varphi_b}{\pi} \le \frac{1}{2}$	$-\left(\frac{1}{2}-\frac{D_1}{2}\right) \le \frac{\varphi_a}{\pi} \le \left(\frac{1}{2}-\frac{D_1}{2}\right) \le \frac{\varphi_b}{\pi}$	$-\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s \le \frac{\varphi_a}{\pi} \le \frac{\varphi_b}{\pi} \le \left(\frac{1}{2}-\frac{D_1}{2}\right)T_s$	$\frac{\varphi_a}{\pi} \le -\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s \le 0 \le \left(\frac{1}{2}-\frac{D_1}{2}\right)T_s \le \frac{\varphi_b}{\pi}$
$t_0 = 0$	$t_0 = 0$	$t_0 = 0$	$t_0 = 0$
$t_1 = \left(\frac{D_1}{4}+\frac{\varphi_a}{2\pi}-\frac{1}{4}\right)T_s$	$t_1 = \left(\frac{1}{4}-\frac{D_1}{4}-\frac{\varphi_a}{2\pi}\right)T_s$	$t_1 = \left(\frac{\varphi_b}{2\pi}-\frac{\varphi_a}{2\pi}\right)T_s$	$t_1 = \left(\frac{D_1}{4}-\frac{\varphi_a}{2\pi}-\frac{1}{4}\right)T_s$
$t_2 = \left(\frac{D_1}{4}+\frac{\varphi_b}{2\pi}-\frac{1}{4}\right)T_s$	$t_2 = \left(\frac{\varphi_b}{2\pi}-\frac{\varphi_a}{2\pi}\right)T_s$	$t_2 = \left(\frac{1}{4}-\frac{\varphi_a}{2\pi}-\frac{D_1}{4}\right)T_s$	$t_2 = \left(\frac{1}{4}-\frac{\varphi_a}{2\pi}-\frac{D_1}{4}\right)T_s$
$t_3 = \frac{D_1 T_s}{2}$	$t_3 = \left(\frac{1}{4}+\frac{D_1}{4}-\frac{\varphi_a}{2\pi}\right)T_s$	$t_3 = \left(\frac{1}{4}-\frac{\varphi_a}{2\pi}+\frac{D_1}{4}\right)T_s$	$t_3 = \left(\frac{\varphi_b}{2\pi}-\frac{\varphi_a}{2\pi}\right)T_s$
$t_4 = \frac{T_s}{2}$	$t_4 = \frac{T_s}{2}$	$t_4 = \frac{T_s}{2}$	$t_4 = \frac{T_s}{2}$

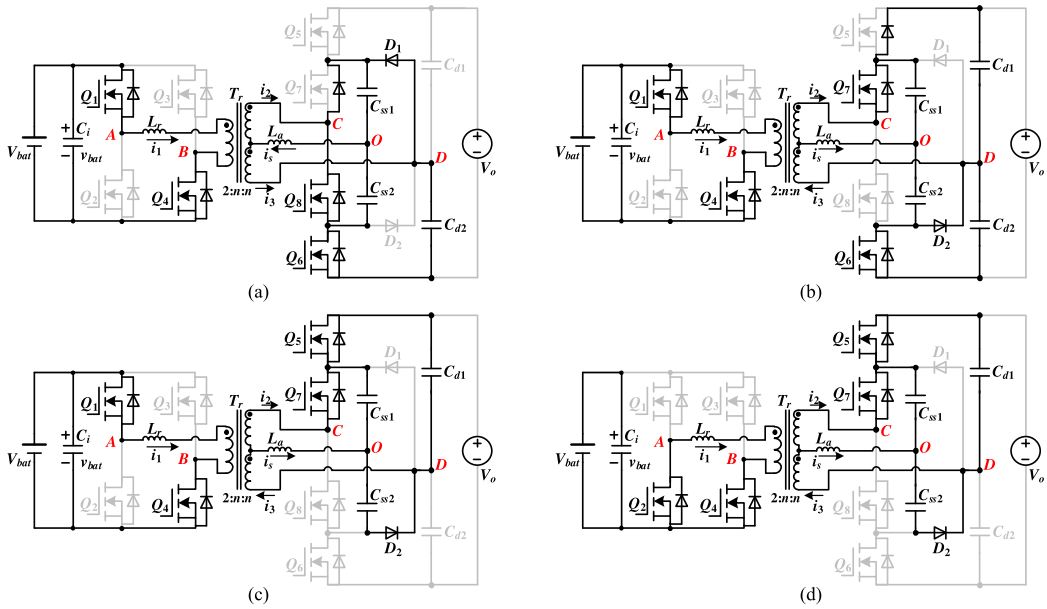


Fig. 5. Topological stages with half-switching period for Mode 1a: (a) $[t_0, t_1]$, (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, and (d) $[t_3, t_4]$.

PWM in this case. The effective voltage amplitude in the batter side of the full bridge is expressed as $nV_{\rm bat}$. It must larger than the voltage amplitude across $v_{\rm CD}$ in the three-level stage in EPPS modulation, which is expressed as $V_o/2$. Therefore, the converter must meet the conditions: $nV_{\rm bat} \ge V_o/2$.

The boundary conditions of each mode are shown in Table I. Because of the symmetry of the working mode, the same conclusions for reversed power flow can be drawn. i_{12} is assigned as the current component in winding N_2 interacted by winding N_1. i_{13} is assigned as the current component in winding N_3 interacted by winding N_1. i_{23} is assigned as the current component in winding N_3 interacted by winding N_2. Therefore, the winding current meets the following condition:

$$\begin{cases} i_s = 2i_{23} \\ i_2 = i_{12} - i_{23} \\ i_3 = i_{13} + i_{23}. \end{cases} \tag{1}$$

Ignoring the dead time of the gate signals, there are four working stages for each working mode in half of the switching period. To illustrate, the working stages in Mode 1a are shown in Fig. 5.

Stage 1 $[t_0, t_1]$ [see Fig. 5(a)]: prior to t_0, Q_1, Q_3, Q_6, and Q_8 are on, and Q_2, Q_4, Q_5, and Q_7 are off. At t_0, Q_3 is switched off and i_1 is negative. The junction capacitor of Q_4 is discharged, and Q_4 is turned on with ZVS. i_1, i_2, and i_3 start to increase. Clamping diode D_1 is forward biased. The energy stored in auxiliary inductor discharges capacitor C_{ss2} and charges capacitor C_{ss1} until i_s becomes positive. When i_2 is positive, the body diode of Q_7 is forward biased. The currents in each winding in this stage are expressed as

$$\begin{cases} i_1(t) = i_1(t_0) + \frac{V_{\rm bat}+V_o/(2n)}{L_r}(t-t_0) \\ i_{12}(t) = i_{12}(t_0) + \frac{nV_{\rm bat}/2+V_o/4}{n^2 L_r/2}(t-t_0) \\ i_{13}(t) = i_{13}(t_0) + \frac{nV_{\rm bat}/2+V_o/4}{n^2 L_r/2}(t-t_0) \\ i_{23}(t) = i_{23}(t_0). \end{cases} \tag{2}$$

Stage 2 $[t_1, t_2]$ [see Fig. 5(b)]: at t_1, Q_8 is switched off and Q_7 is turned on with ZVS. When i_3 becomes positive, i_3 flows

through the body diode of Q_5. When i_s is positive, clamping diode D_2 starts to become forward biased in this stage. The energy stored in auxiliary discharges capacitor C_{ss1} and charges capacitor C_{ss2}. The current in each winding in this stage is expressed as

$$\begin{cases} i_1(t) = i_1(t_1) + \frac{V_{\rm bat}}{L_r}(t-t_1) \\ i_{12}(t) = i_{12}(t_1) + \frac{nV_{\rm bat}/2 - V_o/4}{n^2 L_r/2}(t-t_1) \\ i_{13}(t) = i_{13}(t_1) + \frac{nV_{\rm bat}/2 + V_o/4}{n^2 L_r/2}(t-t_1) \\ i_{23}(t) = i_{23}(t_1) + \frac{2V_o/4}{4L_a}(t-t_1). \end{cases} \tag{3}$$

Stage 3 [t_2, t_3] [see Fig. 5(c)]: at t_2, Q_6 is switched off and Q_5 is turned on with ZVS. In this stage, the power is transmitted from the battery to the output. i_s still discharge C_{ss1} and charges capacitor C_{ss2}. The voltage $v_{Css1} + v_{Css2}$ are clamped to the half of the output voltage C_{d1} through D_2 and Q_5. The current in each winding in this stage is expressed as

$$\begin{cases} i_1(t) = i_1(t_2) + \frac{V_{\rm bat} - V_o/(2n)}{L_r}(t-t_2) \\ i_{12}(t) = i_{12}(t_2) + \frac{nV_{\rm bat}/2 - V_o/4}{n^2 L_r/2}(t-t_2) \\ i_{13}(t) = i_{13}(t_2) + \frac{V_{\rm bat}/2 - V_o/4}{n^2 L_r/2}(t-t_2) \\ i_{23}(t) = i_{23}(t_2). \end{cases} \tag{4}$$

Stage 4 [t_3, t_4] [see Fig. 5(d)]: at t_3, Q_1 is switched off, and i_1 starts to charge and discharge the junction capacitor of Q_1 and Q_2. When i_1 flows through the body diode of Q_2, Q_2 is turned on with ZVS. The status of the switches in the three-level stage is the same as Stage 3. The current in each winding in this stage is expressed as

$$\begin{cases} i_1(t) = i_1(t_3) - \frac{V_o/(2n)}{L_r}(t-t_3) \\ i_{12}(t) = i_{12}(t_3) - \frac{V_o/4}{n^2 L_r/2}(t-t_3) \\ i_{13}(t) = i_{13}(t_3) - \frac{V_o/4}{n^2 L_r/2}(t-t_3) \\ i_{23}(t) = i_{23}(t_3). \end{cases} \tag{5}$$

Based on (1)–(5), current i_1, i_2, and i_3 at the time of t_0, t_1, t_2, and t_3 can be derived. The working stages in Modes 2a, 3, and 4 can be analyzed in the same manner. Current i_1, i_2, and i_3 for different working modes at the time of t_0, t_1, t_2, and t_3 are also shown in the Appendix.

III. Key Feature and Modulation Scheme of the Converter

A. Voltage Balance of the Flying Capacitor

The key feature for three-level converter is that the voltage stress of the switches is reduced to half of the dc-link voltage. Therefore, the challenge for the three-level converter is how to maintain the voltage stress of the outer and inner switches. Whether the modulation scheme for conventional three-level circuits in dc–ac inverters or dc–dc converters [26]–[28], the outer switch should be turned off before the inner switch is turned off, or the voltage stress of the switches is not equal to half of the dc-link voltage. As seen the conventional three-level stage in Fig. 6(a), when Q_5 is turned off before Q_7 is turned off, node M is clamped to the node D. The voltage across Q_5

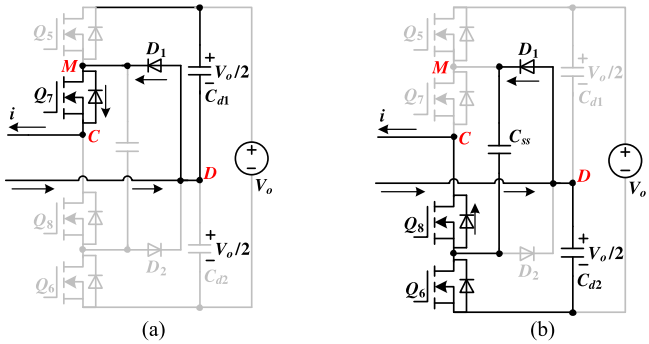


Fig. 6. Equivalent circuit in conventional three-level stage: (a) Q_5, Q_6, and Q_8 are turned off, and Q_7 is turned on, (b) Q_5 and Q_7 are turned off, and Q_6 and Q_8 are turned on.

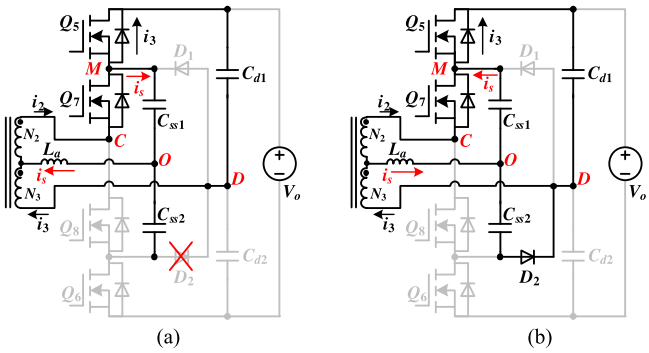


Fig. 7. Equivalent circuit in the proposed three-level stage: (a) Q_5 is turned off before Q_7 is turned off, and (b) Q_7 is turned off before Q_5 is turned off.

is equal to the voltage across capacitor C_{d1}, which is half of the dc-link voltage. As seen in Fig. 6(b), when Q_8 and Q_6 is turned on, the voltage across Q_5 still can be clamped to half of the dc-link voltage. The flying capacitor is clamped to C_{d2} through D_1 and Q_6, and the voltage across the flying capacitor maintains $V_o/2$.

Fig. 7 shows the equivalent circuit of the three-level stage in the proposed converter. When Q_5 is turned off before Q_7 is turned off, the equivalent circuit is shown in Fig. 7(a). $v_{\rm OD}$ leads $v_{\rm CO}$, and i_s flows out of node O. i_2 is larger than i_3. Therefore, the energy stored in the L_a will charge capacitor C_{ss1}. The voltage $v_{Css1} + v_{Css2}$ will become larger than $V_o/2$, and D_2 will be reverse biased. The voltage stresses of the inner switches Q_7 and Q_8 will be larger than half of the dc-link voltage, so the switches may be damaged. When Q_7 is turned off before Q_5 is turned off, i.e., $v_{\rm CO}$ leads $v_{\rm OD}$, the equivalent circuit is shown in Fig. 7(a). In this case, i_s flows into node O. i_3 is larger than i_2, so the energy stored in the auxiliary inductor will discharge the capacitor C_{ss1}. The voltage $v_{Css1} + v_{Css2}$ will be less than $V_o/2$. In this case, C_{ss1} and C_{ss2} will be clamped by C_{d1} through D_2 and Q_5. Therefore, the flying capacitor can maintain half of the dc-link voltage. When Q_6 and Q_8 are switched on, the same conclusion can be drawn.

In above, the constraint for conventional three-level converters is not suitable for the proposed three-level structure with auxiliary inductor. In order to keep the voltage stress of the

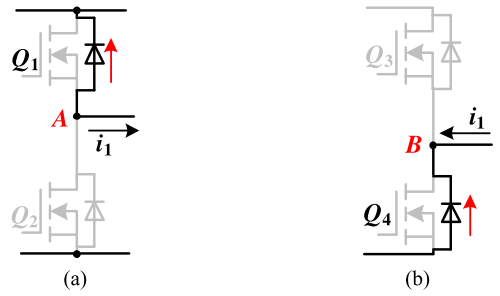


Fig. 8. Commutation during the dead time for Q_1 and Q_4: (a) Q_1 and (b) Q_4.

switches to be half of the dc-link voltage, $v_{\rm CO}$ should not lag behind $v_{\rm OD}$, i.e., φ_b should be no less than φ_a.

B. ZVS Analyses for $Q_1 - Q_4$

Because of the symmetry in two halves of the switching period, the ZVS conditions for Q_1 and Q_2 are the same, and the ZVS conditions for Q_3 and Q_4 are the same. Therefore, the conditions for Q_1 and Q_4 are analyzed in half of the switching period. The commutation during the dead time for Q_1 and Q_4 is shown in Fig. 8. To achieve ZVS of Q_1 and Q_4, i_1 should be negative and large enough, i.e., $i_1 \le I_{\rm ZVS}$, where $I_{\rm ZVS}$ is the minimum current to charge and discharge the junction capacitors of the switches during the dead time. Therefore, the ZVS constraint for Q_1 and Q_4 is shown in Table II.

Considering the voltage–second balance of the primary and secondary windings in the transformer, $nV_{\rm bat}D_1$ should equal $\frac{V_o}{2}(1-\frac{\varphi_b}{\pi}+\frac{\varphi_a}{\pi})$. If the effective duty cycle D_1 is designed as

$$D_1 = \frac{V_o}{2nV_{\rm bat}}\left(1-\frac{\varphi_b}{\pi}+\frac{\varphi_a}{\pi}\right)+D_m. \tag{6}$$

Table II can be rewritten to Table III.

Summarizing Table III, as long as $\frac{V_{\rm in}D_mT_s}{4L_r} \ge I_{\rm ZVS}$, i.e., $D_m \ge \frac{4L_rI_{\rm ZVS}}{V_{\rm in}T_s}$, then $Q_1 - Q_4$ in every mode can achieve ZVS. Therefore, D_m is selected as $\frac{4L_rI_{\rm ZVS}}{V_{\rm in}T_s}$ in the following analyses and prototype design.

C. ZVS Analyses for $Q_5 - Q_8$

Because of the symmetry in two halves of the switching period, the ZVS conditions for Q_5 and Q_6 are the same, and the ZVS conditions for Q_7 and Q_8 are the same. Therefore, the conditions for Q_5 and Q_7 are analyzed in half of the switching period. The commutation during the dead time for Q_5 and Q_7 is shown in Fig. 9. To achieve ZVS of Q_5 and Q_7, i_2 and i_3 should be positive and large enough, i.e., $i_2 > I_{\rm ZVS}$ and $i_3 > I_{\rm ZVS}$. The angle error between φ_a and φ_b is denoted as $\Delta\varphi$. Defining $\varphi_a = \varphi - \frac{\Delta\varphi}{2}$ and $\varphi_b = \varphi + \frac{\Delta\varphi}{2}$, i.e., $\varphi = \frac{\varphi_a+\varphi_b}{2}$ and $\Delta\varphi = \varphi_b - \varphi_a$, the ZVS constraints for $Q_5 - Q_8$ are shown in Table IV.

To achieve ZVS for Q_5 and Q_7 in all the operation modes, the following condition conditions should be satisfied:

1) As seen for Mode 1a in Table IV, if the phase shift angle φ is large enough, the ZVS for Q_5 and Q_7 is easy to achieve ZVS. When $\Delta\varphi = 0$, the following condition should be satisfied for the soft switching of Q_5 and Q_7:

$$\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi} \ge I_{\rm ZVS}. \tag{7}$$

Rewriting (7), the phase-shift angle φ should meet the following condition in this case:

$$\varphi \ge \varphi_{m1} \tag{8}$$

where $\varphi_{m1} = \frac{2\pi I_{\rm ZVS}nL_r}{V_{\rm bat}T_s} + (2-\frac{V_o}{nV_{\rm bat}})\frac{\pi}{4}$. If $\varphi \ge \varphi_{m1}$ and $\Delta\varphi \ge 0$, then Q_5 and Q_7 in Mode 1a can achieve ZVS.

2) When $\varphi < \varphi_{m1}$, the ZVS of $Q_5 - Q_8$ is obtained with the aid of auxiliary inductor L_a. As seen for Mode 1a in Table IV, the ZVS condition for Q_5 is expressed as

$$i_3(t_2) = \frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi} + \left(\frac{nV_{\rm bat}T_s}{4n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi} \ge I_{\rm ZVS}. \tag{9}$$

Rearranging (9), $\Delta\varphi$ is expressed as

$$\Delta\varphi \ge \frac{\pi}{\frac{nV_{\rm bat}T_s}{4n^2L_r}+\frac{V_oT_s}{32L_a}}\left(I_{\rm ZVS}-\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r} - \frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}\right). \tag{10}$$

As seen for Mode 1a in Table IV, the ZVS condition for Q_7 is expressed as

$$i_2(t_1) = \frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi} + \left(\frac{V_oT_s}{32L_a}-\frac{nV_{\rm bat}T_s}{4n^2L_r}\right)\frac{\Delta\varphi}{\pi} > I_{\rm ZVS}. \tag{11}$$

Rearranging inequality (11), $\Delta\varphi$ is expressed as

$$\Delta\varphi \ge \frac{\pi}{\frac{V_oT_s}{32L_a}-\frac{V_{\rm bat}T_s}{4nL_r}}\left(I_{\rm ZVS}-\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r} - \frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}\right). \tag{12}$$

If (12) is satisfied, then (13) is satisfied. Moreover, $\frac{V_oT_s}{32L_a} - \frac{V_{\rm bat}T_s}{4nL_r}$ should be greater than zero. Therefore, the auxiliary inductor should meet the following condition:

$$L_a < \frac{nV_oL_r}{8V_{\rm bat}}. \tag{13}$$

3) As seen in Table IV, the ZVS condition for Q_5 in Mode 2a is the same as that in Mode 1a, so it is also expressed in (10).

4) The ZVS condition for Q_7 in Mode 2a is expressed as

$$i_2(t_0) = \left(\frac{V_oT_s}{8L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi}-\frac{nV_{\rm bat}D_mT_s}{4L_r} \ge I_{\rm ZVS}. \tag{14}$$

TABLE II
ZVS CONDITIONS FOR Q_1 AND Q_4

	Mode 1a $\frac{1}{2}-\frac{D_1}{2}\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le\frac{1}{2}$	Mode 2a $-\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_a}{\pi}\le\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_b}{\pi}$	Mode 3 $-\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s$	Mode 4 $\frac{\varphi_a}{\pi}\le-\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s\le0\le\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s\le\frac{\varphi_b}{\pi}$
ZVS for Q_1	$-i_1(t_3)=-\left[\left(\frac{\varphi_a}{\pi}+\frac{\varphi_b}{\pi}-D_1\right)\frac{V_oT_s}{8nL_r}+\frac{V_{\rm bat}D_1T_s}{4L_r}\right]<-I_{\rm ZVS}$	$-i_1(t_3)=-\left[\frac{V_{bat}D_1T_s}{4L_r}-\left(D_1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_oT_s}{8nL_r}\right]<-I_{ZVS}$	$-i_1(t_3)=-\left[\frac{V_{\rm bat}D_1T_s}{4L_r}-\left(D_1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_oT_s}{8nL_r}\right]<-I_{\rm ZVS}$	$i_1(t_1)=\left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_1T_s}{4L_r}<-I_{\rm ZVS}$
ZVS for Q_4	$i_1(t_0)=\left(2-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}-D_1\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_1T_s}{4L_r}<-I_{\rm ZVS}$	$i_1(t_1)=\left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_1T_s}{4L_r}<-I_{\rm ZVS}$	$i_1(t_2)=\left(D_1+\frac{\varphi_b}{\pi}+\frac{\varphi_a}{\pi}\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_1T_s}{4L_r}<-I_{\rm ZVS}$	$i_1(t_2)=\left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_1T_s}{4L_r}<-I_{\rm ZVS}$

TABLE III
DERIVED ZVS CONDITIONS FOR Q_1 AND Q_4

	Mode 1a $\frac{1}{2}-\frac{D_1}{2}\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le\frac{1}{2}$	Mode 2a $-\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_a}{\pi}\le\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_b}{\pi}$	Mode 3 $-\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s$	Mode 4 $\frac{\varphi_a}{\pi}\le-\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s\le0\le\left(\frac{1}{2}-\frac{D_1}{2}\right)T_s\le\frac{\varphi_b}{\pi}$
ZVS for Q_1	$-i_1(t_3)=-\left(\frac{2\varphi_a}{\pi}+1-D_1\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$	$-i_1(t_3)=-\left(\frac{2\varphi_a}{\pi}+1-D_1\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$	$-i_1(t_3)=-\left(\frac{2\varphi_a}{\pi}+1-D_1\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$	$i_1(t_1)=-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$
ZVS for Q_4	$i_1(t_0)=\left(1-D_1-\frac{2\varphi_a}{\pi}\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$	$i_1(t_1)=-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$	$i_1(t_2)=-\left(1-D_1-\frac{2\varphi_b}{\pi}\right)\frac{V_oT_s}{8nL_r}-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$	$i_1(t_1)=-\frac{V_{\rm bat}D_mT_s}{4L_r}\le-I_{\rm ZVS}$

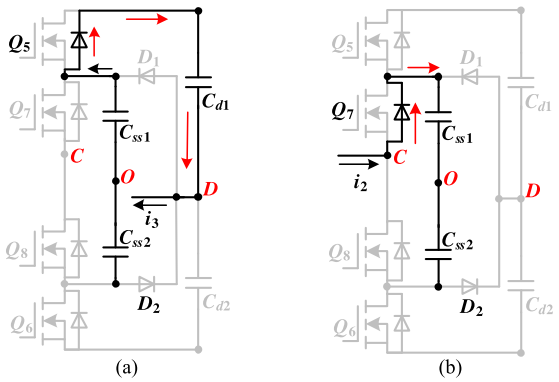


Fig. 9. Commutation during the dead time for Q_5 and Q_7: (a) Q_5 and (b) Q_7.

It is independent of φ. Rearranging (14), $\Delta\varphi$ is expressed as

$$\Delta\varphi\ge\Delta\varphi_m \tag{15}$$

where $\Delta\varphi_m=\frac{3\pi I_{\rm ZVS}}{\frac{V_oT_s}{4L_r}+\frac{V_oT_s}{16L_s}}$.

5) As seen in Table IV, the ZVS condition for Q_5 and Q_7 in Mode 3 is the same as the condition for Q_7 in Mode 2a, which is expressed in (15).
6) As seen in Table IV, the ZVS condition for Q_5 in Mode 4 is the same as in Mode 1a, which is expressed in (10).
7) The ZVS condition for Q_7 in Mode 4 is expressed as

$$i_2(t_0)>\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}-\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}+\left(\frac{V_oT_s}{32L_a}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\right)\frac{\Delta\varphi}{\pi}\ge I_{\rm ZVS}. \tag{16}$$

Rewriting (16), $\Delta\varphi$ is expressed as

$$\Delta\varphi\ge\frac{\pi}{\frac{V_oT_s}{32L_a}+\frac{V_{\rm bat}T_s}{4nL_r}}\left[I_{\rm ZVS}-\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{V_{\rm bat}T_s}{4nL_r}\frac{2\varphi}{\pi}\right]. \tag{17}$$

Above all, the ZVS condition for Q_5-Q_8 can be synthesized to (12) in Mode 1a, (10) and (15) in Mode 2a, (15) in Mode 3, and (10) and (17) in Mode 4.

D. Modulation Trajectory

According to the ZVS conditions for Q_5-Q_8 in different working modes, Fig. 10 shows the ZVS range of Q_5-Q_8 for different voltage conversion ratios, where $L_r=24\ \mu$H, $T_s=12.5\ \mu$s, $L_a=12\ \mu$H, $n=1.5$, $I_{\rm zvs}=1$ A, and $V_o=600$ V. The ZVS area is in the shadow region of the figures. As seen,

TABLE IV
ZVS CONDITIONS FOR Q_5 AND Q_7

	Mode 1a $\frac{1}{2}-\frac{D_1}{2} \le \frac{\varphi_a}{\pi} \le \frac{\varphi_b}{\pi} \le \frac{1}{2}$	Mode 2a $-\left(\frac{1}{2}-\frac{D_1}{2}\right) \le \frac{\varphi_a}{\pi} \le \left(\frac{1}{2}-\frac{D_1}{2}\right) \le \frac{\varphi_b}{\pi}$	Mode 3 $-\left(\frac{1}{2}-\frac{D_1}{2}\right) \le \frac{\varphi_a}{\pi} \le \frac{\varphi_b}{\pi} \le \frac{1}{2}-\frac{D_1}{2}$	Mode 4 $\frac{\varphi_a}{\pi} \le -(\frac{1}{2}-\frac{D_1}{2}) \le 0 \le \frac{1}{2}-\frac{D_1}{2} \le \frac{\varphi_b}{\pi}$
ZVS for Q_5	$i_3(t_2)=\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}+\left(\frac{nV_{\rm bat}T_s}{4n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi} \ge I_{\rm ZVS}$	$i_3(t_2)=\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}+\left(\frac{nV_{\rm bat}T_s}{4n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi} \ge I_{\rm ZVS}$	$i_3(t_1)=\left(\frac{V_oT_s}{8n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi}-\frac{nV_{\rm bat}D_mT_s}{4n^2L_r} \ge I_{\rm ZVS}$	$i_3(t_3)>\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}+\left(\frac{nV_{\rm bat}T_s}{4n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi} \ge I_{\rm ZVS}$
ZVS for Q_7	$i_2(t_1)=\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}+\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}+\left(\frac{V_oT_s}{32L_a}-\frac{nV_{\rm bat}T_s}{4n^2L_r}\right)\frac{\Delta\varphi}{\pi} \ge I_{\rm ZVS}$	$i_2(t_0)=\left(\frac{V_oT_s}{8n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi}-\frac{nV_{\rm bat}D_mT_s}{4L_r} \ge I_{\rm ZVS}$	$i_2(t_0)=\left(\frac{V_oT_s}{8n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi}-\frac{nV_{\rm bat}D_mT_s}{4n^2L_r} \ge I_{\rm ZVS}$	$i_2(t_0)>\frac{(V_o-2nV_{\rm bat})T_s}{8n^2L_r}-\frac{nV_{\rm bat}T_s}{4n^2L_r}\frac{2\varphi}{\pi}+\left(\frac{nV_{\rm bat}T_s}{4n^2L_r}+\frac{V_oT_s}{32L_a}\right)\frac{\Delta\varphi}{\pi} \ge I_{\rm ZVS}$

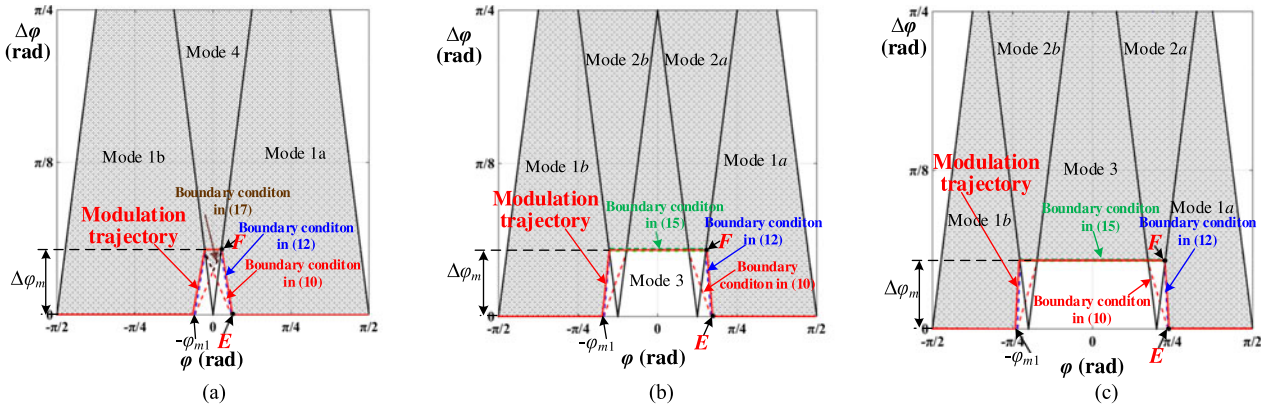


Fig. 10. ZVS range and modulation trajectory for different voltage conversion ratios: (a) $V_o/(nV_{\rm bat})=2$, (b) $V_o/(nV_{\rm bat})=1.5$, and (c) $V_o/(nV_{\rm bat})=1.2$.

with the increase of the conversion ratio, the ZVS area becomes smaller. As seen in Fig. 6(a), the conversion ratio is 2, so the effective voltage amplitudes across the primary and secondary windings of the transformer are the same. In this case, the converter only loses ZVS in light loads. When the output voltage is constant and the battery voltage is increased, the conversion ratio is decreased simultaneously. It is more difficult for the converter to achieve ZVS with the increase of the battery voltage. Therefore, if the effective voltages across the primary and secondary windings of the transformer do not coincide, the ZVS range dramatically decreases.

With the help of the auxiliary inductor, the converter can maintain ZVS performance within the whole power and full voltage range. However, it may cause more conduction loss. The modulation strategy for ZVS should be designed based on the boundary of the ZVS range at the cost of low conduction loss. As seen in Fig. 10, the coordinates of point E are $(\varphi_{m2}, \Delta\varphi_m)$, where φ_{m2} is equal to $\frac{\pi(1-D_1)+\Delta\varphi_m}{2}$. The coordinates of point F are $(\varphi_{m1}, 0)$. The line EF is expressed as

$$\Delta\varphi = \frac{\Delta\varphi_m}{\varphi_{m2}-\varphi_{m1}}(\varphi-\varphi_{m1}). \tag{18}$$

The modulation trajectories are shown in the solid line in Fig. 10, which is based on the boundary condition analyzed in Section III-C. The flowchart of the modulation trajectory is shown in Fig. 11. The control diagram is shown in Fig. 12. The output voltage reference $V_{o\_\rm ref}$ is compared with the output voltage. The voltage error is the input of the voltage controller $G_v(s)$. The output of the voltage controller is the phase shift angle φ. According to the flowchart in Fig. 11, D_1, φ_a, and φ_b are calculated based on the φ. Finally, the PWM signals of Q_1-Q_8 are obtained.

Based on the flowchart of the modulation trajectory in Fig. 11, the output power versus the phase-shift angle φ in per unit (p.u.) for different conversion ratios is shown in Fig. 13. For different conversion ratios, the modulation trajectories are seamless transfers in different operation modes. The output power increases monotonically with the phase-shift angle φ, when $-\pi/2 \le \varphi \le \pi/2$. In the proposed modulation trajectory, the modulation trajectories for φ_a and φ_b for different conversion ratios are shown in Fig. 14. It illustrates that φ_a equals φ_b when the phase angle is large enough. Otherwise, $\Delta\varphi$ is greater than zero for the ZVS of Q_5-Q_8. As illustrated in Fig. 14, $\Delta\varphi$ equals $\Delta\varphi_m$ in Modes 3, 4, 2a, and 2b.

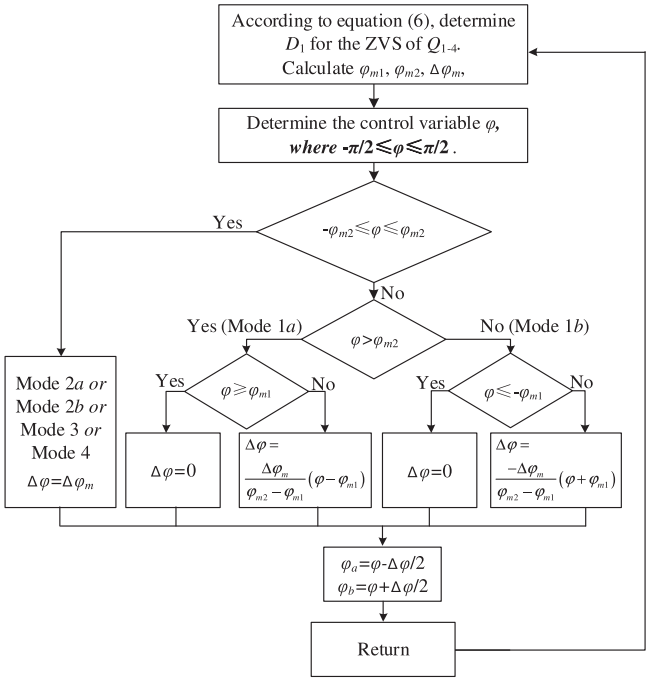


Fig. 11. Flowchart of the modulation trajectory.

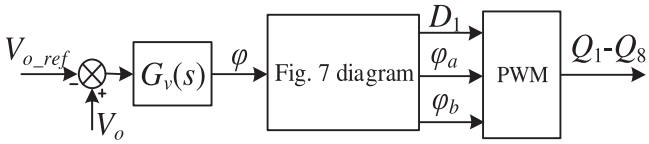


Fig. 12. Control diagram of the converter.

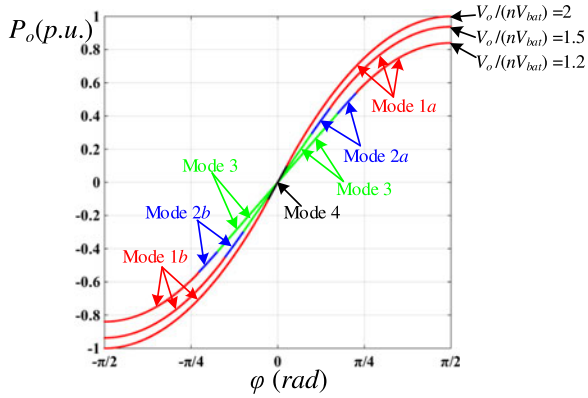


Fig. 13. Output power versus phase-shift angle φ for different voltage conversion ratios.

Within the whole load range, the proposed converter can achieve ZVS. Actually, if $\Delta\varphi$ equals zero, the working modes in the proposed converter are the same as the three-level bidirectional converter with EPPS, whose output power versus the phase-shift angle φ in per unit (p.u.) is shown in Fig. 15. The shadow area is the hard-switching range. With the decrease of the voltage conversion ratios, it becomes harder for the converter to achieve soft switching.

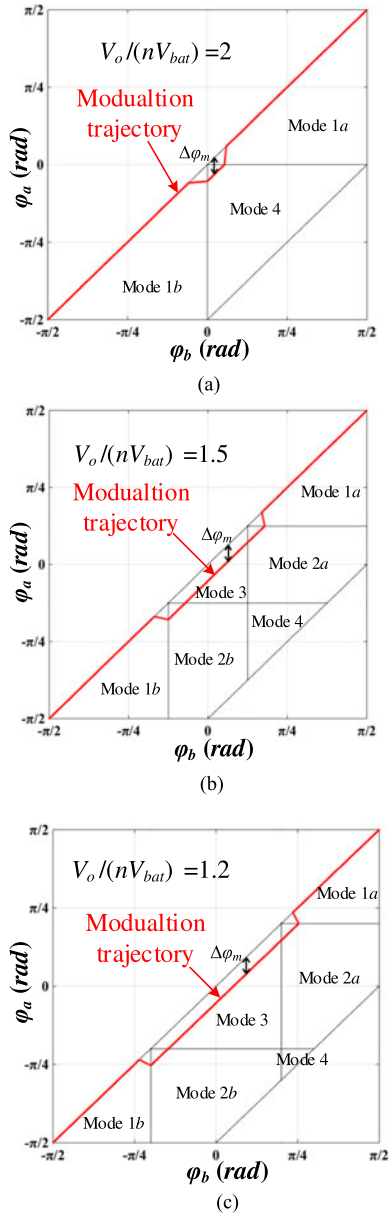


Fig. 14. Modulation trajectories for φ_a and φ_b for different voltage conversion ratios: (a) $V_o/(nV_{\rm bat}) = 2$, (b) $V_o/(nV_{\rm bat}) = 1.5$, and (c) $V_o/(nV_{\rm bat}) = 1.2$.

E. Conduction Loss Comparison

To study the conduction loss, the RMS of the current in the transformer should be calculated. The RMS of i_1 reflects the conduction loss on the battery side of the switches, and the RMS of i_2 and i_3 reflects the conduction loss on the output side of the switches. Therefore, the RMS current in the converter is defined as

$$I_{\rm RMS} = \frac{1}{n}\sqrt{\frac{1}{T_s}\int_0^{Ts} {i_1}^2(t)dt} + \sqrt{\frac{1}{T_s}\int_0^{Ts} {i_2}^2(t)dt} + \sqrt{\frac{1}{T_s}\int_0^{Ts} {i_3}^2(t)dt}. \quad (19)$$

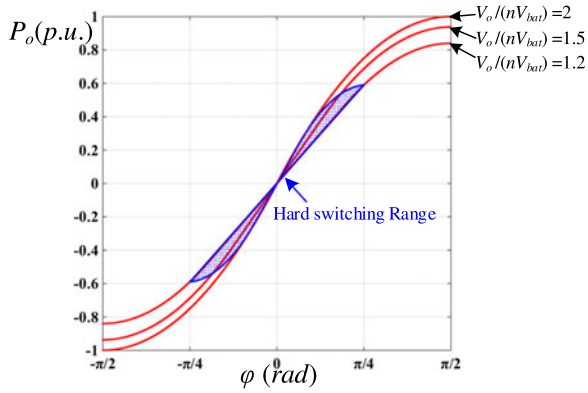


Fig. 15. Output power versus phase-shift angle φ in per unit for extended phase-shift control.

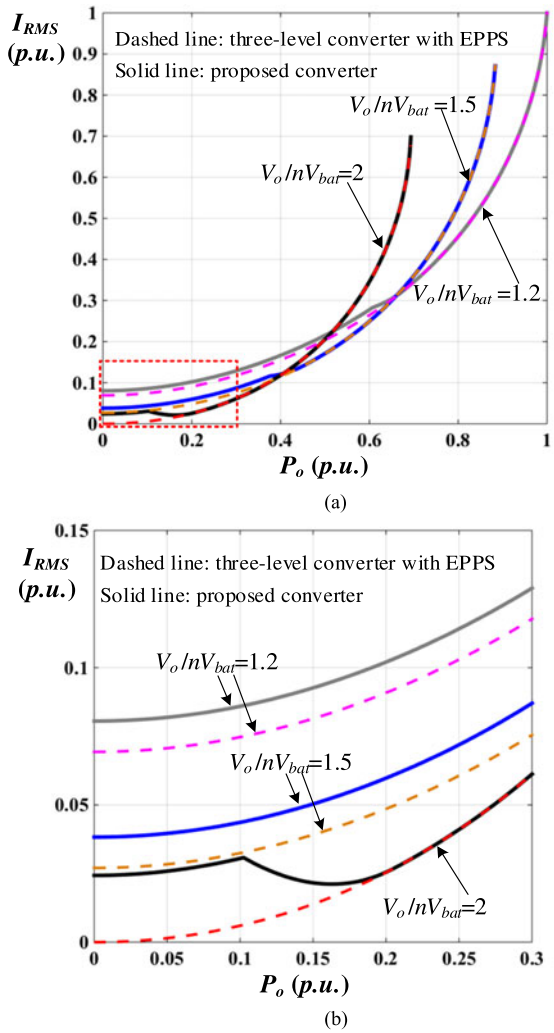


Fig. 16. (a) RMS current of the proposed converter and three-level converter with EPPS. (b) Zoom-in figure of the dashed box in Fig. 12(a).

With the help of MATLAB, the RMS currents in the converter for different conversion ratios are shown in Fig. 16. The solid lines are the RMS current in the proposed converter, and the dashed lines are the RMS current in the three-level converter shown in Fig. 2 with EPPS. Fig. 16(b) is the zoom-in figure

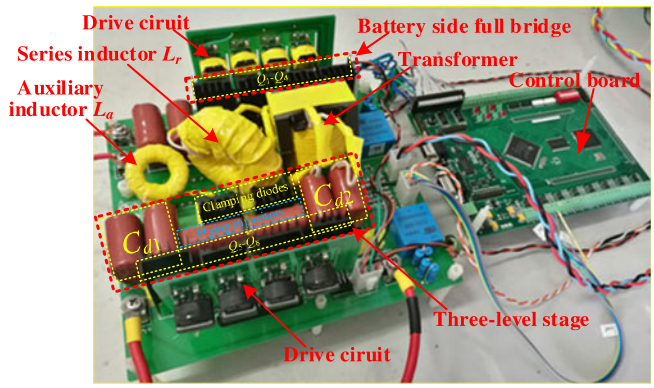


Fig. 17. 1.2-kW proposed converter.

TABLE V
DETAILED SPECIFICATIONS

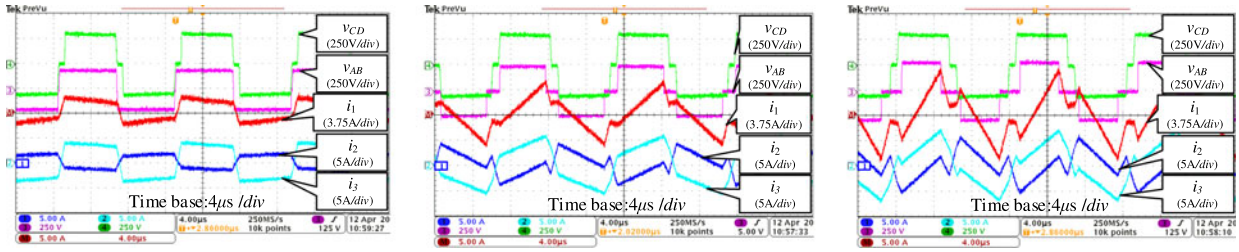
Items	Symbol	Parameter
Battery voltage	$V_{\rm bat}$	200–300 V
Output voltage	V_o	600 V
Turns ratio of the transformers	n	1.5
Switching frequency	$f_s\,(T_s)$	80 kHz (12.5 μs)
Primary switches	Q_{1-4}	FQL40N50
Secondary switches	Q_{5-8}	FQL40N50
Clamping diodes	D_1, D_2	DSEP12-12A
Series inductor	L_r	24 μH
Auxiliary inductor	L_a	12 μH
Output filter capacitance	C_{d1}, C_{d2}	10 μF
Flying capacitance	C_{ss1}, C_{ss2}	4.7 μF

of the dashed box in Fig. 16(a). As seen, the conduction loss in the two converters is the same under heavy loads. When the effective conversion ratio is 2, the three-level converter with EPPS only loses ZVS status with light loads. To guarantee the ZVS within whole power range, the proposed converter has more conduction loss. However, the switching loss is the dominant losses with light loads, and the conduction loss does not have a strong impact on the efficiency in this case. Moreover, the conduction loss with heavy loads in the proposed converter is the same as the three-level converter with EPPS. Therefore, hard switching in the three-level converter with EPPS may degrade the efficiency. With the decrease of the conversion ratio, i.e., with the increase of the battery voltage for the constant output voltage, it is much harder for the three-level converter with EPPS to achieve ZVS of all the switches. According to the modulation trajectory, the proposed converter can maintain ZVS of all the switches within the whole power range and over a wide voltage range with low conduction loss, so the efficiency can be improved.

IV. EXPERIMENTAL VERIFICATIONS

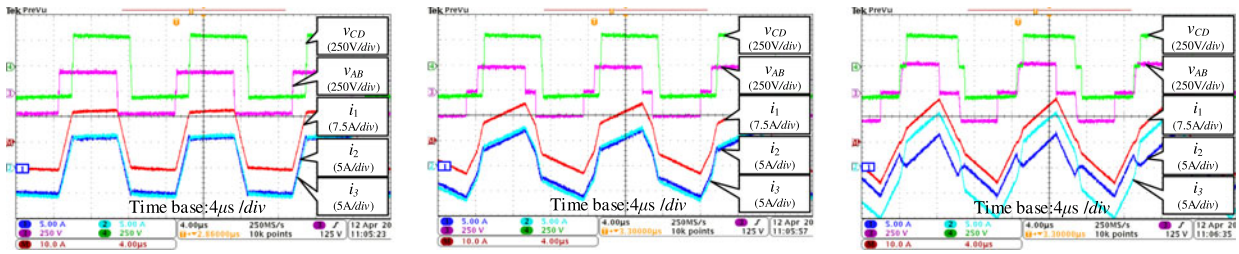
A 1200-W experimental prototype with a 200–300 V battery voltage and 600-V output voltage was built to verify the proposed converter. Fig. 17 shows the prototype used for test. The detailed specifications are shown in Table V.

Fig. 18 shows key waveforms for the forward power flow with light loads. To achieve ZVS of all the switches with light



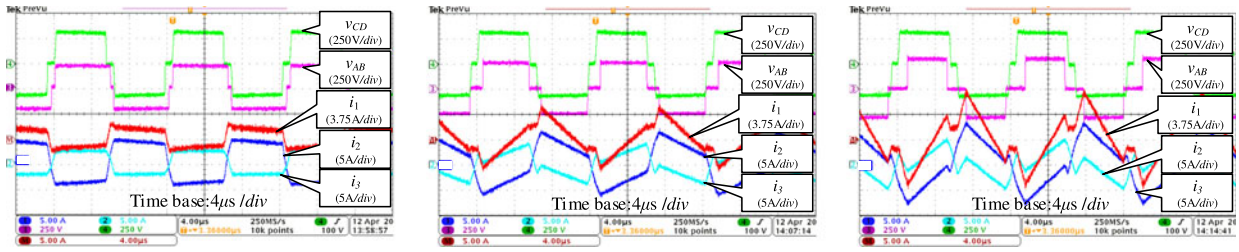
(a) (b) (c)

Fig. 18. Measured key waveforms for the forward power flow in light loads: (a) $V_{\rm bat} = 200$ V, $P_o = 280$ W, (b) $V_{\rm bat} = 240$ V, $P_o = 280$ W, and (c) $V_{\rm bat} = 280$ V, $P_o = 280$ W.



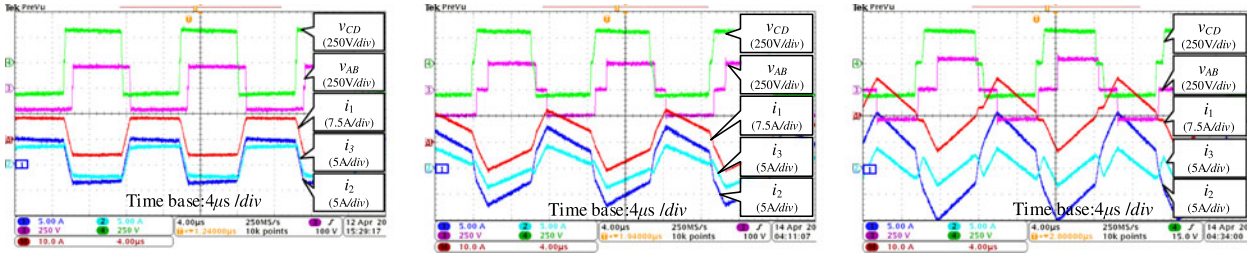
(a) (b) (c)

Fig. 19. Measured key waveforms for the forward power flow in heavy loads: (a) $V_{\rm bat} = 200$ V, $P_o = 1200$ W, (b) $V_{\rm bat} = 240$ V, $P_o = 1200$ W, and (c) $V_{\rm bat} = 280$ V, $P_o = 1200$ W.



(a) (b) (c)

Fig. 20. Measured key waveforms for the reverse power flow in light loads: (a) $V_{\rm bat} = 200$ V, $P_o = -240$ W, (b) $V_{\rm bat} = 240$ V, $P_o = -280$ W, and (c) $V_{\rm bat} = 280$ V, $P_o = -330$ W.

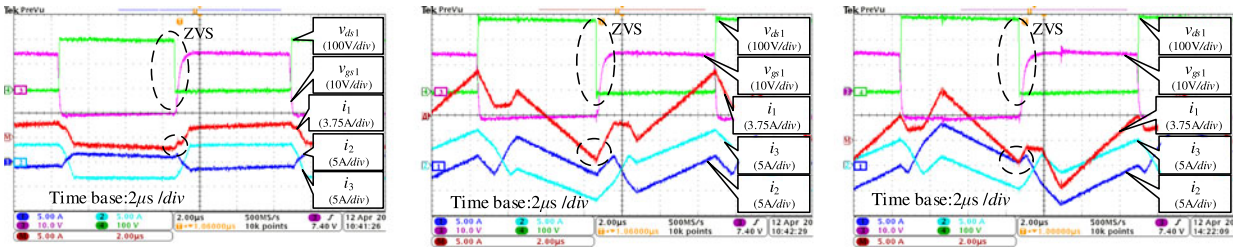


(a) (b) (c)

Fig. 21. Measured key waveforms for the reverse power flow in heavy loads: (a) $V_{\rm bat} = 200$ V, $P_o = -1000$ W, (b) $V_{\rm bat} = 240$ V, $P_o = -1000$ W, and (c) $V_{\rm bat} = 280$ V, $P_o = -1000$ W.

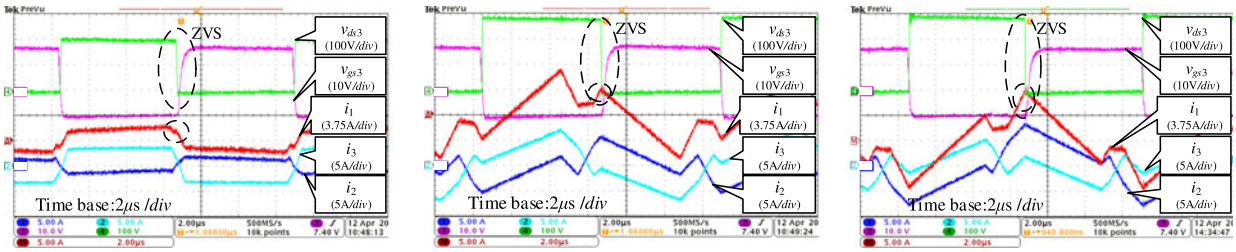
loads, the current in the auxiliary inductor should be used, and the angle error $\Delta\varphi$ is greater than zero. Fig. 18(a) shows the key waveforms when $V_{\rm bat} = 200$ V and $P_o = 280$ W. In this case, the converter works in Mode 4. As seen in Fig. 18(b) and (c), with the increase of the battery voltage, D_1 is decreased. In these cases, the converter transits into Mode 3.

Fig. 19 shows the key waveforms for the forward power flow with heavy loads. In Fig. 19(a), when the battery voltage is 200 V, the converter works in Mode 1a for a 1200-W load and the angle error $\Delta\varphi$ becomes zero. In Fig. 19(b), when the battery voltage increases to 240 V, the converter still works in Mode 1a. The currents in the transformer are large enough for ZVS



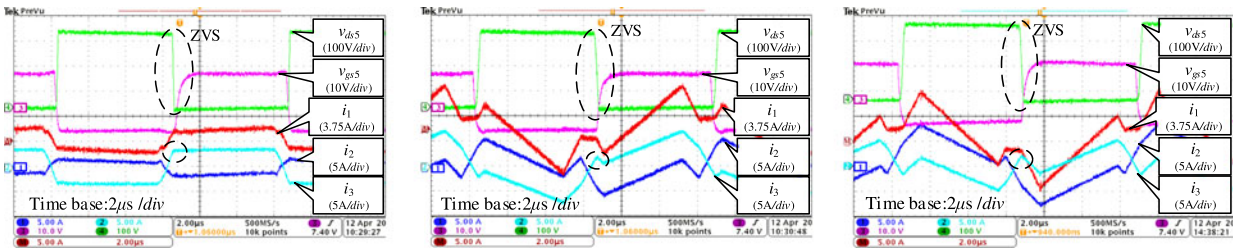
(a) (b) (c)

Fig. 22. Gate signal and drain–source voltage of switch Q_1: (a) $V_{\rm bat} = 200$ V, $P_o = 280$ W, (b) $V_{\rm bat} = 280$ V, $P_o = 280$ W, and (c) $V_{\rm bat} = 280$ V, $P_o = -334$ W.



(a) (b) (c)

Fig. 23. Gate signal and drain–source voltage of switch Q_3: (a) $V_{\rm bat} = 200$ V, $P_o = 280$ W, (b) $V_{\rm bat} = 280$ V, $P_o = 280$ W, and (c) $V_{\rm bat} = 280$ V, $P_o = -334$ W.



(a) (b) (c)

Fig. 24. Gate signal and drain–source voltage of switch Q_5: (a) $V_{\rm bat} = 200$ V, $P_o = 280$ W, (b) $V_{\rm bat} = 280$ V, $P_o = 280$ W, (c) $V_{\rm bat} = 280$ V, $P_o = -334$ W.

during the commutation, so the angle error $\Delta\varphi$ is still zero. In Fig. 19(c), when the input voltage is 280 V, not all the switches can achieve ZVS for a conventional three-level converter with EPPS, so the angle error $\Delta\varphi$ is greater than zero. As seen in Fig. 19(c), the converter works in Mode 2a in this case.

Fig. 20 shows the key waveforms for the reverse power flow with light loads. In Fig. 20(a), the converter works in Mode 4. In Fig. 20(b), the converter works in Mode 2b. In Fig. 20(c), the converter works in Mode 3. In these cases, $\Delta\varphi$ is greater than zero for the ZVS of $Q_5 - Q_8$. The working modes in Fig. 20 are nearly symmetrical with those in Fig. 18.

Fig. 21 shows the key waveforms for the reverse power flow with heavy loads. In Fig. 21(a), the converter works in Mode 1b. The current in the transformer is large enough to achieve the ZVS of all the switches, so $\Delta\varphi$ is equal to zero. In Fig. 21(b), the battery voltage is 240 V, and the power is –1000 W. The converter works in Mode 1b, but $\Delta\varphi$ is greater than zero. As illustrated in Fig. 21(c), with the increase of the battery voltage, the phase angle is decreased and the converter switches to Mode 2b.

Fig. 22 shows the gate signal and drain–source voltage of switch Q_1. In different working states, i_1 is less than zero during this commutation, illustrating that Q_1 works in ZVS in both forward and reverse power flow. Q_2 operates in the same working mode in the other half of the switching period, so it also can achieve ZVS.

Fig. 23 shows the gate signal and drain–source voltage of switch Q_3. Before Q_3 is turned on, i_1 is greater than zero in different working modes, which highlights the ZVS of Q_3 in both forward and reverse power flow. Q_4 operates in the same working mode in the other half of the switching period, so it is also easy to achieve ZVS.

Fig. 24 shows the gate signal and drain–source voltage of switch Q_5. As seen in different working states, before Q_5 is turned on, i_3 has a large current to charge and discharge the junction capacitors of Q_6 and Q_5. Therefore, Q_5 can work in ZVS in both forward and reverse power flow. Q_6 operates in the same working mode in the other half of the switching period, so it is also easy to achieve ZVS.

Fig. 25 shows the gate signal and drain–source voltage of switch Q_7. As seen in different working states, i_2 has large enough value to charge and discharge the junction capacitors of Q_8 and Q_7 before Q_7 is turned on. It demonstrates the ZVS performance for Q_7 in both forward and reverse power flow.

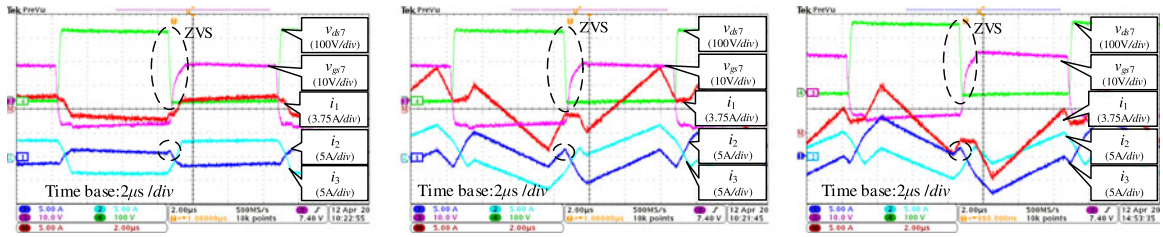


Fig. 25. Gate signal and drain–source voltage of switch Q_7: (a) $V_{\rm bat} = 200$ V, $P_o = 280$ W, (b) $V_{\rm bat} = 280$ V, $P_o = 280$ W, and (c) $V_{\rm bat} = 280$ V, $P_o = -334$ W.

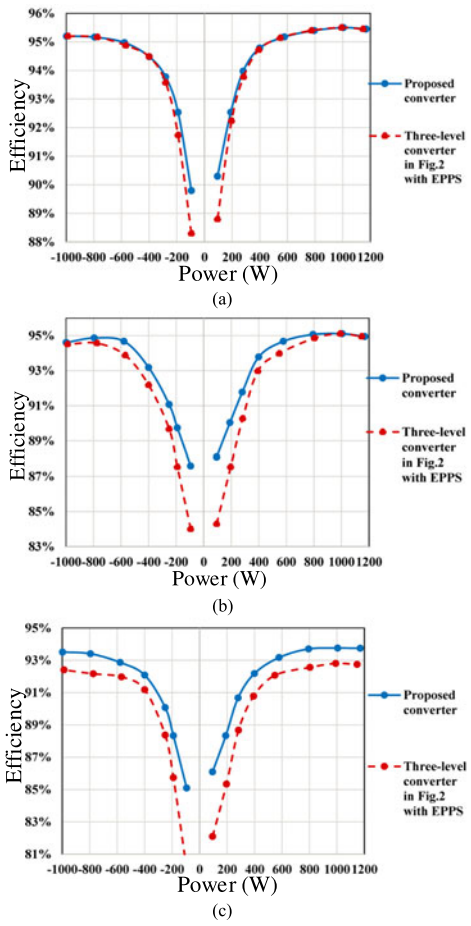


Fig. 26. Efficiency curves for the proposed converter and the three-level bidirectional converter with EPPS at (a) $V_{\rm bat} = 200$ V, (b) $V_{\rm bat} = 240$ V, and (c) $V_{\rm bat} = 280$ V.

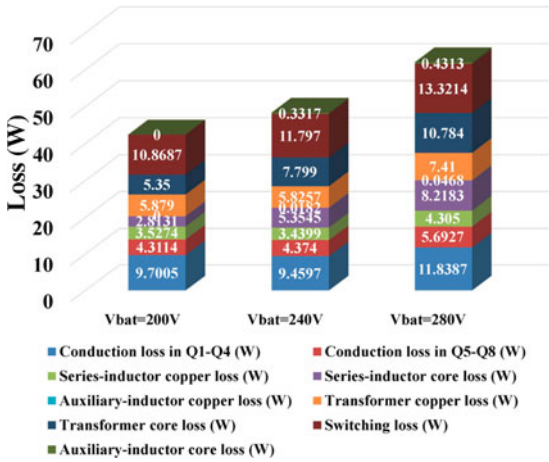


Fig. 27. Calculated power loss distribution under the rated load condition.

Q_8 operates in the same working mode in the other half of the switching period, so it also achieves ZVS.

The measured efficiency curves for the proposed converter and the conventional three-level bidirectional converter shown in Fig. 2 with EPPS are illustrated in Fig. 26. Fig. 26(a) shows the efficiency curve for the 200-V battery voltage. In this case, the effective conversion ratio is 2, while the slew rate of the current in the transformer during the power transmission interval is zero. Therefore, the three-level bidirectional converter with EPPS has a wide ZVS range. The converter loses ZVS status only in light loads. The proposed converter can achieve full-operation ZVS, so the efficiency in light loads is higher than that of the three-level converter with EPPS. As seen in Fig. 26(b) and (c), with the increase of the battery voltage, it becomes harder for the three-level converter with EPPS to achieve ZVS of all the switches. However, the proposed converter still can maintain high efficiency because of the ZVS performance within the whole power and voltage range. Especially at the 280-V battery voltage and a 1200-W load, an efficiency improvement of more than 1% is achieved.

The calculated loss distribution under rated load condition is shown in Fig. 27. With increase of the battery voltage, the loss is increased. The conduction loss in the three-level stage and loss in the auxiliary inductor are only in a small portion. Therefore, the loss caused by the auxiliary components is very low. However, because of the ZVS of all the switching, the efficiency can be improved.

V. Conclusion

In this paper, a three-level bidirectional dc–dc converter with an auxiliary inductor is proposed. The converter is composed of a full bridge on the low voltage side and a three-level stage on the high voltage side, linked with a transformer and a series inductor. The flying capacitor in the three-level stage is split into two series-connected capacitors. The auxiliary inductor is connected across the middle node of the split flying capacitors and the center tap of the secondary winding of the transformer. The outer and inner switches in the three-level stage can generate two independent 50% square waveforms, which can be

used to control the current in the auxiliary inductor. According to the different working modes of the converter, the ZVS range is analyzed, which is associated with not only the loads but also the voltage conversion ratio. When the effective voltage conversion ratio is 2, the converter only loses ZVS status under light loads. With the decrease of the conversion ratio, the converter encounters difficulty for achieving ZVS. Therefore, the current in the auxiliary inductor is used to maintain the ZVS within the whole power and over a wide voltage range. To reduce the conduction loss in the auxiliary inductor, the boundary condition of the ZVS range is used to design the modulation trajectory. The flowchart of the modulation trajectory can guarantee the ZVS of all the switches with low conduction loss. Finally, the experimental results verified the ZVS performance in the proposed converter. The efficiency curves demonstrate the efficiency improvement for the conventional three-level bidirectional dc–dc converter with EPPS.

APPENDIX

The current i_1, i_2, and i_3 at the time of t_0, t_1, t_2, and t_3 in Mode 1a is expressed as follows:

$$\begin{cases} i_1(t_0) = \left(2 - \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi} - D_1\right) \frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_1) = \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} + \left(\frac{2\varphi_a}{\pi} - 1\right) \frac{V_{\rm bat} T_s}{4L_r} \\ i_1(t_2) = \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} + \left(\frac{2\varphi_b}{\pi} - 1\right) \frac{V_{\rm bat} T_s}{4L_r} \\ i_1(t_3) = \left(\frac{\varphi_a}{\pi} + \frac{\varphi_b}{\pi} - D_1\right) \frac{V_o T_s}{8nL_r} + \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_4) = \frac{V_{bat} D_1 T_s}{4L_r} - \left(2 - \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi} - D_1\right) \frac{V_o T_s}{8nL_r} \end{cases} \tag{A1}$$

$$\begin{cases} i_2(t_0) = \left(2 - \frac{2\varphi_a}{\pi} - D_1\right) \frac{V_o T_s}{16n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{8nL_r} \\ \qquad - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_1) = \frac{V_o T_s}{8n^2 L_r} - \left(1 - \frac{2\varphi_a}{\pi}\right) \frac{V_{\rm bat} T_s}{4nL_r} - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_2) = \left(1 + \frac{2\varphi_a}{\pi} - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \left(1 - \frac{2\varphi_b}{\pi}\right) \frac{V_{\rm bat} T_s}{4nL_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_3) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(D_1 - \frac{2\varphi_a}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_4) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(2 - \frac{2\varphi_a}{\pi} - D_1\right) \frac{V_o T_s}{8n^2 L_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \end{cases} \tag{A2}$$

$$\begin{cases} i_3(t_0) = \left(2 - \frac{2\varphi_b}{\pi} - D_1\right) \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_3(t_1) = \left(1 - \frac{2\varphi_b}{\pi} + \frac{2\varphi_a}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \left(1 - \frac{2\varphi_a}{\pi}\right) \frac{V_{\rm bat} T_s}{4nL_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_3(t_2) = \frac{V_o T_s}{8n^2 L_r} - \left(1 - \frac{2\varphi_b}{\pi}\right) \frac{V_{\rm bat} T_s}{4nL_r} - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_3(t_3) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(D_1 - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} \\ \qquad - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_3(t_4) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(2 - \frac{2\varphi_b}{\pi} - D_1\right) \frac{V_o T_s}{8n^2 L_r} \\ \qquad - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right). \end{cases} \tag{A3}$$

The current i_1, i_2, and i_3 at the time of t_0, t_1, t_2, and t_3 in Mode 2a is expressed as follows:

$$\begin{cases} i_1(t_0) = \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_1) = \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_2) = \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} - \left(1 - \frac{2\varphi_b}{\pi}\right) \frac{V_{\rm bat} T_s}{4L_r} \\ i_1(t_3) = \frac{V_{\rm bat} D_1 T_s}{4L_r} - \left(D_1 - \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} \\ i_1(t_4) = \frac{V_{\rm bat} D_1 T_s}{4L_r} - \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} \end{cases} \tag{A4}$$

$$\begin{cases} i_2(t_0) = \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_1) = \left(D_1 + \frac{2\varphi_a}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} \\ \qquad - \frac{V_o T_s}{32L_a} \left(1 - \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi} - D_1\right) \\ i_2(t_2) = \left(1 + \frac{2\varphi_a}{\pi} - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \left(1 - \frac{2\varphi_b}{\pi}\right) \frac{V_{\rm bat} T_s}{4nL_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_3) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(D_1 - \frac{2\varphi_a}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_4) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{8n^2 L_r} + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \end{cases} \tag{A5}$$

$$\begin{cases} i_3(t_0) = \left(1 + \frac{2\varphi_a}{\pi} - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_3(t_1) = \left(2 - D_1 - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(1 - \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi} - D_1\right) \\ i_3(t_2) = \frac{V_o T_s}{8n^2 L_r} - \left(1 - \frac{2\varphi_b}{\pi}\right) \frac{V_{\rm bat} T_s}{4nL_r} - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_3(t_3) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(D_1 - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_3(t_4) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(1 + \frac{2\varphi_a}{\pi} - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} \\ \qquad - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right). \end{cases} \tag{A6}$$

The current i_1, i_2, and i_3 at the time of t_0, t_1, t_2, and t_3 in Mode 3 is expressed as follows:

$$\begin{cases} i_1(t_0) = \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_1) = \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_2) = \left(D_1 + \frac{\varphi_b}{\pi} + \frac{\varphi_a}{\pi}\right) \frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_3) = \frac{V_{\rm bat} D_1 T_s}{4L_r} - \left(D_1 - \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} \\ i_1(t_4) = \frac{V_{\rm bat} D_1 T_s}{4L_r} - \left(1 + \frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \frac{V_o T_s}{8nL_r} \end{cases} \tag{A7}$$

$$\begin{cases} i_2(t_0) = \frac{V_o T_s}{18n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_1) = \left(1 + \frac{2\varphi_a}{\pi} - \frac{2\varphi_b}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} \\ \qquad + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_2) = \left(D_1 + \frac{2\varphi_a}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_3) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(D_1 - \frac{2\varphi_a}{\pi}\right) \frac{V_o T_s}{8n^2 L_r} + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \\ i_2(t_4) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{8n^2 L_r} + \frac{V_o T_s}{32L_a} \left(\frac{\varphi_a}{\pi} - \frac{\varphi_b}{\pi}\right) \end{cases} \tag{A8}$$

$$\begin{cases} i_3(t_0) = \left(1+\frac{2\varphi_a}{\pi}-\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} \\ \qquad +\frac{V_o T_s}{32L_a}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_1) = \frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{32L_a}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_2) = \left(D_1+\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{32L_a}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_3) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(D_1-\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} - \frac{V_o T_s}{32L_a}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_4) = \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \left(1+\frac{2\varphi_a}{\pi}-\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} \\ \qquad -\frac{V_o T_s}{32L_a}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right). \end{cases} \tag{A9}$$

The current i_1, i_2, and i_3 at the time of t_0, t_1, t_2, and t_3 in Mode 4 is expressed as follows:

$$\begin{cases} i_1(t_0) = \left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_o T_s}{8nL_r} - \left(1+\frac{2\varphi_a}{\pi}\right)\frac{V_{\rm bat} T_s}{4L_r} \\ i_1(t_1) = \left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_2) = \left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_o T_s}{8nL_r} - \frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_3) = \left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_o T_s}{8nL_r} - \left(1-\frac{2\varphi_b}{\pi}\right)\frac{V_{\rm bat} D_1 T_s}{4L_r} \\ i_1(t_4) = \left(1+\frac{2\varphi_a}{\pi}\right)\frac{V_{\rm bat} T_s}{4L_r} - \left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\frac{V_o T_s}{8nL_r} \end{cases} \tag{A10}$$

$$\begin{cases} i_2(t_0) = \frac{V_o T_s}{8n^2 L_r} - \left(1+\frac{2\varphi_a}{\pi}\right)\frac{V_{\rm bat} T_s}{4nL_r} - \frac{V_o T_s}{32L_s}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_2(t_1) = \left(2+\frac{2\varphi_a}{\pi}-D_1\right)\frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{32L_s} \\ \qquad \times\left(D_1-1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_2(t_2) = \left(D_1+\frac{2\varphi_a}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{32L_s} \\ \qquad \times\left(1-D_1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_2(t_3) = \left(1+\frac{2\varphi_a}{\pi}-\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} - \left(1-\frac{2\varphi_b}{\pi}\right)\frac{V_{\rm bat} T_s}{4nL_r} \\ \qquad +\frac{V_o T_s}{32L_s}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_2(t_4) = \left(1+\frac{2\varphi_a}{\pi}\right)\frac{V_{\rm bat} T_s}{4nL_r} - \frac{V_o T_s}{8n^2 L_r} + \frac{V_o T_s}{32L_s}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \end{cases} \tag{A11}$$

$$\begin{cases} i_3(t_0) = \left(1+\frac{2\varphi_a}{\pi}-\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} - \left(1+\frac{2\varphi_a}{\pi}\right)\frac{V_{\rm bat} T_s}{4nL_r} \\ \qquad +\frac{V_o T_s}{32L_s}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_1) = \left(D_1-\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} + \frac{V_o T_s}{32L_s} \\ \qquad \times\left(D_1-1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_2) = \left(2-\frac{2\varphi_b}{\pi}-D_1\right)\frac{V_o T_s}{8n^2 L_r} - \frac{V_{\rm bat} D_1 T_s}{4nL_r} + \frac{V_o T_s}{32L_s} \\ \qquad \times\left(1-D_1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_3) = \frac{V_o T_s}{8n^2 L_r} - \left(1-\frac{2\varphi_b}{\pi}\right)\frac{V_{\rm bat} D_1 T_s}{4nL_r} - \frac{V_o T_s}{32L_s}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right) \\ i_3(t_4) = \left(1+\frac{2\varphi_a}{\pi}\right)\frac{V_{\rm bat} T_s}{4nL_r} - \left(1+\frac{2\varphi_a}{\pi}-\frac{2\varphi_b}{\pi}\right)\frac{V_o T_s}{8n^2 L_r} \\ \qquad -\frac{V_o T_s}{32L_s}\left(\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right). \end{cases} \tag{A12}$$

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