Matrix Converter Based Open-End Winding Drives With Common-Mode Elimination: Topologies, Analysis, and Comparison

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***Abstract*—Matrix converter based open-end winding drives modulated with rotating vectors eliminate the high-frequency common-mode output voltage that could otherwise cause motor failure. Unlike back-to-back converters, no intermediate dc bus capacitor is required—better power density and reliability may, therefore, be achievable. A high voltage transfer ratio and input power factor control capability put these open-end winding drives at a significant advantage over conventional matrix converters. At least three realizations of the matrix converter based open-end drive are possible. This paper compares these three realizations to identify the best topology and presents experimental results validating its capabilities. Filter optimization, loss-optimal vector sequences, and other practical considerations are also discussed. Finally, a comparison with the state-of-the-art back-to-back converters is provided to investigate if the potential improvements are in fact attainable.**

***Index Terms*—AC motor drives, ac–ac power conversion, power electronics, pulse width modulated (PWM) power converters.**

I. Introduction

BEARING currents attributed to the high-frequency (HF) common-mode voltage (HF CMV) generated by pulse width modulated (PWM) electric drives have been linked to motor failure [1]–[5]. Since this HF CMV is inevitable in conventional space vector PWM voltage source inverters (VSIs), several mitigation measures have been reported. These may include passive measures, e.g., common-mode chokes that impede the common-mode current, Y-capacitors that shunt the common-mode current, or a common-mode filter that utilizes both common-mode chokes and capacitors. Other passive measures are shaft grounding brushes that attempt to short the shaft to the motor frame such that the shaft voltage cannot build up, and insulating bearings that do not allow electric current [6]. A notable passive method to eliminate the bearing currents is an electrostatically shielded motor wherein a conductive shield bypasses the rotor in the common-mode circuit [2].

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Aforementioned approaches have been criticized for limited efficacy and added weight/volume from passive components; and for the cost, complexity, or availability of the more effective methods, such as the electrostatically shielded motor. A comprehensive summary of these solutions and their drawbacks is included in [6].

Active common-mode filters that generate a compensating voltage to cancel the high-frequency CMV have also been proposed. The active filters need auxiliary power supplies, and either require the operation of semiconductor devices in the active region (linear amplification) [7], [8] or at a very high switching frequency [9]. Therefore, the thermal management and/or control could pose a challenge. Furthermore, a passive common-mode transformer is still necessary to add the filter's output to the main drive output. The common-mode transformer design is difficult due to the intentional low-frequency output CMV typical in VSIs; and some implementations have used an additional series capacitor [10] to limit the transformer size. Although effective, active filters are generally more complex than the passive solutions and have not enjoyed widespread adoption.

Due to the various drawbacks discussed so far, considerable research has focused on reducing or eliminating the HF CMV at the source (the power electronic converter). Such solutions may retain the more common ac–dc–ac drive paradigm with a rectifier and a VSI tied at a dc-link, or may utilize alternative drive topologies using matrix converters and open-end winding (OE Wdg.) drives.

Reduction in the CMV generated by a two-level VSI (2L-VSI) has been reported in the literature [11], [12] but the reduction is achieved at the cost of higher current ripple/harmonic distortion, and an additional filter choke may be required. Multilevel inverters generate less severe HF CMV and, therefore, are a potential solution [13]. For low-voltage drives, due to cost and complexity, three-level VSIs (3L-VSI) are more justifiable over higher leveled VSIs [14]. Further reduction in the HF CMV from 3L-VSIs is possible if some of the advantages are relinquished—using a limited set of vectors increases the output voltage harmonic distortion but leads to reduced or eliminated CMV [15]–[17].

VSI-based OE Wdg. drives, two-level and multilevel, can eliminate the CMV entirely [18]–[22]. Although examples of VSI-based OE Wdg. drives without a rigid dc-link exist [23], in general all VSI-based drives, whether conventional or OE Wdg., require a large dc-link capacitor to maintain the dc-bus voltage

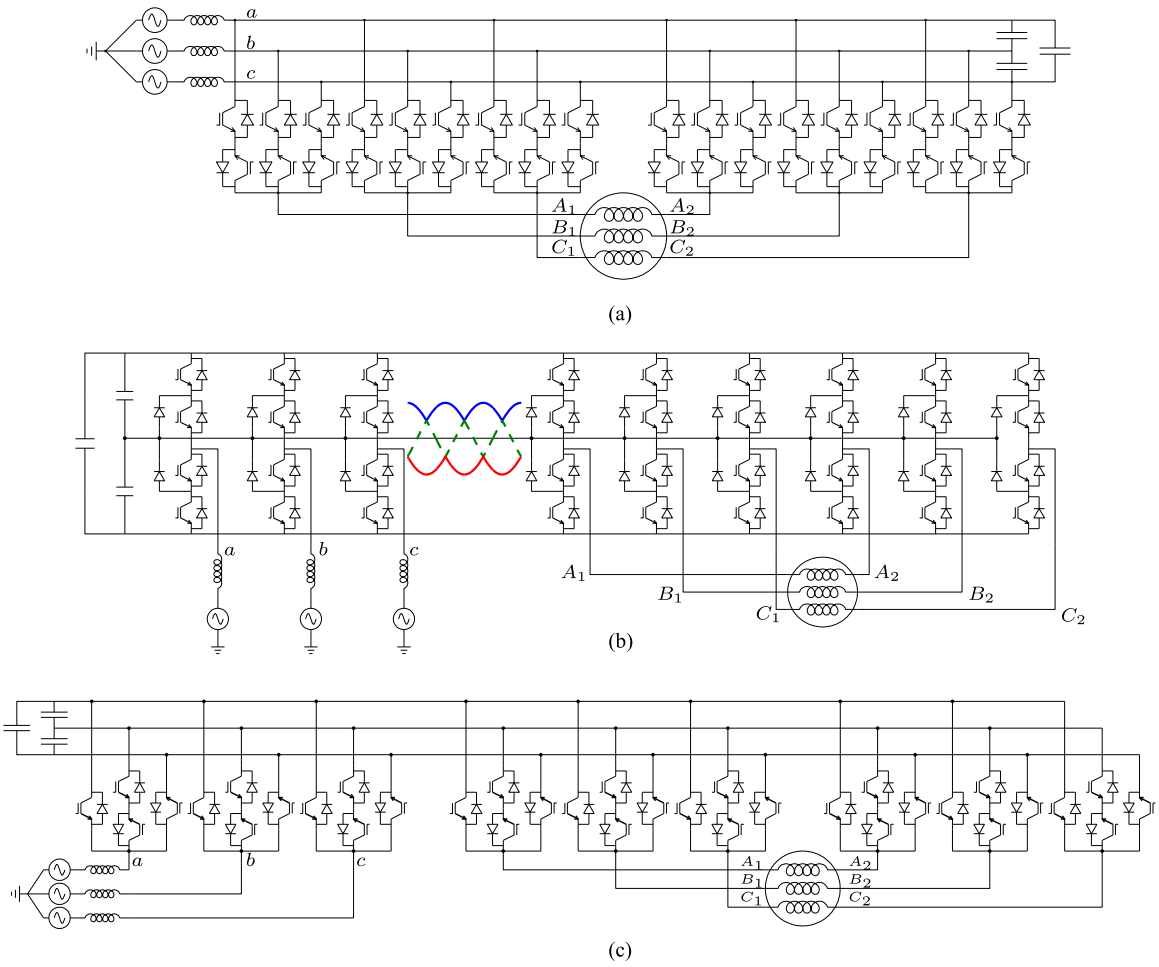

Fig. 1. Circuit diagrams of the matrix converter based OE Wdg. drives. The converters' inputs are marked a, b, c and the OE Wdg. machine terminals are marked A_1, B_1, C_1 and A_2, B_2, C_2. (a) Direct matrix converter based OE Wdg. drive [33], [34]. (b) I-type IMC based OE Wdg. drive [39]. (c) T-type IMC based OE Wdg. drive [39].

in event of torque transients at the motor load. The design of the dc-link capacitance is a complex topic. Most drives use some combination of film and electrolytic capacitors. Film capacitors provide the HF PWM current and a fast response whereas electrolytic capacitors, with significantly higher equivalent series resistance (ESR) and equivalent series inductance (ESL), provide energy storage to absorb the line and load transients—electrolytic capacitors have higher capacitance than film capacitors at a lower volume and cost [24]; however, they also suffer from inevitable degradation and affect the reliability adversely [25], [26].

Matrix converters can generate a variable frequency ac output without an intermediate dc link. But conventional matrix converters (CMC) still generate a switching CMV. Similar to VSIs, research has been reported on reducing the CMV generated by matrix converters [27]–[32]. Among matrix converters, OE Wdg. drives modulated with rotating vectors are especially interesting since they succeed in eliminating the CMV entirely, thus addressing two major problems with conventional drives — namely HF CMV induced bearing failure, and electrolytic capacitor degradation and its effect on drive reliability.

Experimental validation of a direct matrix converter (DMC) based OE Wdg. drive modulated with rotating vectors was reported in 2010 by Gupta *et al.* [33], [34]. This drive consisted of two identical DMCs serving the two sets of terminals of an OE Wdg. induction machine as shown in Fig. 1(a). Two indirect matrix converter (IMC) based realizations of the same concept were proposed in [35] and further developed in [36]–[39]. These are shown in Fig. 1(b) and (c).

For the purpose of this paper, the modulation with rotating vectors and thus common-mode elimination is considered implicit to the operation of matrix converter based OE Wdg. drives. These drives, depicted in Fig. 1, utilize all three input phases at all times to generate the output voltage. Alternatively, the voltage for the OE Wdg. machine could also be generated from the pulsating DC-link of a conventional IMC [40], [41] — such drives are effectively modulated with stationary vectors and can reduce, but not completely eliminate, the output CMV. This paper focuses exclusively on the drives modulated with rotating vectors.

This paper is organized as follows: Section II presents the theory of operation and CMV elimination in OE Wdg. drives, and is concluded with a qualitative comparison. In Section III,

the practical realization of these drives is presented and experimental results are discussed. A framework for quantitative comparison is set forth in Section III-C, and the best topology among the three MC OE Wdg. drives is selected for comparison with the state-of-the-art. Only limited results from the operation of the selected topology, the T-type IMC OE Wdg. drive of Fig. 1(c), have been presented in the past that do not include operation with a motor load. Therefore, Section III-E presents detailed results from the operation of this drive.

Having validated the choice of the T-type IMC OE Wdg. drive as the best topology in Section III, Section IV compares this drive against the state-of-the-art. The parameters include CMV related phenomena, output voltage quality, passive element requirement and input current quality, and power losses. This section also investigates whether and why these results are expected. Effects of nonidealities are also examined.

While the ideal T-type IMC OE Wdg. drive is a full-Silicon solution with zero CMV and high reliability, the capabilities of this drive are affected by the limitations of practical semiconductor switches. Whether this drive is a viable alternative to the state-of-the-art back-to-back converters is discussed in Section V.

Exclusive of the previously reported research on this topic, the additional contributions of this paper are as follows:

1) new experimental results from the T-type IMC-based OE Wdg. drive are reported, including operation with a motor load;
2) new investigation of CMV-related phenomena in the MC OE Wdg. drives is reported that, at times, contradicts earlier results;
3) comparison with the state-of-the-art drives using detailed experimental results is reported;
4) in addition to the new results, the causes of expected and unexpected common-mode performance and output voltage quality are examined.

Overall, this paper serves to consolidate the existing research on matrix converter OE Wdg. drives and to bolster the evidence in favor of these drives by providing new experimental results. Simultaneously, however, this paper takes a more critical look at these drives and analyzes whether the theoretical benefits are in fact achievable.

II. Matrix Converter Based OE Wdg Drives: Theory of Operation

The matrix converter introduced in [42] was a generalized ac/ac converter. Applied to three-phase adjustable speed drives, it could generate an output voltage at an arbitrary frequency. The output voltage amplitude was also variable but restricted to half the amplitude of the input voltage. Subsequent research led to improvement in the voltage transfer ratio [43] and the development of an indirect CSR-VSI treatment of matrix converters [44]. The direct and the indirect topologies with an improved voltage transfer ratio of up to $\sqrt{3}/2$ are called CMCs hereafter [45].

CMCs' voltage transfer ratio is still restricted to $\sqrt{3}/2$ at unity input power factor with further degradation at nonunity input power factors. Furthermore, low- and high-frequency common-mode components are present in the output voltage, same as state-of-the-art drive topologies.

The matrix converter based OE Wdg. drives have the following advantages over the CMCs and VSI-based state-of-the-art drives:

1) the output CMV can be eliminated;
2) the voltage transfer ratio can be as high as 1.5;
3) the input power factor can be controlled at no penalty to the voltage transfer ratio (over CMCs);
4) the large dc-link capacitor is eliminated (over VSIs).

The following sections describe the modulation of the MC OE Wdg. drives of Fig. 1 and compare the three drives to each other qualitatively.

A. Modulation of the Direct MC OE Wdg. Drive

Let v_a, v_b, v_c be the three-phase input voltages. The space-vector $\vec{v}_{abc}$ can be defined as

$$\vec{v}_{abc} = v_a + v_b\, e^{j2\pi/3} + v_c\, e^{-j2\pi/3}. \tag{1}$$

The vector $\vec{v}_{abc}$ rotates counterclockwise (CCW) in the complex plane at the angular frequency of the input voltage ($:= \omega_i$). The vectors $\vec{v}_{bca}, \vec{v}_{cab}$, defined similar to (1), also rotate CCW; whereas the vectors $\vec{v}_{acb}, \vec{v}_{cba}, \vec{v}_{bac}$ rotate clockwise (CW) in the complex plane. Thus, a set of three-phase voltages has three CCW and three CW rotating vectors corresponding to it. Other stationary and zero vectors are possible that are not used in the modulation described here.

Let the terminals of the OE Wdg. machine be called A_1, B_1, C_1 and A_2, B_2, C_2. The DMC OE Wdg. drive of Fig. 1(a) generates the output voltage by a convex combination of the input voltage space-vectors

$$\begin{aligned}\vec{v}_{A_1B_1C_1} &= \alpha \times (\lambda_{abc,1}\vec{v}_{abc} + \lambda_{bca,1}\vec{v}_{bca} + \lambda_{cab,1}\vec{v}_{cab}) \\ &+ (1-\alpha) \times (\lambda_{acb,1}\vec{v}_{acb} + \lambda_{cba,1}\vec{v}_{cba} + \lambda_{bac,1}\vec{v}_{bac}).\end{aligned} \tag{2}$$

In (2), $\alpha \in [0, 1]$ is an input power factor control parameter. The output vector $\vec{v}_{A_2B_2C_2}$ is generated similarly with the coefficients being $\lambda_{abc,2}, \ldots$; the effective load voltage vector is $\vec{v}_{A_1B_1C_1} - \vec{v}_{A_2B_2C_2}$.

Applying a rotating vector at one end of the OE Wdg. machine connects each motor phase at that end to a unique input phase, e.g., applying $\vec{v}_{abc}$ at the first set of motor terminals ($A_1B_1C_1$) means switching the suitable devices such that $v_{A_1} = v_a, v_{B_1} = v_b, v_{C_1} = v_c$. Since a balanced input ensures that $\sum v_{\text{in}\,abc} = 0$, using only the rotating vectors, therefore, ensures that $\sum v_{\text{out}\,A_1B_1C_1} = 0$ and $\sum v_{\text{out}\,A_2B_2C_2} = 0$. Thus, the CMV at both sets of motor terminals is eliminated. The modulation of this drive is described in detail in [33] and [34].

B. Modulation of the Indirect MC OE Wdg. Drives

Instead of using the grid inputs directly, the indirect MC OE Wdg. drives of Fig. 1(b) and (c) employ a front-end converter to arrange the grid voltages by their instantaneous value. This rectification leads to another set of three-phase voltages

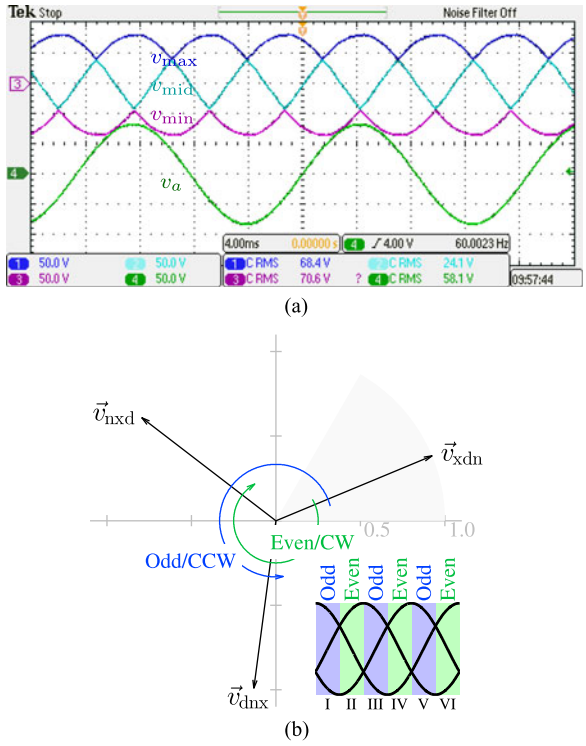

Fig. 2. Front-end operation. (a) Time-domain waveforms of the front-end converter: "max," "mid," and "min" voltages generated by the front-end converter and the phase "a" voltage at no-load. The input voltage is ~ 100 V. (b) Vector diagram of the front-end outputs.

$v_{\max}, v_{\mathrm{mid}}, v_{\min}$. Formally

$$\begin{aligned} v_{\max} &= \max\{v_a, v_b, v_c\} \\ v_{\min} &= \min\{v_a, v_b, v_c\} \\ v_{\mathrm{mid}} &= \{v_a, v_b, v_c\} \setminus \{v_{\max}, v_{\min}\}. \end{aligned} \tag{3}$$

The $v_{\max}, v_{\mathrm{mid}}, v_{\min}$ voltages form a pulsating link between the front-end and the load-end converters. These voltages are also balanced as long as the input voltages are, i.e., $v_{\max} + v_{\mathrm{mid}} + v_{\min} = \sum v_{\mathrm{in}abc} = 0$. Similar to the input voltage space vectors discussed in the previous section, link voltage space vectors can be defined. Fig. 2(a) shows the pulsating link voltages defined in (3) and Fig. 2(b) shows the space vectors $\vec{v}_{\mathrm{xdn}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{nxd}}$. The letters "x," "d," and "n" in the subscript stand for max, mid, and min, respectively.

The three vectors in Fig. 2(b) rotate CCW in the odd sectors of the input voltage (sectors I, III, and V based on $\angle\vec{v}_{abc}$) and rotate CW in the even sectors II, IV, and VI. Corresponding to these, another set of vectors $\vec{v}_{\mathrm{xnd}}, \vec{v}_{\mathrm{ndx}}, \vec{v}_{\mathrm{dxn}}$ rotates CW in the odd sectors and CCW in the even sectors. Thus, similar to the direct MC-based OE Wdg. drive, one set of CCW rotating vectors and one set of CW rotating vectors is available to the load-end converters for output voltage synthesis and input power factor control.

The output voltage synthesis and input power factor control in the direct *and* the indirect drives of Fig. 1 can be generalized as

$$\begin{aligned} \vec{v}^* = {} & \alpha(\mathbf{\Lambda}_{1,\mathrm{pos}} - \mathbf{\Lambda}_{2,\mathrm{pos}})\mathbf{V}_{\mathrm{pos}} \\ & + (1-\alpha)(\mathbf{\Lambda}_{1,\mathrm{neg}} - \mathbf{\Lambda}_{2,\mathrm{neg}})\mathbf{V}_{\mathrm{neg}}. \end{aligned} \tag{4}$$

In (4), $\vec{v}^*$ is the target output voltage vector. $\mathbf{V}_{\mathrm{pos}}$ is a 3×1 column vector of the CCW rotating space vectors and $\mathbf{V}_{\mathrm{neg}}$ is a 3×1 column vector of the CW rotating space vectors. $\mathbf{\Lambda}$ denote 1×3 row vectors of the coefficients of the convex combination (duty ratios) corresponding to the CCW and CW rotating vectors, and to the two sets of motor terminals. α is the power factor control parameter.

The modulation of the indirect MC OE Wdg. drives is described in detail in [39] and is being omitted here for brevity. It must be stressed that as long as the input voltages, and therefore, the link voltages sum to zero, the CMV at both ends of the machine is eliminated.

C. Qualitative Comparison of the Direct and the Indirect Topologies

Although many advantages of the direct and the indirect MC OE Wdg. drives are common, the indirect structure offers some unique advantages that are absent in the direct topology.

1) *Clamp circuit elimination*: The direct MC OE Wdg. drive is constructed using four-quadrant switches. In case of simple dead-time commutation or current direction sensing failure in intelligent commutation (four-step commutation), it is necessary to use clamping diodes at both sets of the motor terminals. These diodes need to be rated for the full voltage and current (repetitive pulse rating). Additionally, a clamp capacitor is required; and either a lossy resistor or an active energy recovery mechanism is further required to limit the clamp capacitor voltage.
   In contrast, the indirect implementations exploit a VSI structure where the inductive elements (input inductors and the motor) are always clamped eliminating the need for additional diodes and passive elements.
2) *Low-voltage ride-through (LVRT) integration*: A number of LVRT strategies for matrix converters necessitate additional auxiliary circuitry, e.g. [46]. However, in the special case of the indirect MC OE Wdg. drives of Fig. 1(b) and (c) and their single-ended version [38], the front-end converter offers a way to isolate the converter and the motor from the grid in case of a grid-side undervoltage. The load-end converters can still recover the energy from the motor to maintain the charge at the filter capacitors, and use the filter capacitors as a voltage source to maintain/control the motor flux. Thus, the LVRT strategy of [46] can be utilized in the indirect MC OE Wdg. drives without additional switches.
3) *Lower switching stress*: The switches of the direct MC OE Wdg. drive of Fig. 1(a) would switch the maximum line-to-line input voltage at some point or the other. However, by selecting the vector sequence appropriately, it is possible to eliminate the full line-to-line (or $v_{\max} \leftrightarrow v_{\min}$) switching transitions in the indirect implementations. An example of one such vector sequence is shown in Fig. 3.

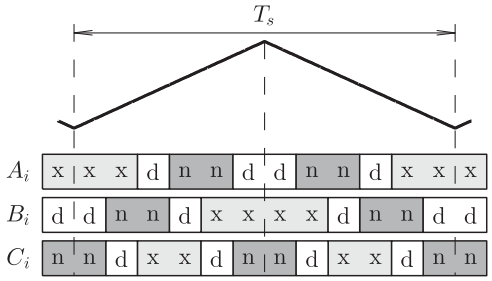

Fig. 3. Intelligent vector sequence that minimizes the voltage switched: $\vec{v}_{\mathrm{xdn}}, \vec{v}_{\mathrm{xnd}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{ndx}}, \vec{v}_{\mathrm{nxd}}, \vec{v}_{\mathrm{dxn}}, \vec{v}_{\mathrm{dxn}}, \vec{v}_{\mathrm{nxd}}, \vec{v}_{\mathrm{ndx}}, \vec{v}_{\mathrm{dnx}}, \vec{v}_{\mathrm{xnd}}, \ldots$.

4) *Naturally intelligent commutation*: Intelligent commutation in the direct MC drive would require load current direction sensing and associated clamp circuit for failsafe operation (already discussed). On the other hand, utilizing the vector sequence of Fig. 3 also ensures that the current commutates from the outgoing switch position to the incoming switch positions directly, *without* the need to know the current direction. Once again, this is a consequence of the VSI structure of the indirect drives and a distinct advantage over the direct drive in switching simplicity and robustness.

Thus, the indirect implementations of the rotating vector modulated MC OE Wdg. drives seem superior to the direct implementation. Whether the direct topology, in spite of slight complexity, could offer lower losses is investigated in the following section using power loss simulations.

III. Matrix Converter Based OE Wdg. Drives: Implementation

Section II described the principle of operation of the matrix converter based OE Wdg. drives of Fig. 1. Differences among the direct and the indirect implementations that follow from the topology were also discussed. To complete the drives, it is necessary to add an input filter and investigate semiconductor requirements and losses. In this section, an input filter applicable to all three topologies is designed. Switch design is considered for an example system and semiconductor losses are investigated. Vector sequences that minimize the switching losses are also presented. At the end of this section, the best topology among the drives of Fig. 1 is identified based on the results of this section and the qualitative comparison in Section II-C.

A. Input Filter

A second-order LC filter is common in matrix converter applications. Addition of the necessary damping reduces the HF attenuation to -20 dB/decade. Therefore, a third-order filter was designed with an additional inductor in series with the damping resistor [47]. The filter equivalent circuit at the switching frequency is shown in Fig. 4. In [47], the filter is optimized to minimize the peak output impedance for dc/dc applications. For ac/ac applications, the filter resonant frequency is generally chosen to be:

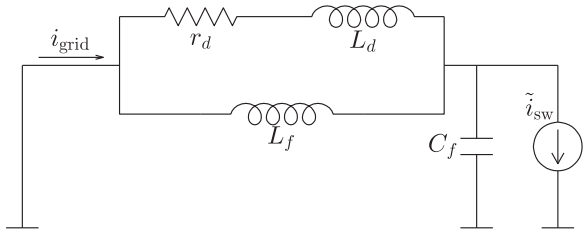

Fig. 4. Filter topology and the equivalent circuit at the switching frequency.

1) sufficiently larger than the input fundamental frequency to limit the size and the reactive power consumption of the filter components;
2) and sufficiently lower than the switching frequency to avoid the amplification of the sidebands of the switching frequency.

Bearing the above in mind, it is proposed that the third-order filter's resonant frequency should be located approximately geometrically between the input fundamental frequency and the switching frequency; and the filter components should be optimized to minimize the peak amplification (infinity norm) of the switching current to input current transfer function ($G(s) := i_{\mathrm{grid}}(s)/\tilde{i}_{\mathrm{sw}}(s)$ in Fig. 4).

Let the filter inductor be L_f, the filter capacitor be C_f, the damping resistor be r_d, and the damping branch inductor be L_d. Furthermore, let us define

$$n = \frac{L_d}{L_f} \tag{5}$$

$$\omega_0 = \frac{1}{\sqrt{L_f C_f}}. \tag{6}$$

The switching current to grid current transfer function can be calculated as

$$G(s) = \frac{sL_f(n+1) + r_d}{s^3 n L_f^2 C_f + s^2 L_f C_f r_d + sL_f(n+1) + r_d}. \tag{7}$$

Due to an additional pole compared to a damped second-order filter, the HF attenuation of the filter of Fig. 4 is -40 dB/decade. Following the steps outlined in [47], it is found that for a given n, there exists an ω^* such that $|G(j\omega^*)|$ is independent of r_d for all $r_d \geq 0$

$$\omega^* = \sqrt{\frac{2(n+1)}{2n+1}}\,\omega_0$$

$$|G(j\omega^*)| = 2n+1. \tag{8}$$

That the magnitude of $G(j\omega)$ equals $2n+1$ at some frequency or the other further implies that its maximum absolute value is such that $\|G(j\omega)\|_\infty \geq 2n+1$. Therefore, by finding an appropriate r_d such that $|G(j\omega)|$ is maximized at ω^*, the amplification over all frequencies can be limited to $2n+1$ completing the optimization. For brevity, the steps are omitted; the final value of r_d that minimizes the maximum absolute value of

TABLE I
DESIGN VALUES ARE EXPRESSED IN P.U.

	Third order		Second order	
	Design (p.u.)	Prototype	Design (p.u.)	Prototype
L_f	0.0261	0.95 mH	0.0300	1.5 mH
C_f	0.1631	10.75 μF (Δ)	0.3333	18 μF (Δ)
L_d	0.0083	330 μH	–	–
r_d	0.5547	8 Ω	0.6000	10 Ω
P_{loss}	0.0013		0.0017	

The prototypes are for a 208 V, 3 kVA system.

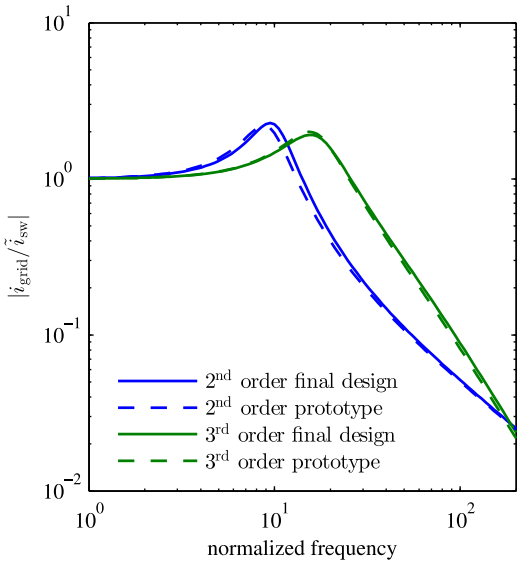

Fig. 5. Filter response against conventional LC: The proposed filter exhibits superior attenuation of higher frequencies.

$G(j\omega)$ is found to be

$$r_d = \omega_0 L_f \left(\frac{n + \frac{1}{2}}{n(n+1)^2} \right)^{-\frac{1}{2}}. \tag{9}$$

A comparison of this third-order filter with a conventional second-order LC filter is shown in Table I and Fig. 5. The second-order filter uses a damping resistor in parallel to the filter inductor. Both designs assume a switching frequency approximately a hundred times the input fundamental frequency or higher. The per-unit values are independent of the system base whereas the values in the physical units are for a 208 V, 3 kVA converter prototype.

The ratio $n(= L_d/L_f)$ provides a way of balancing the damping resistor power loss and the damping branch inductor current rating while choosing parts necessary for the design. A comparison of the damping branch inductor versus the main filter inductor for the case of Table I is shown in Fig. 6

B. Loss-Optimal Vector Sequences

An example vector sequence for the IMC OE Wdg. drives is shown in Fig. 3. It was discussed earlier that this vector sequence eliminates the $v_{\max} \leftrightarrow v_{\min}$ switching transitions. This

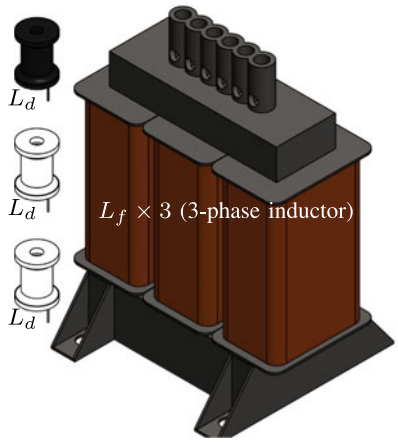

Fig. 6. Scaled three-dimensional drawing comparing the sizes of L_f and L_d for the third-order filter in Table I. L_f is 0.95 mH, three-phase rated for 10.7 A; L_d is 330 μH rated for 1.72 A. From the figure above and Table I, it is easy to see that the extra damping branch inductor L_d would occupy little volume relative to the main inductor L_f.

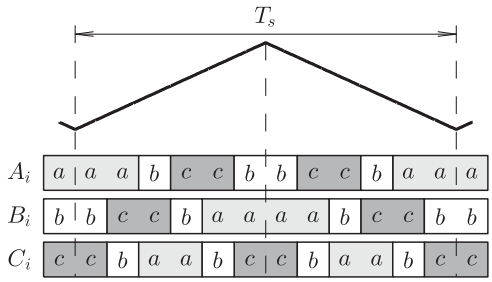

Fig. 7. Loss-optimal vector sequence for the direct matrix converters of the DMC OE Wdg. drive.

vector sequence is also special in that it minimizes the total number of switching transitions within a PWM cycle. A similar vector sequence can be found for the DMC OE Wdg. drive by substituting $v_{\max}, v_{\text{mid}}, v_{\min}$ by v_a, v_b, v_c, respectively. This vector sequence is illustrated in Fig. 7. Of course, as mentioned earlier in the case of the DMC OE Wdg. drive, the $\max\{v_a, v_b, v_c\} \leftrightarrow \min\{v_a, v_b, v_c\}$ transitions are not readily eliminated.

C. Framework for Quantitative Comparison

It is clear from the circuit diagram of the DMC OE Wdg. drive in Fig. 1(a) that all insulated gate bipolar transistors (IGBTs) need to be able to block the maximum line-to-line voltage ($:= \widehat{v}_{ll}$). For practical switches, this requirement translates to using 1200V IGBTs in a 480V system (a 480V system is considered because it is a common industrial voltage level).

In the I-type IMC OE Wdg. drive of Fig. 1(b), the IGBTs need to block $\max(v_{\max} - v_{\text{mid}})$. While lower than the maximum line-to-line voltage of 678 V (nominal), $\max(v_{\max} - v_{\text{mid}})$ equals 588 V (nominal) and still necessitates using 1200 V IGBTs.

The T-type 3L inverter modules are typically constructed with nonidentical switches (half-bridge versus bidirectional arm) but in this case of IMC OE Wdg. drive, the half-bridge switches

TABLE II
BUCK CONVERTER OPERATING POINTS USED FOR VALIDATION

CM200DU24NFH (1200 V, 200 A)				CM200DU12NFH (600 V, 200 A)			
	V_{in} (V)	Duty cycle	I_{out} (A)		V_{in} (V)	Duty cycle	I_{out} (A)
OP1	600	50%	100	OP1	300	50%	100
OP2	600	75%	150	OP2	300	75%	150
OP3	300	75%	150	OP3	150	75%	150
OP4	900	25%	50	OP4	450	25%	50

Switching frequency is fixed at 10 kHz, the heat sink is connected to the 25°C ambient with a small thermal impedance.

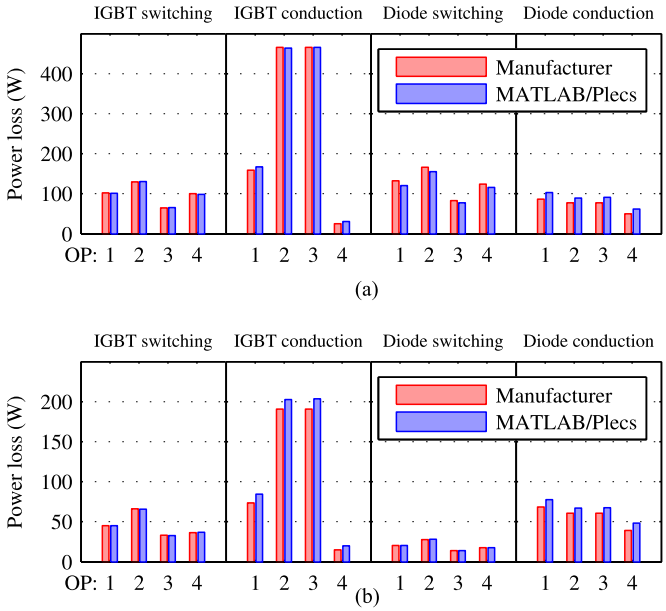

Fig. 8. Model validation for semiconductor losses against manufacturer's software. OP1,...,4 for the two devices are defined in Table II. (a) 1200 V, 200 A IGBT CM200DU24NFH. (b) 600 V, 200 A IGBT CM200DU12NFH.

would need to block $\widehat{v}_{ll}$ whereas the bidirectional switches would block only a slightly lower voltage of $\max(v_{\max} - v_{\mathrm{mid}})$. Therefore, all switches would need to be 1200 V IGBTs.

1200 V, 200 A IGBTs are commonly available and are used to analyze all three topologies of Fig. 1 for a 480 V, 80 kVA system. For this study, the data are taken from Powerex CM200DU-24NFH IGBT module. The data were imported into Plecs and the losses for a step-down converter were compared against the manufacturer's software to qualify the Plecs model. Same steps were followed for the 600 V, 200 A module CM200DU-12NFH for use in Section IV. The models were validated at the operating points of Table II and the results are shown in Fig. 8.

D. Losses in the Matrix Converter OE Wdg. Drives

In this section, the semiconductor losses in the three MC OE Wdg. drives of Fig. 1 are compared using the MATLAB/Plecs simulation framework laid out in Section III-C. The loss-optimal vector sequences of Figs. 3 and 7 are used for modulation. The filter components from Table I are used for a 480 V, 80 kVA system.

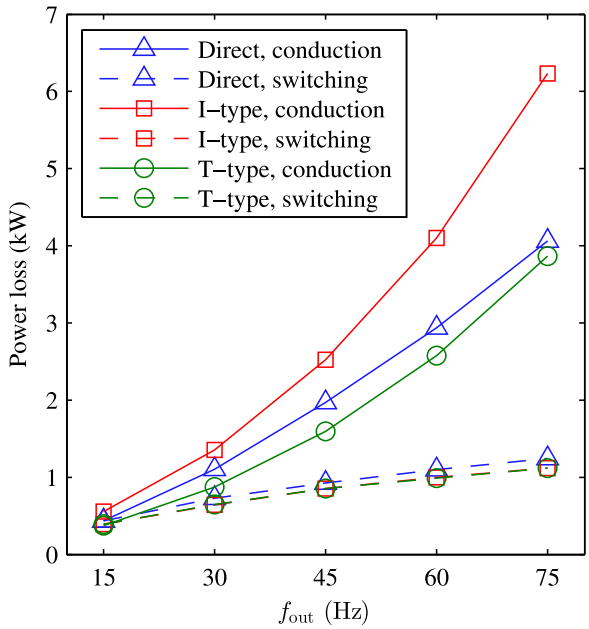

Fig. 9. Total losses for the matrix converter based drives at $\alpha = 0.5$.

To expedite the simulations, an RL load is used. The impedance of the load is fixed at $Z_{\mathrm{base}}\angle\phi$ where $\phi : \cos\phi = 0.8, \phi > 0$. The input voltage is fixed at 480 V (1 p.u.) and the output frequency is varied from 15 to 75 Hz in steps of 15 Hz. The output voltage is set according to a V/f control law

$$V_{\mathrm{out}} = \frac{f_{\mathrm{out}}}{f_{\mathrm{base}}} V_{\mathrm{base}} \tag{10}$$

where $f_{\mathrm{base}} = 60$ Hz.

The simulated semiconductor losses at a switching frequency of 6 kHz are shown in Fig. 9. The plots are shown for $\alpha = 0.50$, i.e., the input power factor is set to unity. Following conclusions can be drawn from Fig. 9.

1) The losses at low to moderate switching frequencies would be dominated by conduction losses.
2) The conduction losses are highest for the I-type indirect MC OE Wdg. drive due to the large number of conducting devices.
3) The conduction losses for the DMC OE Wdg. drive and the T-type IMC OE Wdg. drive are similar, with the T-type drive exhibiting slightly lower losses.
4) The switching losses in both of the indirect drives are similar since identical currents and voltages are switched.
5) The switching losses are slightly higher in the direct implementation, due to higher switching voltage at times (the vector sequence for the indirect implementations eliminates the $\max\{v_a, v_b, v_c\} \leftrightarrow \min\{v_a, v_b, v_c\}$ transitions).

The 3L leg used in the I-type drive needs to be constructed with the same voltage rated devices as the direct and the T-type drive. Due to a larger number of conducting devices, the I-type drive incurs high conduction losses and is ruled out as a competing topology. The losses in the T-type drive are slightly lower than the direct MC drive. Combined with the qualitative

advantages discussed earlier in Section II-C, the T-type drive emerges as the best topology among the matrix converter based OE Wdg. drives of Fig. 1. The experimental results from the operation of this drive and a comparison with the state-of-the-art VSIs will be presented in the following sections.

It is, once again, stressed that this discussion is limited to the three matrix converter based OE Wdg. drives that are modulated with *rotating* vectors (see Fig. 1) and can completely eliminate the output CMV.

E. Experimental Results From the T-type IMC OE Wdg. Drive

Having established the T-type IMC-based drive as the topology of choice among the drives in Fig. 1, this section presents the experimental results validating the operation of this drive. The key advantages of the MC OE Wdg. approach discussed in this paper are as follows:

1) output CMV elimination;
2) elimination of the large dc link capacitor;
3) a high voltage transfer ratio of 1.50;
4) input power factor control.

Results pertinent to the output CMV and discussion on the capacitance, and passive components in general, are included in the following section. The input/output waveforms with power factor control are shown in Fig. 10, whereas the evidence of the high voltage transfer ratio is shown in Fig. 11. For Figs. 10 and 11, following operating conditions are used:

1) 208 V, 60 Hz input (120 V line-to-neutral);
2) third-order input filter (prototype values in Table I);
3) RL load with $10\,\Omega, 45$ mH in each phase;
4) 10kHz switching frequency;
5) input power factor set to unity unless specified otherwise;
6) output voltage at different output frequencies set according to $V/f = 200/60$ (V/Hz).

The construction of the T-type drive using IGBT module APTGLQ40HR120CT3G by Microsemi Corporation is illustrated in Fig. 12. The filter capacitors (not shown) are mounted onto the busbar printed circuit board (PCB). The main inductor and the damping network are not shown in this illustration.

Figs. 10 and 11 prove that the T-type drive can generate a sinusoidal output while controlling the input power factor and the output voltage transfer ratio. The results with a motor load including the common-mode performance are included in the following section.

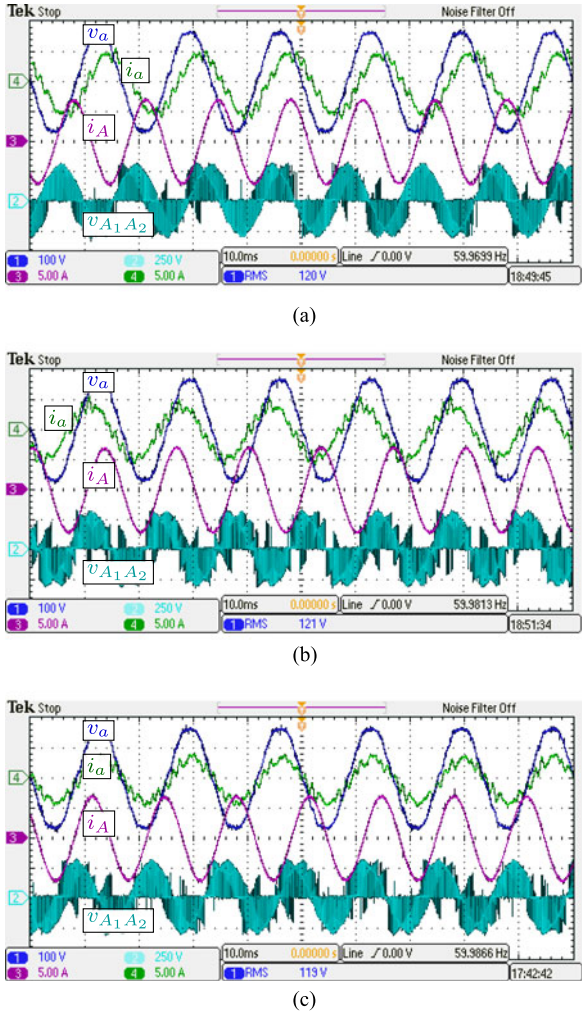

Fig. 10. Source voltage (v_a), source current (i_a), load voltage ($v_{A_1A_2}$), and load current (i_A) in the T-type IMC drive of Fig. 1(c) with the input power factor controlled to (a) lagging input power factor ($\alpha = 0.88$), (b) leading input power factor ($\alpha = 0.45$), and (c) unity input power factor ($\alpha = 0.67$). For all cases the voltage transfer ratio is commanded to 1.25. In practice, a slightly lower voltage transfer ratio is achieved (see Fig. 11) due to voltage drops along the current path. Having $\alpha \approx 0.50$ results in leading input power factor, e.g. (b); to achieve unity power factor (upf), compensation for the reactive power injected by the filter capacitors is necessary in (c) by increasing α beyond 0.50.

IV. Comparison With the State of the Art

In this section, the T-type matrix converter based OE Wdg. drive is compared to the state-of-the-art solution. For the purpose of this paper, back-to-back VSIs are considered state-of-the-art drive topologies. Both, 2L inverter (2L-VSI) and 3L inverter (3L-VSI), based solutions are included for the comparison and are accordingly called 2L-BBC and 3L-BBC (2/3L back-to-back converter).

The T-type IMC OE Wdg. drive prototype illustrated in Fig. 12 can also be utilized as a 2L-VSI and a 3L-VSI. The same experimental setup is, therefore, used to compare the output waveform quality and common-mode performance in the three topologies (T-type IMC OE Wdg. drive, 2L-VSI, 3L-VSI). A 200 V, 3 hp ac induction motor (ACIM) is used at the drive output. This motor is coupled to a matched dc generator; a resistor at the dc generator terminals serves to load the drive. While using the setup as VSIs, the "max–mid–min" bus is fed from regulated dc voltage sources with additional capacitance across the bus and the unused switches are gated off.

The prototype is designed with off-the-shelf modules to prove the principle of operation and is not optimized for device utilization/power losses. Furthermore, for the VSI operating modes, the regulated dc supplies force a rigid voltage. For these reasons, the comparison of the necessary reactive elements and the losses is conducted using simulation. A 460 V, 75 hp ACIM and a 480 V, 60 Hz source is assumed. The hypothetical T-type IMC OE Wdg. drive and the 2L-BBC use the 1200 V IGBTs and

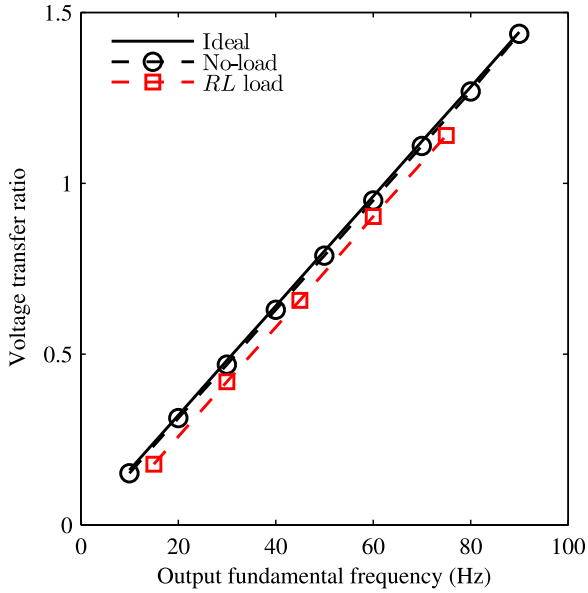

Fig. 11. Commanded (ideal) and measured voltage transfer ratio in the T-type IMC OE Wdg. drive of Fig. 1(c) at no-load and with an RL load.

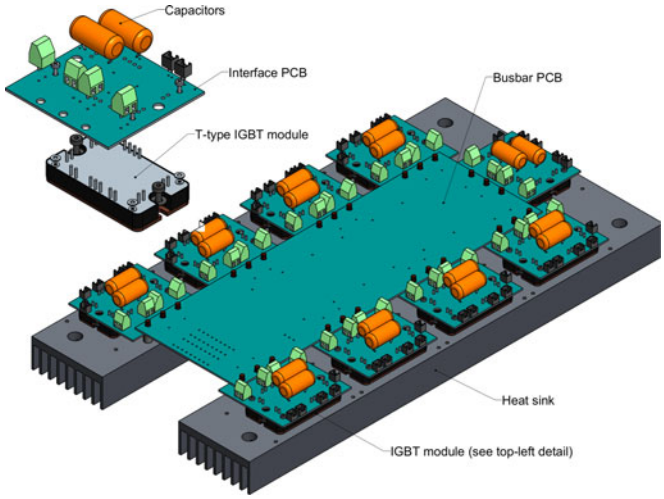

Fig. 12. Construction of the T-type IMC-based OE Wdg. drive.

the hypothetical 3L-BBC uses the 600 V IGBTs, both of which have been modeled in Fig. 8. The comparison of the reactive elements and the power losses is conducted using the operating points of Fig. 13.

A. Common-Mode Performance

In this section, the common-mode performance of the T-type IMC OE Wdg. drive is compared to that of the state-of-the-art solutions namely 2L-VSI and 3L-VSI. Results for other drives of Fig. 1 have been reported in the past for the DMC OE Wdg. drive [33], [34], [48] and the I-type IMC OE Wdg. drive [39], [49] and are not repeated here.

1) HF Effects: In electric drives, the HF common-mode current causes a finite shaft voltage to build up. Smooth conduction-mode current may continuously flow through the

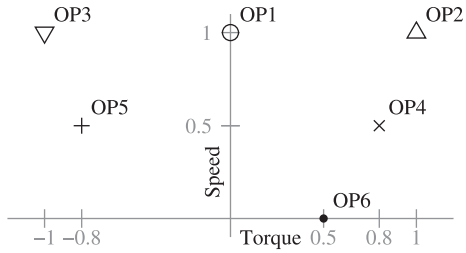

Fig. 13. Motor operating points used for comparison in the simulations. Speed and torque are expressed as a fraction of their rated values.

parasitic capacitances of the motor due to excitation from the CMV; the resulting shaft voltage might also cause the bearing lubrication to break down resulting in a relatively erratic discharge-mode current that causes bearing erosion through electrical discharge machining (EDM). The shaft voltage can be considered a reliable indicator of the bearing currents in the absence of specially modified motors that have sometimes been used to study the effects of the CMV [1], [2], [5].

For the results presented here, the shaft voltage and the common-mode current are recorded using a differential probe and a Pearson coil, respectively. All three topologies, the T-type IMC OE Wdg. drive, the 2L-VSI and the 3L-VSI, are used to run the ACIM-DC generator-resistor load described earlier. Fig. 14 shows the typical waveforms for the three topologies at different time-scales. Following can be observed.

1) The amplitude of the shaft voltage is the highest in the 2L-VSI [see Fig. 14(a) and (b)] and the lowest in the T-type IMC OE Wdg. drive [see Fig. 14(e) and (f)].
2) The amplitude of the shaft voltage in the 3L-VSI [see Fig. 14(c) and (d)] is close to, but lower than that in the 2L-VSI—The peak shaft voltage consistently exceeds 10 V (absolute value) in the 2L-VSI [see Fig. 14(a) and (b)].
3) Significant common-mode current flows in the T-type IMC OE Wdg. drive, whereas the common-mode current is the smallest in the 3L-VSI (occurrence as well as the amplitude of the waveform). At this stage, the reader is urged to consider only the shaft voltage as a measure of the HF common-mode performance—The common-mode current is discussed in the following section.
4) In case of the VSIs [see Fig. 14(a)–(d)], the relatively slow variations in the CMV ($\sim$100 ns) are correlated with the common-mode current; whereas more abrupt variations ($\sim$10 ns) occur independent of the common-mode current. The slower variations in the shaft voltage are a result of the capacitive voltage division of the CMV and are, therefore, accompanied by a common-mode current flowing through the parasitic capacitances. The faster variations, on the other hand, are not necessarily accompanied by a common-mode current and result in shaft voltage collapse. These indicate a capacitive discharge (EDM) phenomenon local to the shaft-bearing-frame region.

Although the experimental setup does not allow a measurement of the bearing currents, it can be inferred, based on the pioneering work on the topic of inverter-induced bearing cur-

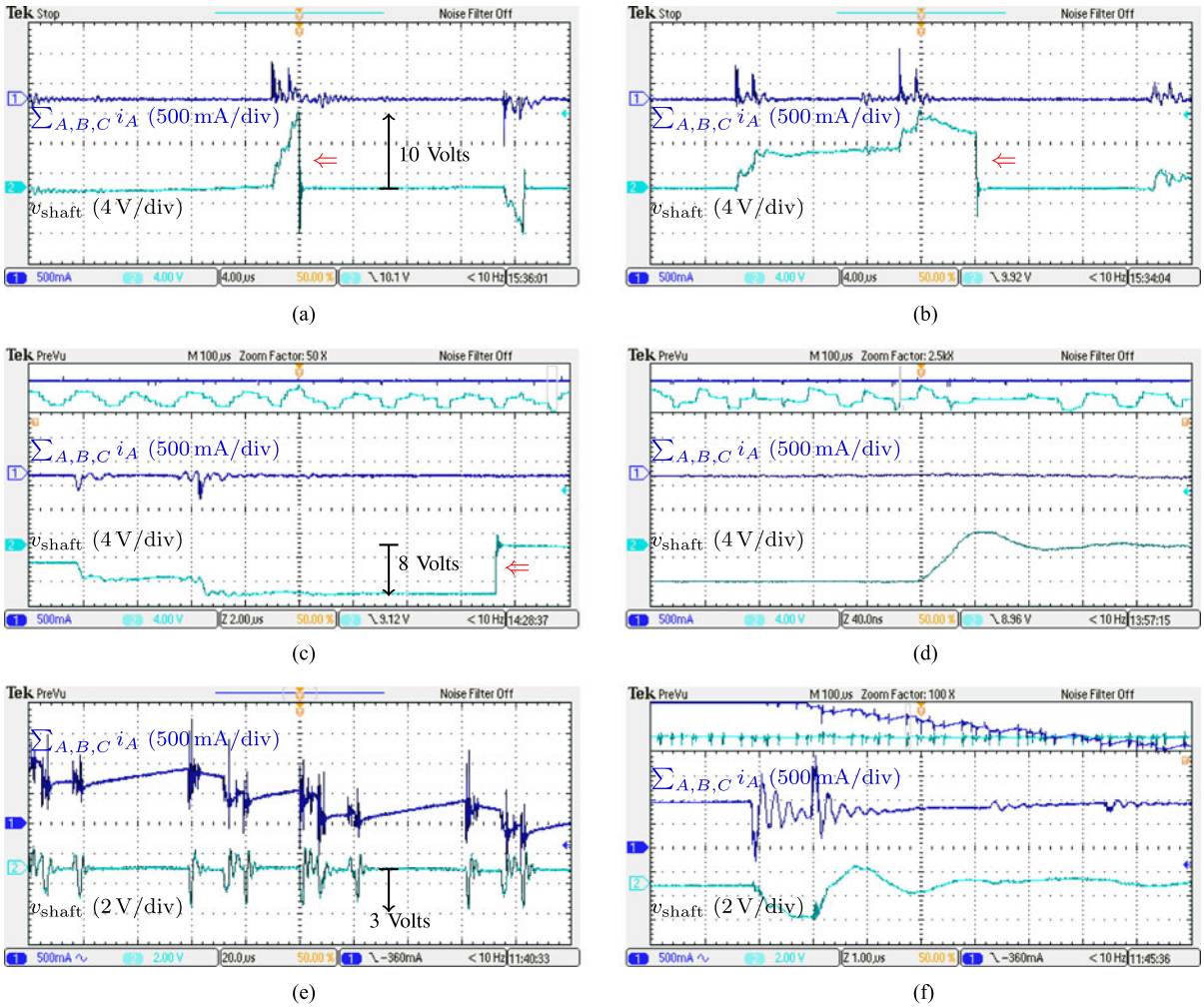

Fig. 14. Total common-mode current ($i_A + i_B + i_C$) and the shaft voltage (v_{shaft}) in (a) 2L-VSI: The shaft voltage collapse is likely uncorrelated with the common-mode current, especially at $t = 0$, (b) 2L-VSI: The shaft voltage collapse is uncorrelated with the common-mode current; (c) 3L-VSI: The shaft voltage collapse is uncorrelated with the common-mode current, (d) 3L-VSI: Detail of a typical shaft voltage collapse event; and (e) T-type IMC OE Wdg. drive: Transitions in the shaft voltage are correlated with the HF common-mode current, (f) T-type IMC OE Wdg. drive: Detail of the shaft voltage transitions. For the VSIs, the input dc bus voltage is 300 V; for the T-type drive the input ac voltage is 208 V. For all plots the ACIM is running under 200/60 V/Hz at $\sim$75% of the rated speed and the dc generator is loaded by 10 Ω (nominal). In all cases, the total common-mode current is recorded at 500 mA/div. For the VSIs, (a)-(d), the shaft voltage is recorded at 4 V/div, whereas for the T-type drive, the shaft voltage is recorded at 2 V/div.

rents [1], [2], that a sudden collapse of the shaft voltage would result in a large current through the bearings that is especially damaging. It is noteworthy that collapsing shaft voltage such as shown in Fig. 14(a)–(d) was observed consistently in the 2L-VSI and the 3L-VSI along with the large amplitude of the shaft voltage, whereas the sudden collapse was not *readily* observed in the T-type IMC OE Wdg. drive. Based on the amplitude and the dV/dt of the shaft voltage, it can, therefore, be concluded that the T-type drive has significantly lower bearing current than the state-of-the-art VSI drives.

While the typical waveforms such as shown in Fig. 14 clearly demonstrate a *reduction* in the shaft voltage (and therefore bearing currents), the theoretical *elimination* is not observed in the T-type drive. The finite shaft voltage can be attributed to the CMV generated during the finite dead-time necessary for commutation. The previous research has also reported a finite shaft voltage for direct (DMC OE Wdg.) [34] and indirect (I-type IMC OE Wdg.) [49] drives of Fig. 1; but the existence or absence of discharge mode currents has not been discussed. Indeed, based on the typical results (e.g., Fig. 14), it might be incorrectly concluded that the shaft voltage in the matrix converter based OE Wdg. drives is relatively smooth and the bearing currents are exclusively conduction mode.

Due to the high voltage transfer ratio, it is possible in MC OE Wdg. drives to generate the rated output voltage at a lower input voltage. Previously reported experimental results have used a lower input voltage to demonstrate the voltage transfer ratio along with the common-mode performance. In a key departure, the experiments reported here were conducted at the full input voltage (208 V three-phase corresponding to a 200 V ACIM). This higher voltage subjects the motor insulation (and parasitic capacitances) to the rated voltage. The experiments were repeated at different loading conditions at the full input voltage and occasionally a sudden transition in the shaft voltage was observed that appeared uncorrelated with the common-mode current. Two such transitions are shown in Fig. 15: in (a), the

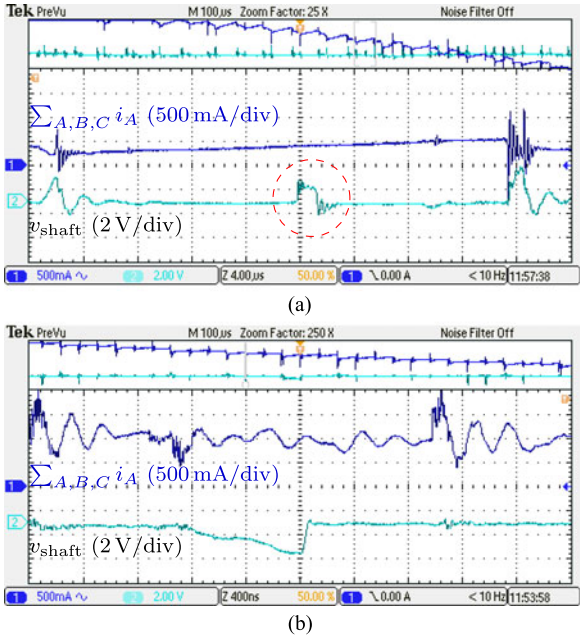

Fig. 15. Total common-mode current ($i_A + i_B + i_C$) and the shaft voltage (v_{shaft}) in the T-type IMC OE Wdg. drive: Possible evidence of discharge mode (EDM) bearing currents. (a) Between smooth transitions in the shaft voltage correlated with the common-mode current, occasional abrupt transitions are observed. (b) Abrupt collapse of the shaft voltage that is an order of magnitude faster than the buildup.

magnification time scale is chosen to contrast the sudden and uncorrelated transition against the two typical transitions also seen in the same plot; in (b), the difference in the time scale of the smoother and the sharper transitions is clearly appreciated. The waveform of Fig. 15(a) is somewhat inconclusive in that in addition to the collapse, the buildup is also uncorrelated with the common-mode current. However, the waveform of Fig. 15(b) clearly shows a gentle buildup in presence of common-mode currents followed by a much faster collapse.

It is emphasized that the waveforms of Fig. 15 are far from typical—Thorough examination of multiple waveform captures over different operating conditions was required to observe these, whereas the shaft voltage collapse in the VSIs [see Fig. 14(a)–(d)] could be observed with excellent repeatability. Nevertheless, even if Fig. 15(a) is deemed inconclusive, Fig. 15(b) is sufficient to conclude that in spite of a generally superior HF common-mode/bearing current performance of the T-type drive observed in Fig. 14, the existence of discharge mode bearing currents in the T-type drive, and by extension the other matrix converter based OE Wdg. drives of Fig. 1, cannot be ruled out.

2) Low-Frequency Effects: In the waveforms of Fig. 14(e) and (f), the HF common-mode current is seen superimposed on a slowly varying current of relatively larger amplitude. This low-frequency common-mode current is observed only in the T-type IMC OE Wdg. drive and it is absent in the 2L-VSI and the 3L-VSI [see Fig. 14(a)–(d)]. However, this current is hardly unique to the T-type drive under consideration—The existence of this circulating common-mode current, which flows from one load-end converter to the other, has been reported in the I-type

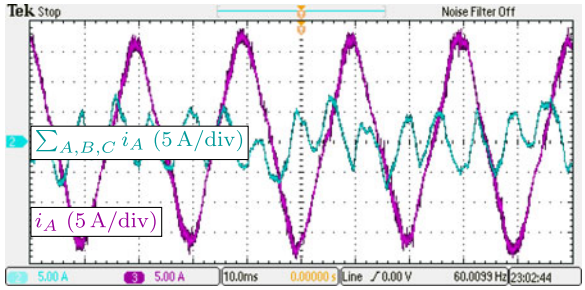

Fig. 16. Circulating current in the T-type IMC OE Wdg. drive at near-rated operating point.

IMC OE Wdg. drive of Fig. 1(b) [49] and also in the DMC OE Wdg. drive of Fig. 1(a) and other VSI-based OE Wdg. drives [48].

It was argued in the previous section on the HF effects that a finite dead-time required for commutation leads to a finite CMV that would ideally be absent in the OE Wdg. drives modulated with rotating vectors. This CMV need not be identical at both sets of motor terminals. Furthermore, finite device voltage drops inevitable in practical switches also lead to different CMVs at the two sets of motor terminals [48]. Therefore, a net *differential* voltage exists in the common-mode circuit of the converter-motor system between the two sets of motor terminals: This voltage contains components that vary at the order of the motor fundamental frequency as well as faster components that occur due to the finite dead-time. Consequently, low- and high-frequency circulating currents result that are impeded only by the motor's leakage inductance, which is small in comparison to the magnetizing inductance.

The HF common-mode current shown in Fig. 14(e) and (f) comprises of the current that flows through the motor capacitances as well as between the two load-end converters. Therefore, even though the amplitude of the shaft voltage is lower than the VSIs (see Fig. 14), the HF common-mode current is either similar or larger than the VSIs. Even if the HF circulating current is considered benign since it is approximately two orders of magnitude lower than the rated motor current, the low-frequency circulating current cannot be ignored: Fig. 16 shows the total circulating current ($i_A + i_B + i_C$) along with the current of one motor phase. While the HF current is imperceptible at the chosen Amperes/division, it is seen that the low-frequency circulating current is at least 10% of the phase current.

Mitigation methods against circulating currents in OE Wdg. drives are discussed in [48]. The discussed methods require additional components and precise current direction detection that diminish the advantages of the indirect MC OE Wdg. approach. At the same time, if left unchecked, the circulating currents could be quite large as seen in Fig. 16 leading to additional converter and motor losses.

The HF performance of the T-type IMC based OE Wdg. drive is decidedly superior to the state-of-the-art VSIs as seen in the shaft voltage plots of Fig. 14. However, the theoretical expectation of complete CMV elimination is hardly met: The same shaft voltage results that show a better performance than the VSIs also provide evidence of conduction-mode and discharge-mode

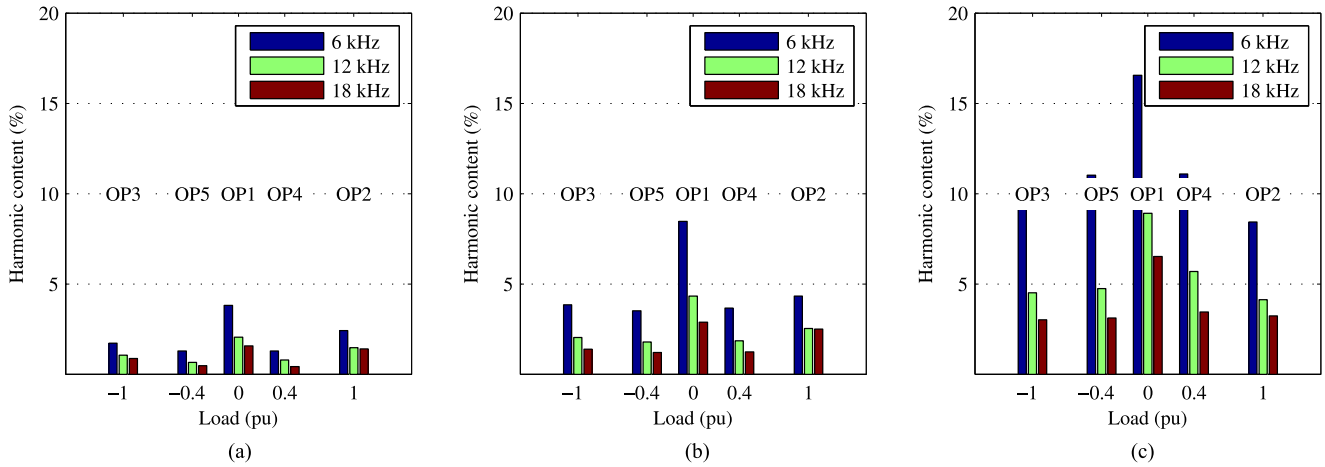

Fig. 17. Comparison of the output current harmonic distortion [49]. The output current distortion has not been calculated for standstill (OP6 in Fig. 13). (a) 3L-VSI. (b) 2L-VSI. (c) T-type IMC OE Wdg. drive.

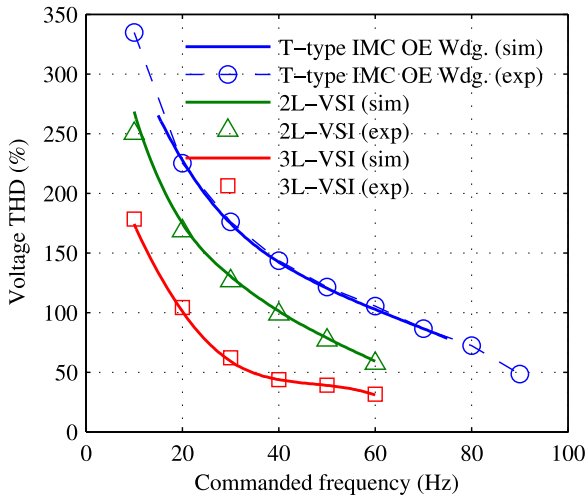

Fig. 18. Simulated and experimental output voltage THD for different drive topologies (output V/f ratio fixed at 200/60 V/Hz).

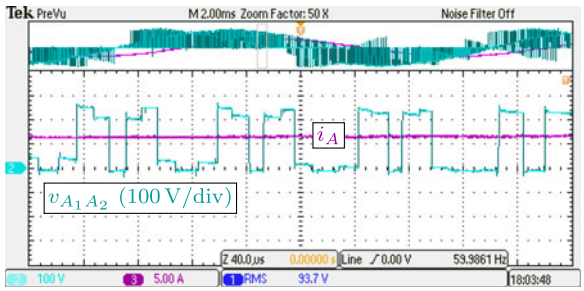

Fig. 19. Output voltage waveform of the T-type IMC OE Wdg. drive. Since a positive voltage is being synthesized, only the four positive or zero levels are used from the seven available levels. In a 2L-VSI, the same voltage would be synthesized using the three levels $\{0, V_{\rm DC}/3, 2V_{\rm DC}/3\}$.

bearing currents—The bearing currents are only mitigated, but not eliminated, by the proposed approach. Moreover, large low-frequency circulating currents occur that increase the losses. In summary, due to the necessary dead-time and the finite device voltage drops, the common-mode performance of the practical T-type IMC OE Wdg. drive gets degraded over its ideal counterpart, and the overall benefit is not dramatic but moderate.

B. Output Voltage Quality

The simulated output current total harmonic distortion (THD) for the operating points of Fig. 13 was reported in [49] and is reproduced in Fig. 17. It is seen that the T-type IMC OE Wdg. drive has the largest THD of all three topologies considered; the THD of the 3L-VSI output current is lower than that of the 2L-VSI (expected).

The trend in the current THD among the drive topologies compared is substantiated by additional simulation and experimental results of the output voltage THD in Fig. 18:

1) experimental results agree with the simulation results for all three topologies across the full range of the output;
2) the experimental performance of different drive topologies (T-type, 2L-VSI, 3L-VSI) relative to one another agrees with simulation results of Fig. 17.

Compared to a 2L-VSI, a better output voltage quality is expected from the 3L-VSI. In general, in the context of VSIs, a higher number of input voltage levels leads to a lower output voltage THD [13]. In a 2L-VSI, the output phase-to-neutral voltage is a five-level waveform that steps between $\{0, \pm V_{\rm DC}/3, \pm 2V_{\rm DC}/3\}$. In the T-type drive, and the other MC OE Wdg. drives of Fig. 1, the phase voltage is a seven-level waveforms that steps between $\{0, \pm v_{ab}, \pm v_{bc}, \pm v_{ca}\}$ [the max–mid–min voltages belong to the set $\{v_a, v_b, v_c\}$ as described in (3)]. Fig. 19 shows the detail of the output voltage in which different levels are seen.

Based on the fact that the MC OE Wdg. output waveform is a seven-level waveform, the intuition from VSIs would lead one to expect a lower output voltage THD in the T-type IMC OE Wdg. drive. This expectation is, however, contradicted from the simulation and the experimental results in Figs. 17 and 18.

While Fig. 19 shows a higher number of levels in the output voltage, it is also seen that the available levels vary with time due to the sinusoidal input voltage waveform, unlike a VSI

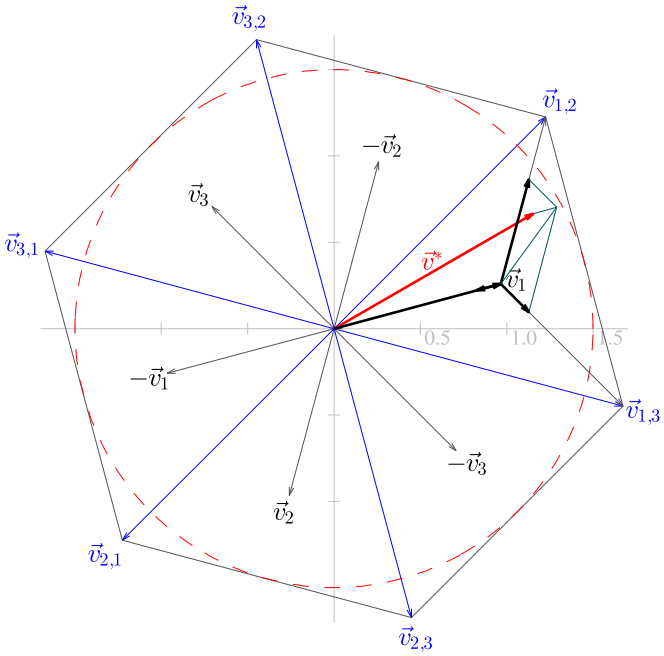

Fig. 20. Vector diagram of the MC OE Wdg. drives of Fig. 1.

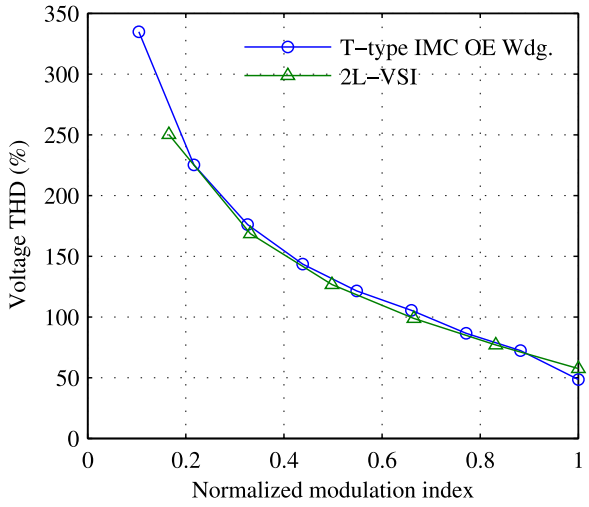

Fig. 21. At the same normalized voltage transfer ratio/normalized modulation index, the 2L-VSI and the T-type drive result in similar output voltage THD.

where the voltage levels are fixed. Indeed, the levels available to synthesize a positive phase voltage go down from four in the initial part of the plot to effectively two in the later part of the plot. Therefore, the mean squared error between the output voltage and its target value (i.e., the fundamental component) would vary with the output phase angle as well as the input phase angle. This interaction between two sinusoids was found to be exceedingly tedious to analyze; instead, the apparent discrepancy between the number of levels and THD is resolved in the space-vector domain in the following section.

1) Modulation of the T-Type IMC OE Wdg. Drive: The detailed modulation of the T-type (and the I-type) drive described in [39] is reviewed here briefly. Fig. 20 shows the space vectors available to synthesize a target vector $\vec{v}^*$. $\vec{v}_1, \vec{v}_2, \vec{v}_3$ could either be the CCW rotating vectors or the CW rotating vectors available at one end of the motor. Corresponding to these, $-\vec{v}_1, -\vec{v}_2, -\vec{v}_3$ are available at the other end. Effectively, the resultant vectors $\vec{v}_{12}, \ldots$ are available to synthesize the target output voltage space vector. These resultant vectors are longer than the input voltage space vector, which allows these drives to achieve a voltage transfer ratio of up to 1.50.

In Fig. 20, the target vector $\vec{v}^*$ lies in the sector formed by the vectors $\vec{v}_{12}$ and $\vec{v}_{13}$. As explained in [39] for the indirect MC OE Wdg. drives and before that in [34] for the direct MC OE Wdg. drive, the target vector is synthesized by applying a constant vector at one end ($\vec{v}_1$ in Fig. 20) and generating the remainder at the other end as illustrated. Mathematically

$$\vec{v}^* = \vec{v}_1 - (\sigma_1 \vec{v}_1 + \sigma_2 \vec{v}_2 + \sigma_3 \vec{v}_3) \tag{11}$$

where $\sigma_1, \sigma_2, \sigma_3$ is a convex combination. The above can be rewritten as

$$\vec{v}^* = \sigma_1 \vec{0} + \sigma_2 \vec{v}_{12} + \sigma_3 \vec{v}_{13}. \tag{12}$$

Equation (12) has the same form as the space vector equation of a 2L-VSI where the output voltage is synthesized from a zero vector and two vectors that are 60° apart. In Fig. 20, the vectors $\vec{v}_{12}$ and $\vec{v}_{13}$ are also 60° apart. Thus, similar output voltage THD could be expected for the same normalized voltage transfer ratio in the MC OE Wdg. drives and the 2L-VSI (i.e., for $|\vec{v}^*|/|\vec{v}_{12}| = |\vec{v}^*_{2\text{LVSI}}|/V_{\text{DC}}$ where $\vec{v}^*_{2\text{LVSI}}$ is the target output voltage vector of the 2L-VSI and V_{DC} is the dc bus voltage).

Indeed, the correspondence of the MC OE Wdg. drive to the 2L-VSI is confirmed when the results of Fig. 18 are replotted against the normalized voltage transfer ratio/normalized modulation index (see Fig. 21). To generate the same output voltage vector ($\vec{v}^* = \vec{v}^*_{2\text{LVSI}}$), the MC OE Wdg. drives operate at a lower voltage transfer ratio explaining the poorer THD in Figs. 17 and 18. As a consequence, MC OE Wdg. drives will result in a higher output THD than 2L-VSIs in systems with nominal output voltage equal to or slightly under the nominal input voltage (e.g., 460 V motor on a 480 V system).

Based on Fig. 21, MC OE Wdg. drives could be expected to achieve a similar THD to 2L-VSIs in an application where the nominal output voltage exceeds the nominal input voltage (e.g., 600 V motor on a 480 V system). Even in such an application where the voltage transfer ratio could be adjusted for a performance similar to 2L-VSI, the 3L-VSI will outperform the MC OE Wdg. drives and the 2L-VSI when it comes to output THD.

C. Input Current Quality and Passives

The passive element requirements and the input current quality in the matrix converter OE Wdg. drives were compared to the state-of-the-art VSIs in [49]. The comparison reported in [49] is summarized here with some additional insight.

1) Input Inductance: The passive element requirements of the MC OE Wdg. drives are taken from Table I (per-unit values) based on the filter design proposed in [39]/Section III-A. With the input filter inductor kept fixed at the design value for the MC OE Wdg. drives, the input current harmonic distortion is plotted in Fig. 22 at the operating points of Fig. 13 for different

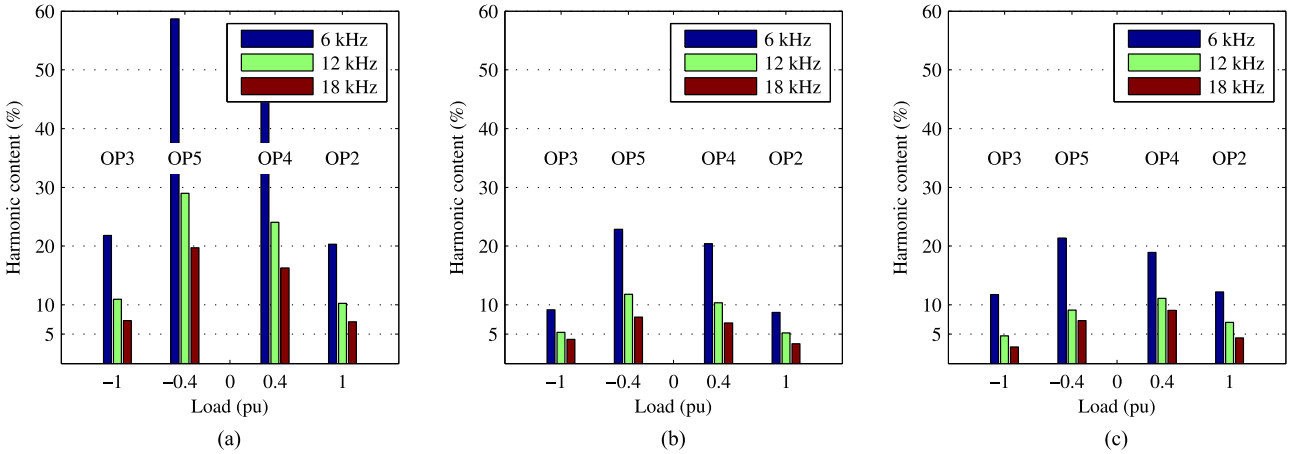

Fig. 22. Comparison of the input current harmonic distortion at the same input inductance (not calculated for no-load (OP1) and standstill (OP6) in Fig. 13). Plot reproduced from [49]. (a) 2L-BBC. (b) 3L-BBC. (c) T-type IMC OE Wdg. drive.

topologies. Exploiting the fact that the peak-to-peak input current ripple in VSI front-ends is inversely proportional to the filter inductance [50], [51], and assuming that the peak-to-peak ripple is a reliable indicator of the harmonic distortion, the current THD can be used to compare the input inductance requirements across topologies.

In Fig. 22, the input THD for the 3L-BBC and the T-type IMC OE Wdg. drive is similar for the same input inductance, whereas it is approximately twice as high for the 2L-BBC. Therefore, it could be concluded that the input inductance requirements for the 3L-BBC are similar to MC OE Wdg. drives, whereas the input inductance in a 2L-BBC would be approximately twice the input inductance in the MC OE Wdg. drive.

This analysis assumes that the VSI input filter is purely inductive—by utilizing higher order filters, e.g., [52]–[54], the input inductance(s) in the back-to-back converters (2L-BBC, 3L-BBC) could be reduced. Furthermore, Fig. 22 does not consider the extra damping branch inductance in the MC OE Wdg. drive's filter although it is much smaller in value and current rating (see Table I) and can be ignored while comparing the main inductor.

2) Capacitance: In [49], the capacitance requirements of the MC OE Wdg. drive and the back-to-back converters were compared under the following conditions.

1) The capacitance required in the MC OE Wdg. drive was obtained from the filter design in Table I.
2) The capacitance required in the back-to-back converters was such that the dc bus voltage perturbation was limited to $\pm 2.5\%$ in the event of a transition from motoring at the full power to generating at the full power.

It was concluded that the capacitance required in the back-to-back VSIs is approximately four times as much as the capacitance required in the MC OE Wdg. drives [49]. This conclusion is consistent with the advantages of matrix converters/direct ac–ac converters established in the literature [55]. However, this conclusion does not account for the exact composition of the dc-link capacitance—The filter capacitance in the matrix converters *must* be sourced entirely from film/ceramic capacitors rated for line-frequency and HF ac current, whereas the capacitance in the 2L-BBC and the 3L-BBC could be sourced in part from dc-link electrolytic capacitors that are lighter and less expensive: The chief function of the dc-link capacitance in this case is to absorb/source the instantaneous energy demand in event of a large torque step. Furthermore, it could be argued that such transitions, from fully motoring to fully generating, are rare. The limit of $\pm 2.5\%$ placed on the dc-link voltage perturbation is also somewhat arbitrary—different applications may require tighter limits or permit higher perturbation.

As a clear guideline for the dc-link capacitance design is absent, it is concluded that the capacitance required in the back-to-back VSIs would be significantly larger than MC OE Wdg. drives; but is acknowledged that the capacitance requirements need not be four times as much in the microfarad value, volume, and cost compared to the MC OE Wdg. drives.

D. Semiconductor Losses

Using the MATLAB/Plecs model described in Section III-C, the semiconductor losses for the T-type drive and 2L- and 3L-BBC were calculated. The losses were calculated at the operating points marked in Fig. 13. The devices were assumed to be mounted onto an ideal heat sink held at $25\,^{\circ}\mathrm{C}$. The losses at a switching frequency $f_{\mathrm{sw}} = 6\,\mathrm{kHz}$ are shown in Fig. 23.

Ignoring the effect of the junction temperature on the semiconductor losses, the losses across all switching frequencies can be estimated by separating the conduction and the switching losses at $6\,\mathrm{kHz}$. For the operating points of Fig. 13, the same data as Fig. 23 are also shown in Table III.

1) The total semiconductor losses are the highest in the T-type IMC OE Wdg. drive and the lowest in the 3L-BBC across all operating points.
2) The conduction losses in the 3L-BBC are slightly higher than the 2L-BBC due to more than twice the number of conducting devices (but half the blocking voltage). Still, the low switching losses in the 3L-BBC lead to overall lower losses at switching frequencies greater than $6\,\mathrm{kHz}$. This conclusion is consistent with the research on low-voltage drives based on 3L-VSIs [56].

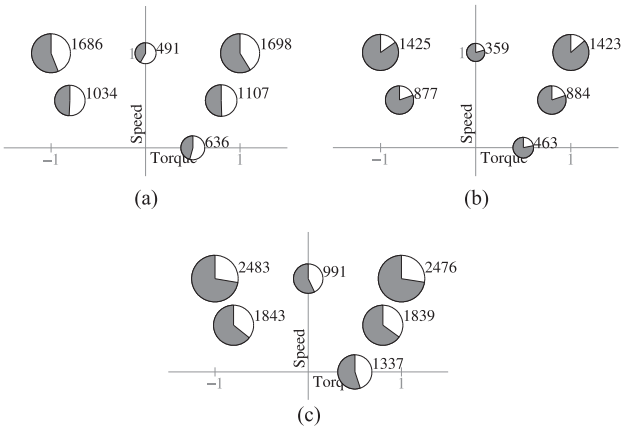

Fig. 23. Semiconductor losses at $f_{\rm sw} = 6\,{\rm kHz}$. The area in gray represents conduction losses. A circle of unit diameter represents $10\,{\rm kW}$. (a) 2L-BBC. (b) 3L-BBC. (c) T-type IMC OE Wdg. drive.

TABLE III
SEMICONDUCTOR LOSSES AT 6 kHz

	Torque	Speed	2L-BBC		3L-BBC		T-type IMC OE Wdg.	
	(p.u.)	(p.u.)	$P_{\rm cond}$	$P_{\rm sw}$	$P_{\rm cond}$	$P_{\rm sw}$	$P_{\rm cond}$	$P_{\rm sw}$
OP1	0	1	206	284	285	74	**565**	**426**
OP2	1	1	998	**699**	1230	193	**1797**	679
OP3	−1	1	947	**738**	1207	217	**1797**	686
OP4	0.8	0.5	561	546	710	174	**1200**	**640**
OP5	−0.8	0.5	510	524	707	170	**1186**	**657**
OP6	0.5	0	291	344	362	101	**736**	**601**

The losses at a given switching frequency can be approximated as $P_{\rm loss} = P_{\rm cond} + P_{\rm sw} \times f_{\rm sw}/6{\rm kHz}$. All losses in the table are in Watts. The bold values are the maximum and in their respective row, i.e., at that operating point.

3) The high conduction losses in the T-type drive are due to a larger number of conducting devices that are rated to block the entire line-to-line voltage (see Section III-C).
4) Operating points OP2 and OP3 are the full-load motoring and generating operating points. At these points the input (grid) and the output (motor) voltages and currents are nearly equal.
   a) In the 2L-BBC the front-end VSI and the load-end VSI switch a similar current (amplitude) at OP2 and OP3. At other operating points the front-end switches a current lower than the motor current.
   b) Although the switching losses in the T-type drive are lower than the 2L-BBC at OP2 and OP3, the advantage is not maintained while developing torque at lower speeds (operating points 4,...,6). This is because the front-end VSI in the 2L-BBC switches a lower current at lower speeds, whereas in the T-type drive, two converters (the load-end matrix converters) always switch the motor current irrespective of the operating point.
5) Operating point OP1 is the no-load operating point at which the motor runs at the synchronous speed with zero load torque. At this operating point, the drive only supplies the no-load losses. Therefore, the grid current and the motor current are both small. It is seen in Table III that the T-type drive still has significantly larger switching losses than the 2L-BBC. The 2L-BBC's load-end inverter switches the magnetizing current of the motor, whereas the front-end VSI switches an even smaller current. On the other hand, in the T-type drive, two converters switch the magnetizing current causing larger switching losses.
6) Even if the motor were to largely run at near-rated conditions, the slightly lower switching losses in the T-type drive (compared to the 2L-BBC) are not sufficient to offset the much larger conduction losses; and the T-type drive ends up exhibiting the largest semiconductor losses among the topologies considered.

TABLE IV
COMPARISON OF THE T-TYPE IMC OE WDG. DRIVE AGAINST THE BACK-TO-BACK TOPOLOGIES: "+" INDICATES AN ADVANTAGE, "−" A DISADVANTAGE

	2L-BBC	3L-BBC	T-type
Input inductance	−	+	+
Capacitance	−	−	+
HF common-mode	−	−	+
LF common-mode	+	+	−
Output quality	+	+	−
Semiconductor requirement	+	+	−
Semiconductor losses	+	+	−

E. Summary

In this section, the T-type drive was compared to the state-of-the-art 2L-BBC and 3L-BBC on the following criteria:
1) the common-mode performance;
2) the output voltage quality;
3) the passive element requirements;
4) the semiconductor losses.

The comparison used existing simulation results from [49] and new simulation and experimental results. In addition to the results of the comparison, explanation for these results was also provided. It was found that the T-type drive achieves the advantages claimed in Section I, i.e., a better output CMV quality and lower capacitance requirement. At the same time, the effects of the HF CMV were found to be present due to real switches with finite switching times. The lower capacitance requirement was also, to some degree, conditional upon the dc-link capacitance design in the back-to-back topologies.

On the other hand, the T-type drive was outperformed by the back-to-back topologies in the output voltage quality and the semiconductor losses. Justification for the poorer performance of the T-type drive was provided. Table IV summarizes the findings of this section. The semiconductor requirements of the 2L-BBC and 3L-BBC are indicated as similar in Table IV since the 3L-BBC utilizes just over twice as many devices of half the voltage rating as the 2L-BBC.

V. CONCLUSION

This paper presented the matrix converter based OE Wdg. drives for output CMV elimination and passive element reduction. The theory of operation of these drives was reviewed, and

modulation and commutation strategies were discussed. Based on a comparison within this class of drives, the T-type IMC OE Wdg. drive was identified as the best topology.

New experimental results validating the capabilities of the T-type drive were presented in Section III and it was shown that this topology retains all the advantages of the direct MC OE Wdg. drive [33], [34] and the I-type indirect MC OE Wdg. drive [39] that have been presented in the past.

In Section IV, the T-type drive was compared against the state-of-the-art back-to-back converters over multiple criteria. The results of the comparison were either consistent with the theory of operation, or were explained by accounting for nonideal behavior. Although the results demonstrated the expected advantages in the HF CMV and the reactive components, the overall improvement was not as dramatic as initially thought.

Referring to the summary of the comparison in Table IV, the T-type drive delivers a better (lower) HF CMV and requires lower capacitance than the VSI-based drives. The input inductance requirement is lower than the 2L-BBC when the third-order input filter design proposed in [39] is used. Since the input inductance in the 2L-BBC and the 3L-BBC can also be reduced by employing higher order input filters, the reduction in the input inductance cannot be considered a fundamental advantage.

In [49], it was concluded that the filter capacitor in the T-type drive would be up to four times lower than the dc-link capacitor in the VSI-based solutions (2L-BBC, 3L-BBC). However, it is acknowledged in this paper that the dc-link capacitance requirement may not be as large: The capacitance can be cut in half if the allowable perturbation (transient) in the dc-link voltage is doubled from $\pm 2.5\%$ to $\pm 5\%$, or a less severe torque step is used to determine the capacitance required. Furthermore, the dc-link capacitance allows for limited power-loss ride-through and a way to extend it by adding more storage capacitance. Therefore, the reduction in the capacitance offered by the T-type drive is considered as a limited advantage.

The elimination of the HF output CMV, however, is a fundamental advantage offered by the T-type drive that follows from the basic theory of operation. But due to finite dead-time intervals necessary with practical semiconductor switches, the complete elimination of CMV is not attained. Low- and high-frequency common-mode current still flows along with evidence of intermittent EDM bearing currents necessitating a mitigation measure.

Overall, the T-type drive would reduce the bearing currents even without additional mitigation, and would reduce the capacitance required. However, the T-type drive would require more semiconductor switches and associated auxiliary circuitry; and would incur more semiconductor losses and more motor losses. The semiconductor losses would be larger due to larger number of conducting devices and larger number of devices switching the motor current. The motor losses would be larger due to poorer output voltage harmonic content and low-frequency common-mode current.

Therefore, it is recommended to retain the state-of-the-art back-to-back converters for low-voltage drives employed in general applications with the following measures to enhance the power density and reliability.

1) Active filters and effective passive measures to curb bearing currents.
2) Higher order input filters to reduce the input inductance.
3) Careful dc-link capacitance design: Having sufficient film capacitance in the dc-link would ensure that the steady-state PWM current flows through the low-ESR/ESL film capacitors and the electrolytic capacitors would only source current during torque transients and ride-through greatly increasing their lifetime.

The applicability of the matrix converter based OE Wdg. drives cannot, however, be ruled out in harsh environments. Most capacitor technologies have not kept up with the advances in wide bandgap semiconductors. Switching frequencies of the order of 100 kHz would enable SiC-based matrix converter's input filter to be designed with high-temperature ceramic capacitors. A modest output common-mode filter would need to be included to eliminate the infrequent bearing currents discussed earlier. The drive and the motor could be housed together for extreme temperature applications requiring high reliability since this drive would be capable of operating at high ambient temperature and would eliminate electrolytic capacitors and bearing damage.

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