Interleaved Current-Driven Phase-Shift Full-Bridge Converter With Magnetic Integration and Voltage Doubler Rectifiers

Kaimin Shi, Donglai Zhang, *Senior Member, IEEE*, and Yu Gu, *Member, IEEE*

***Abstract*—This paper presents an interleaved current-driven phase-shift full-bridge converter for plug-in hybrid electric vehicle (PHEV) applications. In the proposed converter, soft switching of the active switches can be realized for a wide range of operating conditions by using a simple auxiliary circuit. Due to the current-driven nature of secondary rectifiers, the proposed converter is able to eliminate the voltage spikes across the output diodes and provides smooth commutations for the secondary rectifiers. Thus, diodes with lower breakdown voltage rate and lower forward voltage drop can be used to further improve the efficiency. All the passive magnetic components are integrated into the main transformer. The numbers of the output diodes are minimized because of the voltage doubler rectifier configuration. The input filtering requirements, as well as the current stresses of the switch devices, are also significantly reduced owing to the interleaving approach. Therefore, the proposed converter would be a good candidate for PHEV applications. The steady-state operation and relevant analysis results of the proposed converter are presented. Experimental results obtained from a 2-kW prototype with a peak efficiency of 97.4% validate feasibility of the proposed converter.**

***Index Terms*—DC–DC power conversion, interleaving approach, magnetic integration, phase-shift control, soft switching.**

I. Introduction

In RECENT years, a conventional phase-shift full-bridge (PSFB) converter has widely been used in several applications, such as plug-in hybrid electric vehicle (PHEV), renewable energy power conditioning systems, Telecom, etc., [1]–[4]. It employs the transformer leakage inductance and switch intrinsic capacitance to realize zero-voltage-switching (ZVS) for the active switches [5]–[8]. The main attractive features of this converter are simple circuit, high conversion efficiency, high power density, constant operation frequency, and low electromagnetic interference (EMI). For medium-power applications, MOSFETs are mostly used to implement the full-bridge inverter. Also, MOSFETs are majority carrier semiconductors; hence, the best soft-switching choice would be ZVS, where the turn-on capacitive losses can be eliminated. Therefore, in order to have a robust and reliable operation, MOSFETs should be switched with ZVS. It is well known that the energy stored in the output inductor is sufficient to help the leading-leg switches realize ZVS for a wide load range. But it is difficult to realize ZVS for the lagging-leg switches under light-load conditions because the energy stored in the small leakage inductance is always insufficient [9], [10]. The ZVS range for the lagging-leg switches can be extended by increasing the leakage inductance and/or adding a suitable external series inductance. However, having a large series inductance will result in some other problems, such as large duty cycle loss, excessive primary circulating current, and high-voltage spikes on the secondary-side rectifiers [11]–[14]. Specially, high-voltage spikes increases the voltage stress across the rectifiers. Thus, the rectifiers are usually designed to be overrated in order to withstand the voltage spikes, and this leads to higher losses because the diodes with higher forward voltage drop and poorer reverse recovery characteristics are used. In addition, the voltage spikes significantly increase the EMI noise of the converter. These aforementioned problems make the conventional PSFB converter not very practical for high-frequency, high output voltage, and high-power applications. The voltage spikes are caused by the interaction between the leakage inductance of the transformer and the secondary parasitic lumped capacitance, and therefore, some references tried to decrease the leakage inductance as much as possible in order to decrease the peak of the voltage spikes on the rectifiers. However, decreasing the leakage inductance leads to a narrower ZVS operating range of the PSFB converter. In [4], an R-C-D snubber circuit is employed to reduce the voltage spikes across the output diodes, whereas the amount of losses in the snubber resistor degrades the efficiency of the converter.

Several auxiliary circuits have been proposed in the literature to extend the ZVS range of the full-bridge converter, which can be mainly categorized as active or passive [3], [7], [15]–[23]. Active auxiliary circuits usually can provide soft switching from no-load to full-load. However, they generally require extra active switches, which make the power circuitry of the converter very complicated. As a result, the reliability of the full-bridge converter is also reduced and this limits the active auxiliary circuits to be used in practical applications. In contrast, passive

Manuscript received August 3, 2017; revised October 17, 2017; accepted November 20, 2017. Date of publication December 4, 2017; date of current version July 15, 2018. This work was supported in part by the National Nature Science Foundation of China under Grant 51777041 and in part by Shenzhen Municipal Commission of Science and Technology Innovation Project under Grant JCYJ20170413112018620. Recommended for publication by Associate Editor E. Babaei. *(Corresponding author: Donglai Zhang.)*

The authors are with the Power Electronics and Electrical Drives Research Center, Shenzhen Graduate School of Harbin Institute of Technology, Shenzhen 518055, China (e-mail: hitskm@sina.com; zhangdonglai@hit.edu.cn; 175282933@qq.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2777459

auxiliary circuits are relatively easier to implement and more reliable due to the fact that they do not require extra active components. However, they generally have higher circulating current and, therefore, more conduction losses, which may deteriorate the overall efficiency of the converter. In order to solve these problems, several passive auxiliary circuits with a modulation scheme have been proposed. In these techniques, the switching frequency is generally adjusted according to the load condition such that soft-switching conditions and minimized extra conduction losses are both guaranteed. In particular, a ZVS PSFB converter with adaptive energy storage has been proposed in [3]. It adjusts the bridge–bridge phase-shift angle to minimize auxiliary circulating currents for all line and load conditions. The main drawback of the PSFB converter used in [3] is that there are high-voltage spikes on the output diodes because of the lack of clamping feature. Therefore, it is not very preferable in high-voltage and high-power applications.

In order to solve the problems with the voltage-driven full-bridge converters, the current-driven PSFB (CD-PSFB) converters have been proposed in [24]–[26]. In these topologies, an ac inductor is connected in series with the primary side of the transformer, which acts as a current source for the output rectifiers. The ac inductor operates in the discontinuous conduction mode (DCM) to ensure complete energy transfer, and therefore, there is no duty cycle loss. A capacitive filter, rather than an inductive filter, is placed at the output of the diode bridge. Therefore, the voltage spikes across the secondary rectifiers can be completely eliminated and zero-voltage and zero-current switching (ZVZCS) operation conditions can be also satisfied. In [24], a series–parallel current-driven full-bridge converter is proposed, which can provide soft switching over a wide range of load variations without extra auxiliary circuits. It is able to integrate all magnetic components into an integrated transformer and also eliminate the voltage spikes across the output rectifiers. The main drawback of the CD-PSFB is that the current stress increases because of the DCM operation of the ac inductor, which may cause high conduction loss and deteriorate the efficiency at heavy loads.

The interleaving technique is very attractive for high-power applications, which usually require high power density and low-profile packaging characteristic [27], [28]. It is able to distribute the power losses and thermal stresses of the magnetics and the semiconductors because of a smaller power processed through the individual interleaved power stages. The input and output ripple current can also be reduced because of the ripple cancellation effect, and therefore, the size of the input and output filters can be decreased [29]–[34].

This paper proposes a novel interleaved current-driven PSFB (ICD-PSFB) converter with voltage doubler rectifier and magnetic integration. In this converter scheme, ZVS of the active switches can be realized over a wide load range by using a simple auxiliary circuit. The voltage spikes across the secondary rectifiers can be eliminated, and the output diodes undergo natural lossless commutation because of the current-driven rectifier configuration. As a result, the diodes with lower breakdown voltage rate, lower forward voltage drop, and better reverse recovery characteristic can be used to further improve the efficiency. The input ripple current in the filter capacitors is significantly reduced because of the interleaving approach. The voltage doubler rectifier is adopted for high output voltage applications, and the numbers of rectifier components are also minimized. Therefore, the proposed converter would be a good candidate to charge the traction battery (high-voltage battery) in an electric vehicle.

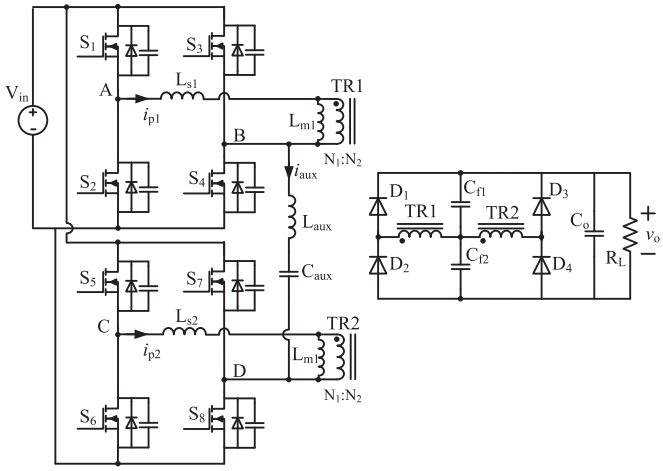


Fig. 1. Proposed converter configuration.

This paper is organized as follows. In Section II, the circuit configuration and detailed operation principle of the power stage are described. Some detailed features and characteristics are analyzed in Section III. In Section IV, a 2-kW hardware converter prototype has been designed, made, and tested to verify the validity and performance of the proposed circuit. Finally, Section V is the conclusion.

II. Circuit Description and Operation Principle

The circuit diagram of ICD-PSFB with an auxiliary *LC* network is shown in Fig. 1. Phase 1 consists of four MOSFETs S_1–S_4, transformer TR1, a series inductor L_{s1}, a secondary voltage doubler rectifier (rectifier capacitor C_{f1} and C_{f2} and diodes D_1 and D_2). Phase 2 consists of four MOSFETs S_5–S_8, transformer TR2, a series inductor L_{s2}, a secondary voltage doubler rectifier (rectifier capacitor C_{f1} and C_{f2} and diodes D_3 and D_4). The auxiliary *LC* network, which consists of an inductor $L_{\rm aux}$ and a dc blocking capacitor $C_{\rm aux}$, is connected between the two lagging-leg midpoints B and D.

It is assumed that $T_{\rm on}$ is the active interval when the diagonal switches are turned ON, and T_s is the switching cycle, then we can derive $D = 2T_{\rm on}/T_s$ as the duty cycle. There is a constant 90° phase shift between Phase 1 and Phase 2. The two phases operate similarly to each other. The operation of the proposed converter, which is the combination of the operation of the two phases, can be generally divided into two cases according to the value of duty cycle. When the load current is high, the duty cycle D is larger than 0.5 (Case 1). When the load current is small, the proposed converter enters into Case 2, namely $D < 0.5$. The key waveforms of the two cases are shown in Fig. 2. The two cases are similar to each other, and therefore, only Case 1 is analyzed in detail in this section. The equivalent operation circuits of Case 1 for different stages are shown in Fig. 3. The analysis is based on the following assumptions.

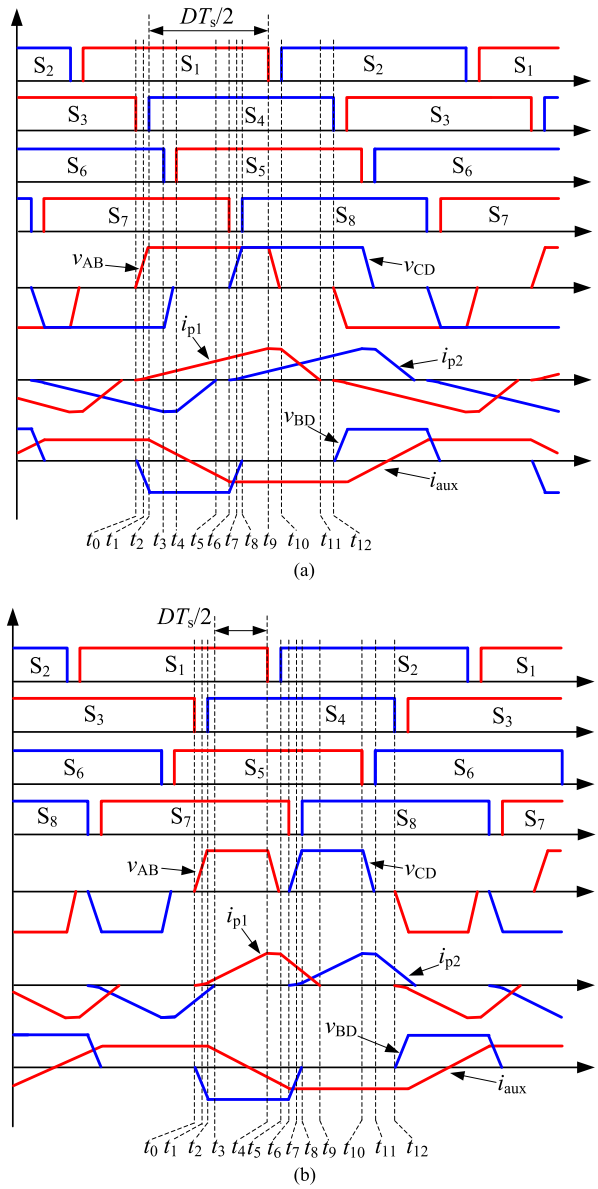


Fig. 2. Key operation waveforms: (a) Case 1: $D > 0.5$, and (b) Case 2: $D < 0.5$.

1) All components and devices are ideal.
2) The converter works in a steady state so that the average current through a capacitor and the average voltage across an inductor are all zero.
3) The output capacitors of switches S_1–S_8 are equivalent and expressed as $C_{\rm so}$. The voltage doubler capacitors C_{f1} and C_{f2} are large enough and equivalent to each other so that the output voltage are shared by them, which means $C_{f1} = C_{f2} = C_f$.
4) The interleaved two-phase CD-PSFBs are identical, which means that $L_s = L_{s1} = L_{s2}$, $L_m = L_{m1} = L_{m2}$.

Stage 1 [$t_0 \le t < t_1$]: At t_0, S_3 is turned OFF. The output capacitor of S_4 is discharging and that of S_3 is charging up by the auxiliary LC circuit current $i_{\rm aux}$. During this interval, $i_{\rm aux}$ is at its peak value $I_{\rm aux}$, and $I_{\rm aux}$ is given by

$$I_{\rm aux} = \frac{V_{\rm in} T_s}{8 L_{\rm aux}} \tag{1}$$

where $V_{\rm in}$ is the input voltage, T_s is the switching cycle, and $L_{\rm aux}$ is auxiliary network inductance. During this stage, diodes D_1 and D_2 are all reversed biased and are OFF. The rising inverter voltage $v_{\rm AB}$ is applied to the primary side of TR1, hence the primary current i_{p1} increases nonlinearly and can be expressed as

$$v_{\rm AB} = (L_{s1} + L_{m1}) \frac{di_{p1}}{dt} \tag{2}$$

where L_{m1} is the magnetizing inductance of the TR1. During this stage, i_{p1} is much smaller than $I_{\rm aux}$ due to the fact that L_{m1} is large. According to this assumption, $v_{\rm AB}$ is given by

$$v_{\rm AB}(t) = \frac{I_{\rm aux}}{2C_{\rm so}} (t - t_0). \tag{3}$$

By using (2) and (3), the expression for i_{p1} is calculated as

$$i_{p1}(t) = \frac{I_{\rm aux}}{4C_{\rm so}(L_{s1} + L_{m1})} (t - t_0)^2. \tag{4}$$

During this stage, S_6, S_7, and D_3 are ON, and therefore, the secondary voltage of the TR2 is clamped to the voltage across C_{f2}, which is $v_{\rm o}/2$. As a result, the primary current i_{p2} ramps up during this stage. This stage ends once transformer TR1 secondary voltage reaches $v_{\rm o}/2$, and the end of this interval t_1 can be obtained by solving (3) and t_1 is given by

$$t_1 = t_0 + \frac{v_o C_{\rm so}}{k I_{\rm aux}} \frac{L_{m1} + L_{s1}}{L_{m1}} \tag{5}$$

where k denotes the turns ratio $N_2 : N_1$ of transformers TR1 and TR2, and $v_{\rm o}$ is the output voltage.

Stage 2 [$t_1 \le t < t_2$]: During this stage, the output diode D_1 conducts and clamps the secondary voltage of TR1 to the voltage across the capacitor C_{f1}. The output capacitor of S_4 continues to be discharged down to zero and that of S_3 is charged up to $V_{\rm in}$ by current $I_{\rm aux}$. Thus, the primary current i_{p1} can be expressed as

$$v_{\rm AB} - \frac{v_o}{2k} = L_{s1} \frac{di_{p1}}{dt}. \tag{6}$$

By using (3)–(6), the expression for i_{p1} is calculated as

$$i_{p1}(t) = \frac{I_{\rm aux}}{4L_{s1}C_{\rm so}} (t - t_1)^2 - \frac{v_o}{2kL_{s1}} (t - t_1) + \frac{v_o^2 C_{\rm so}(L_{m1} + L_{s1})}{4k^2 L_{m1}^2 I_{\rm aux}}. \tag{7}$$

This stage ends once the output capacitor of S_4 has been completely discharged and the body diode of S_4 begins to conduct. Thus, t_2 is calculated by using (3) as follows:

$$t_2 = t_0 + \frac{2C_{\rm so} V_{\rm in}}{I_{\rm aux}}. \tag{8}$$

Stage 3 [$t_2 \le t < t_3$]: At t_2, S_4 is turned ON with ZVS. During this interval, the voltage difference between the input voltage $V_{\rm in}$ and the transformer TR1 primary voltage is applied to the series inductance L_{s1}. Thus, the primary current i_{p1} is given by

$$i_{p1}(t) = \frac{V_{\rm in} - \frac{v_o}{2k}}{L_{s1}} (t - t_2). \tag{9}$$

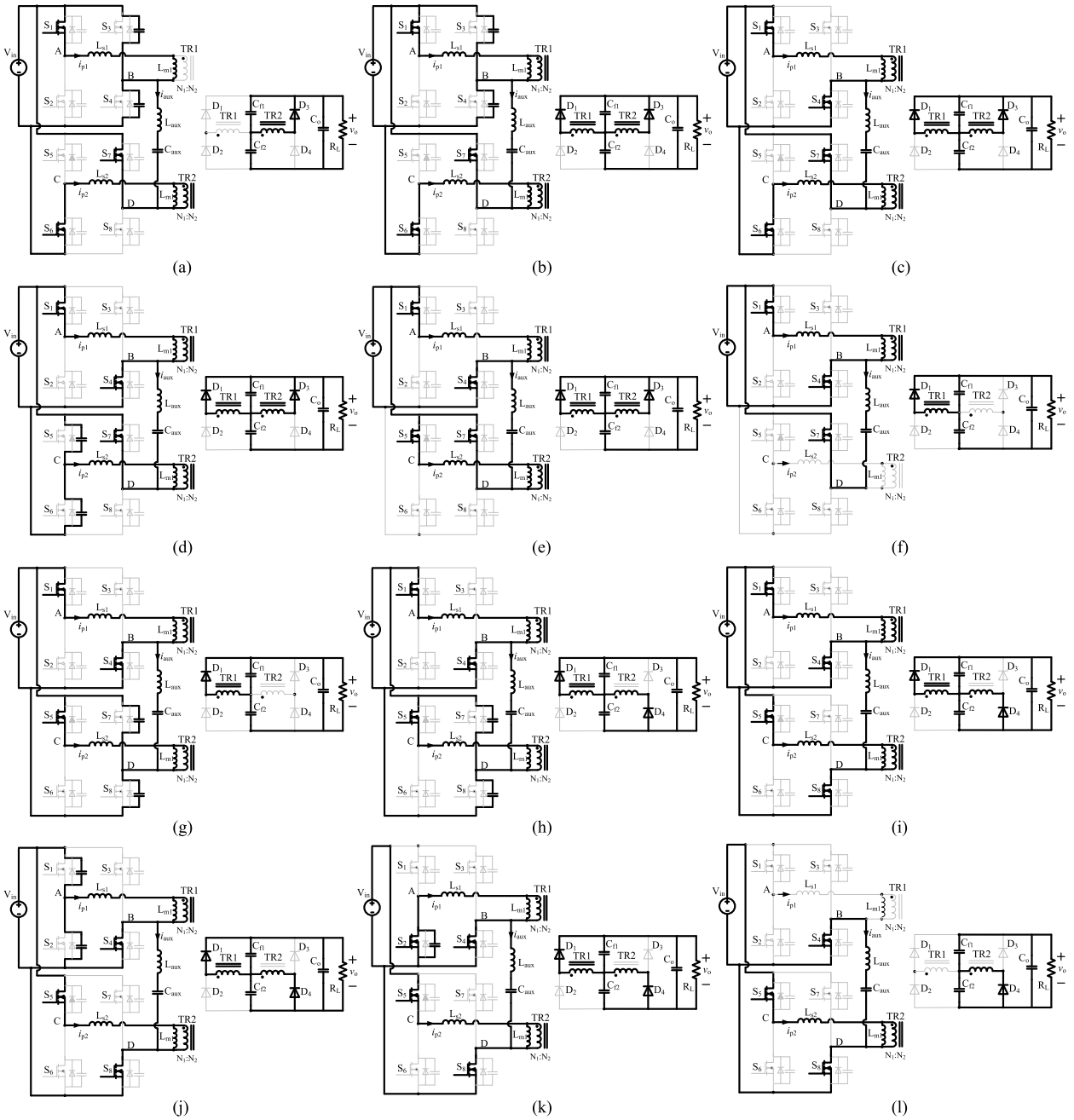


Fig. 3. Topological stages of the proposed converter in Case 2. (a) Stage 1, (b) Stage 2, (c) Stage 3, (d) Stage 4, (e) Stage 5, (f) Stage 6, (g) Stage 7, (h) Stage 8, (i) Stage 9, (j) Stage 10, (k) Stage 11, and (l) Stage 12.

By using (4), (5), (7)–(9), the peak values of the primary i_{p1} and i_{p2} are given as follows:

$$I_p = I_{p1} = I_{p2} = \frac{C_{\rm so} v_o^2 (L_{m1} + L_{s1})}{4k^2 I_{\rm aux} L_{m1}^2} + \frac{I_{\rm aux}}{4L_{s1}C_{\rm so}} \left(\frac{2C_{\rm so}V_{\rm in}}{I_{\rm aux}} - \frac{C_{\rm so} v_o}{kI_{\rm aux}} \frac{L_{m1}+L_{s1}}{L_{m1}} \right)^2 - \frac{v_o}{2kL_{s1}} \left(\frac{2C_{\rm so}V_{\rm in}}{I_{\rm aux}} - \frac{C_{\rm so} v_o}{kI_{\rm aux}} \frac{L_{m1}+L_{s1}}{L_{m1}} \right) + \frac{V_{\rm in} - \frac{v_o}{2k}}{L_{s1}} D \frac{T_s}{2}. \quad (10)$$

During this stage, the input voltage $V_{\rm in}$ is applied across the auxiliary *LC* network. As a result, the auxiliary current $i_{\rm aux}$ decreases with a constant slope. This stage ends once S_6 is turned OFF.

Stage 4 [$t_3 \le t < t_4$]: During this stage, the output capacitor of S_5 is discharging down to zero and that of S_6 is charging up to $V_{\rm in}$ by the primary current i_{p2}. The voltage across S_5 is given by

$$v_{s5}(t) = V_{\rm in} \cos\left[\omega(t-t_3)\right] - Z I_{p2} \sin\left[\omega(t-t_3)\right] + \frac{v_o}{2k} \left\{1 - \cos\left[\omega(t-t_3)\right]\right\} \quad (11)$$

where $\omega = 1/\sqrt{2C_{\rm so}L_{s1}}$ and $Z = \sqrt{L_{s1}/2C_{\rm so}}$. The primary current i_{p2} is calculated by using (11) and is given by

$$i_{p2}(t) = -I_{p2}\cos\left[\omega(t-t_3)\right] - \frac{V_{\rm in} - \frac{v_o}{2k}}{Z}\sin\left[\omega(t-t_3)\right]. \quad (12)$$

This stage ends once the output capacitor of switch S_5 is completely discharged to zero and the body diode of S_5 begins to conduct.

Stage 5 [$t_4 \le t < t_5$]: At t_4, switch S_5 has been turned ON with ZVS. During this stage, the inverter voltage $v_{\rm CD}$ is zero, and therefore, the primary current i_{p2} decreases with a constant slope, as depicted by the following equation:

$$-\frac{di_{p2}(t)}{dt} = \frac{v_o}{2kL_{s2}}. \quad (13)$$

This stage ends once the primary current i_{p2} reaches zero and the output diodes D_3 turns off naturally with zero current.

Stage 6 [$t_5 \le t < t_6$]: During this stage, switches S_5 and S_7 are ON and i_{p2} remains at zero. Meanwhile, the input energy continues to be transferred to the output through Phase 1.

Stage 7 [$t_6 \le t < t_7$]: At t_6, S_7 is turned OFF. The output capacitor of S_8 is discharging and that of S_7 is charging up by the auxiliary *LC* circuit current $i_{\rm aux}$. This stage ends once transformer TR2 secondary voltage reaches $v_{\rm o}/2$.

Stage 8 [$t_7 \le t < t_8$]: During this stage, the output diode D_4 conducts and clamps the secondary voltage of TR2 to the voltage across the capacitor C_{f2}. The output capacitor of S_8 continues to be discharged down to zero and that of S_7 is charged up to $V_{\rm in}$ by current $I_{\rm aux}$. This stage ends once the output capacitor of S_8 has been completely discharged and the body diode of S_8 begins to conduct.

Stage 9 [$t_8 \le t < t_9$]: At t_8, S_8 is turned ON with ZVS. During this stage, both of the primary currents i_{p1} and i_{p2} increase with a constant slope. Meanwhile, the voltage across the auxiliary *LC* network is zero. As a result, the auxiliary inductor current remains at its peak value $I_{\rm aux}$. This stage ends once S_1 is turned OFF.

Stage 10 [$t_9 \le t < t_{10}$]: During this stage, the output capacitor of S_2 is discharging down to zero and that of S_1 is charging up to $V_{\rm in}$ by the primary current i_{p1}. This stage ends once the output capacitor of switch S_2 is completely discharged to zero and the body diode of S_2 begins to conduct.

Stage 11 [$t_{10} \le t < t_{11}$]: At t_{11}, switch S_2 has been turned ON with ZVS. During this stage, the inverter voltage $v_{\rm AB}$ is zero, and therefore, the primary current i_{p1} decreases with a constant slope. This stage ends once the primary current i_{p1} reaches zero and the output diodes D_1 turns off naturally with zero current.

Stage 12 [$t_{11} \le t < t_{12}$]: During this stage, switches S_2 and S_4 are ON and i_{p1} remains at zero. Meanwhile, the input energy continues to be transferred to the output through Phase 2. This stage will end once S_4 is turned OFF and the next half switching cycle starts.

III. Analysis of the Proposed Converter

A. DCM Operation of the Series Inductor

Fig. 4 shows the primary-side current waveforms for the conventional PSFB converter and Phase 1 of ICD-PSFB. Because

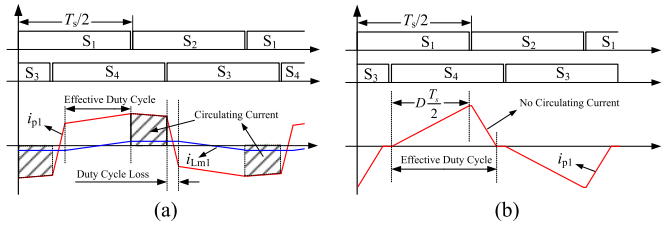


Fig. 4. Current waveform and gate pulses sequences of the primary-side full-bridge circuits: (a) conventional PSFB converter and (b) Phase 1.

of the DCM operation of the series inductor, there is no circulating current and duty cycle loss in the proposed converter compared to the conventional PSFB converter. The operation in DCM of the series ac inductor plays an important role in eliminating the voltage spikes across the secondary rectifiers, as well as reducing the turn-off/on losses in the lagging-leg switches. It can be seen from Fig. 4 that when the lagging-leg switch S_3 or S_4 (S_7 or S_8) is turned off/on, the current in the series inductor remains at zero. During these stages, the auxiliary *LC* circuit current $i_{\rm aux}$ is the only current in the lagging-leg switches. Since the auxiliary *LC* circuit current is considerably smaller than the current though the series inductor, it can be concluded that the turn-off/on loss of the lagging-leg switches is significantly reduced by the DCM operation of the series inductor. Also, when the current through the ac series inductor reaches zero, the output diodes turn OFF naturally because of the current-driven nature of the output rectifier, and therefore, the reverse recovery and switching losses in the secondary rectifiers are significantly reduced. However, the rms and peak values of the series inductance current increase because of the DCM operation, which may cause high conduction loss at very heavy loads and degrades the efficiency of the converter. The rms value of the current though the series inductor is given by

$$I_{p\_\rm RMS} = \frac{V_{\rm in}\left(1 - D_{\max}\right)D_{\max}T_s}{2\sqrt{3}L_s} \quad (14)$$

where $I_{p\_\rm RMS}$ is the rms value of the series inductance current, and $D_{\max}$ is the maximum duty cycle in a boundary conduction mode (BCM) which appears under the situation that the lagging-leg switches are turned OFF exactly at the time when the current in the series inductor reaches zero. Fig. 5 shows the variation of the rms value in (14) as a function of the maximum duty cycle $D_{\max}$ for different series inductance.

According to Fig. 5, when $D_{\max} = 0.5$, the rms value of the current in the series inductor reaches its maximum. Meanwhile, the rms value decreases as $D_{\max}$ increases when $D_{\max}$ is larger than 0.5, and also it increases as the series inductance decreases for a given value of the maximum duty cycle. Thus, increasing $D_{\max}$ (when $D_{\max} > 0.5$) and L_s may be a good choice to reduce the rms value of the current in the series inductance. However, a larger $D_{\max}$ results in faster downslope of the triangular current in the series inductor and this will increase the reverse recovery and switching losses in output diodes. In order to guarantee DCM conduction of the series inductor, the DCM operation condition should be determined, which can be

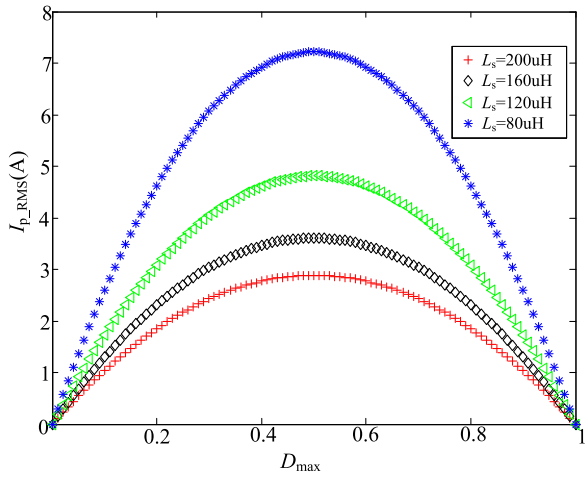


Fig. 5. RMS value of the current through the series inductor as a function of $D_{\max}$ for different L_s.

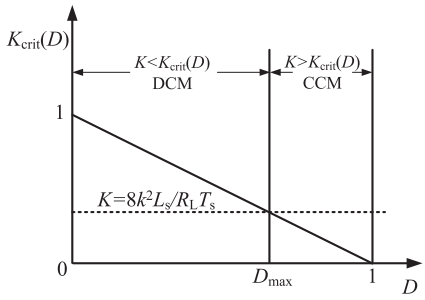


Fig. 6. Critical value $K_{\rm crit}(D)$ as a function of *D*.

expressed as follows based on Fig. 4(b):

$$\begin{cases} \frac{v_o}{L_s}\frac{(1-D)T_s}{2}\frac{1}{2k^2} \geq 2i_L \\ i_L = \frac{v_o}{R_L} \end{cases} \tag{15}$$

where i_L is the load current, R_L is the load resistance of the converter, and (15) can be rewritten as

$$\begin{cases} K \leq K_{\rm crit}(D) \\ D_{\max} = 1 - K \\ K = 8k^2 L_s / R_L T_s, K_{\rm crit}(D) = 1 - D. \end{cases} \tag{16}$$

The critical value $K_{\rm crit}(D)$ varying with *D* is shown in Fig. 6. An arbitrary choice of *K* is also illustrated. It can be seen from Fig. 6 that the series inductor operates in the DCM at low duty cycle and in continuous conduction mode (CCM) at high duty cycle. Meanwhile, the dimensionless parameter *K* increases as the load resistance R_L decreases, and if *K* is larger than one the series inductor operates in CCM for all duty cycles. In order to extend the DCM operation region, the value of the series inductance should be reduced for a given value of R_L. According to Fig. 5, however, the rms value of the series inductor current increases significantly as L_s decreases. The series inductor should be designed under the condition that the converter operates in BCM and at full-loads, and the value of series inductance is given by

$$L_s = \frac{V_{\rm in}(V_{\rm in} - v_o/2k)D_{\max}^2 T_s}{2P_{o,\max}} \tag{17}$$

where $P_{\rm o,max}$ is the maximum output power, and the turn ratio *k* is given by

$$k = \frac{v_o}{2V_{\rm in}D_{\max}}. \tag{18}$$

By using (18), (17) can be rewritten as

$$L_s = \frac{V_{\rm in}^2(1 - D_{\max})D_{\max}^2 T_s}{2P_{o,\max}}. \tag{19}$$

B. DC Gain

In this section, the voltage conversion ratio of the proposed converter is analyzed. In order to calculate the conversion ratio of the proposed converter, the average primary current through the series inductor over the positive half pulse width modulation (PWM) cycle should be determined. To simplify the steady-state analysis, the changes in the waveform of the primary current i_{p1} during Stages 1, 2, and 10 are neglected in this section. According to Fig. 4(b), the average value of the current i_{p1} over the positive half PWM cycle is given by

$$\begin{aligned} \bar{I}_{p1} &= \int_{t_0}^{t_0 + \frac{T_s}{2}} i_{p1}(t)dt = \frac{I_{p1}D_{\rm eff}}{2} \\ &= \frac{1}{T_s}\left(\frac{V_{\rm in} - v_o/2k}{L_s}\right)\left(D\frac{T_s}{2}\right)^2\left(\frac{2kV_{\rm in}}{v_o}\right) \end{aligned} \tag{20}$$

where $D_{\rm eff}$ is the effective duty cycle.

It is assumed that the converter losses are neglected, and it implies that the output power of the converter equals to the input power. According to this assumption, the following equations can be derived:

$$\frac{v_o}{2k}\bar{I}_{p1} = \frac{v_o i_L}{2}. \tag{21}$$

By using (15), (16), (20), and (21), the dc gain characteristic of the proposed converter is given by

$$G = \frac{v_o}{V_{\rm in}} = \frac{4k}{1 + \sqrt{1 + 4K/D^2}} \tag{22}$$

where $K = 8k^2 L_s / R_L T_s$ and $K < K_{\rm crit}(D)$. Fig. 7 shows the variation of dc gain as a function of the duty cycle *D* for several values of *K* when $k = 0.65$, $T_s = 16.7\,\mu$s, and $L_s = 75\,\mu$H. It can be seen that the variation of the gain is more obvious for smaller value of *K* in smaller values of duty cycle, and less prominent for larger value of *K*. Meanwhile, as *K* tends to zero, the dc gain tends to the maximum attainable voltage gain for all nonzero *D*.

C. Soft-Switching Conditions

In this section, the switching performance of the proposed converter is analyzed in detail. As shown in Fig. 4(b), the energy

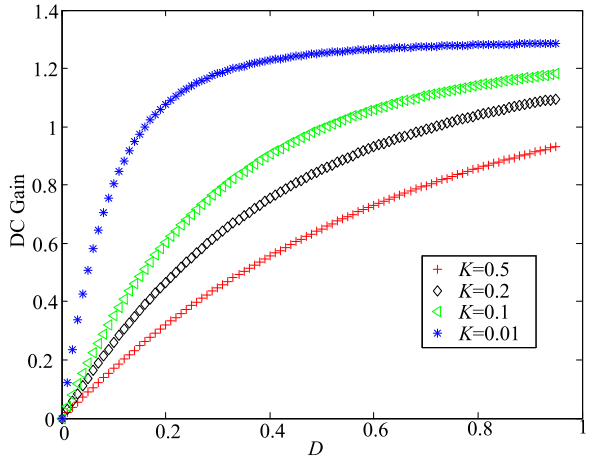


Fig. 7. Converter gain as a function of the duty cycle for several values of *K*.

stored in the series inductance is employed to help the leading-leg switches realize ZVS. Therefore, due to the sufficient energy stored in the series inductor, very wide ZVS range of the leading-leg switches can be achieved without any other auxiliary circuits. The ZVS conditions for the leading-leg switches can be expressed as

$$\frac{1}{2}L_s I_p^2 > C_{\rm so} V_{\rm in}^2 \tag{23}$$

where I_p is the peak value of the current through series inductor, and it is given by

$$I_p = \frac{V_{\rm in} - v_o/2k}{L_s}\frac{DT_s}{2}. \tag{24}$$

By using (23) and (24), the ZVS condition of the leading-leg switches can be expressed as

$$\frac{1 - G/2k}{L_s}\frac{DT_s}{2} - \sqrt{\frac{2C_{\rm so}}{L_s}} > 0. \tag{25}$$

By using (22), the ZVS condition in (25) can be rewritten as

$$Z(D,K) = D - \frac{2}{T_s}\sqrt{2C_{\rm so}L_s} - \frac{2D}{1+\sqrt{1+4K/D^2}} > 0. \tag{26}$$

Fig. 8 shows the ZVS condition *Z*(*D*, *K*) varying with *D* and *K* when $k = 0.65$, $T_s = 16.7\,\mu$s, $C_{\rm so} = 1$ nF, and $L_s = 75\,\mu$H. The ZVS region (the shadow area) as a function of *D* and *K* and the curve of dc gain characteristic with constant dc gains ($G = 0.75$ and 1) are illustrated in Fig. 9. It can be seen that ZVS of the leading-leg switches can be realized for a very wide duty cycle and power ranges ($D > 0.05$ and $K > 0.02$), which can be calculated for a given value of dc gain *G* according to Fig. 9.

In order to realize ZVS of the leading-leg switches, the dead time $t_{d,\rm leading}$ should be adjusted to allow the output capacitors of the leading-leg switches to fully charge and discharge, and it is given by

$$t_{d,\rm leading} > \Delta t_{34} \tag{27}$$

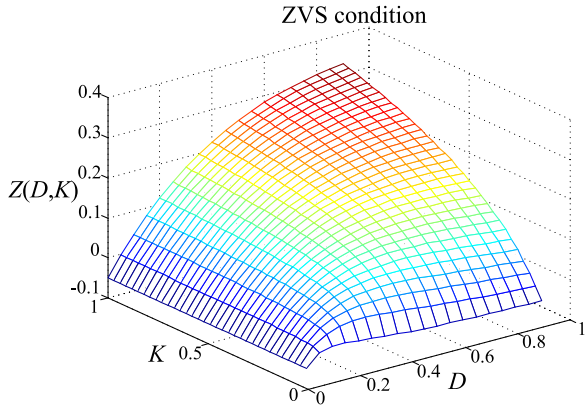


Fig. 8. ZVS condition of the leading-leg switches as a function of the duty cycle and parameter *K*.

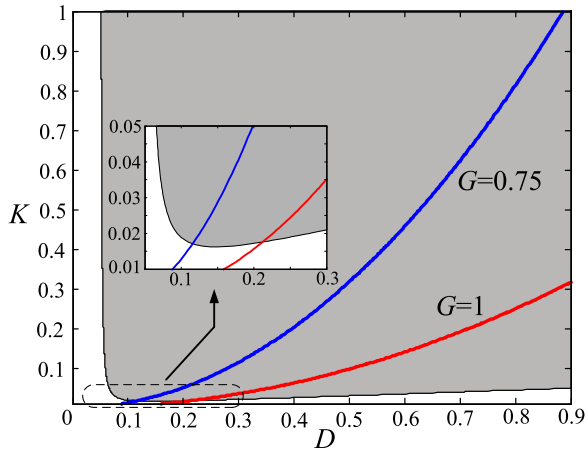


Fig. 9. ZVS region (the shadow area) as a function of *D* and *K*, and the curve of dc gain characteristic with constant dc gains.

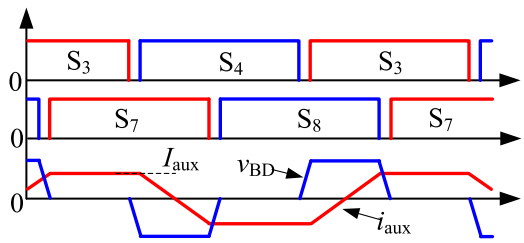


Fig. 10. Auxiliary circuit waveforms.

where Δt_{34} is the time interval of Stage 4, and it can be expressed as follows based on (11):

$$V_{\rm in}\cos(\omega\Delta t_{34}) - ZI_p\sin(\omega\Delta t_{34}) + \frac{v_o}{2k}\left[1 - \cos(\omega\Delta t_{34})\right] = 0. \tag{28}$$

In the proposed converter, the auxiliary *LC* circuit provides the reactive current to help the lagging-leg switches realize ZVS. The auxiliary *LC* circuit waveforms are illustrated in Fig. 10. The current in the auxiliary circuit remains pretty constant during the dead time because of the relatively large value of auxiliary inductance. The ZVS condition for the lagging-leg switches can

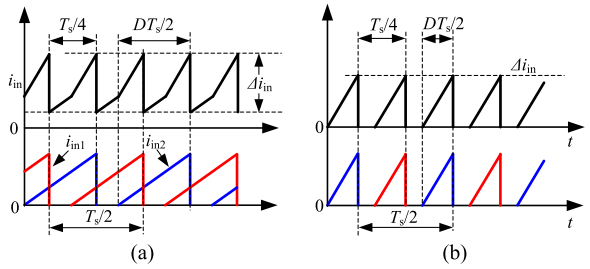


Fig. 11. Input current waveforms: (a) Case 1: $D > 0.5$, and (b) Case 2: $D < 0.5$.

be expressed as

$$\begin{cases} \frac{1}{2} L_{\text{aux}} I_{\text{aux}}^2 \geq C_{\text{so}} V_{\text{in}}^2 \\ I_{\text{aux}} = \frac{V_{\text{in}} T_s}{8 L_{\text{aux}}}. \end{cases} \tag{29}$$

Based on (29), the value of the auxiliary inductance can be designed as

$$L_{\text{aux}} \leq \frac{T_s^2}{128 C_{\text{so}}}. \tag{30}$$

The dead time $t_{d,\text{lagging}}$ is designed to allow the output capacitors of the lagging-leg switches to fully charge and discharge under no-load condition, and it is given by

$$t_{d,\text{lagging}} \geq \frac{2 C_{\text{so}} V_{\text{in}}}{I_{\text{aux}}} = \frac{16 C_{\text{so}} L_{\text{aux}}}{T_s}. \tag{31}$$

The dc blocking capacitor C_{aux} is connected in series with the auxiliary inductor to eliminate the dc bias current in the auxiliary circuit. If C_{aux} was not used, a nonzero average current would flow through the auxiliary circuit to reduce the peak value of the auxiliary inductor current. As a result, the lagging-leg switches may lose lossless turn-on. According to Mason *et al.* [3], the dc blocking capacitor is chosen under the condition that the switching frequency is at least five times larger than the auxiliary resonant frequency. Therefore, the dc blocking capacitor is given by

$$C_{\text{aux}} \geq \frac{1}{\left(2\pi \frac{f_s}{5}\right)^2 L_{\text{aux}}}. \tag{32}$$

D. Input Ripple Current

Because of the interleaving approach, the two phase power stages share equal power and also the input ripple current frequency is four times the switching frequency. Fig. 11 shows input current waveforms of the proposed converter for two different cases. The peak-to-peak ripple current is given by

$$\Delta i_{\text{in}} = \frac{V_{\text{in}} (1 - G/2k)}{L_s} \frac{DT_s}{2}. \tag{33}$$

By using (22), (33) can be rewritten as

$$\Delta i_{\text{in}} = \frac{V_{\text{in}} T_s D}{2 L_s} \left(1 - \frac{2}{1 + \sqrt{1 + 4K/D^2}}\right). \tag{34}$$

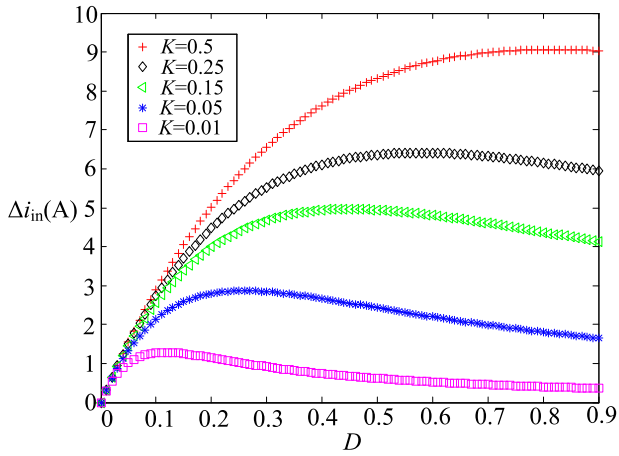


Fig. 12. Peak-to-peak ripple current Δi_{in} varying with D for several values of K.

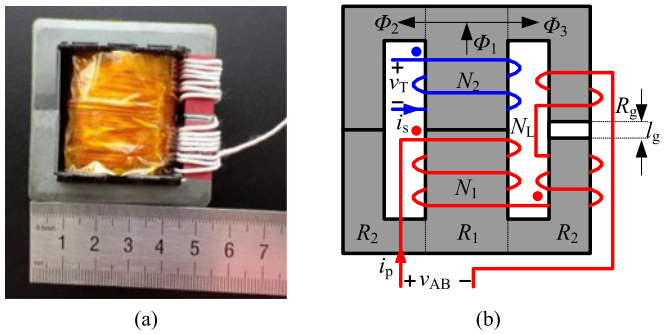


Fig. 13. Structure of the main transformer: (a) photograph and (b) winding arrangement diagram of the main transformer.

The peak-to-peak ripple current Δi_{in} varying with D for several values of K when $k = 0.65$, $T_s = 16.7\,\mu$s, and $L_s = 75\,\mu$H is illustrated in Fig. 12. It can be seen that Δi_{in} increases quickly when the duty cycle D is relatively small for a given value of K, and then decreases slowly when D is larger than some value. Therefore, the input filter should be designed based on the peak value of Δi_{in} according to Fig. 12.

E. Integrated Magnetic

Recently, the integration of the series inductor into the main transformer as the leakage inductor has been widely used in [24], [25], [35]. However, this configuration has several drawbacks for high-power applications. First, the value of leakage inductance is very difficult to be precisely designed. Meanwhile, the proximity effect is really serious since the top–bottom winding arrangement is employed instead of side-by-side interleaving configuration to provide enough series inductance [36], [37]. As a result, the copper loss increases significantly and the transformer may become a "hot spot." Therefore, the series inductor is integrated into the main transformer by using an additional winding in order to solve these problems. To simplify the analysis, the leakage inductances are ignored in this section. Fig. 13(a) shows a photograph of the main transformer and the winding arrangement diagram is illustrated in Fig. 13(b). The winding voltage and current waveforms and the equivalent magnetic

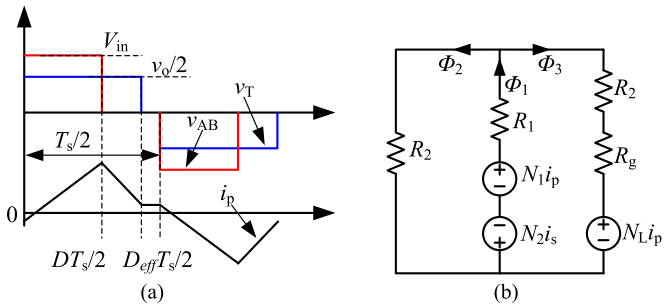


Fig. 14. Winding voltage and current waveforms and the equivalent magnetic circuit model of the main transformer: (a) winding voltage and current waveforms, and (b) equivalent magnetic circuit model.

circuit model are shown in Fig. 14(a) and (b), respectively. In the magnetic circuit model, R_1, R_2, and R_g represent the reluctances of the core and the air gap in the outer leg. According to Faraday's law, the fluxes induce voltages across the windings and the following equations can be derived:

$$\begin{cases} v_{\mathrm{AB}} = \frac{d(N_1\Phi_1 + N_L\Phi_3)}{dt} \\ v_T = N_2\frac{d\Phi_1}{dt} \\ \Phi_1 = \Phi_2 + \Phi_3 \end{cases} \tag{35}$$

where N_L is the number of series inductance winding turns. Based on (35) and Fig. 14(a), the flux changes can be derived as follows:

$$\Delta\Phi_1 = \frac{v_o t}{2N_2} \qquad 0 \le t < \frac{D_{\mathrm{eff}}T_s}{2} \tag{36}$$

$$\Delta\Phi_2 = \begin{cases} \frac{(N_L+N_1)v_o t}{2N_2N_L} - \frac{V_{\mathrm{in}}t}{N_L} & 0 \le t < \frac{DT_s}{2} \\ \frac{(N_L+N_1)v_o}{2N_2N_L}\left(t - \frac{DT_s}{2}\right) & \frac{DT_s}{2} \le t < \frac{D_{\mathrm{eff}}T_s}{2} \end{cases} \tag{37}$$

$$\Delta\Phi_3 = \begin{cases} \left(V_{\mathrm{in}} - \frac{N_1 v_o}{2N_2}\right)\frac{t}{N_L} & 0 \le t < \frac{DT_s}{2} \\ -\frac{N_1 v_o}{2N_2N_L}\left(t - \frac{DT_s}{2}\right) & \frac{DT_s}{2} \le t < \frac{D_{\mathrm{eff}}T_s}{2}. \end{cases} \tag{38}$$

Based on Kirchhoff's current and voltage law, the following equations can be derived from the equivalent magnetic circuit model illustrated in Fig. 14(b):

$$\begin{cases} N_1 i_p - N_2 i_s - \Phi_1 R_1 = \Phi_2 R_2 \\ N_1 i_p - N_2 i_s - \Phi_1 R_1 = \Phi_3 (R_2 + R_g) + N_L i_p \\ \Phi_1 = \Phi_2 + \Phi_3. \end{cases} \tag{39}$$

The fluxes distribution can be obtained by solving (39) and is given by

$$\begin{cases} \Phi_1 = \frac{(2R_2+R_g)(N_1 i_p - N_2 i_s) - R_2 N_L i_p}{\Delta} \\ \Phi_2 = \frac{(R_2+R_g)(N_1 i_p - N_2 i_s) + R_1 N_L i_p}{\Delta} \\ \Phi_3 = \frac{R_2(N_1 i_p - N_2 i_s) - (R_1+R_2)N_L i_p}{\Delta} \\ \Delta = (R_1+R_2)(R_2 + R_g + R_1 // R_2). \end{cases} \tag{40}$$

According to Fig. 14(a) and (36), the flux Φ_1 in the center leg reaches its peak value Φ_{1m} when $D_{\mathrm{eff}}T_s/2 \le t < T_s/2$ and Φ_{1m} is given by

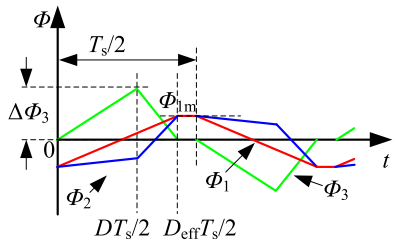


Fig. 15. Flux waveforms of the main transformer.

$$\Phi_{1m} = \frac{v_o D_{\mathrm{eff}} T_s}{8N_2}. \tag{41}$$

During this interval, the secondary current i_s is zero, and the outer leg fluxes Φ_{2m} and Φ_{3m} are given by

$$\begin{cases} \Phi_{2m} = \frac{(R_2+R_g)N_1 + R_1 N_L}{(2R_2+R_g)N_1 - R_2 N_2}\Phi_{1m} \approx \Phi_{1m} \\ \Phi_{3m} = \frac{R_2 N_1 - (R_1+R_2)N_L}{(2R_2+R_g)N_1 - R_2 N_2}\Phi_{1m} \approx 0 \\ R_g \gg R_1, R_2. \end{cases} \tag{42}$$

According to (36)–(38) and (40)–(42), the flux waveforms of the main transformer are shown in Fig. 15. It can be seen that the maximum values of fluxes occur when the converter operates in the BCM mode, and they are given by

$$\begin{cases} \Phi_{1\,\max} = \frac{v_o T_s}{8N_2} \\ \Phi_{2\,\max} = \Phi_{1\,\max} \\ \Phi_{3\,\max} = \left(V_{\mathrm{in}} - \frac{N_1 v_o}{2N_2}\right)\frac{D_{\max}T_s}{2N_L}. \end{cases} \tag{43}$$

The maximum values of the magnetic flux densities can be calculated as

$$B_{1\,\max} = \frac{\Phi_{1\,\max}}{A_c} \quad B_{2\max} = \frac{\Phi_{2\max}}{A_o} \quad B_{3\max} = \frac{\Phi_{3\max}}{A_o} \tag{44}$$

where A_c and A_o are the cross-sectional areas of center and outer legs, respectively. The turns numbers N_1, N_2, and N_L can be derived based on the maximum allowable magnetic flux densities in (43) and (44). Then, the air gap l_g can be calculated as

$$l_g = \frac{\mu_0 A_o N_L^2}{L_s}. \tag{45}$$

IV. Experiment Results and Discussions

In order to evaluate the performance of the proposed ICD-PSFB converter, an experimental hardware prototype has been designed, made, and tested. Fig. 16 illustrates the schematic diagram of experimental circuit. The parameters of the experimental prototype are presented in Table I. Fig. 17 shows a photograph of the experimental prototype. In this scheme, the average current mode control scheme is employed and the control circuit is implemented by using the conventional phase-shift control IC UCC2895. The interleaving control signals are generated by the high-speed PWM controller UC2825 and then fed into the SYNC pin of ICs UCC2895. It can be seen from

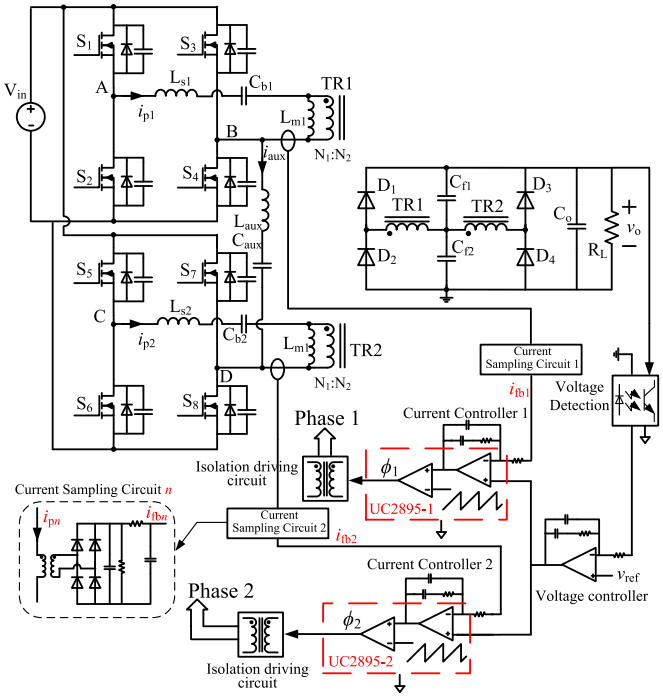


Fig. 16. Schematic diagram of an experimental circuit.

TABLE I
CIRCUIT PARAMETERS

Parameter	Value/Part Number
Maximum output power P_o	2 kW
Input voltage V_{in}	400 V
Output voltage v_o	200–400 V
Switching frequency f_s	60 kHz
Primary switches S_1–S_8	STMicroelectronics STW45NM60 600 V, 45 A. $R_{ds,on} = 90\,m\Omega$
Transformer TR1 and TR2	Ferroxcube E55/28/21-3C95 ferrite core; primary turns $N_1 = 30$; secondary turns $N_2 = 20$; $N_L = 15$; air gap $l_g = 0.92$ mm; magnetizing inductance $L_m = 2.8\,mH$; series inductance $L_s = 75\,\mu$H
DC blocking capacitor C_{b1} and C_{b2}	1.5 μF, 150 V high-frequency film capacitor
Output diodes D_1–D_4	Fairchild semiconductor diode ISL9R1560 600 V, 15 A
Rectifier capacitors Cf_1 and C_{f2}	4.7 μF, 400 V high-frequency film capacitor
Output capacitors C_o	4.7 μF, 630 V high-frequency film capacitor
Auxiliary inductance L_{aux}	Ferroxcube E30/15/7-3C90 ferrite core; turns = 100; air gap = 1 mm; auxiliary inductance $L_{aux} = 820\,\mu$H
Auxiliary dc blocking capacitor C_{aux}	0.47 μF, 630 V high-frequency film capacitor

Fig. 16 that the output of the outer voltage controller provides the primary current reference for the two phases and serves as the current sharing bus. The inner current controllers are used to realize current sharing among both the phases and generate the desired phase-shift angles between the legs. The primary currents of the main transformers are sampled by current transformers as the current feedback signals. It should be noted that the current feedback signals are also fed into the CS pin of the ICs UCC2895 for overcurrent protection.

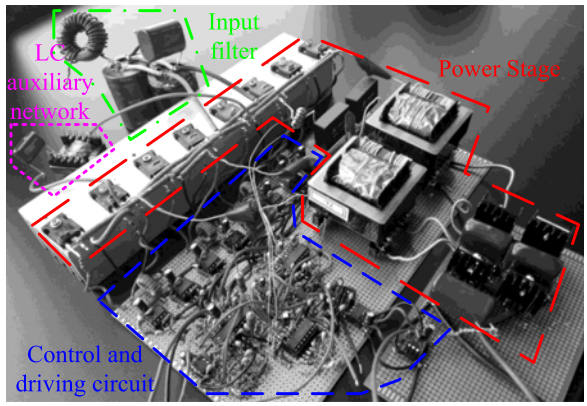


Fig. 17. Experimental prototype.

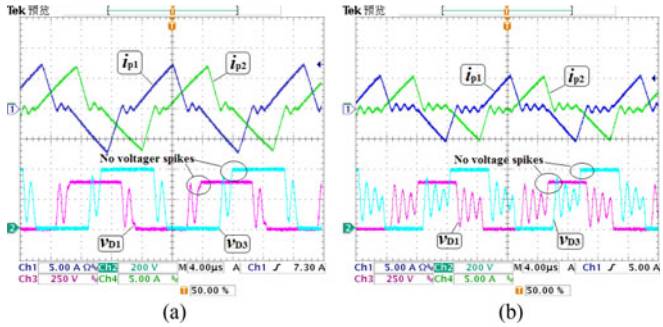


Fig. 18. Key experimental waveforms of CD-FBC at $v_o = 400$ V for different load conditions. (a) Full-load, and (b) 50% load.

Fig. 18 illustrates the key experimental waveforms of the ICD-PSFB at $v_o = 400$ V for different load conditions. It can be seen that the primary current of the main transformer remains at zero when the lagging-leg switches are turned OFF. During this interval, the only current in the lagging-leg switches is the *LC* auxiliary network current, which is much smaller than the current in the series inductor. Therefore, it can be concluded that the lagging-leg switches undergo near ZCS turn-off because of the DCM operation of the series inductor. Meanwhile, there are no voltage spikes across the secondary diodes of ICD-PSFB. Considering the fact that the output diodes turn OFF naturally when the series inductance current reaches zero, it can be clearly demonstrated that the well-clamped voltage stress and smooth operation of the output diodes can be realized. It should be noted that the current stress of the output diodes is also reduced significantly because of the interleaving approach. As a result, the expensive and high performance SiC schottky diodes are not required to implement the output diode bridge. In contrast, the diodes with lower breakdown voltage rate and lower forward voltage drop can be used to further improve the efficiency.

Figs. 19 and 20 show the switching waveforms of the leading-leg switch S_2 for different load conditions. These figures show that ZVS of the leading-leg switches is realized over very wide load range owing to the sufficient energy stored in the series inductor. The lagging-leg switch waveforms and the auxiliary *LC* network current for different load conditions are illustrated in Figs. 21 and 22. According to these figures, the lagging-leg switch can realize ZVS at very light load by using the auxiliary

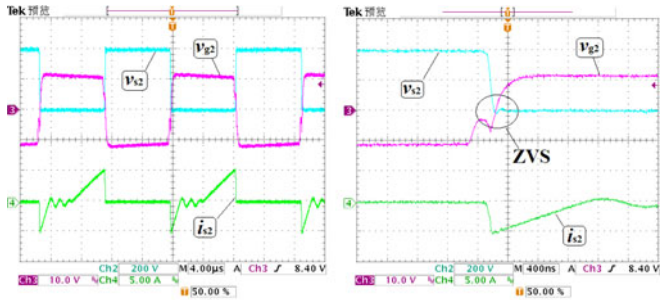


Fig. 19. (a) Measured switching waveforms of the leading-leg switch S_2 at $v_o = 400\,\text{V}$ and 50% load, and (b) enlarged switching waveforms of S_2 at $v_o = 400\,\text{V}$ and 50% load.

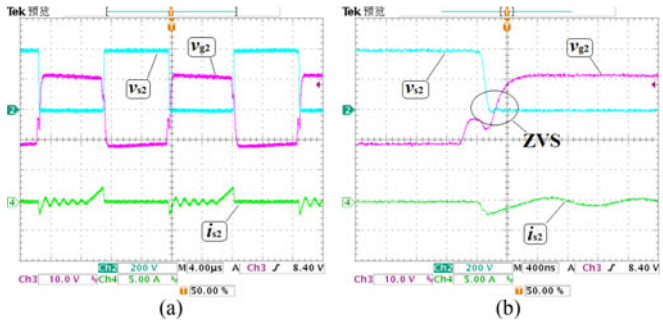


Fig. 20. (a) Measured switching waveforms of the leading-leg switch S_2 at $v_o = 400\,\text{V}$ and 10% load, and (b) enlarged switching waveforms of S_2 at $v_o = 400\,\text{V}$ and 10% load.

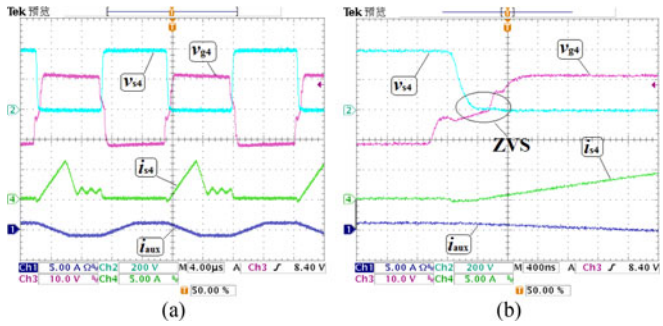


Fig. 21. (a) Measured switching waveforms of the lagging-leg switch S_4 at $v_o = 400\,\text{V}$ and 50% load, and (b) enlarged switching waveforms of S_4 at $v_o = 400\,\text{V}$ and 50% load.

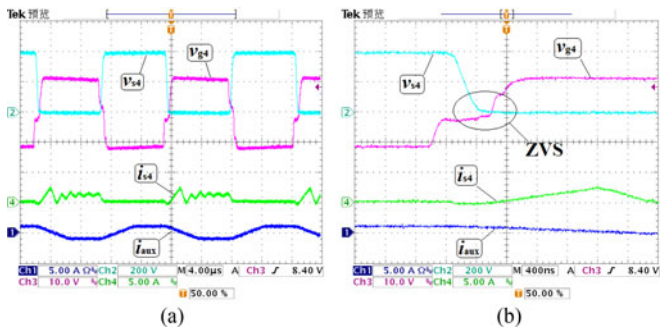


Fig. 22. (a) Measured switching waveforms of the lagging-leg switch S_4 at $v_o = 400\,\text{V}$ and 10% load, and (b) enlarged switching waveforms of S_4 at $v_o = 400\,\text{V}$ and 10% load.

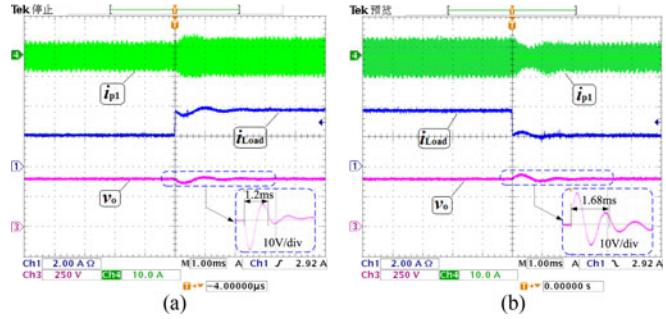


Fig. 23. Experimental waveforms of the load step change (a) from 2 to 3.8 A, and (b) from 3.8 to 2 A.

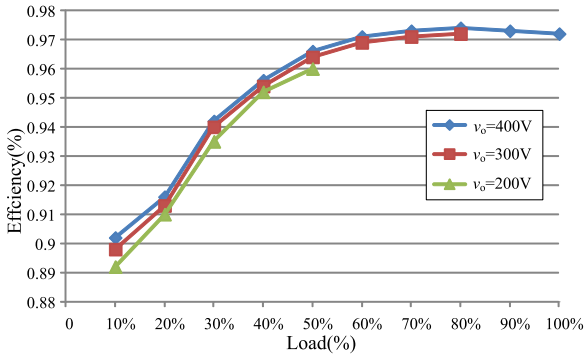


Fig. 24. Efficiency curves of the proposed converter for different output voltages.

LC network current i_{aux}, which is independent of load conditions. It should be noted that the dead time for light loads should be larger than the one for heavier loads. Therefore, the adaptive delay set function of IC UCC2895 is used to adjust the dead time according to the load conditions. The load step change experimental waveforms are shown in Fig. 23 to illustrate the dynamic response of the proposed converter. It can be identified that the ICD-PSFB takes 1.2 ms settle time with a maximum overshoot voltage 38 V under a load step-up change from 2 to 3.8 A. Also, the ICD-PSFB takes 1.68 ms settle time with a maximum overshoot voltage 34 V under a load step-down change from 3.8 to 2 A. Therefore, a good dynamic response of the proposed converter is clearly verified herein.

The efficiency curves of the proposed converter for different output voltages are illustrated in Fig. 24. This figure shows that the efficiency is more or less higher for higher output voltage because of the reduced conduction losses in the active switches and output diodes. It can also be seen that the efficiency is higher than 90% for very wide load range due to the soft switching and interleaving approach. The peak efficiency of 97.4% is achieved under the conditions $P_{\text{o}} = 1.6\,\text{kW}$ and $v_{\text{o}} = 400\,\text{V}$. Therefore, highly efficient operation of the proposed converter is clearly confirmed herein.

V. Comparative Study

To provide a fair basis for comparison, a prototype of reference converter (see Fig. 25) in [3] is designed and implemented with the same specifications. Fig. 26 shows the auxiliary circuit

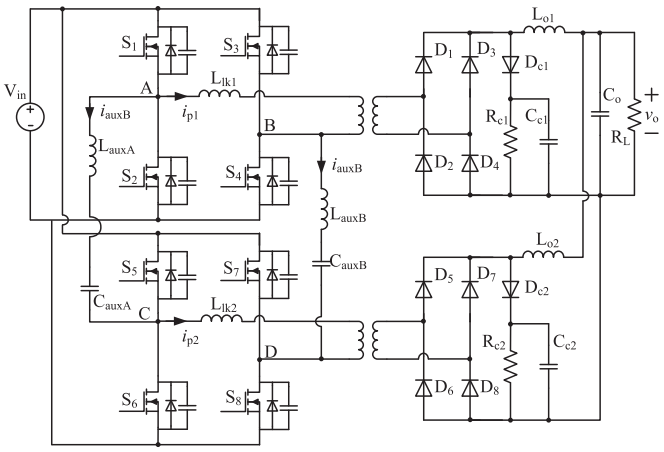


Fig. 25. Reference topology: two-cell ZVS phase-shift-modulated full-bridge converter with adaptive energy storage.

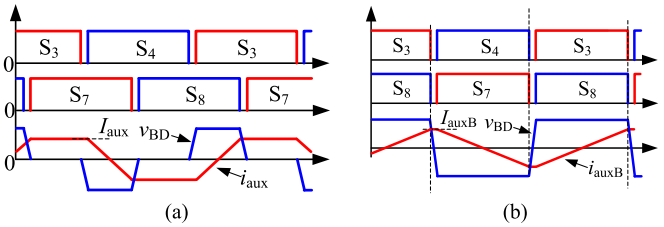


Fig. 26. Auxiliary circuit waveforms of the (a) proposed converter and (b) reference converter under no-load conditions.

waveforms of the proposed converter and the reference converter under no-load conditions. To achieve ZVS turn-on, the output capacitors of the active switches must be discharged in the deadtime under no-load condition. Therefore, the peak values of the auxiliary circuit currents are equivalent to each other with the same deadtime, and they are given by

$$I_{\text{aux}} = I_{\text{aux}B} = \frac{2C_{\text{so}}V_{\text{in}}}{t_d}. \tag{46}$$

According to Fig. 26, the rms values of the auxiliary currents are given by

$$\begin{cases} \bar{I}_{\text{aux}} = \frac{\sqrt{6}I_{\text{aux}}}{3} \\ \bar{I}_{\text{aux}B} = \frac{\sqrt{3}I_{\text{aux}}}{3}. \end{cases} \tag{47}$$

The rms values of the voltages across the auxiliary circuits are given by

$$\begin{cases} \bar{V}_{\text{aux}} = \frac{\sqrt{2}V_{\text{in}}}{2} \\ \bar{V}_{\text{aux}B} = V_{\text{in}}. \end{cases} \tag{48}$$

The area product of a core is proportional to the apparent power handled by the ac inductor. Therefore, the size ratio of the auxiliary inductors between the proposed converter and reference converter can be given by

$$\frac{A_{p,\text{aux}}}{A_{p,\text{aux}B}} = \frac{\bar{V}_{\text{aux}}\bar{I}_{\text{aux}}}{\bar{V}_{\text{aux}B}\bar{I}_{\text{aux}B}} = 1. \tag{49}$$

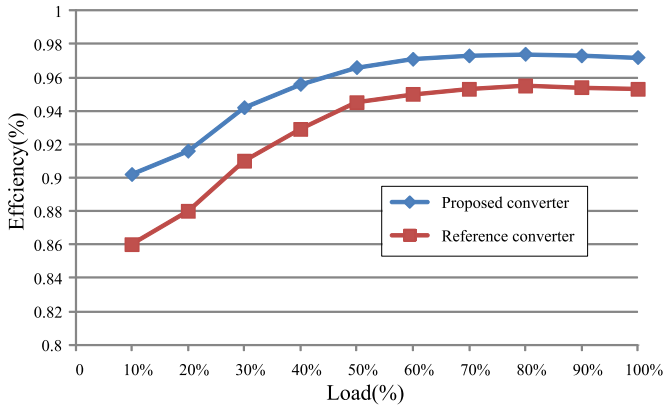


Fig. 27. Efficiency comparison of the proposed converter with the reference converter at 400 V output voltage.

According to (49), it can be concluded that the size of auxiliary inductor in the proposed converter is the same with the one in the reference converter. Considering the fact that only one auxiliary circuit is needed in the proposed converter, it can be clearly demonstrated that the size of auxiliary components in the proposed converter is significantly reduced comparing with the reference converter. According to (47), the rms value of the auxiliary currents in the proposed converter is relatively larger than the one in the reference converter. However, the increase in the conduction losses in the switches due to the auxiliary current, in the proposed converter, is really small since the current in the auxiliary circuit is much smaller than the current in the series inductor. An efficiency comparison of the proposed converter with the two-cell reference converter is provided in Fig. 27. It is shown in Fig. 27 that the overall efficiency of the proposed converter is relatively higher than the reference counterpart, especially under light-load conditions. This is due to the fact that the reference converters suffers from the losses in the secondary-side RCD clamp circuits and reverse recovery losses in the output diodes.

VI. Conclusion

In this paper, an ICD-PSFB converter with magnetic integration and voltage doubler rectifiers is introduced. Soft switching of the active switches is realized over a very wide load range. The voltage stresses of the secondary rectifiers are significantly reduced. The smooth commutations of the output diodes are realized due to the current-driven nature of the secondary rectifiers. Therefore, the general ultrafast diodes, instead of high performance and expensive SiC schottky diodes, are used to implement the output diode bridge. The required inductive passive components are all integrated into the main transformer, leading to fewer components and a simple circuit. The input ripple current is significantly reduced because of the interleaving approach. Therefore, there is a great potential for the proposed converter to be used in PHEV battery chargers applications. Experimental results obtained from a laboratory-made prototype have validated the feasibility and superior performance of the proposed converter.

REFERENCES

[1] Y. Ren, M. Xu, J. Sun, and F. C. Lee, "A family of high power density unregulated bus converters," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

[2] B. Whitaker *et al.*, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[3] A. J. Mason, D. J. Tschirhart, and P. Jain, "New ZVS phase shift modulated full-bridge converter topologies with adaptive energy storage for SOFC application," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 332–342, Jan. 2008.

[4] L. H. Mweenem, C. A. Wright, and M. F. Schlecht, "A 1 kW 500 kHz front-end converter for a distributed power supply system," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 398–407, Jul. 1991.

[5] B. Chen and Y. Lai, "Switching control technique of phase-shift-controlled full-bridge converter to improve efficiency under light-load and standby conditions without additional auxiliary components," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 1001–1011, Apr. 2010.

[6] W. Chen, F. C. Lee, M. M. Jovanovic, and J. A. Sabate, "A comparative study of a class of full bridge zero-voltage-switched PWM converters," in *Proc. IEEE 10th Annu. Appl. Power Electron. Conf. Expo.*, 1995, pp. 893–899.

[7] G. N. B. Yadav and N. L. Narasamma, "An active soft switched phase-shifted full-bridge DC-DC converter: analysis, modeling, design, and implementation," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4538–4550, Sep. 2014.

[8] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high power full-bridge zero-voltage-switched PWM converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 1990, pp. 275–284.

[9] H. Yoon, S. Han, E. Choi, G. Moon, and M. Youn, "Zero-voltage switching and soft-commutating two-transformer full-bridge PWM converter using the voltage-ripple," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1478–1488, Mar. 2008.

[10] Y. Jang and M. M. Jovanovic, "A new family of full-bridge ZVS converters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 701–708, May 2004.

[11] R. Redl, N. O. Sokal, and L. Balogh, "A novel soft-switching full-bridge DC/DC converter: Analysis, design considerations, and experimental results at 1.5 kW, 100 kHz," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 408–418, Jul. 1991.

[12] Z. Ye, "Dual half-bridge DC-DC converter with wide-range ZVS and zero circulating current," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3276–3286, Jul. 2013.

[13] M. Borage, S. Tiwari, S. Bhardwaj, and S. Kotaiah, "A full-bridge DC-DC converter with zero-voltage-switching over the entire conversion range," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1743–1750, Jul. 2008.

[14] W. Song and B. Lehman, "Current-fed dual-bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 461–469, Mar. 2007.

[15] G. Moschopoulos and P. Jain, "ZVS PWM full-bridge converters with dual auxiliary circuits," in *Proc. 22nd Int. Telecommun. Energy Conf.*, 2000, pp. 574–581.

[16] D. S. Wijeratne and G. Moschopoulos, "A ZVS-PWM full-bridge converter with reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3501–3513, Jul. 2014.

[17] Z. Chen, S. Liu, and L. Shi, "Improved zero-voltage-switching pulse width modulation full bridge converter with self-regulating auxiliary current," *IET Power. Electron.*, vol. 6, no. 2, pp. 287–296, Feb. 2013.

[18] A. Safaee, P. Jain, and A. Bakhshai, "A ZVS pulsewidth modulation full-bridge converter with a low-RMS-current resonant auxiliary circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4031–4047, Jun. 2016.

[19] V. R. K. Kanamarlapudi, B. Wang, P. L. So, and Z. Wang, "Analysis, design, and implementation of an APWM ZVZCS full-bridge DC-DC converter for battery charging in electric vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6145–6160, Aug. 2017.

[20] M. Pahlevani, S. Pan, and P. Jain, "A hybrid phase-shift modulation technique for DC/DC converters with a wide range of operating conditions," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7498–7510, Dec. 2016.

[21] M. Pahlevaninezhad, J. Drobnik, P. K. Jain, and A. Bakhshai, "A load adaptive control approach for a zero-voltage-switching DC/DC converter used for electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 920–933, Feb. 2012.

[22] A. Safaee, P. K. Jain, and A. Bakhshai, "An adaptive ZVS full-bridge DC-DC converter with reduced conduction losses and frequency variation range," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4107–4118, Aug. 2015.

[23] M. Pahlevaninezhad, S. Eren, P. K. Jain, and A. Bakhshai, "Self-sustained oscillating control technique for current-driven full-bridge DC/DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5293–5310, Nov. 2013.

[24] M. Pahlevaninezhad, S. Eren, A. Bakhshai, and P. Jain, "A series-parallel current-driven full-bridge DC/DC converter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1275–1293, Feb. 2016.

[25] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, "A novel ZVZCS full-bridge DC/DC converter used for electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2752–2769, Jun. 2012.

[26] C. Zhao, X. Wu, P. Meng, and Z. Qian, "Optimum design consideration and implementation of a novel synchronous rectified soft-switched phase-shift full-bridge converter for low-output-voltage high-output-current applications," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 388–397, Feb. 2009.

[27] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Analysis and evaluation of interleaving techniques in forward converters," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 690–698, Jul. 1998.

[28] X. Wu, H. Chen, J. Zhang, F. Peng, and Z. Qian, "Interleaved phase-shift full-bridge converter with transformer winding series-parallel autoregulated (SPAR) current doubler rectifier," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4864–4873, Sep. 2015.

[29] D. Wang, X. He, and J. Shi, "Design and analysis of an interleaved flyback forward boost converter with the current autobalance characteristic," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 489–498, Feb. 2010.

[30] B. R. Lin, C. L. Huang, and J. F. Wan, "Analysis, design, and implementation of a parallel ZVS converter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1586–1594, Apr. 2008.

[31] X. Kong and A. M. Khambadkone, "Analysis and implementation of a high efficiency, interleaved current-fed full bridge converter for fuel cell system," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 543–550, Mar. 2007.

[32] L. Sun, Y. Chen, X. Xia, L. Peng, and Y. Kang, "Design and optimization of parallel DC-DC system based on current-driven phase shift full bridge converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 2048–2053.

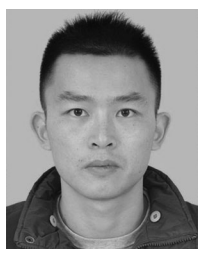
[33] D. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "An isolated interleaved DC-DC converter with voltage doubler rectifier for PHEV battery charger," in *Proc. IEEE Appl. Power Electron. Conf.*, 2013, pp. 3067–3072.

[34] H. Wu, P. Xu, W. Liu, and Y. Xing, "Series-input interleaved forward converter with a shared switching leg for wide input voltage range applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5029–5039, Nov. 2013.

[35] Fairchild Semiconductor Corporation, "Half-bridge LLC resonant converter design using FSFR-series Fairchild power switch," Application Note AN-4151, 2007.

[36] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA, USA: Kluwer.

[37] A. A. Dauhajre, "Modeling and estimation of leakage phenomena in magnetic circuits," Ph.D. thesis, California Inst. Technol., Pasadena, CA, USA, 1986.



Kaimin Shi was born in Fujian, China, in 1986. He received the B.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2009, and the M.S. degree in electrical engineering from the Harbin Institute of Technology Shenzhen Graduate School, Shenzhen, China, in 2011, where he is currently working toward the Ph.D. degree in power electronics and power drives.

His current research interests include power electronics, high-frequency soft-switching techniques, dynamic modeling, and control design.

Donglai Zhang (M'03–SM'16) was born in Jilin, China, in 1973. He received the B.S., M.S., and Ph.D. degrees in mechanical and electronic engineering from the Harbin Institute of Technology, Harbin, China, in 1994, 1996, and 1999, respectively.

Since 2005, he has been a Professor with the Harbin Institute of Technology Shenzhen Graduate School. His research interests include analysis, modeling and control of power converters, digital control techniques for power electronic circuits, and grid-connected converters for renewable energy systems. In these research fields, he has led several industrial and government projects.

Prof. Zhang is a member of the China Power Electronics Society.

Yu Gu (M'12) was born in Shenzhen, China, in 1986. He received the B.S. degree from the South China University of Technology, Guangzhou, China, in 2009, and the M.S. and Ph.D. degrees in electrical engineering from the Harbin Institute of Technology Shenzhen Graduate School, Shenzhen, China, in 2011 and 2017, respectively.

He is currently a Postdoctoral Researcher with the Power Electronics and Electrical Drives Research Center, Harbin Institute of Technology Shenzhen Graduated School. His research interests include power electronics, renewable energy systems, multilevel power converters, and pulse-width modulation techniques.