Digital Constant On-Time V^2 Control With Hybrid Capacitor Current Ramp Compensation

Pei-Hsin Liu, *Student Member, IEEE*, Yingyi Yan, *Student Member, IEEE*, Paolo Mattavelli, *Fellow, IEEE*, and Fred C. Lee, *Fellow, IEEE*

***Abstract*—In order to incorporate the advantage of the V^2 control scheme and the benefits of digital implementation, this paper proposes a digital V^2 control with hybrid capacitor current ramp compensation, which includes the estimated output capacitor current ramp and the external ramp. Since capacitor current responds to the load change immediately, the proposed method has faster transient response than either digital inductor current compensation or external ramp compensation. The proposed estimator does not require high sampling rate and avoids the current ramp distortion due to the parasitic resistance and inductance. The small-signal model is derived by describing function to understand the dynamic characteristics of the proposed control scheme. The model provides design criteria of the current feedback gain and the external ramp slope. The effectiveness of the proposed control architecture and the current ramp estimator is verified by simulation and experimental results. Compared with the benchmark, the proposed control has 70% reduction on settling time and 20% reduction on undershoot deviation.**

***Index Terms*—Capacitors, inductors, estimation, pulse width modulation, switches, transient response.**

I. Introduction

CONSTANT on-time V^2 control of a Buck converter, which features fast load transient response, is widely used in point-of-load converters [1]. However, with small time-constant output capacitors, such as a ceramic capacitor, the fast feedback loop has an instability issue [2], [3]. Physically, the power stage of the Buck converter has a second-order filter. With the small time-constant capacitor, the capacitor voltage ripple with 180°delay dominates the feedback signal, so the feedback loop has the subharmonic instability. To solve the instability issue, several ramp compensation strategies have been presented.

The external ramp compensation strategy has been presented in [4]–[6]. The external ramp can stabilize the system and suppress the double-pole peaking of the control-to-output transfer function. Although the implementation is simple, this method introduces a new set of double-pole, so it usually cannot achieve sufficient damping for the resonant peaking around half of switching frequency, especially for the large-duty-cycle operating points [5].

The inductor current ramp compensation strategy has been proposed to enhance the inductor current signal and provide well-damped response [4]. Intuitively, when the inductor current signal with 90° delay overwhelms the capacitor voltage ripple with 180° delay, the loop has stability margin. To cancel the undesired droop introduced by the inductor current, some commercial analog V^2 controllers insert a high-pass filter in the inductor current feedback path or add an outer-loop compensator [7]. However, physically, the inductor current does not respond to the load change immediately. This nature limits the fast response of V^2 control with inductor current compensation.

Conceptually, the capacitor current feedback in V^2 control is the root reason why V^2 control has fast transient response. Sensing the capacitor current by the equivalent series resistance (ESR) is equivalent to sensing both the inductor current and the load current simultaneously [8]. The inductor current feedback stabilizes the loop, while the load current feedforward provides the fast transient response. The aforementioned solutions do not follow this nature of V^2 control and use other ramp signals to overwhelm the capacitor current signal; therefore, although the loop can be stable, the transient responses are not as good as V^2 control with large ESR capacitors.

V^2 control with capacitor current ramp compensation has faster transient response, compared with the external ramp compensation and inductor current ramp compensation. In the analog implementations, several papers have demonstrated the superior performance of V^2 control with capacitor current ramp compensation [7], [9], [11]–[14], [22], [23].

Recent development of digital control for dc/dc switching converters has shown many unique capabilities such as digital communication, programmability, autotuning, and efficiency optimization [15], [16]. In order to incorporate the advantage of the V^2 control scheme and the benefit of digital implementation, the techniques of digital V^2 control are recently intensively studied [17], [18], [20]. As the state of the art, all these papers use the estimated inductor current ramp to stabilize the feedback loop. Among these papers, paper [20] used hysteresis modulation, while papers [17] and [18] focus on the digital V^2 control with constant on-time modulation, which has been considered as the most promising modulation due to the light-load

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efficiency improvement feature. Since direct sampling the inductor current needs a very high resolution and very high speed analog-to-digital converter (ADC), it is not practical. In [17] and [18], a digital ac inductor current estimator is proposed to reconstruct ac inductor current ramp. The estimator uses two ADCs to sample the input and output voltages, respectively. Then, with the information of V_{in}, V_o and the knowledge of inductor L, the estimated current waveform is generated by an up-and-down counter inside the digital controller. Instead of sensing the V_{in}, paper [20] sensed the switching node voltage and the output voltage to estimate the inductor current. The estimator in [19] used a further simplified implementation with one ADC to estimate the inductor current for current mode control. It assumed the V_{in} was unchanged and the switching node exactly duplicates the pulse width modulation (PWM) signal's timing. The inductor current follows the voltage–second balance rule. However, due to the quantization errors of input and output voltages, uncertainty on gate driver delays, and the dependence between switching node waveform and the load current, the "voltages" and "seconds" in the digital domain are likely imbalanced. The estimation errors accumulate over time and the estimation runs away. The inductance variations due to bias, aging, and temperature may also lead to the offset between the estimated current and the real current. To eliminate the drift, the estimator has an additional drift compensation mechanism. Another digital inductor current estimator proposed in [21] used a simple 1-bit current sensor to correct the similar ramp drifting issue. Papers [17], [18], and [20] have thoroughly investigated the architecture of digital V^2 control with estimated inductor current ramp compensation, and the detailed small-signal model and design procedure have been presented. Nevertheless, the inductor current does not respond to the load change immediately. Intuitively, this nature limits the fast transient response of these controllers with inductor current compensation.

The aim of this paper is to propose a digital V^2 control scheme with capacitor current ramp compensation. The prior research studies on analog V^2 control reported in [7] and [9]–[14] suggest that V^2 control with capacitor current ramp compensation has a faster transient response than inductor current ramp compensation. In the proposed digital implementation, an additional external ramp is added to improve the small-signal property of the system, so it is a hybrid ramp compensation architecture. In this paper, as a building block of the proposed control scheme, a capacitor current estimation technique will be presented. The proposed estimator utilizes the sampled output voltage and PWM signal to generate the estimated waveform. No additional drift compensation loop is needed. Compared with the digital ac inductor current estimator that needs an additional ADC and an additional drift compensation loop [18], it is simpler and more cost effective. It will be shown that the proposed scheme has faster transient response than V^2 with inductor current compensation in [18].

In the remaining parts of this paper, the proposed scheme of digital V^2 control with hybrid capacitor current ramp compensation is presented in Section II. The structure of the current estimator is illustrated in Section III. The small-signal model is derived in Section IV to understand the dynamic characteristics of the proposed control scheme. The design procedure of current feedback gain and external ramp slope is provided. Simulink simulation and experimental results are given in Section V to verify the effectiveness of the proposed method.

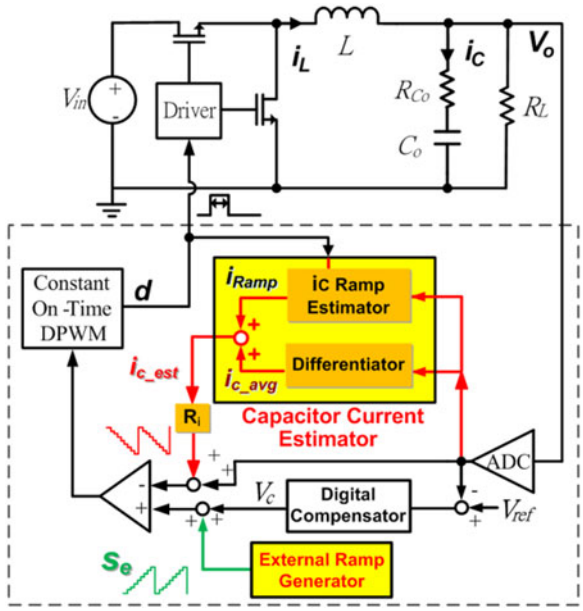

Fig. 1. Block diagram of the proposed digital V^2 control with hybrid capacitor current ramp compensation.

II. Proposed Digital V^2 Control With Hybrid Capacitor Current Ramp Compensation

Fig. 1 shows the block diagram of the proposed digital constant on-time V^2 control scheme with hybrid ramp compensation. The output voltage v_o is digitized by the ADC and fed to three paths. The first path is connected to the inverting input of the comparator, like the traditional V^2 control. The second one goes to the capacitor current estimator, which generates the signal i_{c_est}. The detail implementation of the estimator will be presented in Section III. The i_{c_est} is amplified by a gain R_i and summed with the direct feedback signal. On the noninverting input, the digital compensator integrates the error between the output voltage and reference to provide accurate regulation. A high-resolution digital external ramp s_e is added to V_c to improve the dynamic performance. The mathematical model for the hybrid ramp compensation will be presented later on in Section IV. The comparator output triggers the constant on-time digital modulator to generate the PWM signal d and drives the power stage.

III. Digital Capacitor Current Estimator

For constant on-time modulation, the modulator uses only the off-time signal to determine the switch-on instant of the next switching cycle. Hence, the output voltage is sampled every cycle after the fixed on-time expires.

The capacitor current i_c consists of its average value and the switching ripple. Accordingly, as shown in Fig. 2, the estimated capacitor current waveform i_{c_est} during the ith off-time can be

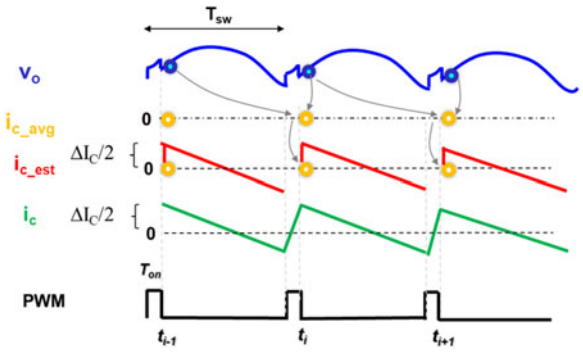

Fig. 2. Illustration of capacitor current estimation with single sampling.

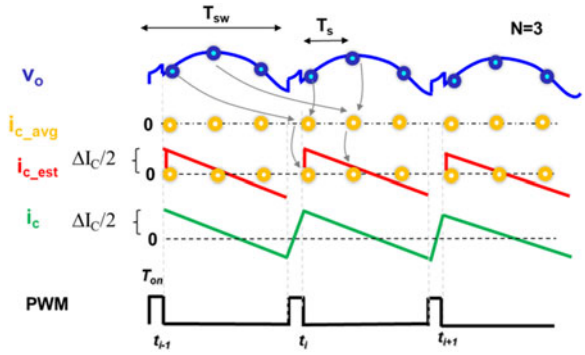

Fig. 3. Illustration of capacitor current estimation with oversampling.

decomposed as (1). The sawtooth ramp in Fig. 2 is the i_{ramp} from the ramp generator, while the circles represent the ramp starting point $i_{c\_\text{avg}}(t_i)$

$$i_{c\_\text{est}}(t) = i_{\text{Ramp}}(t) + i_{c\_\text{avg}}(t_i) \tag{1}$$

where $i_{c\_\text{avg}}(t_i)$ is the average value of capacitor current in the ith switching cycle, $i_{\text{Ramp}}(t)$ is the current ramp ripple in $T_{\text{off}(i)}$ period, and $T_{\text{off}(i)}$ is the ith cycle's off-time.

To generate these, in the capacitor current estimator, the digitized v_o signal is processed by two parallel paths. The output of these two paths is summed together to emulate the real-time capacitor current signal.

On one hand, the i_c ramp estimator utilizes the sampled output voltage and duty cycle information to generate the off-time ramp inside the digital controller, which emulates the capacitor current ripple during the off-time. It is a linear ramp during off-time with half of the capacitor current switching ripple offset, and the ramp signal is reset to zero during on-time by PWM signal d

$$i_{\text{Ramp}}(t)\big|_{t_i<t<t_{i+1}-T_{\text{on}}} = \frac{\Delta I_c}{2} - \frac{v_o(t_i)}{L}(t - t_i) \tag{2}$$

where the first term, $\Delta I_c/2 = V_o \text{T}_{\text{off}}/(2L)$, is a half of capacitor current ripple to offset the $i_{\text{Ramp}}(t)$, and the second term is off-time current ramp slope. L is the inductance of the output inductor.

On the other hand, the differentiator takes the sampled output voltages of the current switching cycle and that of the previous cycle to calculate the average value of capacitor current i_{c_avg}. The $i_{c\_\text{avg}}(t_i)$ is calculated based on the sampled output voltage from the ADC. Using the backward difference in the discrete-time system, it can be expressed by integrating capacitor current over one switching period from t_{i-1} to t_i as

$$i_{c\_\text{avg}}(t_i) = \frac{1}{T_{\text{sw}}}\int_{t_{i-1}}^{t_i} i_c(t)dt \approx \frac{C_o}{T_{\text{sw}}}[v_o(t_i) - v_o(t_{i-1})] \tag{3}$$

where T_{sw} is the switching period, C_o is the capacitance of the output capacitors, and $i_c(t)$ is the capacitor current. The equivalent series inductance ripple does not appear in (3) since the steps at t_{i-1} and t_i canceled each other.

Beyond the minimum requirement, given that the ADCs have higher sampling rate capability, oversampling can update the i_{c_avg} more frequently to improve the transient response. The average current is still estimated by two samples with one T_{sw} interval, but not two adjacent samples, as shown in (4) and Fig. 3. This arrangement makes the estimated average current insensitive to noise and parameter uncertainty. In the steady state, the average capacitor current estimated by (4) is constant zero without switching ripple. Here, N is the number of samples during one off-time period. T_s is the sampling period of the ADC. If $N = 1$, it degenerates to single sample per switching cycle, i.e., $T_s = T_{\text{sw}}$

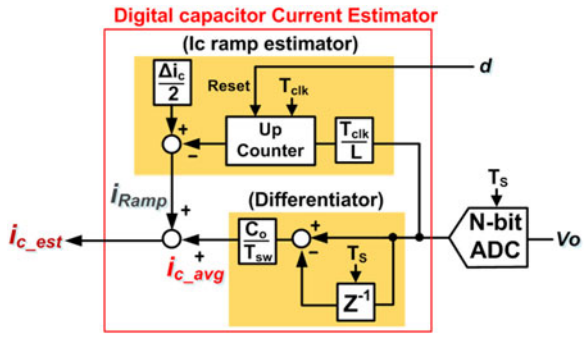

Fig. 4. Block diagram of digital capacitor current estimator.

$$i_{c\_\text{avg}}(t_i + (N-1)T_s) \approx \frac{C_o}{T_{\text{sw}}}[v_o(t_i + (N-1)T_s) - v_o(t_{i-1} + (N-1)T_s)]. \tag{4}$$

According to the preious description, Fig. 4 shows the detailed block diagram of the digital capacitor current estimator. The estimated capacitor current i_{c_est} is the sum of the average value i_{c_avg} in (4) and the ramp function in (2). The ramp generator updates every controller internal clock cycle, so the high-time-resolution summed signal would help to avoid the limit cycle oscillation phenomenon associated with the low-time-resolution ADC.

Compared with the structure with a digital ac inductor current estimator [17], [18], in the proposed scheme, only one ADC is required to sample the output voltage. Unlike the inductor current estimation, the estimated capacitor current is determined by the differentiation of the capacitor voltage, while it is not impacted by the ADC quantization errors and timing errors in the past. The errors do not accumulate and cause the drift problem, so there is no need for additional drift compensation loop.

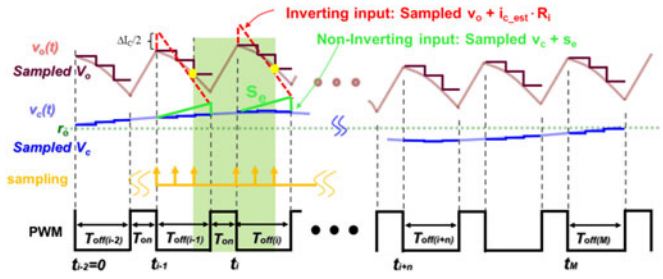

Fig. 5. Perturbed output voltage waveform.

IV. Small-Signal Model and Design Guidelines

A. Small-Signal Model Derivation

The describing function (DF) method is used in the modeling of the proposed digital hybrid ramp V^2 control. It treats the nonlinear closed-loop system as a single entity, which includes the switches, the output voltage feedback, the digital current estimator, the comparator, and the on-time generator [4]. A sinusoidal perturbation with a small magnitude at the frequency f_m is injected to the control signal v_c in Fig. 1. Then, based on the perturbed output voltage waveform, the DF from v_c to v_o is derived. In this derivation, R_{Co} is the ESR of the output capacitors. $T_{\rm on}$ is the fixed on-time.

Four assumptions are made before applying the DF method.

1) The inductor current slopes during the on-period and the off-period stay constant, respectively.
2) The magnitude of the perturbation signal is very small.
3) The perturbation frequency f_m and the switching frequency $f_{\rm sw}$ are commensurable.
4) The quantization errors of the ADC are negligible.

The digital controller system clock frequency is high enough so that the digital signals updated every clock cycle are taken as a continuous time signal.

Following the control law, the modulated duty cycle and the perturbed output voltage waveforms are shown in Fig. 5. Since the on-time $T_{\rm on}$ is fixed, the off-time $T_{\rm off}$ is modulated by the perturbation signal $v_c(t) = r_o + \hat{r}\sin(2\pi f_m \cdot t + \theta)$, where r_o is the steady-state dc value of the control signal, $\hat{r}$ is the magnitude of the perturbation, and θ is the initial angle.

The trip point of the comparator of the proposed hybrid ramp structure is expressed as

$$v_o(t_i + (N-1)T_s) + [i_{c\_\rm avg}(t_i + (N-1)T_s) + i_{\rm Ramp}(t)] \cdot R_i - s_e(t - t_i) = v_c(t_i + (N-1)T_s) \quad (5)$$

where R_i is the current feedback gain and S_e is the external ramp slope.

Using the trip point equation of two adjacent periods, the time-domain equations (6) and (7) are found:

$$v_o(t_i + (N-1)T_s) - v_o(t_{i-1} + (N-1)T_s) = s_n T_{\rm on} - s_f T_{{\rm off}(i-1)} + \frac{1}{C_o}\int_{t_{i-1}+(N-1)T_s}^{t_i+(N-1)T_s}\left(i_L(t) - \frac{v_o(t)}{R_L}\right)dt \quad (6)$$

where $s_n = R_{Co}(V_{\rm in} - V_o)/L$, $s_f = R_{Co}V_o/L$

$$\begin{aligned} &v_o(t_i + (N-1)T_s) - v_o(t_{i-1} + (N-1)T_s) \\ &= [v_c(t_i + (N-1)T_s) - v_c(t_{i-1} + (N-1)T_s)] \\ &\quad - [i_{c\_\rm avg}(t_i + (N-1)T_s) - i_{c\_\rm avg}(t_{i-1} + (N-1)T_s)]R_i \\ &\quad + \frac{V_o}{L}\left(R_i + \frac{s_e}{s_f}R_{Co}\right)(T_{{\rm off}(i)} - T_{{\rm off}(i-1)}). \end{aligned} \quad (7)$$

Then, (6) is substituted into (7) to obtain the expression of off-time as a function of the perturbation signal $v_c(t)$. Then, the modulated duty cycle $d(t)$ and the perturbed inductor current $i_L(t)$ can be expressed by (8) and (9), respectively:

$$d(t) = \sum_{i=1}^{M}[u(t - t_i - T_{{\rm off}(i)}) - u(t - t_i - T_{{\rm off}(i)} - T_{\rm on})] \quad (8)$$

$$i_L(t) = \int_0^t [V_{\rm in}/L_s \cdot d(t) - V_o/L_s]dt + i_{L0} \quad (9)$$

where $u(t) = 1$ when $t > 0$, and i_{L0} is the initial value of the inductor current.

Then, the Fourier analysis can be performed on the inductor current as

$$C_{m(i_L)} = j\frac{2f_m}{MT_{\rm sw}}\int_0^{t_M + T_{{\rm off}(M)} + T_{\rm on}} i_L(t) \cdot e^{-j2\pi f_m t}dt \quad (10)$$

where $c_{m(iL)}$ is the Fourier coefficient at the perturbation frequency f_m for the inductor current.

After that, the Fourier coefficient $c_{m(vo)}$ of the output voltage v_o can be calculated as

$$C_{m(vo)} = C_{m(iL)}\frac{R_L(R_{Co}C_o \cdot j2\pi f_m + 1)}{(R_L + R_{Co})C_o \cdot j2\pi f_m + 1}. \quad (11)$$

Finally, the DF from the control signal to the output voltage in the s-domain can be calculated as

$$\frac{v_o(s)}{v_c(s)} = \frac{f_s}{s_f}\frac{\rm Num(s)}{\rm Denom(s)}(1 - e^{-sT_{\rm on}})\frac{V_{\rm in}}{L_s \cdot s}\frac{R_L(R_{Co}C_o \cdot s + 1)}{(R_{Co} + R_L)C_o \cdot s + 1} \quad (12)$$

where

$$\begin{aligned} {\rm Num}(s) &= \left(1 + \frac{1+\alpha}{sR_LC_o}\right) - \left(1 + \frac{1+2\alpha}{sR_LC_o}\right)e^{-sT_{\rm sw}} \\ &\quad + \frac{\alpha}{sR_LC_o} \cdot e^{-2sT_{\rm sw}} \end{aligned}$$

$$\begin{aligned} {\rm Denom}(s) &= \frac{(R_i + R_e)}{R_{Co}} + \frac{(1+\alpha)(T_{\rm sw} + T_x) - 2(R_i + R_e)C_o}{2C_oR_{Co}} \\ &\quad \times e^{-sT_{\rm sw}} + \frac{T_{\rm sw} - (1+2\alpha)T_x + 2(R_i + R_e)C_o}{2C_oR_{Co}}e^{-2sT_{\rm sw}} \\ &\quad - \frac{\alpha(T_{\rm sw} - T_x)}{2C_oR_{Co}}e^{-3sT_{\rm sw}} \end{aligned}$$

$$T_x = \frac{T_{\rm on}}{2} + 2R_{Co}C_o + (N-1) \cdot T_s$$

$$\alpha = R_iC_o/T_{\rm sw},\ R_e = s_eR_{Co}/S_f.$$

Pade' approximation is used to simplify the transfer function to finite-order form. The poles and zeros beyond the switching frequency are ignored, including the ESR zero of the output

ceramic capacitor and the double pole ω_1. The simplified transfer function that is valid to half of switching frequency is (13). The control-to-output transfer function is a sixth-order transfer function with two stationary, overlapping double zero at half of switching frequency

$$\frac{v_o(s)}{v_c(s)} = \frac{R_{Co}C_o s + 1}{1 + \frac{s}{\omega_1 Q_1} + \frac{s^2}{{\omega_1}^2}} \frac{\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)^2}{\text{Denom}'(s)} \approx \frac{\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)^2}{\text{Denom}'(s)} \tag{13}$$

where

$$\begin{aligned}\text{Denom}'(s) &= 1 + A\left(\frac{s}{\omega_2}\right) + B\left(\frac{s}{\omega_2}\right)^2 + C\left(\frac{s}{\omega_2}\right)^3 \\ &\quad + B\left(\frac{s}{\omega_2}\right)^4 + A\left(\frac{s}{\omega_2}\right)^5 + \left(\frac{s}{\omega_2}\right)^6 \\ A &= \frac{2\alpha T_{\text{sw}} + T_x}{Q_2 T_{\text{sw}}} \\ B &= \frac{2\alpha T_x + 4(R_i + R_e)C_o - (1+2\alpha)T_{\text{sw}}}{{Q_2}^2 T_{\text{sw}}} + 3 \\ C &= 2A - \frac{(1+2\alpha)T_x - 4(R_i + R_e)C_o}{{Q_2}^2 T_{\text{sw}}} \\ \omega_1 &= \pi/T_{\text{on}},\ Q_1 = 2/\pi, \quad \omega_2 = \pi/T_{\text{sw}},\ Q_2 = 2/\pi.\end{aligned}$$

B. Stability Criteria

The denominator in (13) is a sixth-order polynomial. Although it is too complicated to find out an analytical factorized form of it, based on the pole-zero map from the numerical solution, it is found that the system transfer function has three sets of double pole. So, the symbolical factorized form of (13) is rewritten as

$$\frac{v_o(s)}{v_c(s)} \approx \frac{\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)^2}{\left(1 + \frac{s}{Q_{i1}\omega_{i1}} + \frac{s^2}{\omega_{i1}^2}\right)\left(1 + \frac{s}{Q_{i2}\omega_{i2}} + \frac{s^2}{\omega_{i2}^2}\right)\left(1 + \frac{s}{Q_{i3}\omega_{i3}} + \frac{s^2}{\omega_{i3}^2}\right)}. \tag{14}$$

In order to find the stability criteria, the denominator of (14) is expanded and matched with the polynomial form in (13); the expressions of three quality factors are found. It is found that two of them are always positive. Another quality factor, which can be positive and negative, is named as Q_{i3}. The double pole associated Q_{i3} will be called the third double pole in this paper. The Q_{i3} of the third double pole determines the stability of the system. The expression of Q_{i3} is

$$\frac{1}{{Q_{i3}}^3} + \frac{1}{Q_{i3}}(B(R_i, S_e) - 3) - \frac{A(R_i)}{{Q_{i3}}^2} - [C(R_i, S_e) - 2A(R_i)] = 0. \tag{15}$$

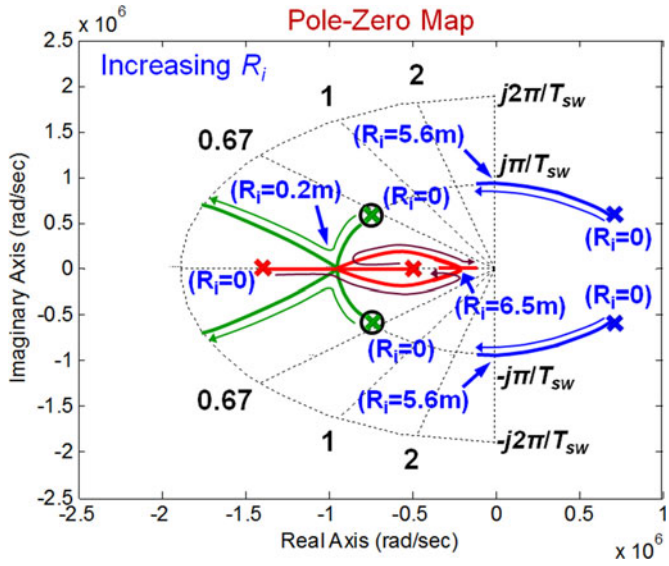

Fig. 6. Pole-zero map of $V_o(s)/V_c(s)$ with an increasing R_i and zero S_e.

The stability boundary condition is $Q_{i3} > 0$. In order to satisfy $Q_{i3} > 0$, based on (15), the stability criterion is derived as

$$R_{eq}C_o - T_x > 0 \tag{16}$$

where $R_{\text{eq}} = (\frac{2}{N} - D - \frac{2R_{Co}C_o}{T_{\text{sw}}})R_i + (\frac{2s_e}{s_f} + 1)R_{Co}$.

The stability criterion (16) is in a similar form of the stability criterion of standard analog V^2 control ($R_{Co}C_o - T_{\text{on}}/2 > 0$), which were derived in [2]–[4]. An equivalent RC time constant associated with the output capacitor is required to be larger than a time constant associated the constant on-time.

C. Pole-Zero Movements and Controller Design Procedure

It is too complicated to find out an analytical factorized form of (13). To better understand the system characteristic and the effect of different current feedback gain (R_i) and external ramp slope (s_e), the pole-zero movements based on the numerical solution are observed. A design example with ceramic capacitors is given: $V_{\text{in}} = 12$ V, $V_o = 1.2$ V, $L = 600$ nH, $T_{\text{on}} = 0.33\ \mu$s, $T_s = T_{\text{sw}}/4$, and the output ceramic capacitors with total capacitance 1200 μF and 117 $\mu\Omega$ ESR.

First, the effect of increasing current feedback gain R_i is observed. The external ramp s_e is zero ($s_e = 0$). The system poles and zeros are plotted in Fig. 6 based on the analytical equation (13). It is found that the sixth-order transfer function contains three sets of double pole, while the first two of them (the green one and the red one in Fig. 6) are always in the left-half plane (LHP). When $R_i = 0\ \Omega$, the system is unstable due to the third double poles (blue) in the right-half plane (RHP). When R_i increases, the third double poles will move toward the LHP along the circle of half of the switching frequency to stabilize the system. Meanwhile, the first double pole (green) in the LHP moves beyond the switching frequency, and the second double pole (red) in the LHP moves into lower frequency and splits into two real poles. The bode plots of the control-to-output transfer functions with different R_i are shown in Fig. 7. From Fig. 7, it is seen that although adding the digital capacitor current ramp can stabilize the system, its side effect is moving a real pole to

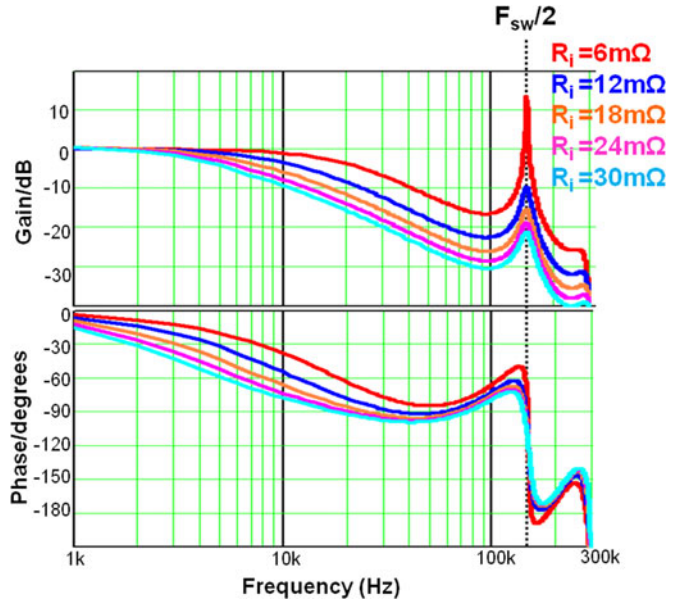

Fig. 7. $v_o(s)/v_c(s)$ with different R_i and zero S_e.

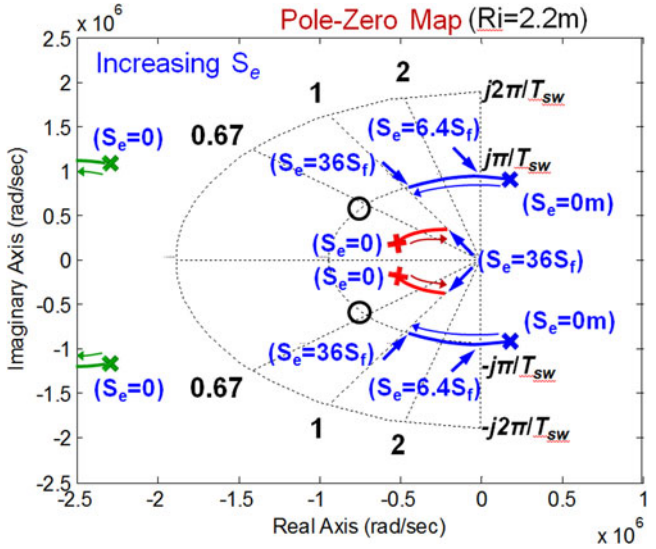

Fig. 8. Pole-zero map of $V_o(s)/V_c(s)$ with an increasing S_e and fixed $R_i = 2.2$ mΩ.

low frequency. This low-frequency dominant pole becomes the bottle neck limiting the system dynamic response.

In order to improve the dynamic performance, an additional external ramp is added to the comparator. The external ramp will help to provide double pole damping with a moderate R_i and avoid the drawback of large R_i. As the external ramp works with capacitor current ramp together, this control scheme is a hybrid ramp compensation architecture.

As mentioned previously, on one hand, increasing the R_i, the second double pole (red in Fig. 6) may generate an undesired low-frequency pole. On the other hand, it is desirable that it pushes the first double pole (green) beyond the frequency range we are interested in. Considering this tradeoff, we have to choose a moderate R_i and add the external ramp to stabilize the system. With the chosen optimal R_i, the first double pole (green) is out of horizon, so within half of switching frequency, the system has been simplified like a fourth-order system.

With the fixed R_i, one can increase the external ramp S_e slope and observe the system poles and zeros movements. Based on (13), the pole-zero movements are plotted in Fig. 8. When $S_e = 0$, the system is unstable, since the third double pole (blue) is in the RHP. When S_e increases, the third double pole will move to the LHP along the circle of half of the switching frequency. In the meantime, the second double pole (red) only slightly moves to lower frequency. Compared with purely increasing R_i, the advantage of adding external ramp is that it does not introduce very low frequency real pole. The bode plots of the control-to-output transfer functions with different external ramp slope S_e are shown in Fig. 9. In contrast to Fig. 7, with the hybrid ramp compensation, the lowest frequency pole in the transfer function is higher than the one with only capacitor current ramp by one order, while the double pole peaking could be well controlled.

In sum, the strategy of designing the hybrid ramp compensation is: first, move the first and second double poles by R_i. Based on the derived small-signal model (13), choose an moderate R_i such that the first double is moved far beyond switching frequency, while the second double pole is still a well-damped complex double pole; second, move the third double pole by S_e. Increase external ramp until the third double pole moves to the LHP and has sufficient damping. In Fig. 9, the orange curve with $R_i = 2.2$ mΩ and $s_e = 17s_f$ is the optimal design.

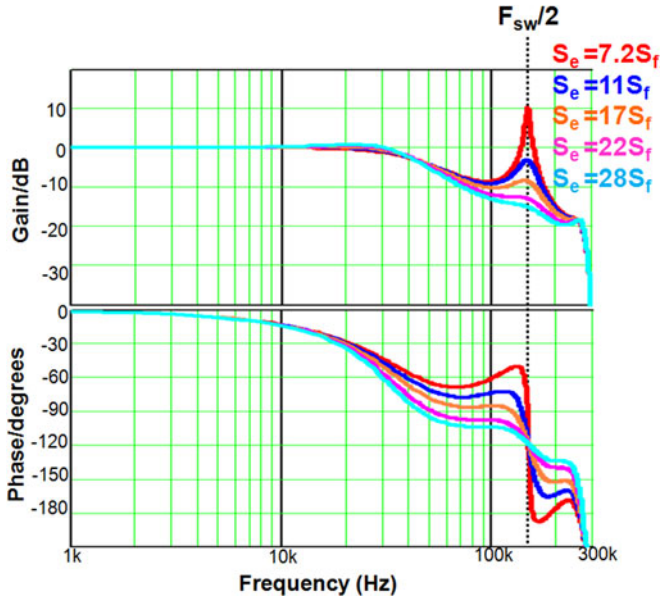

Fig. 9. $V_o(s)/V_c(s)$ with different S_e and fixed $R_i = 2.2$ mΩ.

When the variation of inductance and capacitance are considered, R_i and S_e should be designed for minimum capacitance to ensure the system stability. Fig. 10 shows the impacts of capacitance variation (±30%) and inductance variation (±20%). It is seen that the minimum capacitance determines the maximum Q_{i3} peaking, as smaller capacitance creates larger capacitor voltage ripple feedback and increases Q_{i3}. The inductance variation's impact is negligible.

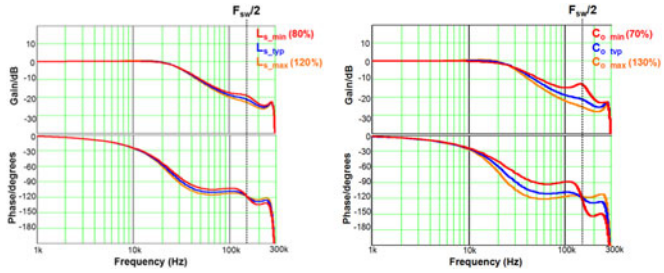

Fig. 10. Impacts of L and C_o variations.

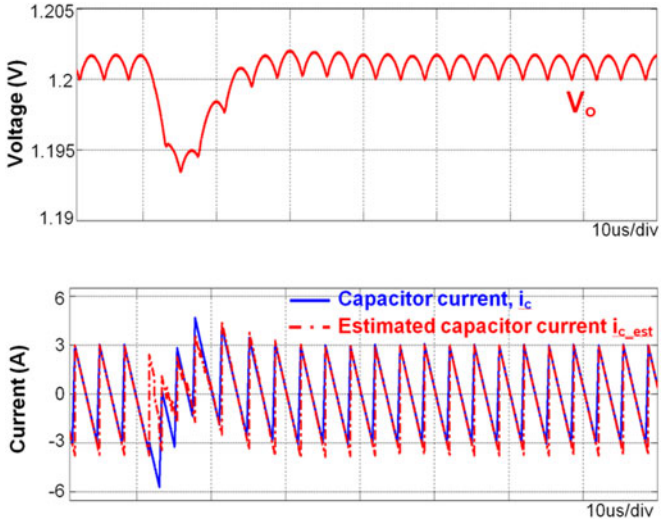

Fig. 11. Performance of current estimation during load step up.

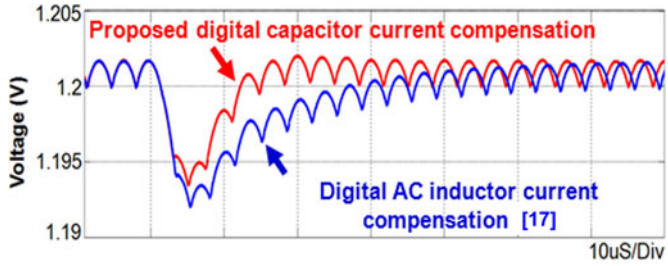

Fig. 12. Simulation comparison of load transient response.

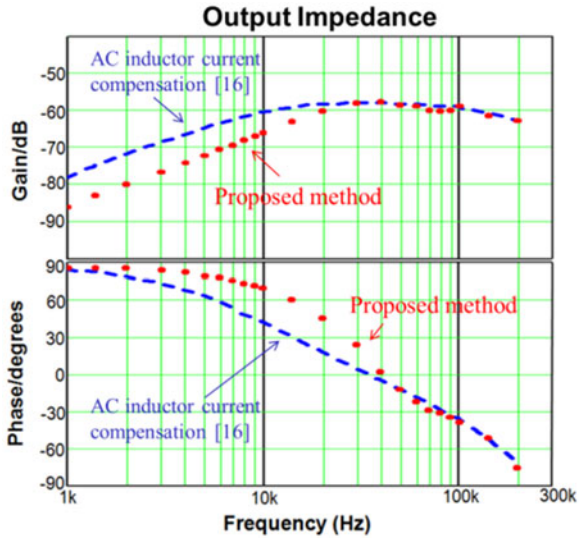

Fig. 13. Simulated output impedance comparison.

V. Simulation and Experimental Verifications

A. Control Scheme Simulational Verification

In order to verify the effectiveness of the proposed structure, simulations are performed on a design example. This design example is a single-phase buck converter with ceramic capacitors, where $V_{\text{in}} = 12$ V, $V_o = 1.2$ V, $L = 600$ nH, $T_{\text{on}} = 0.33$ μs, the output ceramic capacitors with total capacitance 1200 μF and 117 $-$ $\mu\Omega$ ESR. The step load change is from 6 to 12 A.

In Fig. 11, the simulation shows that estimated capacitor current waveform under load step disturbance. Compared with the real-time capacitor current, the estimated capacitor current can follow capacitor current closely except small difference due to sampling delay on initial output voltage change.

In order to demonstrate the benefit of the proposed scheme, Fig. 12 compares the load transient response of the proposed scheme with the digital V^2 control with estimated inductor current compensation [17]. The benchmark is the optimal design from [17], i.e., inductor current gain $R_i = 1.1$ mΩ and $S_e = 7.5S_f$. Sampling period is $T_s = T_{\text{sw}}/5$. The proposed hybrid capacitor current ramp compensation uses the following parameters: capacitor current gain $R_i = 2.2$ mΩ, $S_e = 17S_f$, and sampling period $T_s = T_{\text{sw}}/4$. With a 20% lower sampling rate, as shown in Fig. 12, the proposed method reduces the undershoot by 10% and shortens the settling time by 50%.

The performance difference shown in Fig. 12 can also be explained by the output impedance comparison shown in Fig. 13. Compared with digital inductor current ramp compensation, the proposed hybrid capacitor current compensation has much lower impendence up to 30 kHz.

B. Small-Signal Model Verification

In order to verify the validation of the proposed small-signal model, simulated Bode plots on the control-to-output transfer function are compared with modeling result (13). As shown in Fig. 14, the proposed model can accurately predict the control-to-output transfer function up to half of switching frequency.

C. Experimental Verification on a Field-Programmable Gate Array (FPGA) Platform

An FPGA-based experimental platform (see Fig. 15) is set up for experiments. The components used for the prototype design are summarized in Table I.

Fig. 16 shows the measured estimated capacitor current waveform, which is read from the GUI. It closely follows the real-time capacitor current, which is calculated by the FPGA based on the sensed inductor current i_L and load current i_o. The relationship is $i_c = i_L - i_o$. Fig. 17 shows the experimental result of output voltage load step transient response. It takes only two switching

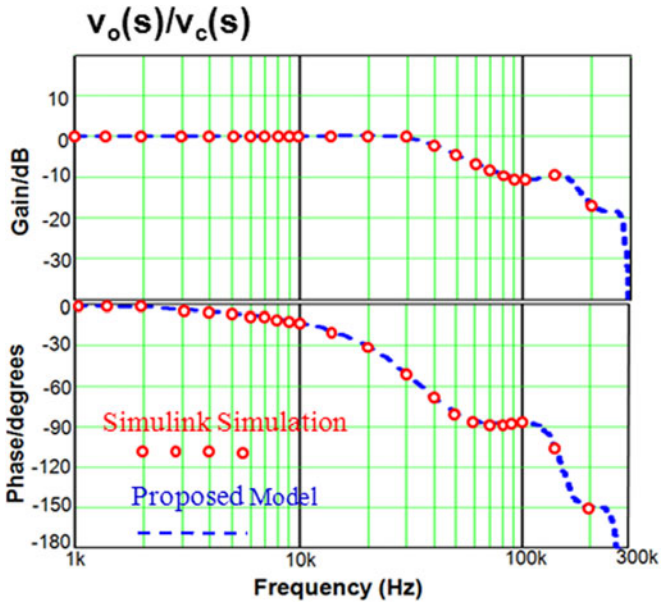

Fig. 14. Small-signal transfer function $v_o(s)/v_c(s)$ verification ($V_{\text{in}} = 12$ V, $V_o = 1.2$ V, $L = 600$ nH, $T_{\text{on}} = 0.33$ μs, $C_o = 1200$ μF, and ESR is 117 $\mu\Omega$. $T_s = T_{\text{sw}}/4$, $R_i = 2.2$ mΩ, and $S_e = 17S_f$).

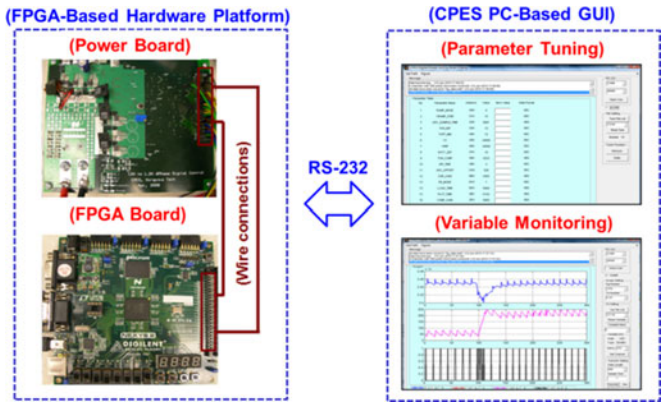

Fig. 15. FPGA-based hardware platform and GUI.

TABLE I
PARTS USED IN THE FABRICATION OF THE PROTOTYPE

Parts	Attributes	Manufacturer
MOSFETs	HAT2164H	Renesas
Inductor	SER1590-601ML, 600 nH	Coilcraft
Output capacitor	GRM31CR60J107M, 100 μF x 12	Murata
ADC IC	10-bit, 2-mV resolution, AD9200	ADI
FPGA controller	Spartan-3E FPGA, 50-MHz system clock rate	Xilinx

actions to recover from the undershoot. Compared with the digital inductor current compensation [17], the proposed control scheme has 70% reduction on settling time and 20% reduction on undershoot deviation. The benchmark setup is exactly the same the one described in [17].

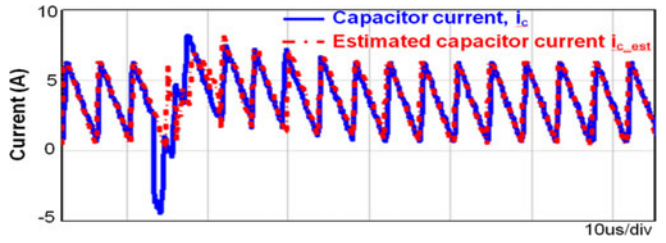

Fig. 16. Measurement of the estimated capacitor current waveform during load step up.

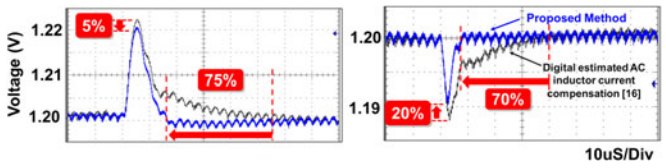

Fig. 17. Measurement and comparison of load transient response.

VI. CONCLUSION

This paper proposes a hybrid capacitor current ramp compensation method for digital V^2 control and provides an implementation of a digital capacitor current estimator. To achieve good dynamic performance, the proposed control scheme uses the combination of the estimated current ramp and the external ramp for V^2-controlled Buck converter with a small-time-constant output capacitor. Compared with the digital inductor current estimator with two ADCs and an additional drift compensation loop, the capacitor current estimator is simpler and has faster transient response.

For design purpose, the small-signal model for the proposed control architecture is derived. The design guidelines and stability criteria are presented. The effectiveness of the proposed control structure and the current ramp estimator are verified by the simulation and experimental results. The proposed scheme shows better dynamic performance than the V^2 control with digital inductor current ramp compensation, with 70% reduction on settling time and 20% reduction on undershoot deviation.

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