Letters

Development of a New Hybrid Multilevel Inverter Using Modified Carrier SPWM Switching Strategy

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***Abstract*—This letter presents a single-phase cascaded transformer based multilevel inverter with a modified carrier-based level shift sinusoidal pulse width modulation (LS-SPWM) technique. The developed topology has two bridges with individual low frequency transformers. The bridges can generate quasi-square waveform and pulse width modulated waveform independently and energized the two transformers whose secondary terminals are cascaded to attain 19-level output voltage waveform across the load. The anticipated configuration has the least number of components to reduce the cost and enhance the reliability of the converter for medium power applications with inbuilt isolation. Furthermore, this letter presents the most common LS-SPWM technique with a new carrier to enhance the fundamental magnitude and shifts the dominant harmonics into three times of the traditional strategy for the same modulation indices. The performance of the proposed topology is validated with experimental results.**

***Index Terms*—Carrier-based pulse width modulation, multilevel inverter (MLI), total harmonic distortion (THD).**

I. Introduction

In RECENT past, multilevel Inverters (MLIs) are considered as the most important power converter for various applications, such as power-active filters, ac traction, direct grid integration systems, electric vehicles, etc. In reality, the quality of multilevel output voltage waveform is enriched as the number of levels moving high. Moreover, an appropriate switching strategy raises their potentiality in terms of good power factor, smaller filter size, improved efficiency, less voltage stress on power devices, and reduce energy waste. In current scenario, diode clamped MLI, flying capacitor MLI, and cascaded MLI are drawn more attention to accomplish the above-mentioned applications. However, to obtain the desired number of output voltage levels by using minimum number of dc sources, switching components, and axillary devices become a hectic job. In this perspective, many new inverter configurations with a claim of less device count are suggested in the literature [1], [2]. In [3], the author suggested a cascaded transformer-based MLI with single dc supply. Herein, all H-bridges are connected to individual transformers to attain optimal output voltage levels. However, it has drawn a huge number of switches and heavy weight transformers. It is addressed in [4] and [5] by replacing the H-bridges with a new arrangement of semiconductor switches. Additionally, the transformer-based MLIs are very much suitable for medium and high power applications [6]. At the same time, other kind of MLIs like asymmetrical or hybrid archetype utilizes an isolated dc supplies and capacitors to get desired multilevel output waveforms. In terms of device concerns, the asymmetrical topologies proposed in [7]–[9] are highly concentrated to diminish the size of the converter by decreasing the switch count. However, these configurations have to overcome the issues, like high design cost, loss of modularity, and charge balancing issues across the input capacitor. Therefore, the improvement is still needed in transformer and non-transformer based topologies. Later on, the selection of suitable switching strategy for a MLI can be treated as a challenging effort from the existed control techniques [10]. Owing to the traditional control techniques have their limitations like:

1) complex to design and implement (in space vector pulse width modulation (SVPWM)) when levels exceed more than five;
2) initial guess (in selective harmonic elimination (SHE)) plays a major role in Newton–Raphson method to calculate the switching angles;
3) a wide sideband harmonics are existed in sinusoidal pulse width modulation (SPWM) technique.

To mitigate aforementioned problems, we proposed a novel carrier-based SPWM technique for a new hybrid MLI. The basic intention behind the implementation of a new control technique is to improve the magnitude and harmonic profile of the load voltage. The recommended topology has the capacity to boost up the number of output voltage steps using only 12 power switches, two dc sources results in reduced gate driver circuits and power supplies. Further, two single-phase transformers are used in the presented topology to minimize the voltage stress on switching devices and provides isolation between supply and load. The working principle of the proposed configuration and superiority of the new pulse width modulated (PWM) technique

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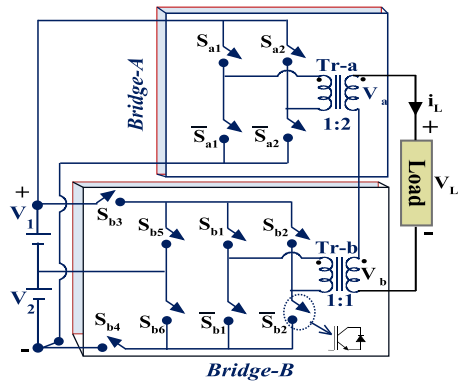

Fig. 1. Schematic of the proposed 19-level inverter.

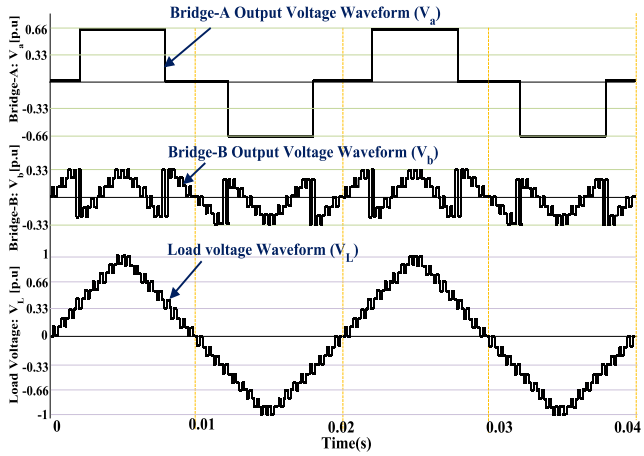

Fig. 2. Key voltage waveforms of the proposed topology.

is presented in Section II. Hardware results and comprehensive comparison among the most recent configuration is carried out in Section III. Conclusions are drawn in Section IV.

II. Proposed 19L-Inverter Configuration

A. Proposed Topology Operating Principle

The proposed single-phase topology is shown in Fig. 1. It contains mainly two bridges. Bridge-A is a traditional H-bridge inverter generates three-level voltage waveform. Bridge-B is a PWM inverter built with an H-bridge and four individual switches. The main idea under the utilization of the transformers in both bridges (Tr-a and Tr-b) are to accomplish a maximum number of levels without using additional switches and individual dc supplies. Thereby, reduction in device count leads the better efficiency, reliability, and economical improvement in the proposed circuit. Herein, all switches are bidirectional current and unipolar voltage switches. An antiparallel diode (D) of the switch conducts only for allowing negative current through it and the insulated-gate bipolar transistor (IGBT) (sw) is conducted to permit the positive current. Regarding the input dc supply, the magnitude of input dc source V_1 selected as twice the magnitude of the dc source V_2. The selection of the dc sources is essential since it decides the number of output levels. In proposed topology, the transformer ratios are 1:2 and 1:1. Thus, the dc supplies are fixed to 2:1 ratio to realize 19-level output voltage waveform. Moreover, the load current and the secondary currents of the transformers should be the same, since the secondaries of the two transformers are shorted through the load. In fact, the primary current waveforms of the transformers are accomplished 19-levels even though primary voltages are different and these can be observed for resistive loads as shown in Fig. 2. Thereafter, individual switching states of the proposed topology are exposed in Table I. Let us consider $V_{\rm dc}$ is equal to the magnitude of V_2 (input dc source).

1) First state: this level is designated as 1L, switches S_{a1}, S_{a2} of Bridge-A and S_{b1}, $\overline{S_{b2}}$, S_{b4}, and S_{b5} of Bridge-B are ON, Thus, the load voltage $V_L = 0 + V_2 = V_{\rm dc}$.
2) Second state (2L): Switches S_{a1}, S_{a2} of Bridge-A are connected to short the transformer-A primary windings and S_{b1}, $\overline{S_{b2}}$, S_{b3}, and S_{b6} of Bridge-B are ON, then V_1 dc source is connected to the Bridge-B, Thereby, voltage across the load becomes $V_L = 0 + V_1 = 2V_{\rm dc}$.
3) Third state (3L): Switches S_{a1} and S_{a2} of Bridge-A are connected to short the transformer-A primary windings and then S_{b1}, $\overline{S_{b2}}$, S_{b3}, and S_{b4} of Bridge-B are ON, V_1 and V_2 dc sources are connected to the Bridge-B, therefore, voltage across the load is $V_L = V_1 + V_2 = 3\,V_{\rm dc}$.
4) Fourth state (4L): from this state the Bridge-A starts to share the load power. Switches S_{a1}, $\overline{S_{a2}}$ of Bridge-A and $\overline{S_{b1}}$, S_{b2}, S_{b3}, and S_{b6} of Bridge-B are ON, thus, the load voltage $V_L = 2(V_1 + V_2) + (-V_1) = 6\,V_{\rm dc} - 2\,V_{\rm dc} = 4\,V_{\rm dc}$. The Bridge-A output peak voltage magnitude is increased from $3\,V_{\rm dc}$ to $6\,V_{\rm dc}$ since the turn's ratios of Tr-a is considered as 1:2.
5) Fifth state (5L): Switches S_{a1}, $\overline{S_{a2}}$ of Bridge-A and $\overline{S_{b1}}$, S_{b2}, S_{b4}, and S_{b5} of Bridge-B are ON, Thus, the load voltage $V_L = 2(V_1 + V_2) + (-V_2) = 6\,V_{\rm dc} - 1\,V_{\rm dc} = 5\,V_{\rm dc}$.
6) Six state (6L): Switches S_{a1}, $\overline{S_{a2}}$ of Bridge-A and S_{b1}, S_{b2} of Bridge-B is activated. Thus, the load voltage $V_L = 2(V_1 + V_2) + 0 = 6\,V_{\rm dc}$.
7) Seventh state (7L): Switches S_{a1}, $\overline{S_{a2}}$ of Bridge-A and S_{b1}, $\overline{S_{b2}}$, S_{b4}, S_{b5} of Bridge-B are ON, Then the voltage across the load is $V_L = 2(V_1 + V_2) + V_2 = 6\,V_{\rm dc} + 1\,V_{\rm dc} = 7\,V_{\rm dc}$.

TABLE I
Triggering States of the Proposed Topology

V_L	S_{a1}	S_{a2}	V_a	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{b5}	S_{b6}	$\boldsymbol{V_b}$
1L	sw	D	***0***	sw	0	0	sw	D	0	***L***
2L	sw	D	***0***	sw	0	sw	0	0	D	***2L***
3L	sw	D	***0***	sw	0	sw	sw	0	0	***3L***
4L	sw	0	***6L***	0	D	D	0	0	sw	***−2L***
5L	sw	0	***6L***	0	D	0	D	sw	0	***−L***
6L	sw	0	***6L***	sw	D	0	0	0	0	***0***
7L	sw	0	***6L***	sw	0	0	sw	D	0	***L***
8L	sw	0	***6L***	sw	0	sw	0	0	D	***2L***
9L	sw	0	***6L***	sw	0	sw	sw	0	0	***3L***
0	sw	D	***0***	sw	D	0	0	0	0	***0***

Bold text represents only voltage level of the corresponding bridges.

8) Eighth state (8L): Switches S_{a1}, $\overline{S_{a2}}$ of Bridge-A and S_{b1}, $\overline{S_{b2}}$, S_{b3}, and S_{b6} of Bridge-B are ON, Thus, a voltage across the load is $V_L = 2(V_1 + V_2) + V_2 = 6\,V_{\rm dc} + 2\,V_{\rm dc} = 8\,V_{\rm dc}$.
9) Ninth state (9L): Switches S_{a1}, $\overline{S_{a2}}$ of Bridge-A and S_{b1}, $\overline{S_{b2}}$, S_{b3}, and S_{b4} of Bridge-B are ON, Thus, a voltage across the load is $V_L = 2(V_1 + V_2) + (V_1 + V_2) = 6\,V_{\rm dc} + 3\,V_{\rm dc} = 9\,V_{\rm dc}$.
10) Zeroth State (0L): this state can achieve in different combinations, herein, switches S_{a1} and S_{a2} of Bridge-A and S_{b1}, S_{b2} of Bridge-B are ON to generate zeroth load voltage state.

Similarly, the negative states of the load voltage waveform are created with appropriate changes. Bridge-B operated at PWM mode and Bridge-A is modulated with the fundamental frequency. The basic idea behind this type of operation is to reduce overall conduction and switching losses of the proposed topology.

B. Proposed Switching Scheme

The proposed switching strategy comes under the level shift pulse width modulation technique (LS-PWM) family. According to the phase position of the carrier waveforms, LS-PWM strategies are categorized into three types [11]. Herein, the proposed topology is switched with the phase opposition disposition (POD) PWM technique. Basically, triangle and ramp signals are used as carrier waveforms in the entire carrier-based switching techniques. Furthermore, the carrier frequency ($f_{\rm cr}$) normally kept high to curtail the lower order harmonics. However, the switching and EMI issues severely affect the operation and control of the converter for higher $f_{\rm cr}$ value. To address aforementioned problems a new carrier is introduced. Here, the proposed carrier operates with lower $f_{\rm cr}$ to suppress the wide range of lower order harmonics than traditional carrier-based techniques. The present section demonstrates the proposed technique in detailed.

Let us assume carrier frequency is too higher, and then the sine reference signal ($V_{\rm ref}$) seen by the carrier waveform is a constant dc signal. It is illustrated in Fig. 3(a). Actually, selection of the carrier count is directly related to the number of levels. Herein, the 19-level output waveform is accomplished with 18 carrier signals. In fact, any multilevel voltage waveform is mathematically expressed in terms of dc offsets, fundamental and its sideband harmonics, and carrier harmonics and its sideband harmonics [12]:

$$V(t) = \frac{A_{00}}{2} + \sum_{q=1}^{\infty}\{A_{0q}\cos(q\omega_0 t) + B_{0q}\sin(q\omega_0 t)\} + \sum_{p=1}^{\infty}\{A_{p0}\cos(p\omega_c t) + B_{p0}\sin(p\omega_c t)\} + \sum_{p=1}^{\infty}\sum_{\substack{q=-\infty \\ q\neq 0}}^{\infty}\{A_{pq}\cos(p\omega_c t + q\omega_0 t) + B_{pq}\sin(p\omega_c t + q\omega_0 t)\}. \quad (1)$$

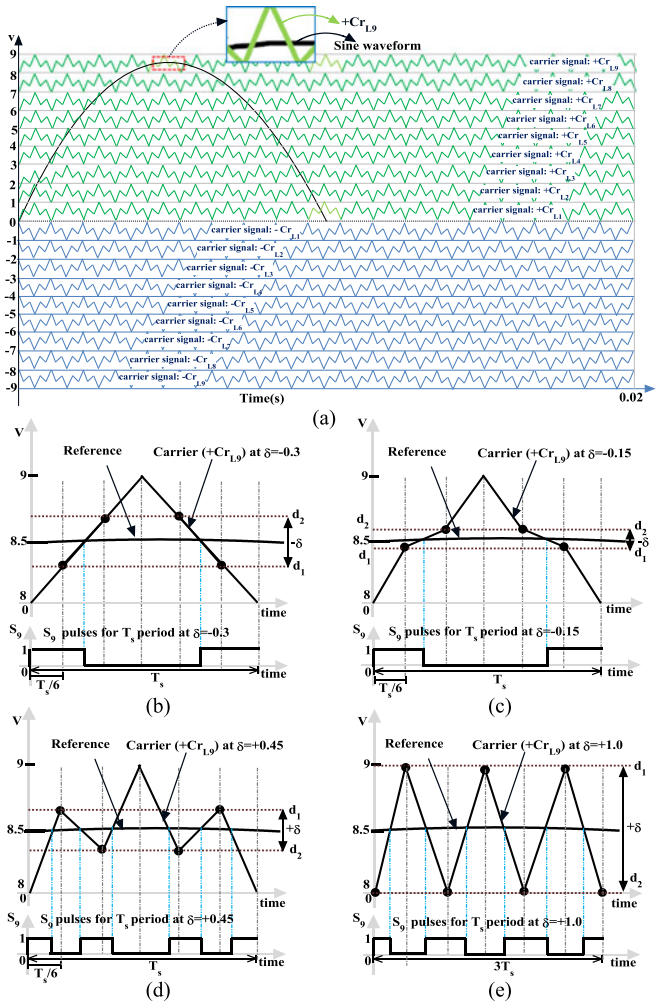

Fig. 3. (a) Schematic arrangement of the POD-PWM strategy with proposed carrier and sinusoidal reference waveforms; (b) S_9 pulse generation for the carrier constraints $m_f = 20$ and delta $= -0.3$; (c) S_9 pulse generation for the carrier constraints $m_f = 20$ and delta $= -0.15$; (d) S_9 pulse generation for the carrier constraints $m_f = 20$ and delta $= +0.45$; (e) S_9 pulse generation for the carrier constraints $m_f = 60$ and delta $= +1$.

The coefficients of (1) are obtained for the general PWM strategy by calculating the double Fourier integral of

$$A_{\rm pq} + jB_{\rm pq} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} V(y,z)e^{j(\rm py\,+\,qz)}dydz \quad (2)$$

where $y = \omega_c t;\ z = \omega_0 t$.

Therefore, the carrier shape can decides the existence of the harmonics in the multilevel output waveform. The proposed carrier is discovered from the center aligned carrier so called triangular waveform without changing the peak-to-peak magnitude and frequency of the carrier wave.

Consider the triangle waveform with the frequency $1/T_s$ that splits equally into six parts by the time scale $T_s/6$, which is shown in Fig. 3(b). The carrier and reference waveforms consider in Fig. 3(b) can generate the positive 9th-level switching pulses S_9. Similarly, other carrier waveforms shown in Fig. 3(a) are compared with a reference waveform to produce pulses for remaining output levels. The positive slope of the carrier (first half-time period of the triangle) intersects the voltage

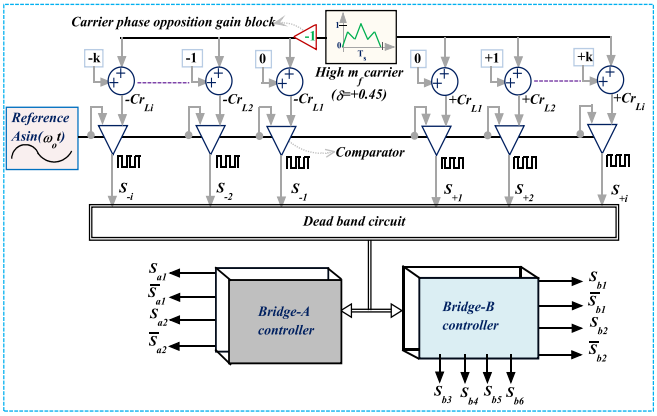

Fig. 4. Implementation of the proposed control technique for the 19-level configuration.

magnitude lines d_1 and d_2 at the T_s/6 and $2T_s$/6 timing instants. The difference between the two cross-over points is noted as delta (δ):

$$\delta = d_1 - d_2. \tag{3}$$

If the magnitude of δ varies, then the number of pulses and the width of the chops are altered accordingly. It can be demonstrated in Fig. 3(b)–(e). Primarily, the polarity of δ is negative, i.e., -0.3, and S_9 has only two pulses. In the second case, also, the polarity is negative ($\delta = -0.15$), but the width of S_9 pulses is different. In the third stage, δ is a positive value ($\delta = +0.45$) and the number of hitting instants with reference waveform is higher, which leads to getting more number of chops without changing the carrier frequency (it is still $1/T_s$). But the carrier frequency becomes triple whenever δ reaches to magnitude one ($\delta = +1$), as shown in Fig. 3(e). Thus, it can be concluded that the number of chops per carrier period depends on the polarity of the delta. In other sense, S_9 can get more number of chopped pulses for positive δ values. Furthermore, the positive delta decreases harmonic content as well as increases the fundamental magnitude of the output voltage.

The implementation of the proposed POD-PWM strategy to trigger Bridge-A and Bridge-B of the developed configuration is depicted in Fig. 4. To build the 19-level output waveform through the LS-PWM strategy, 18 carrier waveforms are needed. Herein, positive nine carrier waveforms (from $+\mathrm{Cr}_{L1}$ to $+\mathrm{Cr}_{L9}$) are out of phase with negative nine carrier waveforms (from $-\mathrm{Cr}_{L1}$ to $-\mathrm{Cr}_{L9}$). As a matter of fact, all carrier waveforms are established with only one carrier waveform. Initial driving pulses are delivered from the comparator that compares the fundamental sinusoidal reference waveform with the proposed carrier waveforms. Later, the dead band circuit is dedicated to avoiding the shoot through faults between the complementary switches. Finally, the actual gate pulses of the bridges (S_{a1}, S_{a2}, S_{b1}, S_{b2}, etc.) are developed by proper logical combination among the initial driving pulses (from S_{-9} to S_{+9}).

Table II describes an effect of the factors like % THD (total harmonic distortion), peak magnitude (V_p), and dominant harmonic (n) of the 19-level output voltage waveform by changing delta magnitudes at $m_a = 1$, $m_f = 20$, $V_2 = 36$ V, and $V_1 = 72$ V. Actually, inverter constraints are varying with the magnitude of δ and three remarkable cases are observed at $\delta = -0.3$, 0.45, and 1.

TABLE II
PERFORMANCE OF THE PROPOSED INVERTER BY CHANGING THE DELTA

δ	THD (%)	V_p (V)	h_{domin} (n)	Shape of the carrier
−0.3	5.97	327.7	21,19	Triangle ($m_f = 20$)
−0.15	5.66	328	21, 19	–
0.15	5.05	328.1	21, 19	–
0.3	5.13	327.2	21, 61	–
0.45	5.29	326.3	61, 59	Proposed ($\boldsymbol{m_f = 20}$)
0.6	5.37	325.5	59, 61	–
0.75	5.50	325	59, 61	–
0.9	5.64	324.4	59, 61	–
1	5.67	324.8	59, 61	Triangle ($m_f = 3 * 20$)

Bold text represents only parameters of the proposed carrier.

TABLE III
DEVICE COUNT OF THE PROPOSED TOPOLOGY WITH OTHER STRUCTURES

Factors	[3]	[4]	[5]	[8]	[9]	Proposed
Number of levels	11	19	19	19	15	19
Number of dc-sources	1	1	1	5	3	2
Number of IGBT-switches	12	20	20	14	12	12
Gate drivers	12	20	20	14	12	12
PIV	$1\,V_{dc}$	$9\,V_{dc}$	$1\,V_{dc}$	$9\,V_{dc}$	$7\,V_{dc}$	$3\,V_{dc}$
Number of Transformers	3	9	9	0	0	2

Case 1 ($\delta = -0.3$):

This case is treated as conventional carrier-based PWM technique since the carrier shape a triangle. The fundamental peak of load voltage (V_p) is 327.7 V and the dominant harmonics are 21st and 19th orders at 1 kHz switching frequency.

Case 2 ($\delta = 0.45$):

In this case, output waveform attains better THD than case-1 i.e., 5.29%. Moreover, the carrier frequency is still 1 kHz but the dominant harmonics are shifted to 61st, 59th order. Thereby, cost of the load side filter is drop down effectively.

Case 3 ($\delta = 1$):

It also treated as a traditional carrier-based PWM technique since the carrier shape is a triangle. Even though the given carrier frequency is 1 kHz, the switching frequency becomes triple due to the delta magnitude is +1. Furthermore, the V_p is lesser compared with case-2 and switching stresses are high.

Thereby, the carrier waveform presented in case-2 has prominent features as follows: reduction in switching and conduction losses (P_{sw} and P_c); improves the FFT spectrum; rise in peak magnitude of the load voltage; and diminish the filter size. These features make the system into more efficient than traditional LSPWM technique.

C. Comparative Study of the Proposed Topology

The performance of the proposed topology is determined in Table III by comparing with recent asymmetrical/hybrid MLIs

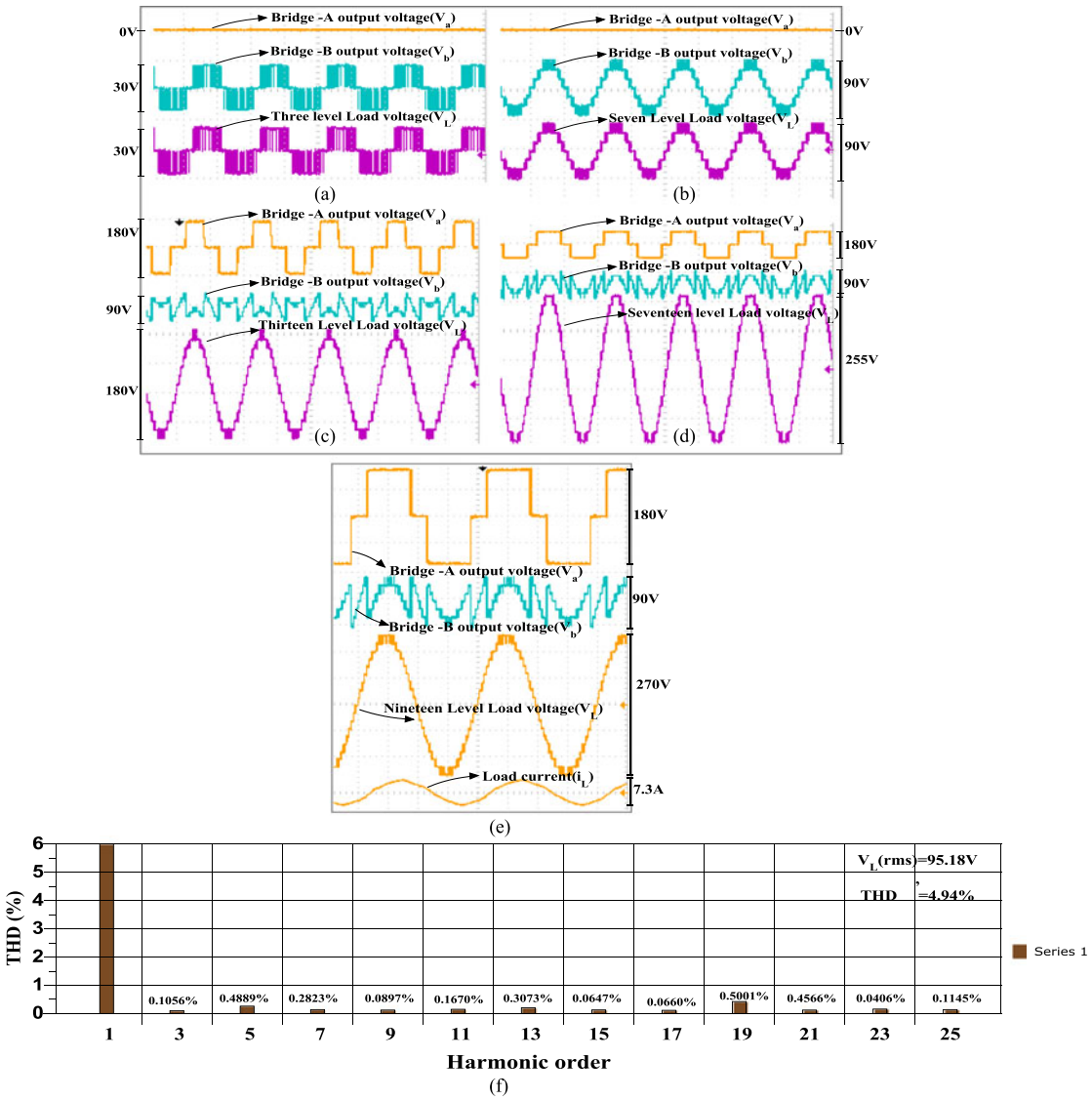

Fig. 5. Hardware results: (a) Bridge-A output voltage (V_a), Bridge-B output voltage (V_b) and load voltage (V_L) at $m_a = 0.085$; (b) Bridge-A, Bridge-B and load voltages at $m_a = 0.25$; (c) Bridge-A, Bridge-B and load voltages at $m_a = 0.52$; (d) Bridge-A, Bridge-B and load voltages at $m_a = 0.81$; (e) Bridge-A, Bridge-B and load across voltages, load current (i_L) waveforms at $m_a = 1$; (f) FFT spectrum for load voltage (V_L) at $m_a = 1$.

are presented in terms of switch count, number of transformers, dc supplies, and peak inverse voltage (PIV), etc.

III. Results and Discussion

To confirm the validity of the proposed topology with suggested switching technique, an experimental setup is constructed with SKM75GB123D half bridge IGBT modules, two linear cold rolled non-grain oriented (CRNGO) core transformers (Tr.1: 200VA, Tr.2: 100VA), and two channel Aplab dual dc power supply that provides two input dc sources ($V_1 = 30$ V and $V_2 = 15$ V), moreover, an appropriate gate driver circuits are built by TLP- 250 optocouplers. Further, the OP5142-RT simulator merely considered as a controller running with simulation time 50e-6 and the operating switching frequency is 1.5 KHz. The load parameters are considered as $R = 36\,\Omega$ and $L = 70$ mH to evaluate the presented topology.

Fig. 5(a)–(d) describes of Bridge-A, Bridge-B output voltages, and load voltage when modulation index m_a changes. The Bridge-A starts to feed the load when $m_a > 0.3$. It is evident that, as m_a changes, the power sharing between the bridges will vary [3]. In the presented configuration, the power sharing of the transformer are distributed as 78% of the transformer-a, and 22% of the transformer-b at the rated load conditions. Further, important issues about transformers when fed with low frequency waveform create heating issues. This further effects efficiency of a converter. However, if winding currents are sinusoidal then extra losses can be minimized. On the other side, presence of the transformer in the proposed design ensures the following: less voltage and current rating switches; drastically minimizes voltage stresses; eliminates higher order harmonics; provides inbuilt isolation; and matches the voltages between source and line [13]. Next, an experimental 19-level load voltage, load current, and corresponding bridge voltages

for $m_a = 1$ are shown in Fig. 5(e), where 180 V, 90 V, 270 V, and 7.3 A are the peak-peak magnitudes of V_a, V_b, V_L, and i_L, respectively. The harmonic spectrum of the load voltage is displayed in Fig. 5(f); herein, the load voltage has achieved 4.97% THD without any additional filter.

IV. Conclusion

In the present letter, a novel hybrid multilevel inverter is recommended to verify the performance of the proposed carrier-based LSPWM technique. The recommended topology is achieved 19-level PWM output waveform with only two bridges. The bridge outputs are connected to the line frequency transformers that provide isolation between the load and dc supply. The proposed topology is extremely suitable for active filters, var compensators, and grid connected systems. Additionally, the proposed switching technique plays a significant role to improve the FFT spectrum of the output waveform with less switching frequency. Moreover, it it can apply to all hybrid and asymmetrical topologies.

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