An Extremely High Efficient Three-Level Active Neutral-Point-Clamped Converter Comprising SiC and Si Hybrid Power Stages

Qing-Xin Guan, *Student Member, IEEE*, Chushan Li, *Member, IEEE*, Yu Zhang, *Member, IEEE*, Shuai Wang, *Member, IEEE*, Dewei (David) Xu, *Member, IEEE*, Wuhua Li, *Member, IEEE*, and Hao Ma, *Member, IEEE*

***Abstract*—Three-level converters typically feature low switching loss and small filter size. In order to realize a high-power-density design for three-level converters, SiC MOSFETs may be selected instead of using Si insulated-gate bipolar transistors. However, all-SiC-MOSFET-based converters suffer from extremely high total cost. In this paper, a SiC MOSFET and Si device hybrid active neutral-point-clamped (ANPC) converter is proposed. It consists of four Si active switches and only two SiC MOSFETs. Thus, it has lower total cost compared to the all-SiC-MOSFET-based ANPC converter. Furthermore, a dedicated modulation scheme is proposed to completely move all the switching events from Si devices to SiC MOSFETs by using redundant switching states. As a result, the switching losses are significantly reduced and extremely high efficiency is achieved. The proposed converter has fully utilized the low-switching-loss advantage of SiC MOSFETs and the low-cost advantage of Si devices, which shows significant superiority in high-end grid-connected inverter and rectifier applications.**

***Index Terms*—Active neutral point clamped (ANPC), hybrid power stage, multilevel converter, neutral point clamped (NPC), SiC.**

I. Introduction

MULTILEVEL converters are industry standard solutions to realize ac–dc or dc–ac power conversion in high-power applications. They have been applied to medium-voltage drive systems, wind energy generation systems, photovoltaic generation systems, battery charging systems for electric vehicles, and power supplies for modern data centers. The three-level (3L) type is one of the most popular choices in the family of multilevel converters. Compared with two-level (2L) converters, 3L converters have lower switching losses. The ac-side filter size is also smaller because the ac-side voltage of a 3L inverter has a lower harmonic content [1].

Among all the existing 3L converter topologies, the "T-type" converter (T^2C) [1]–[5] and the neutral point clamped (NPC) converter [6]–[7] are the two most popular topologies. The single-phase circuits of these two topologies are shown in Fig. 1(a) and (b). The advantages and disadvantages of these topologies have already been thoroughly investigated in previous literature studies. Comparative works can be found in [8] and [9]. It is shown that the T^2C tends to have lower conduction losses, since it has only one device (Q_1 or Q_2) in the current path when the output voltage level is "1" or "–1". However, it has higher switching losses, since the voltage rating of this one device should block the full dc-link voltage. On the contrary, the NPC converter has higher conduction losses, since the current always flow through two devices regardless of the voltage level. But the switching losses are lower because these two devices only require blocking half of the dc-link voltage. According to the comparison, the T^2C is more favorable in applications that require lower switching frequency, while NPC inverters become more advantageous at the higher switching frequency.

The main drawback of the NPC converter is the uneven device loss distribution [7]. This will lead to unequal junction temperature rise and straightly limited the power rating and maximum switching frequency of the converter. In order to solve this, the active NPC (ANPC) converter is proposed, which introduces active switches to replace the clamping diodes in NPC. The schematic of a single-phase ANPC circuit is shown in Fig. 1(c). Although more active switches are used, it has more redundant switching states, which can help to balance the loss distribution [10]–[16]. Furthermore, a number of improved topologies such as the stacked NPC (SNPC) and active SNPC [17]–[19] are proposed aiming to the same problem. These topologies have more degrees of freedom, and the maximum switching loss on each switch can be reduced. The essence of these topologies is to actively distribute the power losses to make the temperature rise on each device become even.

Manuscript received May 29, 2017; revised August 22, 2017 and November 5, 2017; accepted December 4, 2017. Date of publication December 20, 2017; date of current version July 15, 2018. This work was supported by the National Nature Science Foundations of China under Grant 51490682 and Grant 51677166 and the Zhejiang Provincial Natural Science Foundation under Grant LR16E070001. This work was also supported by the China Scholarship Council. Recommended for publication by Associate Editor J. Rabkowski. *(Corresponding author: Chushan Li.)*

Q.-X. Guan and Y. Zhang are with the State Key Laboratory of Advanced Electromagnetic Engineering and Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430073, China (e-mail: guanqingxin@hust.edu.cn; zyu1126@hust.edu.cn).

C. Li and H. Ma are with the Zhejiang University–University of Illinois at Urbana-Champaign Institute, Zhejiang University, Hangzhou 310058, China (e-mail: lichushan@hotmail.com; mahao@zju.edu.cn).

S. Wang and D. (D.) Xu are with Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON M5B 2K3, Canada (e-mail: wangshuai@ryerson.ca; dxu@ryerson.ca).

W. Li is with College of Electrical Engineering, Zhejiang University, Hangzhou 310058, China (e-mail: woohualee@zju.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2784821

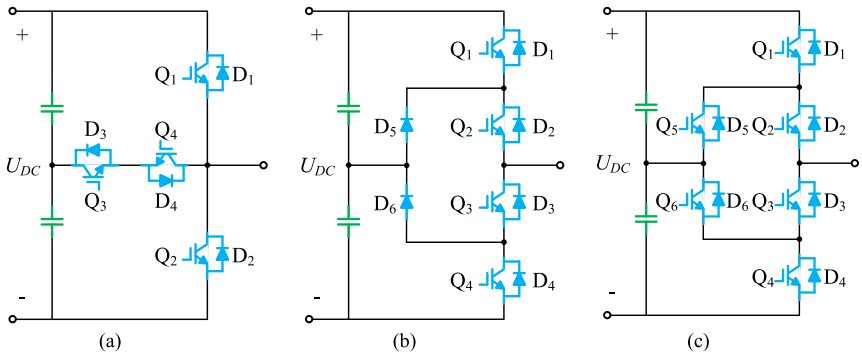


Fig. 1. Different 3L converter topologies. (a) T^{2}C. (b) NPC converter. (c) ANPC converter.

In many applications, such as battery charging systems for electric vehicles and power supplies for modern data centers, the power density of the converters is required. In order to realize a high-power-density design, the converter efficiency should be further increased, and the volume of the ac-side filter should be decreased by increasing the switching frequency. The power density performance of Si-based NPC-type converters is still limited even applying the above-mentioned solutions. A clear tendency in research areas is to increase the switching frequency by using widebandgap (WBG) devices with much lower switching losses. After several years' development, the fabrication process for SiC devices has become mature gradually. In many published papers [1], [2], [4]–[6], [17], [20], [21], SiC devices have been implemented to 3L converters for better performance at the higher switching frequency. Currently, the applications based on SiC diodes and SiC MOSFETs are more popular because of their mass production.

Comparing a SiC MOSFET and a Si insulated-gate bipolar transistor (IGBT), the switching loss performance of the SiC MOSFET is much better than that of the Si IGBT [4], [17], [22], [23]. In [17], a 3L-ANPC based on the SiC MOSFET is proposed. The converter has achieved 97.5% peak efficiency at an output power of 1.5 kW with a switching frequency of 40 kHz. A SiC-MOSFET-based T-type 3L converter is built in [4], which realized 98.4% peak efficiency, while the Si-IGBT-based converter only achieved 97.7% efficiency. However, the up-to-date cost of SiC devices is still several times higher than that of Si devices. For example, a short summary of 650-V SiC and Si devices' price on www.digikey.ca is given Fig. 2. It shows that, in high current range, the price of the SiC MOSFET is almost six to eight times compared to that of the Si IGBT and two times compared to that of the Si MOSFET, while the price of the SiC diode is almost eight times compared to that of the Si diode. As a result, based on the current price, instead of using the all-SiC MOSFET 3L converter, the Si and SiC hybrid 3L converter will be more attractive. The hybrid converters that apply SiC diodes and Si IGBTs are quite common in the research even in some high-end products [5], [6], [20]. Using SiC diodes can significantly reduce the reverse recovery loss on diodes and decrease the turn-on loss on Si IGBTs. For example, a 3L NPC with SiC clamping diodes instead of Si clamping diodes was proposed in [20]. However, the switching losses on IGBTs are still fairly high because of the large turn-off losses and part of turn-on losses still existing in Si IGBTs' switching. This prevents the hybrid converters to operate under higher switching frequency.

In this paper, a SiC MOSFET and Si device hybrid ANPC converter is proposed. Instead of using the all-SiC-based power stage, it consists of four Si active switches and only two SiC MOSFETs. Thus, it has lower total cost. At the same time, different with the normal purpose of loss redistribution method, which is to evenly distribute the switching losses, a dedicated modulation scheme is proposed to completely move all the switching events from Si devices to SiC MOSFETs by using redundant zero states of the ANPC topology. As a result, the switching losses are significantly reduced and high efficiency is achieved. Furthermore, the efficiency can be enhanced under low dc voltage standard by replacing Si IGBTs with Si MOSFETs. The efficiency benefit of the hybrid structure with the proposed modulation scheme is investigated and evaluated by experiments. This paper is organized as follows. In Section II, the topology of the proposed hybrid ANPC converter is demonstrated, and the dedicated modulation scheme for switching loss elimination is derived. In Section III, the method of estimating the power losses for the proposed converter, as well as the power loss performance for both the Si-IGBT- and SiC-MOSFET-based ANPC converters, is analyzed. A comparison of the total losses under different switching frequency, output current, power factor (PF), and dc-bus voltage is made between the three configurations. Section IV presents the experimental results to show the high performance and high efficiency of the proposed converter. Section V concludes this paper.

II. Proposed Hybrid ANPC Converter and Modulation Scheme

The one-phase circuit of the proposed 3L-hybrid ANPC converter is shown in Fig. 3(a). There are six active switches in the one-phase circuit. Among them, Q_2 and Q_3 are using SiC MOSFETs and the others are using Si active switches. Except the comprising of SiC and Si devices, the circuit configuration keeps exactly the same as a regular Si-based ANPC converter shown in Fig. 1(c).

For a regular Si-based ANPC converter, there are many modulation schemes [10]–[16] proposed to balance the loss distribution on all devices. It is because in a regular ANPC converter, all devices $Q_1 - Q_6$ prefer to use the same type of Si IGBT.

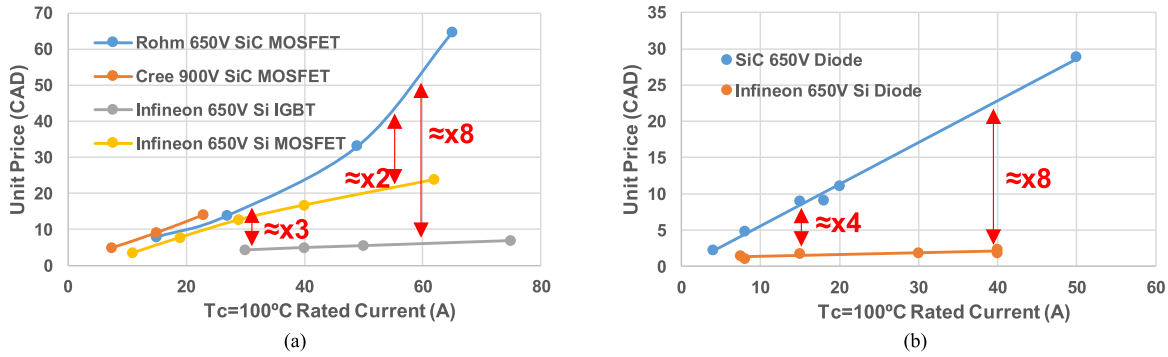


Fig. 2. Summary of typical Si and SiC devices' price on Digikey.ca (TO-220 package or TO-247 Package). (a) Active switches. (b) Diodes.

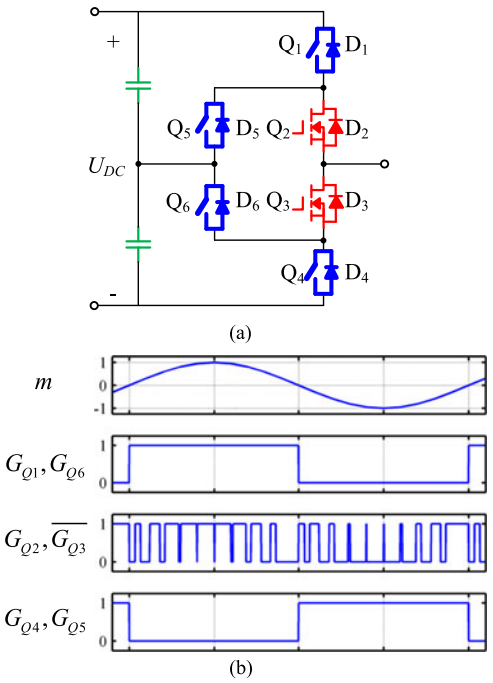


Fig. 3. Topology and modulation of the 3L hybrid ANPC converter. (a) Topology demonstration. (b) Waveforms of the proposed modulation scheme.

TABLE I
SWITCHING STATES OF THE 3L HYBRID ANPC CONVERTER

Switch state	Voltage level	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6
N	1	0	0	1	1	1	0
O–	0	0	1	0	1	1	0
O+	0	1	0	1	0	0	1
P	–1	1	1	0	0	0	1

Therefore, the maximum temperature rise on devices can be lower by balancing the loss distribution. In this way, the converter can operate under higher power rating. However, for the proposed hybrid converter, it is not necessary to balance the loss distribution, since the SiC MOSFET can potentially operate under higher junction temperature as long as an especially designed thermal system can make the Si devices operate with lower temperature. Furthermore, since the SiC MOSFET has much lower switching losses, the total switching losses can be significantly decreased if the SiC MOSFETs can take more switching events than Si devices. These will lead to much higher efficiency and higher switching frequency for the ANPC converter.

The proposed modulation scheme that can decrease the total switching losses is described as follows. Four switching states (N, O-, O+, and P) are designed as listed in Table I. They can output three different voltage levels. The voltage level "0" has two redundant states. The ON–OFF state of all devices in each state is also given in Table I. It can be inferred that during the operation, Si device pairs $Q_1 - Q_6$ and $Q_5 - Q_4$ always share the same gating signals, respectively. Also, these two Si device pairs are complementarily switching. On the other hand, SiC MOSFET Q_2 and Q_3 are complementary pairs.

The waveforms of the proposed modulation scheme are given in Fig. 3(b). The generation of gating patterns follows the routine of phase-deposition pulse width modulation, where a modulation wave is used. In each half cycle of the modulation wave, only one "0" level state is used. The "O+" state is only used in the positive cycle, and the "O-" state is only used in the negative cycle. According to these selected switching patterns, during the positive half cycle, Q_1 and Q_6 are always in the ON state. Q_2 and Q_3 are the only two complementarily switching devices.

Taking Si IGBT and SiC MOSFET hybrid configuration as an example, the detailed commutation process under both the inverter mode and the rectifier mode is demonstrated in Figs. 4 and 5, respectively. Under the inverter mode, when the circuit outputs state "P", the main current will go through Q_1 and Q_2, as shown in Fig. 4(a). The turning OFF of Q_2 will force the main current commutate to Q_6 and D_3, as displayed in Fig. 4(b). The turning ON of Q_3 will make Q_3 operate under the synchronous rectifier mode, as displayed in Fig. 4(c). Under this mode, the changing from state "P" to the deadtime state will create turn-off loss on Q_2. The changing from the deadtime state to state "P" will create turn-on loss on Q_2 and reverse recovery loss on D_3. Under the rectifier mode, when the circuit outputs state "P", as shown in Fig. 5(a), the main current will go through D_1 and Q_2 instead. The turning OFF of Q_2 will force the main current commutate to its body diode D_2, as displayed in Fig. 5(b). The turning ON of Q_3 will make the main current commutate to Q_3 and D_6, as displayed in Fig. 5(c). The changing from state "O+" to the deadtime state will create turn-off loss in Q_3. The changing from the deadtime state to

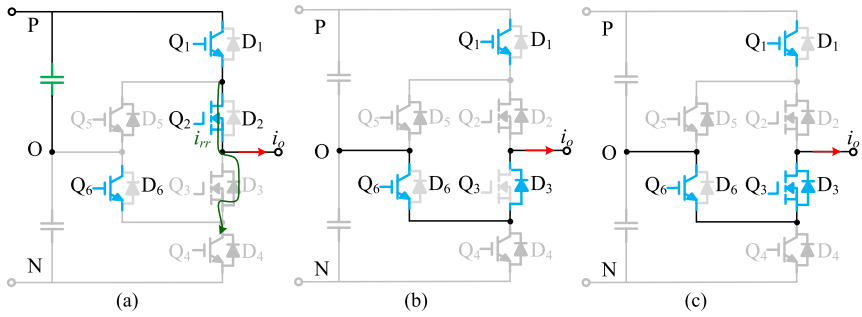


Fig. 4. Demonstration of commutation under the inverter mode. (a) Equivalent circuit of state "P". (b) Equivalent circuit during the deadtime. (c) Equivalent circuit of state "O+".

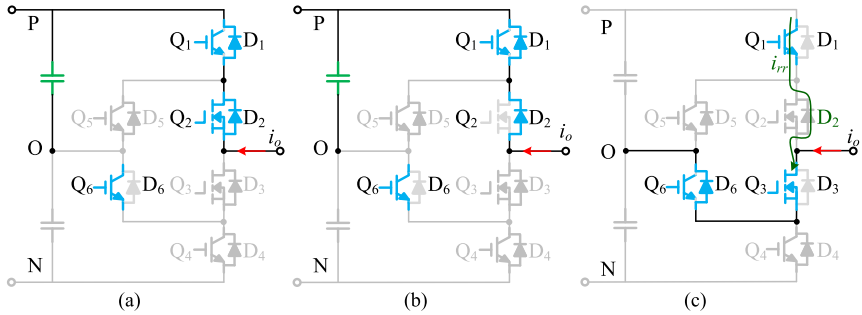


Fig. 5. Demonstration of commutation under the rectifier mode. (a) Equivalent circuit of state "P". (b) Equivalent circuit during the deadtime. (c) Equivalent circuit of state "O+".

state "O+" will create turn-on loss in Q_3 and reverse recovery loss on D_2. Although D_1 is turned OFF during this interval, Q_1 is kept ON, and the off-state voltage on D_1 is zero. It means that D_1 is turned OFF with zero-voltage switching, and there is no reverse recovery loss on D_1.

From the above analysis, it can be concluded that the commutation between the "P" state and the "O+" state only create switching losses on SiC MOSFETs Q_2 and Q_3 or on their body diodes D_2 and D_3. As a result, the switching losses can be significantly decreased by using these two SiC MOSFETs. In the same manner, during the negative half cycle, Q_4 and Q_5 are always in the ON state. Q_2 and Q_3 are still the only two complementarily switching devices. It means that, by applying the proposed scheme, all the switching events are moved to the two SiC MOSFETs. Thus, the proposed hybrid ANPC converter can achieve the same switching loss performance compared to the all-SiC MOSFET-based ANPC converter.

There is another significant benefit of the proposed scheme. In the traditional Si-based ac–dc converter with bidirectional energy flow capability, Si IGBTs are preferred to compose the power stage. Although in the voltage rating of 650-V Si device family, Si MOSFETs such as cool MOSFETs are proved to have better dynamic performance and lower conduction loss under lower current rating compared to Si IGBTs, they cannot be adopted in such an ac–dc converter because the Si MOSFETs have built-in body diodes, which show very poor reverse recovery performance just like the standard recovery diodes. However, by applying the proposed hybrid power stage and modulation scheme, the using of Si MOSFET becomes possible. Four Si devices (Q_1, Q_4, Q_5, and Q_6) shown in Fig. 3(a) can adopt Si MOSFETs. It is because Q_1, Q_4, Q_5, and Q_6 all do not have the switching loss including the reverse recovery loss; the proposed Si MOSFET and SiC MOSFET hybrid ANPC power stages can also achieve a very high efficiency.

III. Power Loss Analysis and Comparison

In order to demonstrate the efficiency improvement of the proposed hybrid ANPC converter compared to the all-Si-IGBT-based ANPC converter and show the efficiency difference compared to the all-SiC-MOSFET-based ANPC converter, the theoretical power loss performance of ANPC converters with four different configurations is analyzed. The power loss distribution on each device of the proposed hybrid converter is given. The power loss performance under different dc-link voltage, switching frequency, output power, and PF are analyzed.

A. Device Selection

Four ANPC converter configurations with different device selection are analyzed. They are (a) the all-Si-IGBT-based configuration, (b) the all-SiC MOSFET-based configuration, (c) the Si IGBT and SiC MOSFET hybrid configuration, and (d) the Si MOSFET and SiC MOSFET hybrid configuration. The selection of devices is shown in Table II. Since the prototype that is going to be built is designed to operate under 600–800-V dc-bus voltage, 650-V Si and SiC devices with similar current rating are selected. In comparison, Infineon's Si IGBT IKW75N65ES5, Si MOSFET Infineon-IPW65R019, and ROHM's SiC MOSFET SCT3022AL-E are chosen for loss evaluation. The Si IGBT is copacked with an antiparallel diode. The MOSFETs are using

TABLE II
SELECTED DEVICES FOR COMPARISON AND THE TOTAL PRICE OF CONVERTERS

Configuration	*Description*	Q_1, Q_4, Q_5 *and* Q_6	Q_2 *and* Q_3	*Total Price(CAD)*
(a)	All-Si-IGBT ANPC	Si IGBT (Infineon-IKW75N65ES5)	Si IGBT (Infineon-IKW75N65ES5)	51.30
(b)	All-SiC-MOSFET ANPC	SiC MOSFET (ROHM-SCT3022AL-E)	SiC MOSFET (ROHM-SCT3022AL-E)	388.86
(c)	Hybrid ANPC (Si IGBTs and SiC MOSFETs)	Si IGBT (Infineon-IKW75N65ES5)	SiC MOSFET (ROHM-SCT3022AL-E)	163.82
(d)	Hybrid ANPC (Si MOSFETs and SiC MOSFETs)	Si MOSFET (Infineon-IPW65R019)	SiC MOSFET (ROHM-SCT3022AL-E)	250.38

TABLE III
CHARACTERISTICS AND PRICES OF SIC AND SI DEVICES ON WEBSITE

	Voltage rating (V)	*Current rating (A)*	*Price (CAD) (@www.digikey.ca)*
Si IGBT (Infineon-IKW75N65ES5)	650	75	8.55
Si MOSFET (Infineon-IPW65R019)	650	65	30.19
SiC MOSFET (ROHM-SCT3022AL-E)	650	65	64.81

their body diodes. Based on this device selection, the total prices of the converter under three different configurations are given. The unit price of each type device is referred to Table III. According to Table II, it is clear that configuration (b) with all-SiC MOSFET ANPC is the most expensive one. The total price of the proposed hybrid configuration has decreased by 60%. Also, by comparing two hybrid configurations, the Si MOSFET and SiC MOSFET hybrid power stage has a higher total price because the Si MOSFET has a higher price than the Si IGBT with a similar power rating.

The theoretical analysis of the power loss performance requires the quantification of the conduction characteristics of all devices and switching characteristics of both Si IGBTs and SiC MOSFETs. Useful information is included in their datasheets.

B. Modeling of Conduction Losses

From the Si IGBT datasheet, the IGBT saturation voltage related to the collector current and the forward voltage of the antiparallel diodes related to the forward current can be extracted. The MOSFET drain–source voltage related to the on-state current can also be extracted from the Si MOSFET and SiC MOSFET datasheet. Similar with Si MOSFET, SiC MOSFET shows an almost constant on-state resistance under a certain temperature. On the other hand, by comparing the conduction characteristics of the Si IGBT or diode, with the MOSFET, it can be found that the MOSFETs have a lower voltage drop when the on-state current is low because of their pure resistance characteristic. After the on-state current becomes high, with the help of the conductivity modulation effect, the voltage drop on the Si IGBT or diode becomes lower compared to the MOSFETs. This infers that for the similar current rating devices, Si IGBTs or diodes potentially can have lower conduction losses if the output current is high enough.

Another important factor is that the body diode of the SiC MOSFET has a very poor conduction characteristic, which is not designed for continuous operation. As a result, under rectifier mode operation, the gating signals are always enabled for the SiC MOSFETs to make the current going through the MOSFET channel instead of the body diode. The body diode is only used for commutation during the deadtime. On the other hand, the body diode of the Si MOSFET has a relatively lower voltage drop. It will conduct if the output current is very high under the rectifier mode. In order for simplification, this situation is not considered into the comparison as long as the gating signals are also enabled for all Si MOSFETs.

The conduction losses of the semiconductor device are modeled by using a piecewise linear model, which is commonly used in many studies [1], [3], [5]–[6], [17]. A generalized equation is given as

$$P_{\rm con} = V_0 I_{\rm avg} + r I_{\rm rms}^2 \tag{1}$$

where V_0 is the initial voltage drop, r is the equivalent resistance when the devices are turned ON, $I_{\rm avg}$ is the average current, and $I_{\rm rms}$ is the root-mean-square (RMS) value of the current going through the device. For the Si IGBT and its antiparallel diode, V_0 is its zero on-state voltage and r is its dynamic on-state resistance. For the Si MOSFET and the SiC MOSFET, V_0 is the zero and r is the on-resistance of the corresponding MOSFET.

The values of V_0 and r are extracted from Fig. 6(a). The results of piecewise linearization are given in Fig. 6(b). According to different modulation index, output current, and PF, the $I_{\rm avg}$ and $I_{\rm rms}$ for each device can be calculated. All the conduction loss for each device can then be calculated by (1).

C. Modeling of Switching Losses

The switching loss behavior of the devices can also be extracted from datasheets, which are given in Fig. 7. The turn-on switching loss $E_{\rm on}$ and turn-off switching loss $E_{\rm off}$ in one switching period are given individually for both the Si IGBT and the SiC MOSFET. The reverse recovery loss on diodes has already included into $E_{\rm on}$ as described in datasheets. The total switching losses $E_{\rm total}$ are calculated from $E_{\rm on}$ and $E_{\rm off}$ curve. It can be found that the $E_{\rm total}$ on the Si IGBT (with losses on diode) is four to five times higher than $E_{\rm total}$ on the

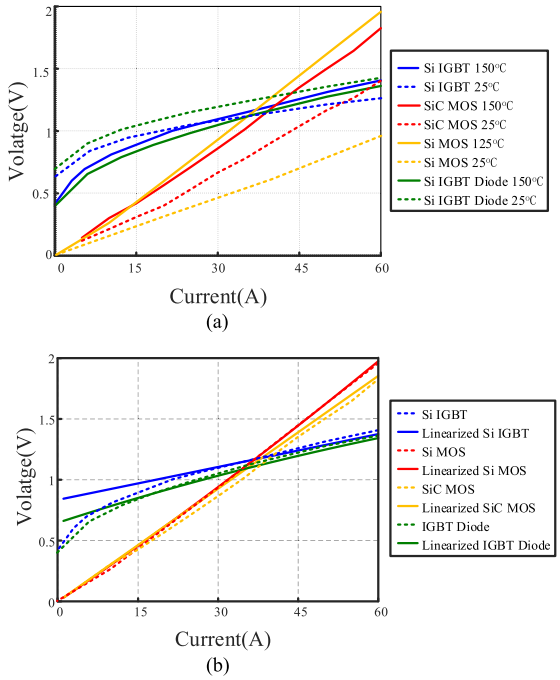


Fig. 6. Typical output characteristics of Si IGBT, Si MOSFET, and SiC MOSFET. (a) Curves on datasheets at 25 and 150 °C. (b) Original curves and linearized curves at 150 °C.

SiC MOSFET. It should be pointed out that for four Si Devices Q_1, Q_4, Q_5, and Q_6, there are no switching losses if applying the proposed modulation scheme. Since Si MOSFETs are only applied to these four switches, no switching losses on Si MOSFETs are considered.

Of course, the switching loss data on datasheets are derived under single test conditions, which are somehow different from the real conditions, where the prototype are applied. As a result, a switching loss model considering the variation of current and voltage is built to estimate the switching loss under the prototype's testing condition. In order to make the loss estimation results comparable with the experimental results, other testing conditions such as gate resistances and gate voltage for driving are kept the same as datasheets recommended. The temperature used for testing has selected the junction temperature $T_j = 150$ °C. Although the data used for SiC are recorded in ambient temperature $T_a = 25$ °C, it will not lose too much accuracy since the temperature hardly affects the switching energies of the SiC MOSFET [1].

In order to simplify the switching loss model, the switching loss is considered to be linear with the dc-link voltage. The relationship between switching loss and device current is derived by using curve-fitting tools. Based on this simplification, a switching loss model is derived. The turn-on switching losses $E_{\mathrm{on}x}$ and turn-off switching losses $E_{\mathrm{off}x}$ of device Q_x are given by (2) and (3), respectively. In this model, $E_{\mathrm{ontest}x}$ and $E_{\mathrm{offtest}x}$ represent the turn-on/turn-off energy losses of the devices shown in datasheets and measured under certain testing voltage U_{test} and testing current I_{test}. The switching voltage of the 3L-ANPC converter prototype is $0.5U_{\mathrm{dc}}$. The device current is the output current i_{ac}. This model is proved to have acceptable accuracy

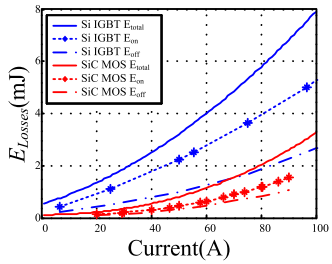


Fig. 7. Switching losses of Si IGBT and SiC MOSFET under inductive load (Test condition: Si IGBT at $T_j = 150$ °C, $V_{\mathrm{CE}} = 400$ V, $V_{\mathrm{GE}} = 15$ V/0 V, $R_{G\mathrm{on}} = 18\ \Omega$, and $R_{G\mathrm{off}} = 5.6\ \Omega$; SiC MOSFET at $T_a = 25$ °C, $V_{dd} = 300$ V, $V_{\mathrm{GS}} = 18$ V/0 V, and $R_G = 0\ \Omega$).

TABLE IV
CONVERTER PARAMETERS USED FOR COMPARISON

Rated output power P_{max}	4.2 kW
DC-link voltage U_{dc}	650 V
Switching frequency f_{sw}	15 kHz, 45 kHz
Grid voltage V_{ac}	208 V_{ac}/60 Hz
Grid ac current I_{ac}	21 A
Grid inductor L_f	870 μH
DC capacitance C_{dc}	9 mF each
Junction temperature T_j	150 °C

according to the results in [3] and [6]

$$E_{\mathrm{on}x} = \frac{0.5U_{\mathrm{dc}}E_{\mathrm{ontest}x}}{U_{\mathrm{test}x}} \cdot \frac{k_{2\mathrm{on}}i_{\mathrm{ac}}^2 + k_{1\mathrm{on}}i_{\mathrm{ac}} + k_{0\mathrm{on}}}{k_{2\mathrm{on}}I_{\mathrm{test}x}^2 + k_{1\mathrm{on}}I_{\mathrm{test}x} + k_{0\mathrm{on}}} \tag{2}$$

$$E_{\mathrm{off}x} = \frac{0.5U_{\mathrm{dc}} \cdot E_{\mathrm{offtest}x}}{U_{\mathrm{test}x}} \cdot \frac{k_{2\mathrm{off}}i_{\mathrm{ac}}^2 + k_{1\mathrm{off}}i_{\mathrm{ac}} + k_{0\mathrm{off}}}{k_{2\mathrm{off}}I_{\mathrm{test}x}^2 + k_{1\mathrm{off}}I_{\mathrm{test}x} + k_{0\mathrm{off}}}. \tag{3}$$

The total switching losses of one device are derived by integrating the one-time switching losses in a complete output ac cycle.

D. Prototype Specification and Power Loss Comparison

The power loss comparison is carried out by using the baseline parameters given in Table IV. With the data derived from datasheets and implementing the loss models, the total losses of ANPC converters with four configurations are estimated. All the calculations are applying the same proposed modulation strategy to make the results of comparison fair. The loss data under the junction temperature $T_j = 150$ °C are selected for both Si devices and SiC devices. As a result, the comparison results given below are for the worst case of operation.

In Fig. 8, the power loss distribution of the proposed ANPC converters with Si IGBTs under PF $= 1$ and PF $= -1$ is calculated. Since the one-phase circuit is symmetrical, half of the switches are considered. According to results, the SiC MOSFETs undertake all the switching loss and, thus, have the highest losses. This will not be a problem, since the SiC device potentially can operate under higher temperature. On the other hand, it can be found that the total loss performances under PF $= 1$ and PF $= -1$ are quite similar. It is because the output

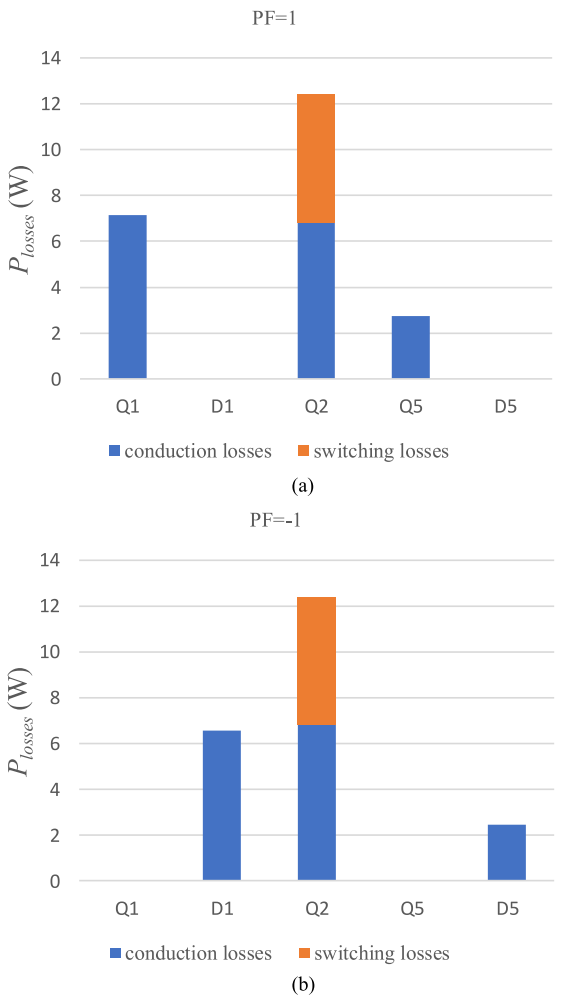


Fig. 8. Power losses distribution of the proposed hybrid ANPC converter under different PF at $f_{\rm sw} = 45$ kHz, $U_{\rm dc} = 650$ V, $I_{\rm ac} = 21$ A, and $V_{\rm ac} = 208$ V. (a) PF $= 1$. (b) PF $= -1$.

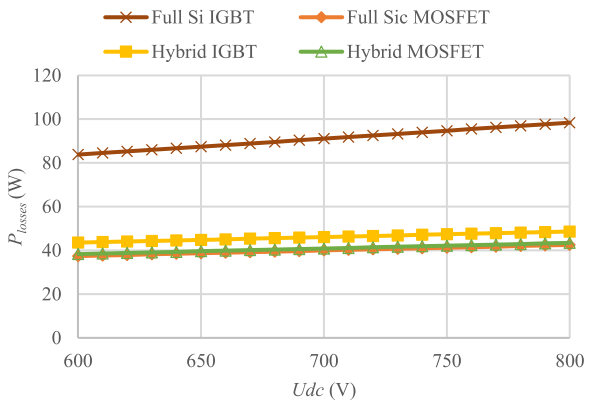


Fig. 9. Power losses under different dc voltage $U_{\rm DC}$ ($f_{\rm sw} = 45$ kHz, $I_{\rm ac} = 21$ A, and $V_{\rm ac} = 208$ V).

characteristics of the Si IGBT and its antiparallel diode are almost the same according to Fig. 6.

Figs. 9 and 10 shows the loss comparison results of ANPC converters with four different configurations at different $U_{\rm DC}$ (from 600 to 800 V) and $f_{\rm sw}$ (from 15 to 60 kHz), respectively.

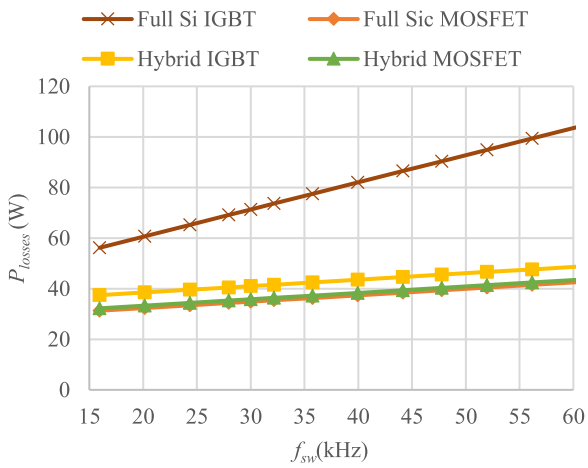


Fig. 10. Power losses under different switching frequency $f_{\rm sw}$ ($U_{\rm dc} = 650$ V, $I_{\rm ac} = 21$ A, and $V_{\rm ac} = 208$ V).

It is clear that the total losses on all-Si IGBT ANPC are the highest, about 20–30 W more than the others. The losses of all-SiC MOSFET ANPC and hybrid MOSFET ANPC is a litter bit higher than that of the hybrid IGBT ANPC. This is mainly because the Si MOSFET has a lower voltage drop under this current rating (21 A), which leads to lower conduction losses, while both power stages have the same switching losses. If operating with higher current, the proposed hybrid converter with Si IGBTs can have higher efficiency compared to the all-SiC MOSFET converter. This tendency can be found in Fig. 11, where $U_{\rm DC}$ and $f_{\rm sw}$ are fixed and the output power P is changing. When P is more than 6.84 kW, i.e., I_O is more than 34 A, the total losses of hybrid ANPC with the Si IGBT become the lowest one among four configurations. It means that this configuration is especially suitable for high-power applications, where IGBTs are normally used.

Fig. 12 gives the comparison for the conduction losses and switching losses in case of (a) $f_{\rm sw} = 15$ kHz and (b) $f_{\rm sw} = 45$ kHz, respectively. It clearly shows that the all-Si-based configuration has almost four times higher switching losses than the other configurations, and the loss difference between the all-SiC-based converter and the proposed hybrid converter are because of the difference in conduction losses. However, this difference is not significant. On the other hand, since the proposed hybrid converter has a much lower total device cost, it should be more attractive compared to the all-SiC-based converter in many industrial applications.

IV. Experimental Results of the Proposed Converter

In order to evaluate the real efficiency performance of the proposed converter, experiments are carried out based on the specifications given in Table IV. The photograph of a single-phase hybrid ANPC power stage is shown in Fig. 13. Both the Si IGBT hybrid configuration and the Si MOSFET hybrid configuration are tested. Since high efficiency is achieved, natural cooling is adopted. The same as the loss evaluation, only a single-phase circuit is tested under both the inverter mode and the rectifier mode. The ac side is connected to the 208 − $V_{\rm ac}$

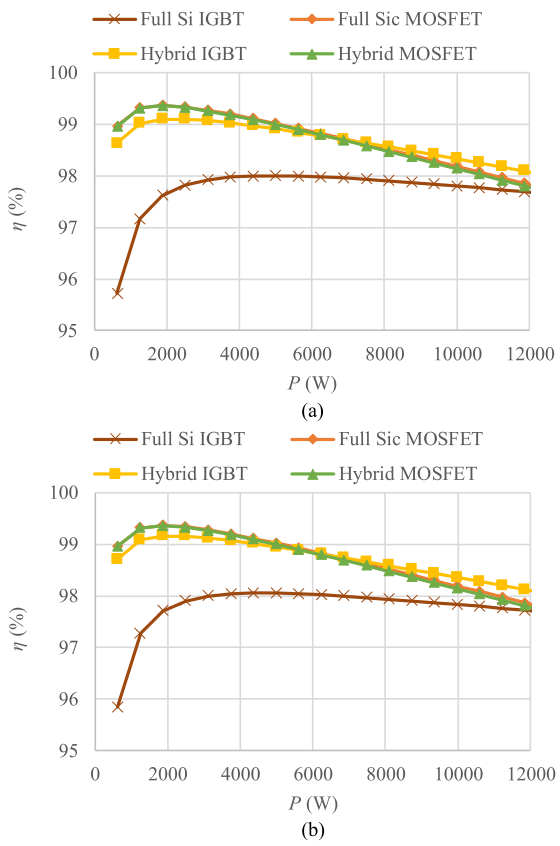


Fig. 11. Power stage efficiency under different output power P. (a) PF $= 1$. (b) PF $= -1$. ($f_{\rm sw} = 45$ kHz, $U_{\rm dc} = 650$ V, and $V_{\rm ac} = 208$ V.)

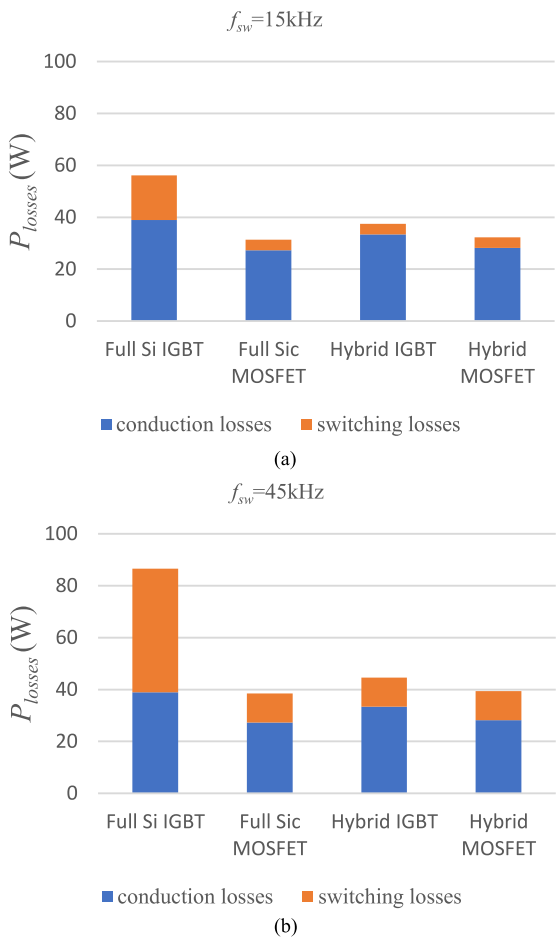


Fig. 12. Comparison of conduction losses and switching losses under different switching frequency. (a) $f_{\rm sw} = 15$ kHz. (b) $f_{\rm sw} = 45$ kHz. (PF $= 1$, $U_{\rm dc} = 650$ V, $I_{\rm ac} = 21$ A, and $V_{\rm ac} = 208$ V.)

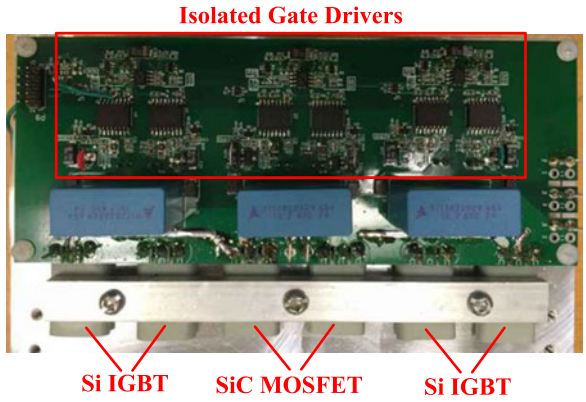


Fig. 13. Photograph of a single-phase hybrid ANPC power stage.

line voltage. Because of the maximum voltage limitation of dc power supply, under the inverter mode, the dc-link voltage has scaled down to 600 $V_{\rm dc}$. The ac grid voltage is decreased to 190 $V_{\rm ac}$ to keep the modulation index the same.

The experimental waveforms of gating signals and the 3L voltage output $v_{\rm inv}$ of the converter are given in Fig. 14. Since $Q_1 - Q_6$ and $Q_4 - Q_5$ are sharing one gating signal, respectively, while Q_2 and Q_3 are switching complementarity; only signals of Q_2, Q_1, and Q_4 are given. It can be found that only Q_2 has high-frequency switching. The gate voltage polarities of Q_1 and Q_4 are changing following the voltage polarity changing of $v_{\rm inv}$, which are only 60 Hz.

The experimental waveforms of the converter operating under the rectifier mode and the inverter mode are given in Fig. 15(a) and (b). The waveforms of the 3L voltage output $v_{\rm inv}$, half dc-link voltage v_{dc1}, ac-side current $i_{\rm ac}$, and ac grid voltage $v_{\rm ac}$ are given, respectively. It can be found that the proposed ANPC converter has exactly the same waveforms compared to waveforms of the other 3L converters. The $i_{\rm ac}$ presents a low total harmonic distortion waveform regardless of the distorted grid voltage. This is because under higher switching frequency, the control bandwidth of the current loop can be increased.

The efficiency performance is evaluated by using a power analyzer. The system configuration for the efficiency testing and the diagram of the system connection is shown in Fig. 16. The input and output power are measured directly from the dc and ac sides of the circuit. As a result, besides the power stage losses, the losses on the dc-link capacitor, connection cables, and the ac inductor are measured at the same time. Information about how to calculate inductor losses and capacitor losses is given in the Appendix. Example of the calculation results under the rectifier mode and 4.2-kW rated power is shown in Table V.

The results show that the core loss and high-frequency ac winding loss can be neglected compared to the low-frequency winding loss. This is because with high inductance, the

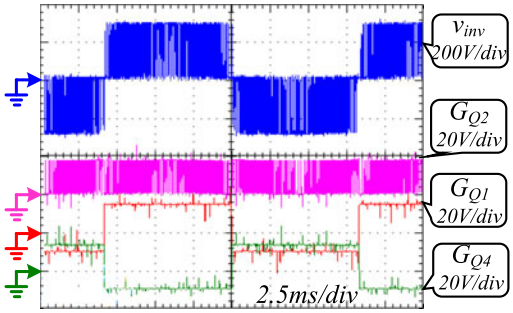


Fig. 14. Waveforms of gating signals.

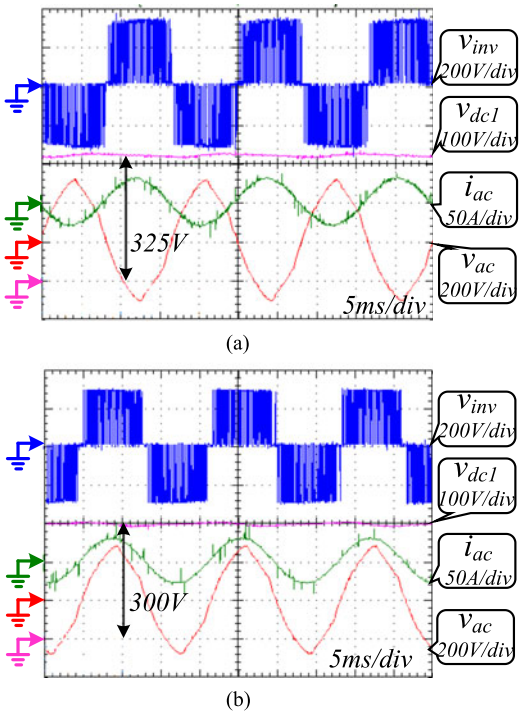


Fig. 15. Waveforms of the converter operating under the rectifier mode and the inverter mode. (a) PF $= -1$, $f_{\rm sw} = 45$ kHz, $U_{\rm dc} = 650$ V, $I_{\rm ac} = 20$ A, and $V_{\rm ac} = 208$ V. (b) PF $= -1$, $f_{\rm sw} = 45$ kHz, $U_{\rm dc} = 600$ V, $I_{\rm ac} = 22$ A, and $V_{\rm ac} = 190$ V.

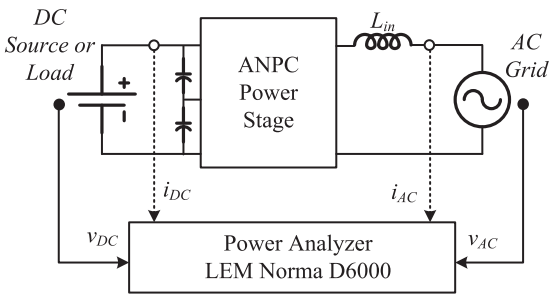


Fig. 16. Efficiency testing system configuration.

incremental flux density ΔB and the RMS value of the ripple current are both very small. Another interesting finding is that, with the increasing switching frequency, instead of becoming larger, the core loss and the ac winding loss become even smaller. This is because following the switching frequency increases, the

TABLE V
RESULTS OF LOSS CALCULATION UNDER THE RECTIFIER MODE AND RATED POWER

	Core loss $P_{\rm ind\_fe}$	Winding loss at low frequency P_{cu_dc}	Winding loss at switching frequency P_{cu_ac}	DC capacitor loss P_{Co}
Power loss @30 kHz	0.875 W	13.5 W	0.185 W	2.09 W
Power loss @45 kHz	0.744 W	13.5 W	0.103 W	2.09 W

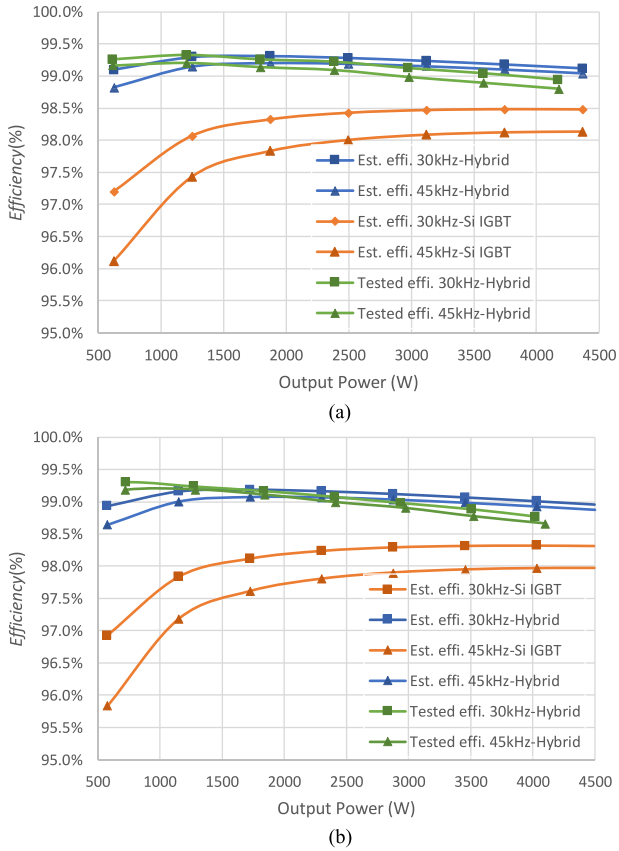


Fig. 17. Power stage efficiency performance and comparison. (a) Rectifier mode. (b) Inverter mode.

inductor current ripple becomes smaller. According to (6), when $\alpha > \beta$, the total core loss $P_{\rm ind\_fe}$ becomes smaller. The high-frequency ac winding loss P_{cu_ac} has a similar tendency.

The final power stage efficiency performance of the proposed converter is given in Fig. 17. The estimated efficiency and the tested efficiency of the proposed hybrid ANPC converter with the Si IGBT and the estimated efficiency of the Si-IGBT-based ANPC converter are compared together. It can be found that around 0.5–1.0% efficiency improvement can be made by using the hybrid power stage instead of all Si IGBTs. On the other hand, according to the differences between efficiency at 45- and 30-kHz switching, the increasing of switching frequency will not significantly affect the efficiency performance if using the proposed hybrid power stage. It means that the proposed ANPC

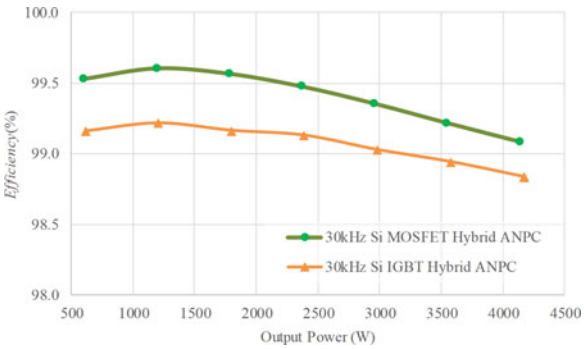


Fig. 18. Efficiency comparison between the Si IGBT and SiC MOSFET power stage and the Si MOSFET and SiC MOSFET power stage under the rectifier mode and 30-kHz switching.

converter can potentially operate under even higher switching frequency to further decrease the filter size.

The Si MOSFET and SiC MOSFET hybrid ANPC converter is also tested by using the same prototype, which just changes the device type of Q_1, Q_4, Q_5, and Q_6. The results of the efficiency comparison are given in Fig. 18. It can be found that based on this device selection, the Si MOSFET and SiC MOSFET hybrid power stage has better efficiency performance. The reason is that the Si MOSFET has a lower voltage drop under the prototype's current rating. However, this situation is not always true. Under higher operating temperature and with higher current, the voltage drop on the Si IGBT may become lower. On the other hand, in higher dc-bus voltage application such as a solar inverter, a 1200-V Si device may be selected. Under this condition, the IGBT becomes superior compared to the MOSFET. As a result, the Si MOSFET and SiC MOSFET hybrid power stage is favorable for applications, where the dc-bus voltage is around 600–800 V, while the Si IGBT and SiC MOSFET hybrid power stage should be more favorable especially for applications where the dc-bus voltage is over 1000 V.

From the results, it can also be found that there is still some error between the tested losses and the evaluated losses. The error between the tested data and theoretical analysis mainly is caused by two reasons. One is that the temperature of the testing is uncontrolled. Because of using TO-247 package discrete commercial products, it is hard to see the real case or junction temperature of the device. At the same time, higher junction temperature will not always lead to higher conduction loss. As shown in Fig. 6(a), higher temperature makes the on-state resistance of Si and SiC MOSFETs become larger but makes the initial voltage drop of the Si IGBT and diode become lower. Thus, the conduction loss on the Si IGBT and diode becomes lower. So, it is difficult to say whether the tested conduction loss data should be higher or lower than the theoretical analysis, which is considered under 150 °C. Another reason is that the specification of the prototype hardware such as stray inductance, gate driver circuit is not the same as the devices are tested. Therefore, the switching energy loss is also not exactly the same as the datasheet shows. Other testing results in [24] show that the parasitic effects can increase the switching losses by a factor of 1.5–1.8. As a result, all these loss analyses are aiming to demonstrate a tendency to show how much benefit could be achieved by using the proposed hybrid configuration and modulation scheme if the layout and the gate driver circuits of the power stage are both well designed.

V. Conclusion

In this paper, a SiC MOSFET and Si device hybrid ANPC converter is proposed. By applying the Si and SiC hybrid power stage, the total cost can be decreased by over 50% compared to the all-SiC-based ANPC converter. By applying the proposed modulation scheme, the switching events can be completely moved from Si devices to SiC MOSFETs to minimize the switching losses. According to the experimental results, around 0.5–1.0% efficiency improvement can be made by using the hybrid power stage instead of the all-Si-IGBT power stage. The power stage maximum efficiency is up to 99% at the 45-kHz switching frequency and with 650-V dc-bus voltage.

The proposed converter has fully utilized the low-switching-loss advantage of the SiC MOSFET and the low-cost advantage of the Si device. Based on the device rating selected in this paper, it has a superior performance in high-end grid-connected inverter and rectifier applications with the 650–800-V dc-bus voltage. On the other hand, because of its 3L power stage, compared to 2L converters, it can potentially be applied to higher voltage rating applications such as using 1200-V SiC MOSFET and Si IGBT for the wind generation system. Similar improvements can be made. Furthermore, as 3L converters naturally have lower switching losses compared to 2L converters [8], the proposed converter can operate with higher switching frequency compared to 2L converters with SiC MOSFETs.

It should be noted that, although the calculation and experiment are carried out by using the SiC MOSFET, other types of WBG devices can also be implemented to this converter without losing the benefits, such as the GaN device. Since currently GaN devices only have a low-voltage-rating version and present even higher price, using multilevel topologies and hybrid power stage may bring more significant benefits.

Moreover, within the multilevel topologies, there are a lot of topologies that have the redundant states and can dynamically shift the switching losses by using different modulation scheme. It is hoped that similar to the method derived in this paper, a number of highly efficient low-cost hybrid multilevel converters can be derived in the future.

Appendix

The calculation methods for inductor loss and capacitor loss are given in the following.

Inductor core loss P_{Ind_fe}*:* The inductor loss includes two parts, the core loss, and the winding loss. The core loss per unit volume P_{Fe_ind} can be found from the material loss chart. The core loss is given by multiplying the core volume V_{e_ind} with P_{Fe_ind}. However, considering the changing voltage–second applied to the inductor because of the ac input voltage variation, the instant value of loss per unit volume P_{Fe_ind} is calculated by improved general Steinmetz equation [25]. The average loss in one line period is the integration of instance loss in every

TABLE VI
PARAMETERS OF THE INDUCTOR AND THE CAPACITOR USED IN THE PROTOTYPE

Inductor $L_{\rm in}$	900 μH/20 A Core information: U-shaped nanocystalline core, $A_e = 4.539\ \text{cm}^2$, $V_e = 113.475\ \text{cm}^3$ K = 0.0053, $\alpha = 2.3$, $\beta = 1.9$ Winding information: $N_{\rm ind} = 45$, AWG #12 Litz wire ($D_{\rm Litz\_wire} = 0.1$ mm, $R_{\rm ind\_dc} = 33\ \text{m}\Omega$, $F_{r\_30\,\rm kHz} = 1.25$, $F_{r\_45\,\rm kHz} = 1.57$)
Capacitor $C_{\rm DC}$	Each half capacitor: 9000 μF (ESR = 0.009 mΩ)

switching cycle

$$P_{\rm Ind\_fe} = \sum V_{e\_\rm ind} \cdot P_{Fe\_\rm ind}\left(v_{\rm ac}, D\right) = \sum V_{e\_\rm ind} \cdot K \cdot \left[\Delta B\left(v_{\rm ac}, D\right)\right]^{\alpha} {f_s}^{\beta}. \quad (4)$$

The relationship between incremental flux density ΔB, ac voltage $v_{\rm ac}$, and duty cycle D is given in (5), where $N_{\rm ind}$ is the turns of the inductor

$$\Delta B = \frac{v_{\rm ac} D}{N_{\rm ind} A_e f_s} = \frac{v_{\rm ac}\left(1 - \frac{v_{\rm ac}}{v_{\rm dc}}\right)}{N_{\rm ind} A_e f_s}. \quad (5)$$

Substituting (5) into (4) gives

$$P_{\rm Ind\_fe} = \sum V_{e\_\rm ind} \cdot K \cdot \left[\frac{v_{\rm ac}\left(1 - \frac{v_{\rm ac}}{v_{\rm dc}}\right)}{N_{\rm ind} A_e f_s}\right]^{\alpha} {f_s}^{\beta} = \sum V_{e\_\rm ind} \cdot K \cdot \left[\frac{v_{\rm ac}\left(1 - \frac{v_{\rm ac}}{v_{\rm dc}}\right)}{N_{\rm ind} A_e}\right]^{\alpha} {f_s}^{\beta-\alpha}. \quad (6)$$

Inductor winding loss $\rm P_{ind\_cu}$*:* The winding loss also includes two parts. One is the low-frequency conduction loss, which is generated by the fundamental ac current $I_{\rm fund\_rms}$. Under this low frequency, the resistance of the winding can be considered the same as its dc resistance $R_{\rm dc}$ if Litz wires are used. The other part is the high-frequency conduction loss, which is generated by switching frequency ac ripple current $I_{\rm ripple\_rms}$. This part of loss can be calculated by referring to the method given in [26]. A factor $F_r(f)$ is calculated to represent the increase of ac resistance related to the high switching frequency. The final equation is given in (7). For the selected Litz wires and 30-kHz switching frequency, $F_r(f) = 1.25$

$$P_{\rm ind\_cu} = P_{cu\_\rm dc} + P_{cu\_\rm ac} = R_{\rm dc} \cdot I^2_{\rm fund\_rms} + R_{\rm dc} \cdot F_r\left(f_s\right) \cdot I^2_{\rm ripple\_rms}. \quad (7)$$

Output capacitor loss $\rm P_{Co}$*:* The output capacitor is modeled as the resistor ESR connected with the ideal capacitor C_o

$$P_{Co} = \text{ESR} \cdot I^2_{Co\_\rm rms}. \quad (8)$$

The design parameters of the inductor and the capacitor are given in Table VI.

REFERENCES

[1] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of SiC MOSFETs in a T-type inverter for grid-tie applications," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2808–2821, Apr. 2017.

[2] C. S. Ner, A. Hensel, and J. Cambero, "Investigation of 3-level-topology MNPC for aerospace applications with SiC-MOSFET-based power modules," in *Proc. 8th IET Int. Conf. Power Electron., Mach. Drives*, 2016, pp. 1–6.

[3] H. Uemura, F. Krismer, and J. W. Kolar, "Comparative evaluation of T-type topologies comprising standard and reverse-blocking IGBTs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1288–1295.

[4] M. Gu, P. Xu, L. Zhang, and K. Sun, "A SiC-based T-type three-phase three-level grid-tied inverter," in *Proc. IEEE 10th Conf. Ind. Electron. Appl.*, 2015, pp. 1116–1121.

[5] H. Uemura, F. Krismer, Y. Okuma, and J. W. Kolar, "η-ρ Pareto optimization of 3-phase 3-level T-type ac-dc-ac converter comprising Si and SiC hybrid power stage," in *Proc. Int. Power Electron. Conf.*, 2014, pp. 2834–2841.

[6] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparison and implementation of a 3-level NPC voltage link back-to-back converter with SiC and Si diodes," in *Proc. Appl. Power Electron. Conf. Expo.*, 2010, pp. 1527–1533.

[7] Q. Chen, Q. Wang, G. Li, and S. Ding, "The control of unequal power losses distribution in three-level neutral-point-clamped VSC," in *Proc. 15th Int. Conf. Elect. Mach. Syst.*, 2012, pp. 1–5.

[8] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.

[9] G. L. Calzo, P. Zanchetta, C. Gerada, A. Gaeta, and F. Crescimbini, "Converter topologies comparison for more electric aircrafts high speed starter/generator application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 3659–3666.

[10] C. Qin, Q. Wang, Q. Chen, and G. Li, "Application of fuzzy PID with loss balancing control in three-level active NPC inverter," in *Proc. IEEE 10th Conf. Ind. Electron. Appl.*, 2015, pp. 1466–1470.

[11] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard, and R. G. Harley, "Improved modulation scheme for loss balancing of three-level active NPC converters," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2521–2532, Apr. 2017.

[12] B. Zhang, Q. Ge, P. Wang, X. Wang, and Y. Yu, "A novel modulation strategy providing loss balancing and neutral point potential balancing for three-level active neutral-point-clamped converter," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–9.

[13] L. Ma, T. Kerekes, P. Rodriguez, X. Jin, R. Teodorescu, and M. Liserre, "A new PWM strategy for grid-connected half-bridge active NPC converters with losses distribution balancing mechanism," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5331–5340, Sep. 2015.

[14] N. Achilladelis, E. Koutroulis, and F. Blaabjerg, "Optimized pulse width modulation for transformerless active-NPC inverters," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, 2014, pp. 1–10.

[15] J. Xin, J. He, and N. Demerdash, "Loss balancing SVPWM for active NPC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 281–288.

[16] D. Floricau, G. Gateau, A. Leredde, and R. Teodorescu, "The efficiency of three-level active NPC converter for different PWM strategies," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–9.

[17] D. Barater, C. Concari, G. Buticchi, E. Gurpinar, D. De, and A. Castellazzi, "Performance evaluation of a three-level ANPC photovoltaic grid-connected inverter with 650-V SiC devices and optimized PWM," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2475–2485, May/Jun. 2016.

[18] D. Floricau, G. Gateau, M. Dumitrescu, and R. Teodorescu, "A new stacked NPC converter: 3L-topology and control," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.

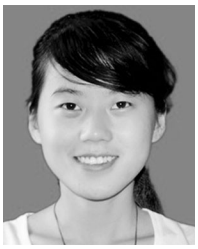
[19] D. Floricau, G. Gateau, E. Floricau, and A. Leredde, "Reducing of the average switching frequency using three-level active-SNPC converter," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–7.

[20] N. J. Ku, H. J. Jung, R. Y. Kim, and D. S. Hyun, "A novel switching loss minimized PWM method for a high switching frequency three-level inverter with a SiC clamp diode," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 3702–3707.

[21] K. Takao, Y. Tanaka, K. Sung, and K. Wada, "3-level power converter with high-voltage SiC-PiN diode and hard-gate-driving of IEGT for future high-voltage power conversion systems," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 1101–1107.

[22] L. Ravi, E. L. Severson, S. Tewari, and N. Mohan, "Circuit-level characterization and loss modeling of SiC-based power electronic converters," in *Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc.*, 2014, pp. 1291–1297.

[23] E. Gurpinar, D. De, A. Castellazzi, and D. Barater, "Performance analysis of SiC MOSFET based 3-level ANPC grid-connected inverter with novel modulation scheme," in *Proc. IEEE 15th Workshop Control Model. Power Electron.*, 2014, pp. 1–7.
[24] I. Josifovi, J. P. Gerber, and J. A. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3843–3854, Aug. 2012.
[25] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, 2002, pp. 36–41.
[26] F. Tourkhani and P. Viarouge, "Accurate analytical model of winding losses in round Litz wire windings," *IEEE Trans. Magn.*, vol. 37, no. 1, pp. 538–543, Jan. 2001.



Qing-Xin Guan (S'17) was born in Jilin Province, China. She received the B.S. degree in electrical engineering and automation from the Harbin Institute of Technology, Harbin, China, in 2013. She is currently working toward the Ph.D. degree in electrical engineering at the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China.

From June 1, 2017 until June 1, 2018, she is a Visiting Scholar with Ryerson University. Her research interests include high-efficiency inverter power supplies.

Chushan Li (M'17) received the B.E.E. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2014, respectively.

He is currently an Assistant Professor in Zhejiang University–University of Illinois at Urbana–Champaign Institute, Zhejiang, China. From April to September in 2008, he was an internship student with the Power Application Design Center, National Semiconductor (Hong Kong) Co. Ltd. From December 2010 to October 2011, he was a Visiting Scholar with the Freedm Center, North Carolina State University. From December 2013 to June 2014, he was a Research Assistant with Hong Kong Polytechnic University. From July 2014 to July 2017, he was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. His research interests include high-power-density power converter design and ac–dc power conversion.

Yu Zhang (M'11) was born in Jiangsu Province, China. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 1992, 1995, and 2005, respectively.

From 1995 to 2002, he was an Engineer working on power supply applications with Wuhan Telecommunication Company. He is currently a Professor at the School of Electrical and Electronic Engineering, HUST, where he teaches power electronics. He has developed several power systems, such as modular uninterruptible power supplies (UPSs). His research interests include power electronics modeling and control, parallel UPSs, and renewable energy generation.

Dr. Zhang is a member of the Power Electronic Systems and Equipment Standard Committee of China. He is a recipient of four Scientific and Technology Awards.

Shuai Wang (M'17) was born in Tianjin, China, in 1987. He received the B.S. degree in electrical engineering from the Tianjin University of Science and Technology, Tianjin, China, in 2009, and the M.S. and Ph.D. degrees in electrical engineering from Tianjin University, Tianjin, in 2016.

He is currently a Postdoctoral Fellow with Ryerson University, Toronto, ON, Canada. His research interests mainly include predictive control of power electronics and electrical drives and sensorless control of ac motors.

Dewei (David) Xu (S'99–M'01) received the B.Sc., M.A.Sc., and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1996, 1998, and 2001 respectively.

Since 2001, he has been with Ryerson University, Toronto, ON, Canada, where he is currently a Full Professor. His research interests include renewable energy systems, high-power converters, electric motor drives, and advanced digital control for power electronics.

Wuhua Li (M'09) received the B.Sc. and Ph.D. degrees in power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From 2004 to 2005, he was a Research Intern, and from 2007 to 2008, a Research Assistant with the GE Global Research Center, Shanghai, China. From 2008 to 2010, he was a Postdoctoral Researcher at the College of Electrical Engineering, Zhejiang University, where he became an Associate Professor in 2010 and has been a Full Professor since 2013. From 2010 to 2011, he was a Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He has authored or coauthored more than 200 peer-reviewed technical papers and holds more than 30 issued/pending patents. His research interests include power devices, converter topologies, and advanced controls for high-power energy conversion systems.

Dr. Li is an Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, *IET Power Electronics*, the *CSEE Journal of Power and Energy Systems*, and the *Proceedings of the Chinese Society for Electrical Engineering*, a Guest Editor of *IET Renewable Power Generation* Special Issue "DC and HVDC system technologies," and a member of the Editorial Board of the *Journal of Modern Power System and Clean Energy*. He was a recipient of the 2012 Delta Young Scholar from Delta Environmental and Educational Foundation, the 2012 Outstanding Young Scholar from the National Science Foundation of China, the 2013 Chief Youth Scientist of National 973 Program, the 2014 Young Top-Notch Scholar of National Ten Thousand Talent Program, and one National Natural Science Award and four Scientific and Technological Achievement Awards from Zhejiang Provincial Government and the State Educational Ministry of China. He was named as one of the Most Cited Chinese Researchers by Elsevier in 2014.

Hao Ma (M'99) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1991, 1994, and 1997, respectively.

He is currently a Professor at the College of Electrical Engineering, Zhejiang University. His current research interests include advanced control in power electronics, fault diagnosis of power electronic circuits and systems, and the application of power electronics.