Letters

Accurate Estimation of Diode Reverse-Recovery Characteristics From Datasheet Specifications

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***Abstract*—This letter proposes a structured approach for accurate estimation of diode reverse-recovery characteristics using datasheet specifications. Considering a conductance model of a diode, the entire reverse-recovery process is divided into four operating modes. The state equations for each mode are derived taking the circuit nonidealities, viz., device capacitance and parasitic inductances, into account. Analytical expressions for reverse-recovery charge, reverse-recovery time, and diode current are derived and numerically solved to estimate the diode conductance directly from manufacturer's data. An empirical model is proposed to characterize the effects of temperature variation on the diode conductance. Numerical simulation and experimental results are presented for antiparallel diodes of three MOSFETs having different current and voltage ratings and also for a discrete p-n diode at different junction temperatures. The maximum estimation error with the proposed approach is 5.1% for peak reverse-recovery current and less than 8% for reverse-recovery time, peak voltage, and energy loss.**

***Index Terms*—Conductance model, datasheet specifications, power diodes, reverse-recovery characteristics.**

I. Introduction

THE design of power converters for wide load and input voltage range applications necessitates thorough loss analysis to achieve high efficiency over the entire operating range. Though estimation of switching, conduction, and magnetic losses from respective component datasheets is quite straightforward [1], no designer-friendly method has been reported for accurate estimation of reverse-recovery loss directly from the diode datasheet. Conventional models [1], [2] for power diodes estimate reverse-recovery metrics using datasheet specifications, but neglect the effects of junction capacitance leading to a significant error in estimation. An analytical model [3] based on a piecewise linear approximation of state variables also neglects the switch capacitance and is thus unable to accurately estimate energy loss (E). Though the switch capacitance is considered in [4], estimation of E remains inaccurate as the steady-state value of the blocking voltage is used. A device-physics-based model [5] estimates only the voltage stress (V_p) across the diode, whereas estimation of peak reverse-recovery current ($I_{\rm rr}$), reverse-recovery time ($t_{\rm rr}$), and V_p is performed using finite-element analysis (FEA) [6]. But all these [3]–[6] require experimental measurements to determine the model input parameters and thus complicate the power converter design. Modeling the diode as a conductance, the nature of reverse recovery (soft/snappy) is analyzed in [7], and guidelines for custom fabrication are proposed. MOSFET switching losses are estimated in [8], considering the nonlinear switch capacitance. But none of these [7], [8] attempts to estimate reverse-recovery metrics of a commercial p-n diode.

The conductance model [7] is used in this letter to estimate the reverse-recovery characteristics of a p-n diode directly from its datasheet specifications. Considering the circuit nonidealities, state equations during different operating modes are derived and presented in Section II. To define the scope of the proposed method, a condition of validity is derived in Section II-A. Section III details a technique to estimate the diode conductance using manufacturer's data. Also, the variation in the diode conductance with the junction temperature is modeled in Section III-A. Numerical simulation and experimental results are presented in Section IV to validate the proposed method.

II. Operating Modes During Reverse Recovery

Fig. 1(a) shows the schematic of the reverse-recovery test circuit, and the switch transition involves turn-ON of M_2 and concurrent turn-OFF of diode D_1. The output current I_s is assumed constant over the reverse-recovery duration, usually much smaller than one switching period. The entire reverse recovery is divided into four subintervals, as explained in the following.

1) Mode 0: This dead-time interval begins when M_1 is turned OFF and I_s starts flowing completely through its antiparallel diode D_1. Denoting the respective currents through top and bottom switches as i_1 and i_2, the state equations are

$$i_1 = -I_s, \;\; v_1 = 0, \;\; i_2 = 0, \;\; v_2 = V_g. \tag{1}$$

Here, v_1 and v_2 represent the voltages across M_1 and M_2, respectively, and V_g is the input voltage.

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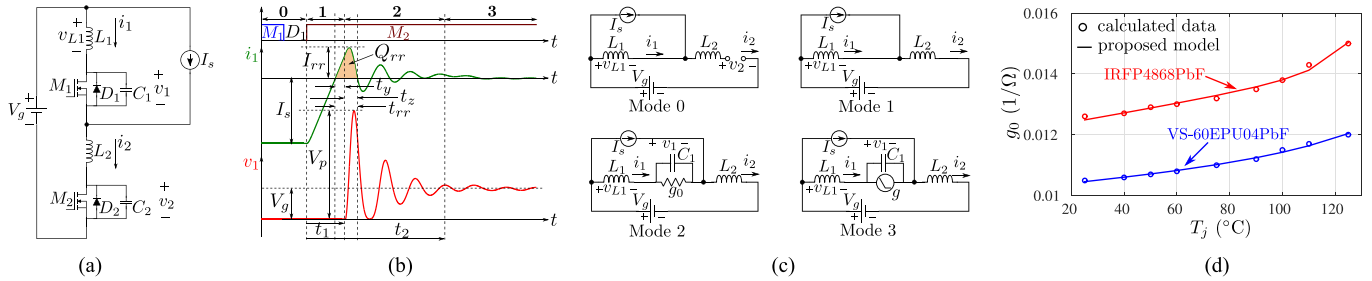

Fig. 1. (a) Schematic of the reverse-recovery test circuit. (b) Key waveforms. (c) Equivalent circuits for different operating modes during reverse recovery. (d) Variation of diode conductance with varying junction temperature.

TABLE I
COEFFICIENTS OF (6) AND (7)

Quantity	Expression	Quantity	Expression
ζ	$(g_0/2)\sqrt{L_e/C_1}$	A	$(at_y - (g_0V_g)/2)/\omega_d C_1$
ω_n	$1/\sqrt{L_e C_1}$	X	$at_y - g_0 V_g$
ω_d	$\omega_n\sqrt{1-\zeta^2}$	Y	$g_0 A/2 + \omega_d V_g C_1$

2) Mode 1 ($0 \le t \le t_1$): This mode starts after the dead-time interval, when M_2 is turned ON and I_s flows through both D_1 and M_2. Denoting the respective track inductances of top and bottom branches as L_1 and L_2, the state equations are

$$i_1 = -I_s + (I_s + at_y)(t/t_1), \quad v_1 = 0, \quad i_2 = i_1 + I_s \tag{2}$$

$$v_2 = 0, \; a = di_1/dt = di_2/dt = V_g/L_e, \; L_e = L_1 + L_2 \tag{3}$$

where the time interval t_y is defined in Fig. 1(b).

3) Mode 2 ($t_1 \le t \le t_2$): This mode begins when the diode becomes reverse biased. The stored charge is completely removed from its p-n$^-$ junction, and thus, v_1 starts rising [1]. Modeling diode D_1 as a constant conductance $g = g_0$ shown in Fig. 1(c), the mode equations are expressed as

$$L_1(di_1/dt') + v_1 + L_2(di_2/dt') = V_g, \quad t' = t - t_1 \tag{4}$$

$$i_1 = C_1(dv_1/dt') + gv_1, \quad i_2 = i_1 + I_s \tag{5}$$

where C_1 denotes the device capacitance. Solving (4) and (5), the state variables are expressed as

$$v_1 = V_g(1 - e^{-\zeta\omega_n t}\cos\omega_d t') + Ae^{-\zeta\omega_n t'}\sin\omega_d t' \tag{6}$$

$$i_1 = Xe^{-\zeta\omega_n t'}\cos\omega_d t' + Ye^{-\zeta\omega_n t'}\sin\omega_d t' + g_0 V_g. \tag{7}$$

The coefficients of (6) and (7) are listed in Table I, where ω_n denotes the natural frequency and ζ is the damping ratio. This mode ends when v_1 reaches 98% of its steady-state voltage, V_g, which means $t_2 - t_1 = 4/\zeta\omega_n$.

4) Mode 3 ($t_2 \le t < \infty$): Since D_1 acts as an open-circuit and blocks V_g in the steady state, the diode is modeled as $g = g_0(1 - \alpha t'')$, where $t'' = t - t_2$. The state equations remain the same as (4) and (5) during this mode. A somewhat empirical estimation is used to quantify α as $\alpha = \omega_d/4\pi$, which indicates that g takes two cycles of damped resonant frequency (ω_d) to reduce from g_0 to zero.

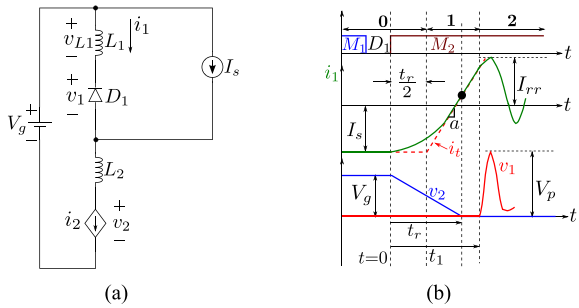

Fig. 2. (a) Equivalent circuit. (b) Key waveforms during the MOSFET turn-ON transition interval.

A. *Effect of MOSFET Turn-ON Transition Interval*

Considering finite turn-on interval (t_r) of M_2, it is modeled as a voltage-dependent current source [2], as shown in Fig. 2(a). Assuming linear variation in v_2, from V_g to zero, the state equations are expressed as

$$v_2 = V_g(1 - (t/t_r)), \quad i_2 = i_1 + I_s, \quad v_1 = 0 \tag{8}$$

$$L_1(di_1/dt) + L_2(di_2/dt) + v_2 = V_g. \tag{9}$$

Solving (8) and (9), i_1 is derived as

$$i_1 = -I_s + (a/2t_r)t^2. \tag{10}$$

An asymptotic approximation i_t of (10), indicated in Fig. 2(b), is based on matching the function and its gradient at $t = t_r$. So

$$i_t = -I_s - (at_r/2) + at. \tag{11}$$

Since $i_t(t_r/2) = -I_s$, the reference axis for the mode analysis is shifted from $t = 0$ to $t = t_r/2$. However, validity of this analysis necessitates reduction of v_2 to zero before v_1 starts rising, which obviously requires that

$$t_r \le t_1. \tag{12}$$

Equation (12) specifies the necessary condition for applicability of the proposed approach. However, it is satisfied in low- and medium-voltage converters, where fast devices, with low turn-ON time, are typically used to enable high-frequency switching.

III. ESTIMATION OF g_0 USING DATASHEET SPECIFICATIONS

Variation of the switch capacitance ($C_{\rm ds}$) with the blocking voltage ($v_{\rm ds}$) is modeled in (13) [8], and its coefficient set

TABLE II
DATASHEET SPECIFICATIONS AND DETAILS OF THE EXPERIMENTAL PROTOTYPE

	Input parameters for the proposed reverse-recovery characteristic estimation method																
	Datasheet parameters										Circuit parameters				Estimated parameters		
	Parameters used for g_0 estimation																
Device part number	γ	C_0 (pF)	V_0 (V)	V_B (V)	V_g (V)	a (A/μs)	Q_{rr} (nC)	t_{rr} (ns)	I_F (A)	r_{ds} (mΩ)	L_1 (nH)	r_1 (mΩ)	L_2 (nH)	r_2 (mΩ)	C_1 (pF)	g_0 (1/Ω)	R_{JC} (°C/W)
IRF1010EZ [9]	0.5	1330	0.6	60	30	100	81 (25 °C)	62 (25 °C)	51	15					240	0.009	1.11
IRFP4868PbF [10]	0.5	5800	0.32	300	255	100	3686 (125 °C) 2520 (25 °C)	454 (125 °C) 351 (25 °C)	42	72	140	250	130	200	367	0.015 0.0126	0.29
SiHG24N65E [11]	1	7100	4.45	650	25	100	7300 (25 °C)	433 (25 °C)	12	290					290	0.035	0.5
VS-60EPU04PbF [12]	0.5	1520	0.4	400	200	200	1120 (125 °C) 375 (25 °C)	145 (125 °C) 50 (25 °C)	60	–					94	0.012 0.0105	0.7

TABLE III
COEFFICIENTS OF g_0

Device part number	g_{01} (1/Ω)	T_1 (°C)	g_{02} (1/Ω)	T_2 (°C)
IRFP4868PbF	0.0121	813	2.42×10^{-8}	11.86
VS-60EPU04PbF	0.0102	1263	2.08×10^{-5}	34.66

TABLE IV
DETAILS OF DIFFERENT OPERATING CONDITIONS

Operating conditions	Device part number	V_g (V)	I_s (A)	f_s (kHz)	I_{1r} (A)	V_F (V)	T_c (°C)	T_j (°C)
O1	IRF1010EZ	19	2.1	188	2.45	–	34.5	34.81
O2	IRFP4868PbF	19	2.1	188	2.48	–	43.8	44.08
O3	SiHG24N65E	19	2.1	188	2.57	–	72.5	74.11
O4	IRF1010EZ	19	3.7	170	3.17	–	36.2	36.68
O5	SiHG24N65E	19	3.7	170	3.28	–	85.3	87.89
O6	SiHG24N65E (with capacitor)	19	3.7	170	3.25	–	97.5	99.95
O7	IRFP4868PbF	19	3.7	170	3.21	–	58.3	58.64
O8	IRFP4868PbF	19	3.7	170	3.27	–	123.5	123.85
O9	IRFP4868PbF	30	1.2	195	3.48	–	65.7	66.28
O10	IRFP4868PbF	30	1.2	195	3.53	–	128	128.6
O11	VS-60EPU04PbF	20	2	58	–	0.75	40.5	41.12
O12	VS-60EPU04PbF	40	1.6	58	–	0.7	48.8	49.41

$\{\gamma, C_0, V_0\}$, listed in Table II, is extracted from datasheet characteristics (C_{ds}–v_{ds}). The device capacitance at $v_{\text{ds}} = 0$ is denoted by C_0 and the parameters V_0 and γ decide the nature of C_{ds} variation with v_{ds}. Also, average capacitance C_1 in terms of the maximum blocking voltage V_B is

$$C_{\text{ds}} = C_0/(1 + (v_{\text{ds}}/V_0))^{\gamma}, \quad C_1 = \frac{1}{V_B}\int_0^{V_B} C_{\text{ds}}\, dv_{\text{ds}} \quad (13)$$

and is listed in the fifth column of Table II. For the test conditions, a and V_g, given in the datasheet, L_e is determined using (3). From Fig. 1(b), the reverse-recovery time (t_{rr}) is

$$t_{\text{rr}} = t_y + t_z. \quad (14)$$

The reverse-recovery charge Q_{rr}, clearly highlighted in Fig. 1(b), is the area enclosed by i_1 waveform in the interval $(t_1 - t_y) \le t \le (t_1 + t_z)$. So

$$Q_{\text{rr}} = 0.5at_y^2 + g_0 V_g t_z + (\omega_d + \zeta\omega_n + Be^{-\zeta\omega_n t_z})/\omega_n^2$$
$$B = (\omega_d - \zeta\omega_n)\sin\omega_d t_z - (\omega_d + \zeta\omega_n)\cos\omega_d t_z. \quad (15)$$

Since both t_{rr} and Q_{rr} are functions of g_0, t_y, and t_z, a third equation for the solution of g_0 is obtained from the first natural zero crossing of i_1 during Mode 2, as shown in Fig. 1(b). This third condition is derived using $i_1(t_1 + t_z) = 0$ and (7) as

$$Xe^{-\zeta\omega_n t_z}\cos\omega_d t_z + Ye^{-\zeta\omega_n t_z}\sin\omega_d t_z + g_0 V_g = 0. \quad (16)$$

Using the datasheet parameters, given in Table II, g_0 is estimated by numerically solving (14)–(16).

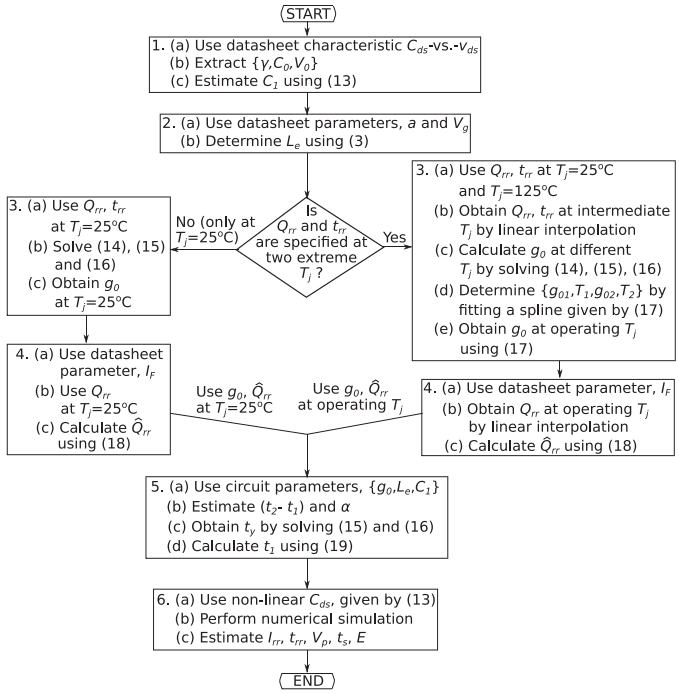

Fig. 3. Flowchart of the proposed estimation method.

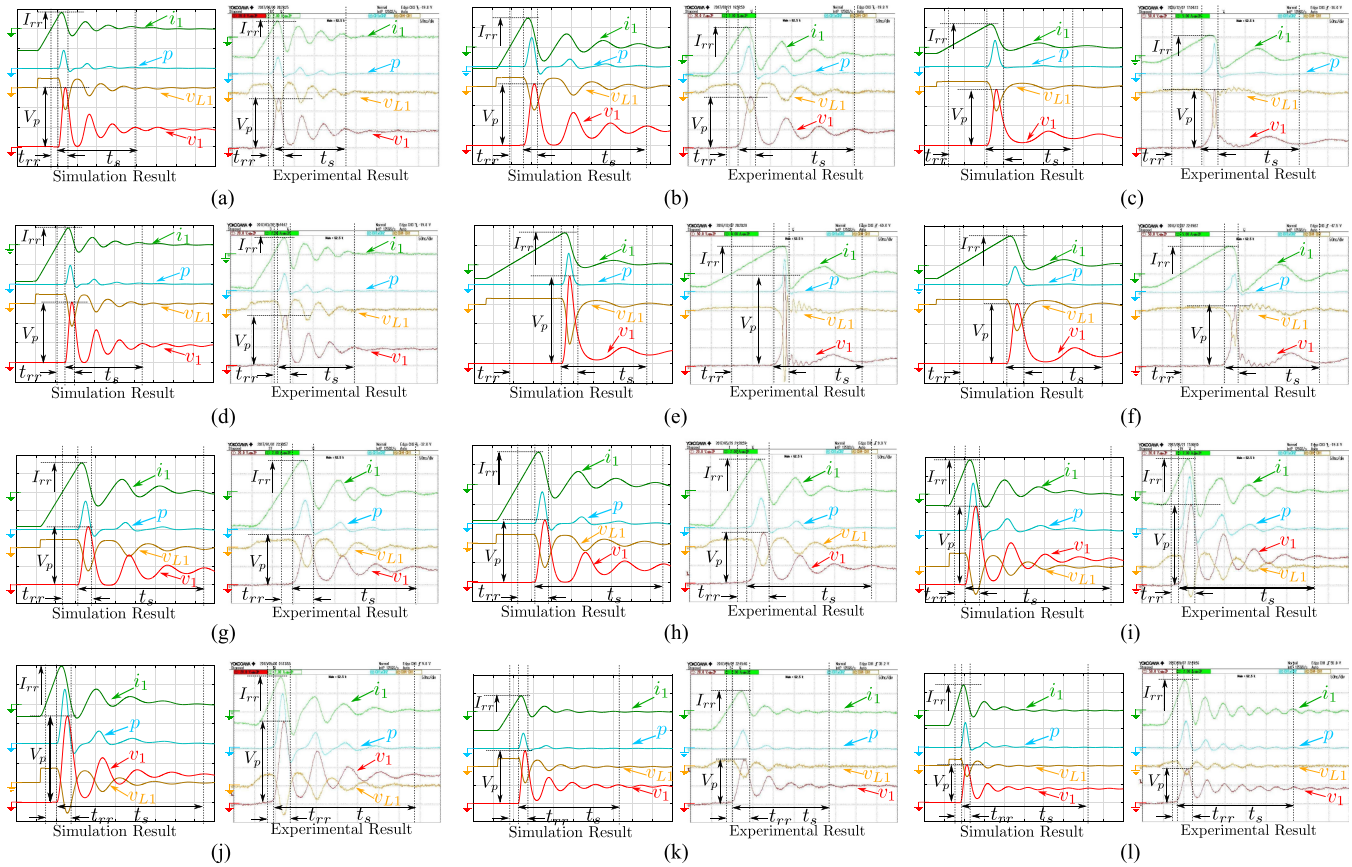

Fig. 4. Electrical variables during reverse recovery at different operating conditions. (a) O1, (b) O2, (c) O3, (d) O4, (e) O5, (f) O6, (g) O7, (h) O8, (i) O9, (j) O10, (k) O11, and (l) O12. Scale: (a), (b), (d), and (g)–(k) v_1, v_{L1} (20 V/div), i_1 (2 A/div), p (100 W/div); (c) v_1, v_{L1} (50 V/div), i_1 (5 A/div), p (500 W/div); (e) and (f) v_1, v_{L1} (50 V/div), i_1 (5 A/div), p (1 kW/div); and (l) v_1, v_{L1} (50 V/div), i_1 (2 A/div), p (200 W/div). X-axis—time: 50 ns/div.

A. *Effects of Temperature Variation on* g_0

Variation of g_0 with the junction temperature (T_j) is modeled as a double exponential of the form

$$g_0(T_j) = g_{01}e^{T_j/T_1} + g_{02}e^{T_j/T_2} \tag{17}$$

and the coefficient set $\{g_{01}, T_1, g_{02}, T_2\}$ is presented in Table III for two devices. Fig. 1(d) shows close agreement between this model and the data derived from device datasheets. For the devices IRFP4868PbF and VS-60EPU04PbF, respective variations in g_0 are noted to be 19% and 14.3% during the variation in T_j from 25 to 125 °C.

IV. Results and Discussions

A laboratory-prototype of a synchronous buck dc–dc converter [1] is fabricated, and its schematic is shown in Fig. 1(a). Different operating conditions, O1–O10, detailed in Table IV, are obtained by adjusting the switching frequency (f_s), the duty ratio (D), and the load resistance. Considering the nonlinear device capacitance, track inductances and resistances (r_1 and r_2 at 20 MHz), and MOSFET ON-resistance (r_{ds} at 125 °C), given in Table II, the entire reverse-recovery process is coded in MATLAB Simulink. Since successive solutions of the mode equations require time intervals of each mode, first, the quantities $(t_2 - t_1)$ and α are directly estimated using the circuit parameters (g_0, L_e, and C_1). To derive t_1, the actual Q_{rr}, $\hat{Q}_{rr}$, is

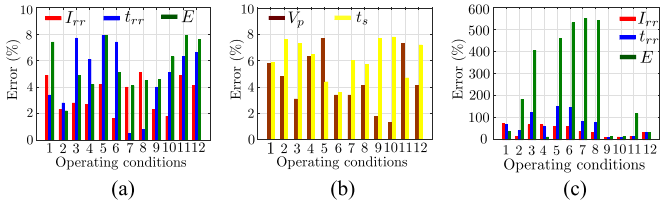

Fig. 5. Errors in estimation. (a) I_{rr}, t_{rr}, and E. (b) V_p and t_s while using the proposed method. (c) Estimation errors while using the conventional approach.

estimated using

$$\hat{Q}_{rr} = (Q_{rr}I_s)/I_F \tag{18}$$

where I_F is the forward current given in the datasheet. Replacing $Q_{rr} = \hat{Q}_{rr}$ in (15), t_y is obtained by solving (15) and (16) numerically, and t_1 is expressed as

$$t_1 = (I_s L_e/V_g) + t_y. \tag{19}$$

A complete flowchart of the proposed estimation method is presented in Fig. 3.

Inevitable attenuation and phase lag in the current (TCP312: 100 MHz) and voltage (DLM2054: 500 MHz) measurement probes are modeled in simulation as first-order low-pass filters. Simulation and experimental results at $V_g = 19$ V and $I_s = 2.1$ A are shown in Fig. 4(a)–(c), where v_{L1} denotes the voltage across L_1 and p is the power loss in D_1. Fig. 4(a)–(c)

TABLE V
INPUT PARAMETERS OF DIFFERENT ESTIMATION TECHNIQUES

	Conventional model [1]		Analytical model [3]							Extraction method [4]		Voltage model [5]					FEA based model [6]					
	Q_{rr}	I_F	Q_{rr}	I_F	$\frac{dI_{TF+}}{dt}$	$\frac{dI_{TF-}}{dt}$	$\frac{dI_{RR}}{dt}$	$\frac{dI_{Tail}}{dt}$	$\frac{dV}{dt}$	τ_p	t_1	t_1	t_y	τ_n	τ^*	τ_r	Q_{rr}	I_F	V_B	W_D	N_D	A
Datasheet	√	√	√	√													√	√	√			
Experiment					√	√	√	√	√	√	√	√	√	√	√	√				√	√	√

indicates that $I_{\rm rr}$ increases with voltage rating of the devices, due to higher $Q_{\rm rr}$. Fig. 4(d), (e), and (g) show higher $I_{\rm rr}$ compared to Fig. 4(a)–(c) for all the devices due to increased forward current ($I_s = 3.7$ A). A 220-pF capacitor is placed across M_1 while using SiHG24N65E, and significant reduction in V_p is evident in Fig. 4(f) compared to Fig. 4(e). Fig. 4(i) shows higher $I_{\rm rr}$ compared to Fig. 4(b) even at a lower forward current ($I_s = 1.2$ A), which is due to higher input voltage ($V_g = 30$ V).

To calculate energy loss (E), first, the gain and phase distortions due to the finite probe bandwidth in the measured samples of i_1 and v_1 are corrected. Then, their harmonic components (I_k and V_k) are obtained using the fast Fourier transform and E is determined using Parseval's theorem as

$$E = (2t_n/N)\sum_{k=0}^{N/2} I_k V_k. \tag{20}$$

Here, t_n is the scope resolution (8 ps) and N is the total number of data points (62 500). A mismatch in simulation and experimental data is calculated using $\text{Error} = ||\text{Exp} - \text{Sim}||/\text{Exp}$. Estimation errors for $I_{\rm rr}$, $t_{\rm rr}$, E and V_p, t_s are shown in Fig. 5(a) and (b), respectively. The maximum estimation error for $I_{\rm rr}$ is 5.1%, while for the other reverse-recovery metrics, it is below 8%, which validates the proposed method.

Device case temperature (T_c) is directly measured using a contact thermometer (Fluke-568) and presented in Table IV. Considering reverse-recovery, switch turn-ON, and conduction losses, the total power loss (P_t) in M_1 is obtained using (21). Here, I_{1r} denotes the measured rms current through M_1, listed in Table IV. Considering the junction-to-case thermal resistance ($R_{\rm JC}$), given in Table II, T_j is calculated using [1]

$$T_j = T_c + P_t R_{\rm JC},\ P_t = (E + 0.5C_1V_g^2)f_s + I_{1r}^2 r_{ds} \tag{21}$$

and listed in Table IV for the operating conditions O1–O10. Numerical simulation is carried out for O2 and O7–O12, with accurate $\hat{Q}_{\rm rr}$ and g_0 values, at the corresponding T_j. From datasheet values of $Q_{\rm rr}$, at two extreme temperatures, accurate $Q_{\rm rr}$ at any T_j is obtained by linear interpolation, and then, $\hat{Q}_{\rm rr}$ is calculated using (18). But accurate g_0 at any T_j is directly estimated using (17). To capture experimental results at higher T_j, the device case of IRFP4868PbF is heated using a hot air blower. The results for $V_g = 19$ V and $I_s = 3.7$ A are shown in Fig. 4(g) and (h) at $T_j = 58.64$ °C and $T_j = 123.85$ °C, respectively. Fig. 4(i) and (j) depict the respective results for $T_j = 66.28$ °C and $T_j = 128.6$ °C when $V_g = 30$ V and $I_s = 1.2$ A. These results indicate that the effects of temperature variation on reverse recovery are insignificant. However, Fig. 5(a) and (b) show excellent estimation accuracy, which validates the proposed approach at different junction temperatures.

TABLE VI
ACCURACY COMPARISON OF DIFFERENT ESTIMATION TECHNIQUES

Different techniques	Maximum errors (%) in estimation $I_{\rm rr}$	$t_{\rm rr}$	V_p	E	t_s
Proposed method	5.1	7.9	7.7	7.8	7.9
Conventional model [1]	73	151	NE	551	NE
Analytical model [3]	NE	NE	NE	20	NE
Extraction method [4]	NE	7.6	NE	13.6	NE
Voltage model [5]	NE	NE	5.5	NE	NE
FEA-based model [6]	25	20	16	NE	NE

NE: Not estimated.

The top device of the synchronous buck converter is replaced by a discrete diode, and the duty ratio (D) is set at 0.45. Two different operating conditions, O11 and O12, are obtained by varying V_g and load resistance. Denoting diode forward voltage drop as V_F, T_j is calculated using [1]

$$T_j = T_c + P_t R_{\rm JC},\ P_t = Ef_s + (1-D)V_F I_s \tag{22}$$

and listed in Table IV. Fig. 4(k) and (l) shows the respective results for O11 and O12. Maximum errors in estimation of $I_{\rm rr}$ and E are noted to be below 5% and 7%, respectively, which validates the proposed technique for discrete p-n diodes also.

As evident from Table V, the techniques, [3]–[6], necessitate experimental measurements. But similar to the proposed method, the conventional model requires only an estimate of the parasitic inductance (L_e) obtainable using any standard software tool [13] for a given circuit layout. Estimation of $I_{\rm rr}$, $t_{\rm rr}$, and E using this model causes unacceptably large errors, as shown in Fig. 5(c). Maximum estimation errors for other approaches, as claimed by the respective authors, are detailed in Table VI. Clearly, the proposed method not only estimates all the reverse-recovery metrics, but the achievable accuracy is also better compared to most of the existing techniques.

V. CONCLUSION

A structured approach is proposed for accurate estimation of diode reverse-recovery characteristics using datasheet specifications. Considering switch capacitance and parasitic inductances, the state equations are derived based on the conductance model of a diode. Analytical expressions for the reverse-recovery charge, the reverse-recovery time, and the switch current are obtained and numerically solved to estimate the diode conductance directly from the device datasheet. An empirical model is proposed to represent the variation in the diode conductance with varying junction temperature. Numerical simulation and experimental results are presented for antiparallel diodes of

three MOSFETs having different voltage and current ratings and also for a discrete p-n diode at different junction temperatures. The maximum error in estimation of $I_{\rm rr}$ is noted to be 5.1%, whereas errors occurred during estimation of $t_{\rm rr}$, V_p, and E are less than 8%. The proposed method can be a useful tool for loss analysis and optimal design of low- and medium-voltage converters. Also, the diode current waveform obtained from this method can be directly used to determine the frequency spectrum of electromagnetic interference emission [14].

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