A Three-Phase Symmetrical DC-Link Multilevel Inverter With Reduced Number of DC Sources

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***Abstract*—This paper presents a novel three-phase DC-link multilevel inverter topology with reduced number of input DC power supplies. The proposed inverter consists of series-connected half-bridge modules to generate the multilevel waveform and a simple H-bridge module, acting as a polarity generator. The inverter output voltage is transferred to the load through a three-phase transformer, which facilitates a galvanic isolation between the inverter and the load. The proposed topology features many advantages when compared with the conventional multilevel inverters proposed in the literatures. These features include scalability, simple control, reduced number of DC voltage sources, and less devices count. A simple sinusoidal pulse-width modulation technique is employed to control the proposed inverter. The performance of the inverter is evaluated under different loading conditions and a comparison with some existing topologies is also presented. The feasibility and effectiveness of the proposed inverter are confirmed through simulation and experimental studies using a scaled down low-voltage laboratory prototype.**

***Index Terms*—DC-link inverter, half-bridge module, hybrid multilevel inverter, symmetric DC voltage supply.**

I. Introduction

MULTILEVEL inverters have received great attention from both academia and industry in the past few decades due to their distinctive features compared to their conventional two-level counterparts [1], [2]. These include, lower switching losses and stress on the semiconductor devices, high quality output waveforms, reduced electromagnetic interference, and smaller filtering requirements [3]–[6]. Cascaded multilevel inverters (CMLI) have received special preference in various industrial applications, especially, renewable energy integration [5], [7], [8]. This is particularly because of their modularity and redundancy features along with the absence of complicated capacitor voltage balancing issue, which is a common problem with other topologies such as diode and capacitor clamped inverters [9]–[11]. Several variations of CMLI circuit topology have been documented in the open literature, aiming to increase the attained voltage levels, which ultimately improve the quality of the output waveform [12]. Hybrid (or else known as asymmetric) cascaded multilevel inverter is one of the proposed variations, where different input voltage levels are usually considered [13]–[16]. Reduced device count can be achieved with hybrid CMLIs, however, lack of modularity and unequal voltage distribution on the power switches makes them unattractive for utility-grade applications. On the other hand, another major challenge with CMLIs is the need for independent isolated DC power supplies, which impose additional restrictions and complexity, especially when higher number of levels in the output voltage waveform is required. Several attempts have been reported in the open literature aimed to reduce the required number of the DC power supplies [11], [17]–[19].

For instance, Ruiz-Caballero *et al.* [19], Gui-Jia [20], and Babaei and Hosseini [21] proposed a new CMLI comprising half-bridge cells to synthesize the unipolar staircase-shape waveform and a full-bridge inverter as a polarity generator. This has considerably reduced the devices count and the required number of DC power supplies compared with conventional multilevel inverters. Some balancing capacitors are utilized within the half-bridge modules to reduce the number of rectifiers in [19]. However as mentioned in [11], balancing these capacitors requires a complicated control scheme. An extension of the topology proposed in [20] and [21] was recently reported in [11], where a further reduction in the required DC power supplies was achieved, however a possible extension to three-phase system was not reported.

A modular three-phase half-bridge based CMLI is proposed in [22]–[24]. However, these topologies require a higher number of isolated DC-supplies, which increases the cost and complexity as well as the requirement for a complicated modulation technique. Hybrid three-phase CMLI is reported in [17] and [18], where the cascaded half-bridge cells are connected with a three-phase voltage source inverter. This has significantly reduced the number of the semiconductor devices as well as the required DC supplies. However, the need for isolated DC power supplies could not be avoided.

Another variation of the topologies studied in [11] was proposed in [25] and [26], where only a single DC power supply is used and the other levels of the output waveform were realized through floating capacitors. However, it is evident that this topology is highly load-dependent and requires

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sophisticated capacitor voltage balancing algorithms, especially if high number of output voltage levels is considered.

Multiwinding transformers are utilized in [27] and [28] to maximize the output voltage levels. The inverter uses only a single DC power supply and the secondary windings of the single-phase transformers are cascaded to form the multilevel output voltages, where the number of levels is a function of the transformers' turns ratios. Although this has helped to reduce the required DC power supplies, the large number of single-phase transformers makes it impractical and not attractive as the size and complexity increases with each additional level in the output voltage [11].

In overall, the above discussion reveals that efforts have been made on CMLI to either reduce the device-count or DC power supplies or both. While the reduction of DC power supplies was achievable for single-phase CMLI [11], it becomes at least three times when extended to three-phase version [17]–[20], [22].

Therefore, this paper proposes a new symmetric three-phase CMLI based on half-bridge cells with reduced number of DC power supplies. This topology can be considered as an extension and upgrade version of the three-phase topology proposed in [19] and [20]. However, nearly 30% more voltage levels in the line voltages can be achieved by utilizing the same number of semiconductor devices. Furthermore, the proposed topology reduces nearly 67% of the rectifiers required as input DC supplies for the symmetric half-bridge modules.

The rest of the paper is organized as follows: Section II presents the operation principle of the proposed symmetric CMLI along with its modulation technique. Section III presents and discusses selected simulation and experimentally validated results. Comparison between the proposed topology and conventional CMLI is drawn in Section IV. Finally, the work is concluded in Section VI.

II. Proposed Multilevel Inverter and Its Modulation Strategy

Fig. 1 illustrates the proposed CMLI, which consists of two stages. The first stage is a level generator, which generates the unipolar multilevel voltage waveforms by utilizing the cascaded half-bride modules. As shown in Fig. 1, each three half-bridge modules in the three-phase legs-A–C are fed from a nonisolated DC power supply. In reality, the DC -power supplies can be battery sources, or rectifier output terminals. Furthermore, the DC supplies can be equally obtained from photovoltaic (PV) output terminals or other renewable energy source. To realize constant output power and voltage for renewable energy sources of intermittent characteristics, some control algorithms such as constant voltage source mode can be employed [29]. It is worth noting that the half-bridge modules will have the same blocking voltage requirement since they are connected across the same DC-supply. This ensures modularity and simple control methods. The second stage is the polarity generator, which utilizes a simple full-bridge inverter to bipolarize the multilevel output voltage waveforms produced by the first stage.

A three-phase transformer couples the outputs of the polarity generator with the load, providing a galvanic isolation as well as

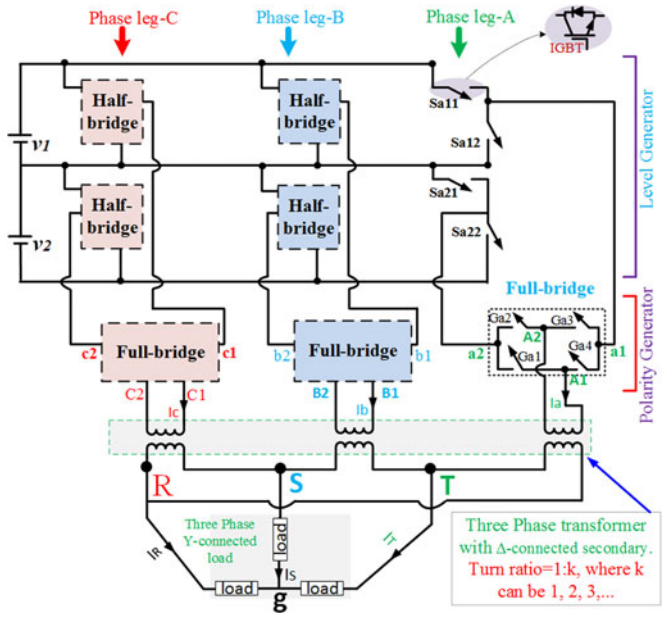

Fig. 1. Proposed three-phase CMLI with two half-bridge cells per phase leg.

boosting to the output voltage. It should be noted that although in Fig. 1 the transformer secondary windings are connected in Δ, it could be also connected in Y, if required. Furthermore, the CMLI presented in Fig. 1 can be easily expanded to generate higher number of levels in the output voltage waveform by adding more half-bridge modules into the level generator. The number of levels, m in the output voltage of each polarity generator by utilizing n-number of half-bridge modules in each phase leg is given by

$$m = 2n + 1. \tag{1}$$

Considering equal input DC voltages $(v_1, v_2, \ldots, v_n)$ to the n-number of the half-bridge modules in the level generator stage, the input DC voltages can be written as

$$v_1 = v_2, \ldots = v_n = V_{\mathrm{DC}} \tag{2}$$

where V_{DC} represents a constant value.

While the half-bridge modules in the level generator utilize low voltage, high switching frequency devices, the low frequency switches used in the full-bridge modules in the polarity generator experience a voltage stress of a magnitude equals to the summation of the input DC voltage sources [20]. Hence, the voltage stress or standing voltage, $V_{pg,\mathrm{stress}}$ on the polarity generator switches can be expressed as

$$V_{pg,\mathrm{stress}} = nV_{\mathrm{DC}}. \tag{3}$$

It is to be noted that because they are operating at the fundamental switching frequency of 50 Hz, full-bridge modules do not exhibit significant switching losses. On the other side, state-of-the-art technology currently offers switching devices such as Insulated Gate Bipolar Transistors (IGBT)-module, FZ500R65KE3 that can withstand a collector to emitter voltage up to 6.5 kV [30]. Moreover, the operating voltage capacity of the switching devices can be extended by connecting multiple

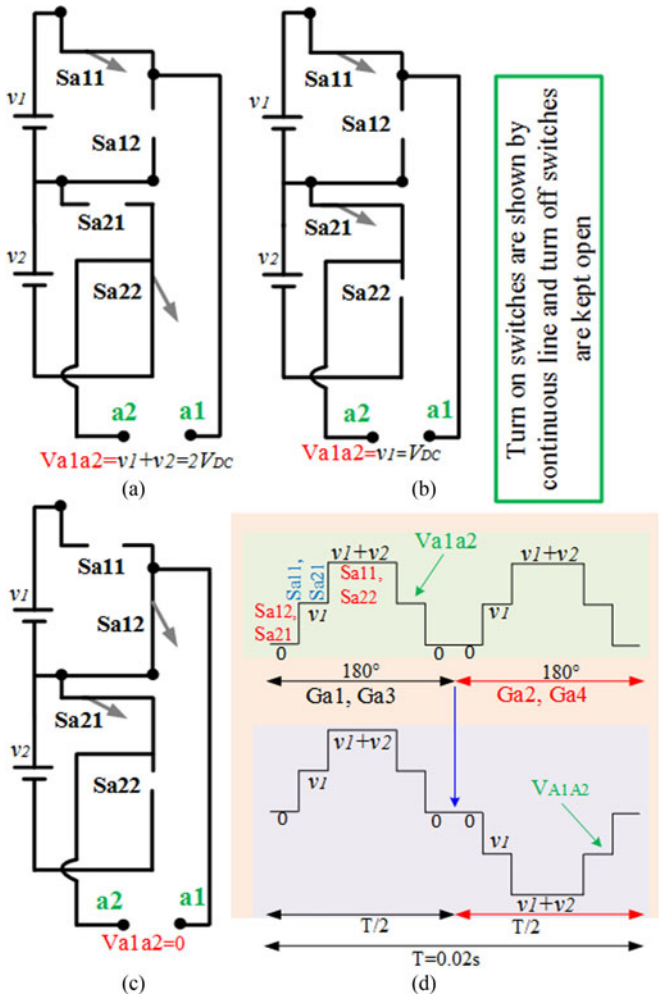

Fig. 2. Switching logics for generating different levels in the level generator output voltages: (a) Logic for generating $2V_{\mathrm{DC}}$, (b) logic for generating V_{DC}, (c) logic for generating 0, and (d) desired output in the level generator and polarity generator output voltage.

switches in series. A number of CMLIs topologies utilizing half-bridge and H-bridge modules have been implemented for high-voltage applications and can be found in the literatures [19], [31]. The rating of the switching devices in the proposed CMLI can be identified according to the voltage requirement of the intended application. It is worth mentioning that as the three-phase transformer is an essential component in the proposed topology, it will inherently fulfill the galvanic isolation requirement for renewable energy grid-connected applications [31].

Fig. 2(a)–(c) shows the different switching states of the level generator, producing different output voltage levels $(v_1 + v_2, v_1, 0)$. Fig. 2(d) illustrates the generated ac output voltage in the polarity generator at phase leg-A, where the polarity generator flips the waveform in every 180°.

The main focus of this paper is to develop a new inverter topology. Conventional sinusoidal pulse-width modulation (SPWM) technique is a well known and easy to implement technique [32]. Hence, SPWM is adopted to demonstrate the effectiveness of the proposed topology. As shown in Fig. 3, the reference signals, Ref-a, Ref-b, and Ref-c are the rectified sinusoidal waveforms

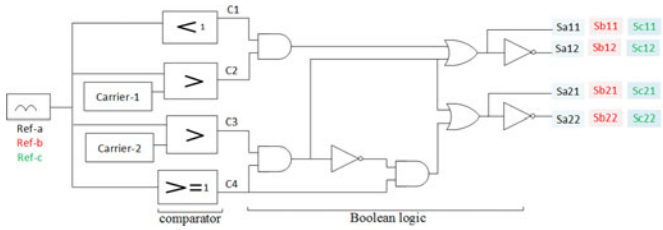

Fig. 3. Block diagram of the modulation technique.

with a 120° phase shift from each other. These are then compared with two carrier signals (carrier-1 and carrier-2) to generate the required gating signals. Same switching signals generation logic is utilized for each phase leg.

III. Semiconductor Losses and Converter Efficiency

The semiconductor losses are considered as a crucial design and selection criterion for any converter circuit as they influence and define the required thermal management, which contributes to the estimation of the overall cost/volume/weight of the inverter. There are two dominant losses in the semiconductor devices; the static and the dynamic losses. The on-state resistance and the forward voltage drop of the semiconductor devices are responsible for the conduction losses, while the dynamic losses are produced during the turn on/off actions dictated by the switching frequency of the device.

The instantaneous conduction losses of a transistor $(\sigma_{c,T})$ and a diode $(\sigma_{c,D})$ at any instant of time (t) can be expressed as

$$\left.\begin{aligned}\sigma_{c,T}(t) &= \left[V_T + R_T\, i^{\beta}(t)\right] i(t)\\ \sigma_{c,D}(t) &= \left[V_D + R_D\, i(t)\right] i(t)\end{aligned}\right\} \tag{4}$$

where the on-state voltage drops of the transistor and diode are expressed by V_T and V_D, respectively. The on-state resistances of the transistor and diode, are given by R_T and R_D, respectively. β and $i(t)$ are the transistor amplification factor and a transistor or diode current at any instant of time, respectively.

Hence, the average conduction losses in both, the transistor and the diode, denoted by $P_{c,T}(t)$ and $P_{c,D}(t)$, respectively are given by

$$\left.\begin{aligned}P_{c,T}(t) &= \tfrac{1}{2\pi}\int_0^{2\pi}\left[\{V_T + R_T i^{\beta}(t)\} i(t)\right] d(\omega t)\\ P_{c,D}(t) &= \tfrac{1}{2\pi}\int_0^{2\pi}\left[\{V_D + R_D\, i(t)\} i(t)\right] d(\omega t)\end{aligned}\right\}. \tag{5}$$

The total average conduction losses can then be calculated from

$$P_c(t) = \int_0^{2\pi}\left[\{N_{\mathrm{Transistor}}(t) * P_{c,T}(t)\} + \{N_{\mathrm{Diode}}(t) * P_{c,D}(t)\}\right] d(\omega t) \tag{6}$$

where $N_{\mathrm{Transistor}}$ and N_{Diode} are the number of transistors and diodes, respectively, in the same current path at any instant of time.

Similarly, the total switching power losses of the semiconductor devices are calculated by the energy losses during turn-on (t_{on}) and turn-off (t_{off}) periods. The switching energy losses

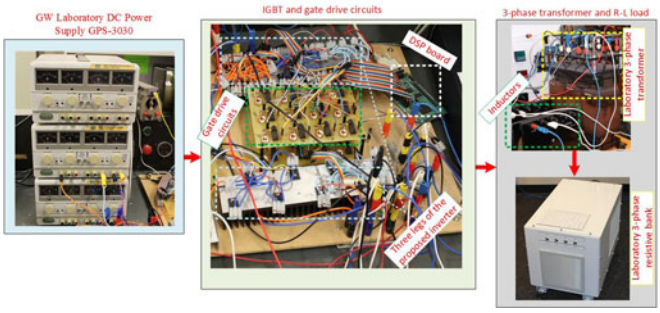

Fig. 4. Experimental test-rig setup.

during turn-on $(E_{\rm on})$ and turn-off $(E_{\rm off})$ can be derived from

$$\left.\begin{aligned} E_{\rm on} &= \int_0^{t_{\rm on}} v(t)i(t)dt = \int_0^{t_{\rm on}} \left[\left(\tfrac{V_{\rm sw}}{t_{\rm on}} * t\right)\left(-\tfrac{I}{t_{\rm on}}\right) \right. \\ &\quad \left. * (t - t_{\rm on})\right] dt = \tfrac{1}{6} V_{\rm sw} * I * t_{\rm on} \\ E_{\rm off} &= \int_0^{t_{\rm off}} v(t)i(t)dt = \int_0^{t_{\rm off}} \left[\left(\tfrac{V_{\rm sw}}{t_{\rm off}} * t\right)\left(-\tfrac{I'}{t_{\rm off}}\right) \right. \\ &\quad \left. * (t - t_{\rm off})\right] dt = \tfrac{1}{6} V_{\rm sw} * I' * t_{\rm off} \end{aligned}\right\} \quad (7)$$

where $V_{\rm sw}$ and I, represent the off-state voltage and current of the device, respectively. I' represents the device current measured just before the device is turned off.

The total switching power losses $(P_{\rm sw})$, for a time-period T can be calculated from

$$P_{\rm sw} = \frac{1}{T}\left[\sum_{1}^{N_{\rm switch}} \{(N_{\rm on} * E_{\rm on}) + (N_{\rm off} * E_{\rm off})\}\right] \quad (8)$$

where the number of turn-on and off counts of a switch in a cycle is given by $N_{\rm on}$ and $N_{\rm off}$, respectively.

The overall semiconductor losses of the proposed CMLI can be estimated by the total conduction and switching losses of all used semiconductors, expressed as

$$P_{\rm total\_loss} = P_c(t) + P_{\rm sw}. \quad (9)$$

If the output power is $P_{\rm out}$, the inverter efficiency (η) can be calculated from

$$\eta\% = \left(\frac{P_{\rm out}}{P_{\rm total\_loss} + P_{\rm out}}\right) * 100\% \quad (10)$$

where the output power is calculated from

$$P_{\rm out} = \sqrt{3} * \frac{3V_{\rm DC}}{\sqrt{2}} * \frac{I_{\rm line}}{\sqrt{2}} * {\rm PF}. \quad (11)$$

If the power factor (PF) of the connected load is nearly 0.8 lagging, when connecting a load of $20 + {\rm j}15.7\,\Omega$ in each phase leg, using (10), the output power is 98.64 watts, which gives an overall efficiency of about 97%.

IV. Simulation and Experimental Results

Fig. 4 illustrates the experimental test-rig of the proposed inverter, developed at the Green Electric Energy Park, Curtin University [33]. On the other hand, simulation analysis is carried out using the MATLAB/Simulink software package. The main parameters of the inverter prototype are summarized in Table I. The input DC voltages from the "GW Laboratory DC power supplies GPS-3030" are set to provide a constant DC voltage of 60 V, i.e., $(v_1 = v_2 = 60\,{\rm volts})$. Both, the level generator and polarity generator stages require twelve IGBTs, each. A digital signal processor (DSP), TMS320F2812 is used to generate the real time switching gate signals. The gate signals from the DSP are connected to the IGBT gates through 24-gate drive circuits. The role of gate drive circuits is to isolate the common ground of the DSP output gate pulses and boost-up their magnitudes to nearly 15 volts. As shown in Fig. 4, there are two printed circuit boards comprising 24-gate drive circuits for the 24 IGBTs in the level generator and polarity generator stages.

TABLE I
Properties System Specifications of the Proposed Inverter

Input DC sources (v_1, v_2)	60 V each
Carrier frequency	4 kHz
Switching controller	TMS320F2812
Ratings of IGBT	HGTG20N60B3D
Magnitudes of the line voltages	270 V (peak)
Number of levels in line voltages	13

In this paper, the conventional SPWM modulation strategy is considered with a carrier frequency of 4 kHz for both, simulation and experimental studies. The modulation index M_i is expressed as [32]

$$M_i = \frac{A_m}{(N_p - 1)\,A_c} \quad (12)$$

where A_m is the magnitude of the reference sine waveform and A_C is the magnitude of the carrier signal. Modulation index, M_i has an influence on the magnitude of the output line voltages and line currents [32]. The output of the polarity generator is connected to the primary of a three-phase isolation transformer with a turn ratio of 1:1, as shown in Fig. 4.

As previously mentioned, the secondary side of the transformer can be connected in either Δ or Y. The output line voltages can therefore be presented by (13) or (14) for Δ or Y connection, respectively

$$\begin{bmatrix} V_{\rm RS} \\ V_{\rm ST} \\ V_{\rm TS} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{C1C2} \\ V_{B1B2} \\ V_{A1A2} \end{bmatrix} \quad (13)$$

$$\begin{bmatrix} V_{\rm RS} \\ V_{\rm ST} \\ V_{\rm TS} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}\begin{bmatrix} V_{C1C2} \\ V_{B1B2} \\ V_{A1A2} \end{bmatrix}. \quad (14)$$

The performance of the proposed inverter under various loading conditions is assessed as elaborated in the following case studies.

A. Case Study 1: The Impact of Load Power Factor

Fig. 5 shows the simulation results of the line voltage and line current waveforms of the proposed inverter under load power factor of nearly 0.8 (lagging) and unity power factor, when each phase leg is connected with balanced inductive loads of $(20 + {\rm j}15.7\,\Omega)$ and $(20 + {\rm j}1.57\,\Omega)$, respectively.

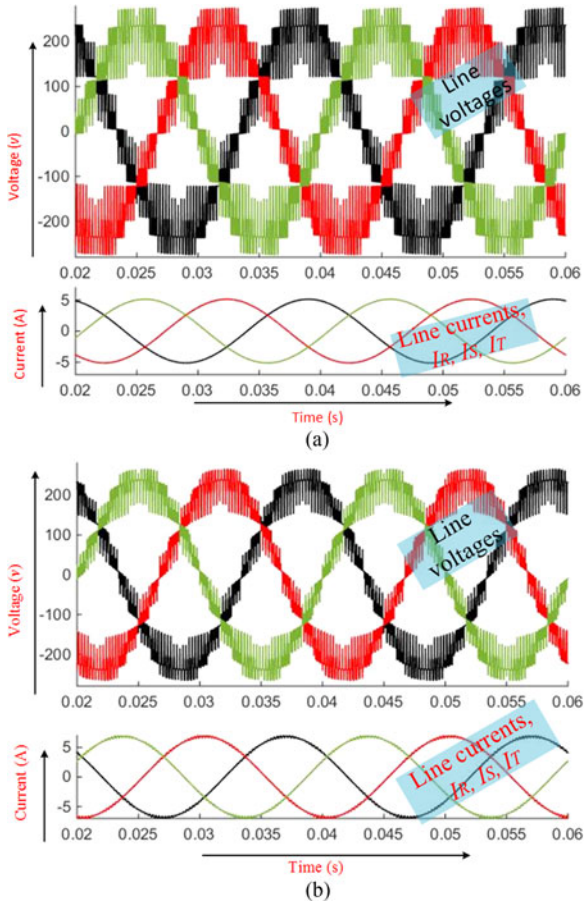

Fig. 5. Simulation results of the output line voltages and line currents for (a) load of nearly 0.8–lagging power factor and (b) load of nearly unity power factor.

On the other hand, Figs. 6 and 7 illustrate different experimental results for nearly 0.8 lagging and unity power factor loads, respectively. Tektronix TPS2014B digital storage oscilloscope is utilized for capturing the experimental waveforms and displaying their harmonic spectrums. It is worth mentioning that, no harmonic filters were utilized while taking the results. Figs. 6(a) and 7(a) illustrate the experimental gating signals for both, the level generator and polarity generator switches, S_{a11}, S_{a21}, G_{a1}, and G_{a2} in phase leg-A. The corresponding level generator output voltage (V_{a1a2}), the polarity generator output voltage (V_{A1A2}), line voltage (V_{TR}), and line current (I_T) are shown in Figs. 6(b) and 7(b). Moreover, Figs. 6(c)–(d) and 7(c)–(d) show the three-phase line voltages and line currents, respectively.

The total harmonic distortions (THD) of the line voltage and line current waveforms of the two cases above are shown in Figs. 8 and 9, respectively. It can be observed that the change of the load PF from 0.8 lagging to unity does not influence the number of levels in the line voltage waveforms. However, the THD in the line voltage and line current waveforms is changed due to the change in the load PF.

It is worth mentioning that the inductance of an inductive load acts as a line current harmonic filter [34], consequently,

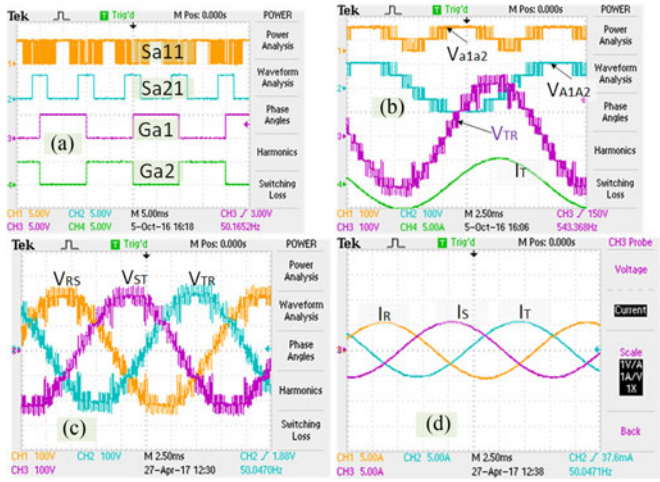

Fig. 6. Different experimental results for phase leg-A with a load of nearly 0.8 lagging power factor: (a) Gate pulses in half-bridge and full bridge module at phase leg-A, (b) level and polarity generator output voltages along with the line voltage and line current for phase leg-A, (c) three-phase line voltages, and (d) three-phase line currents.

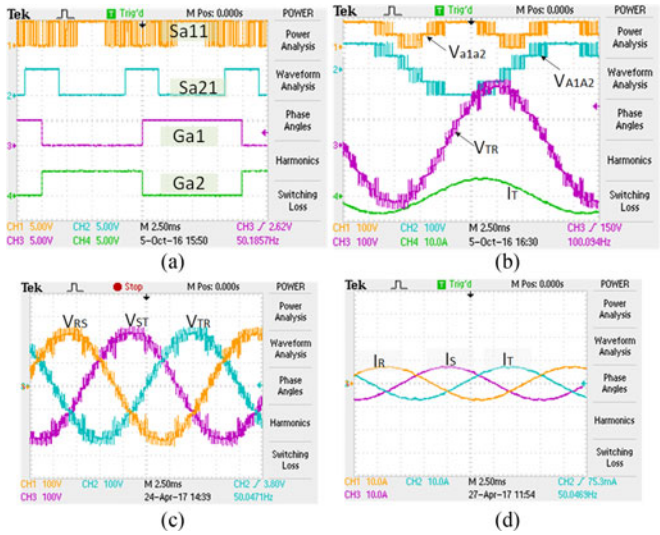

Fig. 7. Different experimental results for phase leg-A with a load of nearly unity power factor: (a) Gate pulses in half-bridge and full bridge module at phase leg-A, (b) level and polarity generator output voltages along with the line voltage and line current for phase leg-A, (c) three-phase line voltages, and (d) three-phase line currents.

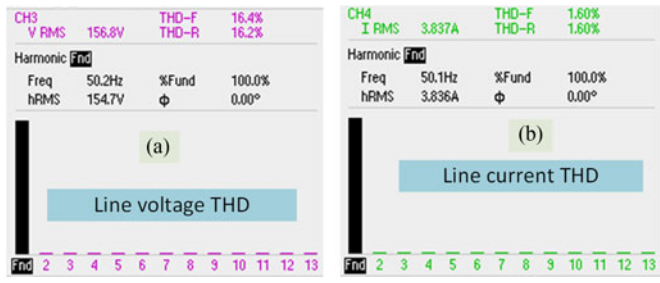

Fig. 8. THD results for nearly 0.8 lagging PF load: (a) THD for line voltage waveform and (b) THD for line current waveform.

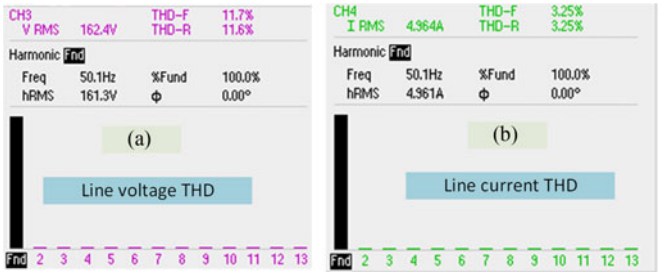

Fig. 9. THD results for nearly unity PF load: (a) THD for line voltage waveform and (b) THD for line current waveform.

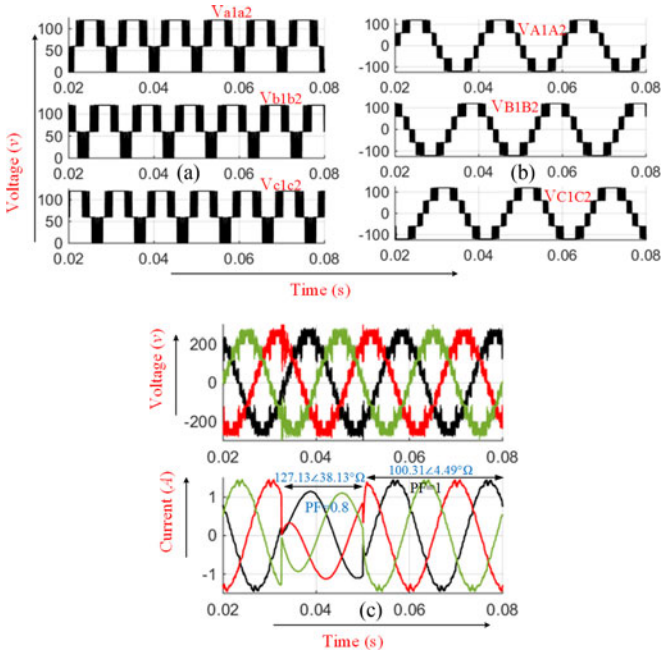

Fig. 10. Simulation results for a dynamic change in the load from nearly unity PF (100.31 ∠4.49° Ω) to 0.8 lagging PF (127.13 ∠38.13° Ω): (a) Level generator output voltage, (b) polarity generator output voltage (phase voltage), and (c) line voltage and line current.

the line current comprises less harmonics in the case of 0.8 lagging PF load as opposed to unity PF load. The THD of the line current waveforms is less than 5% in both loading conditions, which satisfies the IEEE standard [35]. On the other hand, the value of voltage THD is less than the cascaded MLI proposed in [18]–[20], [22]. The line voltage THD can be kept within acceptable limit, if a small filter is connected at the output terminals or through increasing the number of levels in the line voltages by cascading more half-bridge cells in each phase leg.

B. Case Study 2: The Performance of Inverter Under Load Dynamics

Inverter output voltage and current waveforms are observed during load dynamic conditions. Fig. 10 shows the simulation results when a load of nearly unity power factor ($100 + j7.85\ \Omega$ per phase leg) changed at $t = 0.0325$ s to $100 + j78.5\ \Omega$ per phase leg. It is assumed that this change lasts for a duration of 0.0175 s after which the original load is retained.

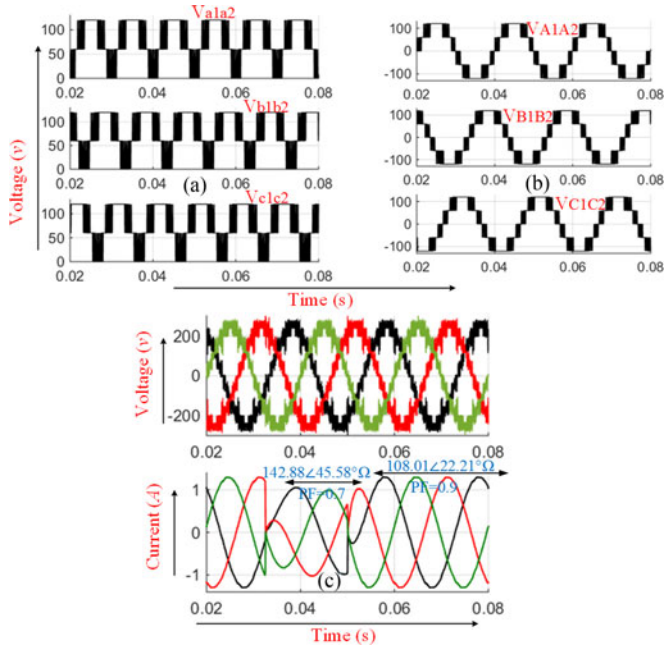

Fig. 11. Simulation results for a dynamic change in the load from nearly 0.9 lagging PF (108.01 ∠22.21° Ω) to 0.7 lagging PF (142.88 ∠45.58° Ω): (a) Level generator output voltage, (b) polarity generator output voltage (phase voltage), and (c) line voltage and line current.

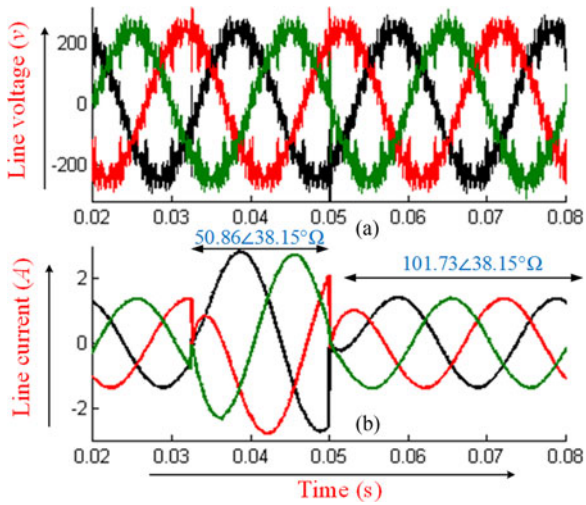

Fig. 12. Simulation results for a dynamic change in the load magnitude with the same PF: (a) Line voltage and (b) line current.

Although a little distortion can be observed in the line voltage waveforms in Fig. 10(c) during the transition period, no effect is found on the level generator output voltages shown in Fig. 10(a) and (b). Similar observation can be seen in Fig. 11, when a load of $100 + j40.82\ \Omega$ per phase leg changes to $100 + j102.05\ \Omega$ per phase leg at $t = 0.0325$ s for a duration of 0.0175 s.

The performance of the proposed CMLI is also investigated with a change in the load magnitude with the same power factor. Fig. 12 shows the inverter line voltage and line current waveforms when the load is doubled (i.e., $40 + j31.42\ \Omega$ /phase leg to $80 + j62.84\ \Omega$ /phase leg) at $t = 0.0325$ s for a duration of 0.0175 s. Same observations in the above two cases can be noticed in this case study as well.

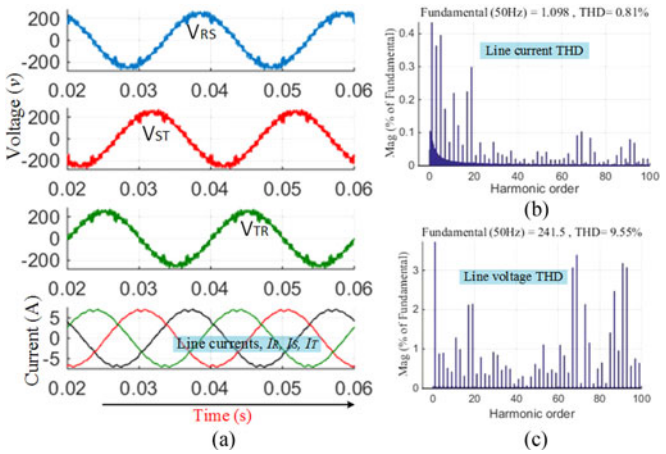

Fig. 13. Simulation results for carrier frequency of 8 kHz: (a) Line voltages and currents, (b) line current THD, and (c) line voltage THD.

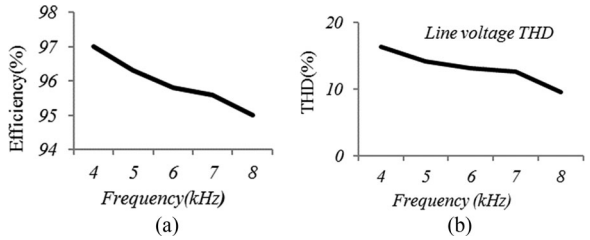

Fig. 14. Effect of carrier frequency on (a) semiconductor efficiency and (b) line voltage THD.

C. Case Study 3: Impact of Changing the Carrier Frequency on the Inverter Performance

To assess the performance of the proposed inverter with high carrier frequency, the carrier frequency is increased from 4 kHz to 8 kHz. Fig. 13 shows the inverter's output line voltages and line currents at 8 kHz carrier frequency and a load of $20 + \text{j}15.7\ \Omega$ /phase leg. In this case, the THD of the line voltage and line current waveforms is reduced from 15.6% and 1.37% in case of 4 kHz carrier frequency to 9.55% and 0.81%, respectively, in case of 8 kHz carrier frequency.

The efficiency of the proposed inverter and the quality of the line voltage waveforms are evaluated in a wide range of carrier frequencies. Fig. 14(a) and (b) shows the THD of the line voltage waveforms and inverter semiconductor efficiency for a set of carrier frequencies. While the quality of the line voltage waveforms is found better for higher carrier frequencies, semiconductor efficiency degrades with higher frequencies due to increased switching losses.

A wide range of SPWM switching frequency (1–12 kHz) has been proposed in the literature for different multilevel inverters topologies [19], [22], [36], [37]. The optimum switching frequency is a tradeoff between switching losses and the quality of the output voltage and hence the size of the system. According to Fig. 14(a), to maintain the efficiency of the proposed inverter at 97% or above, a carrier frequency of 4 kHz is considered. The efficiency will be reduced to 95.8% if a carrier frequency of 6 kHz is used. On the other hand, the line voltage THD corresponding to 4 kHz carrier frequency is 15.6% while it slightly reduced to 13.14% with a carrier frequency of 6 kHz [Fig. 14(b)]. Hence, for the proposed topology a carrier frequency of 4 kHz provides a satisfactory performance in terms of inverter efficiency and quality of the output waveforms. At this frequency, the THD in the line current was found to be 1.37% as per the above case studies.

TABLE II
INVERTER PERFORMANCE AT DIFFERENT MODULATION INDEX (BASED ON SIMULATION RESULTS)

Modulation index	0.6	0.7	0.8	0.9	1
Inverter efficiency (%)	76	80	94	95	97
Peak line voltage (V)	190	200	210	250	270
Peak line current (A)	3.3	3.54	3.8	4.6	5.2
$\text{THD}_{\text{line voltage}}$ (%)	38.11	36.92	34	23.3	15.6
$\text{THD}_{\text{line current}}$ (%)	3.62	2.51	2.14	1.53	1.37

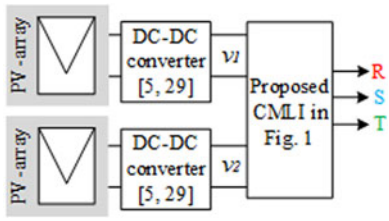

Fig. 15. Simplified block diagram for PV-application of the proposed CMLI.

D. Case Study 4: Impact of Modulation Index

Table II shows the inverter efficiency and the magnitudes of the inverter output line voltage and line current for different modulation indexes, M_i when the inverter is loaded by $20 + \text{j}15.7\ \Omega$ in each phase leg and operated at a carrier frequency of 4 kHz. As can be seen from Table II, the inverter efficiency significantly reduced when M_i is less than 0.8. Table II also shows that while the magnitudes of the line voltage and line current increase with the increase of the modulation index, the THD in both waveforms is decreasing.

E. Case Study 5: Photovoltaic Application

As mentioned in Section II, the input DC supplies can be obtained from photovoltaic output terminals or other renewable energy source. In this case study, the feasibility of the proposed inverter with PV system is assessed. The performance of the proposed inverter is investigated by replacing the two input DC power supplies in Fig. 1 by two PV-modules. A block diagram of PV-array connected to the proposed CMLI in this paper is shown in Fig. 15. DC–DC converter is utilized to maintain the DC voltages v_1 and v_2 at constant levels as per the control approach proposed in [5], [29]. It is assumed that a constant voltage control algorithm as presented in [5] and [29] is utilized to maintain the PV-modules output voltage at 80 V, as shown in Fig. 16(a). With a load of $20 + \text{j}15.7\ \Omega$, the MLI output line voltage waveforms are as shown in Fig. 16(b). The number of levels and the THD of the output line voltage waveforms remain

TABLE III
COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND CONVENTIONAL MLI

	Diode clamped	Flying capacitor	CHB	Proposed CMLI
Number of clamping diodes [20]	$3^*(m-1)^*(m-2)$	0	0	0
Number of clamping capacitors [20]	0	$3(m-1)^*(m-2)/2$	0	0
Number of voltage divider capacitors [20]	$3^*(m-1)$	$3^*(m-1)$	0	0
Number of switching devices [20]	$6^*(m-1)$	$6^*(m-1)$	$6^*(m-1)$	$3^*(m+3)$
Number of DC supplies [20]	1	1	$3(m-1)/2$	$(m-1)/2$
Output transformer [28]	1	1	1	1
Inverter efficiency [40], [41], [42]	Up to 96%	Up to 97%	Up to 95%	97%

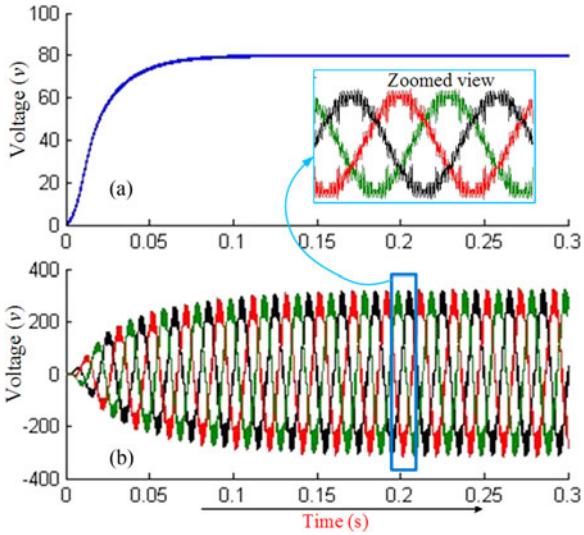

Fig. 16. PV application: (a) PV module output voltage and (b) proposed inverter output line voltage.

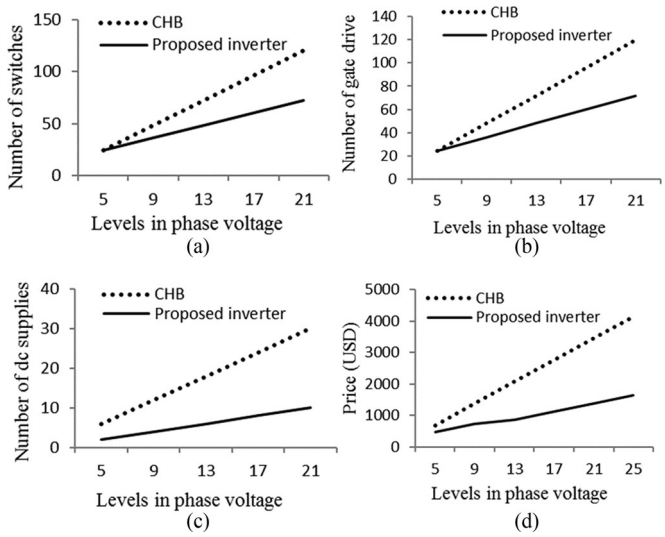

Fig. 17. Device counts and cost comparison with CHB: (a) Number of switching devices, (b) number of gate drivers, (c) number of DC power supplies, and (d) cost comparison per phase voltage level.

unchanged in comparison to the output waveforms depicted in Case study 1.

In addition to their application in PV power conversion, half-bridge module based multilevel inverters have been also utilized for medium voltage and electric vehicle applications as reported in [18] and [38]. It is expected that the topology proposed in this paper can also be utilized for the aforementioned applications and provide additional advantages, e.g., galvanic isolation and reduced input DC voltage supplies. According to manufacturers' data sheets [39], the utilized three-phase transformer is of high efficiency (up to 99%).

Hence, the overall efficiency of the proposed inverter will not be significantly affected in comparison with other existing half-bridge based CMLI. Moreover, as this topology requires less number of power electronic devices in comparison to other cascaded topologies, the overall losses are expected to be decreased.

V. COMPARISON WITH OTHER MLI TOPOLOGIES

A. Comparison With Conventional Topologies

Table III shows a general comparison between the proposed CMLI and conventional MLI, i.e., diode clamped, flying capacitor, and cascaded H-bridge (CHB) topologies with respect to the device count (as a function of the number of levels in the output voltage, m) and overall efficiency. In contrary with conventional MLI, Table III shows that the proposed CMLI does not require any diodes or capacitors, which is the main issue of conventional diode clamped and flying capacitor topologies [20]. The table also shows that the proposed topology requires $3(m+3)$ switching devices while other topologies require $6(m-1)$ switching devices. Hence, for any number of levels above 5, the proposed CMLI will require the least number of switching devices. Moreover, the proposed CMLI requires less number of DC-supplies than the CHB inverter.

Fig. 17 shows a comparison between the proposed inverter and conventional cascade H-bridge inverter [42], [43] as a function of the number of levels m in the output voltage waveform. As shown in Fig. 17(a)–(c), the implementation of the proposed inverter calls for less number of power electronic switches, gate drive circuits and DC supplies. Fig. 17(d) shows a cost comparison between the proposed CMLI and conventional CHB-based MLI to obtain 1.5 kV (peak) in the line voltage. Cost estimation includes IGBT modules, gate drivers, and full-bridge rectifiers and is based on 2017 market prices [44]. It is worth mentioning that a three-phase transformer is an essential part in the conventional multilevel inverters for high-power grid integration to provide the required galvanic isolation [28]. Hence, the isolation transformer in the proposed topology in this paper does not

TABLE IV
COMPARISON OF THE PROPOSED THREE-PHASE SYMMETRIC HALF-BRIDGE TOPOLOGY WITH OTHER HALF-BRIDGE TOPOLOGIES PROPOSED IN THE LITERATURES

	Proposed topology in this paper	Three phase topology proposed in [19]	Three phase topology proposed in [22]	Three phase topology proposed in [18]
No of half-bridge cells	6	6	15	9
No of total switching devices	24	24	42	18
No of gate driver	24	24	42	18
No of DC supplies or capacitors	2	6	15	9
No levels in the line voltage	13	9	11	7

incur extra cost when the proposed cascaded inverter is utilized as a grid connected PV inverter. Fig. 17 shows that the proposed topology is a cost-effective choice when compared with the conventional CHB multilevel inverter topologies.

B. Comparison With Other Half-Bridge Based Topologies

The main emphasis of the proposed inverter aimed at maximizing the number of output voltage levels with reduced number of DC-voltage supplies by utilizing the symmetry properties. Therefore, it is essential to compare the proposed topology with other equivalent half-bridge based topologies reported in the literatures [18], [19], [22] to confirm its superiority. As summarized from Table IV, different aspects are taken into account to draw a sensible comparison, this includes: The number of half-bridge cells, total number of power electronic switching devices, gate drive circuits, number of DC power supplies or DC-link capacitors, and number of the attainable output voltage levels in the line voltages. As can be seen in Table IV, the proposed topology achieves higher number of output voltage levels by utilizing the same number of power electronic switching devices and gate drive circuits when compared with topologies proposed in [18], [19], and [22].

Specifically, the topology proposed in [22] requires more than twice the number of total switching devices, gate drive circuits, and DC supplies for generating lower number of levels in the line voltage compared with the proposed topology in this paper. On the other hand, although the topology proposed in [18] requires less number of symmetric half-bridge cells, it only generates seven-levels in the output line voltage. The topology proposed in [18] would require seven symmetric half-bridge modules in each phase leg to generate 13-level at the output line voltage, which is achieved in the proposed topology in this paper by only using three symmetric half-bridge modules. This means, 42-switching device along with 19 DC power supplies will be required, if the topology proposed in [18] is extended to generate 13-levels in the line voltage.

Interestingly, the proposed cascaded multilevel inverter in this paper requires the lowest number of DC-supplies than any other topology presented in Table IV.

VI. CONCLUSION

This paper presents a new symmetrical multilevel inverter topology with two different stages. The proposed inverter requires less power electronic devices and features modularity, hence simple structure, less cost, and high scalability. The number of input DC supplies for the proposed topology is found to be nearly 67% less than the similar symmetric half-bridge topologies, which is a great achievement for industrial applications. This phenomenon will reduce the complexity of DC voltage management. As being a symmetric structure, all the switching devices experience same voltage stress, which is a very important factor for high-voltage applications. The feasibility of the proposed inverter is confirmed through simulation and experimental analysis for different operating conditions.

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