3-D Wire Bondless Switching Cell Using Flip-Chip-Bonded Silicon Carbide Power Devices

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***Abstract*—This paper presents a three-dimensional (3-D) wire bondless power module using silicon carbide (SiC) power devices. Commercially available SiC power devices are designed for wire bonding. Wire bonds have an inherent parasitic inductance that limits high-frequency switching. This results in an underutilization of the full potential of SiC power devices, which have very low switching losses at high frequencies. Wire-bonded power modules run into a performance ceiling when it comes to ultrafast switching. This paper strives to provide a solution to this issue, which involves reconfiguring a commercially available bare die SiC power device into a flip-chip-capable device. A wire bondless SiC Schottky diode package was demonstrated and its performance was contrasted with a conventional wire-bonded package. A 24% reduction in the ON-state resistance was observed in the wire bondless package. As a next step, wire bondless SiC MOSFET packages were developed and tested in a half-bridge configuration in a highly integrated 3-D arrangement. This approach departs from the conventional concept of a power module—demonstrating a direct-bonded-copper-less and baseplate-less half-bridge switching cell. Double-pulse tests conducted on the cell showed $>3\times$ reduction in the parasitic inductance of the 3-D cell as compared with a conventional wire-bonded module.**

***Index Terms*—Chip scale packaging, electronics packaging, wide band gap semiconductors.**

I. Introduction

SiC power devices are capable of operating at much higher switching frequencies as compared with their silicon (Si) counterparts [1]–[5]. Higher switching frequencies enable a significant reduction in the size of the passive elements. In most power electronic converters, the passive devices and thermal management occupy a large majority of the mass and physical volume. Hence, a significant increase in power density can be obtained by addressing one or both of these issues. This paper describes a novel approach which offers a solution on both fronts.

Modern SiC power devices are packaged in one of two forms—discrete packages like a TO-247 or in the form of multichip power modules (MCPMs). In both these industry standard approaches, the mode of interconnection is wire bonding. Wire bonds are a source of significant parasitic inductance in these packages. At high switching frequencies, these parasitic inductances give rise to undesirable voltage overshoots and ringing that leads to the generation of electromagnetic interference (EMI), which often results in catastrophic failures. A high drain-source voltage overshoot may exceed the maximum rating of the device. On the other hand, a high gate-source overshoot may cause a false turn-on event, resulting in a possible shoot-through condition. The situation is often worse in the case of a discrete package as compared with a multichip power module (MCPM). In a custom wire-bonded MCPM, there is a greater possibility to optimize parasitics by designing short-area switching loops. However, MCPMs are expensive and only customizable to an extent. To achieve the maximum benefits of inductance optimization, one must have access to a packaging facility to design and manufacture the MCPM from scratch. Often, power electronics designers choose discrete devices to have this degree of customizability with respect to topology optimization, even if they must accept slightly inferior switching characteristics. Also, discrete devices are much easier to replace. In case of a catastrophic event compromising a switch (or multiple switches), they can be easily replaced by de-soldering a dysfunctional device and re-soldering a known-good discrete device. Rework for a dysfunctional MCPM is not as straight-forward. It often involves the replacement of the entire module—again an expensive process. This paper provides a solution which combines the ease of use and rework of a discrete device with the performance and customizability of an MCPM.

The proposed solution is a novel flip-chip-capable power device. The power semiconductor device is reengineered to convert a commercial bare die SiC power device into a surface-mount component. The device may, as a result, be flip-chipped onto an interposer (or substrate) using flip-chip bonding techniques. Solder balls were used for electrical interconnections. Flip-chip bonding using solder spheres has been widely used in microwave and radio-frequency (RF) circuits to enable high-frequency operation [6]–[9]. Solder spheres have also been employed in memory modules to realize high power densities through three-dimensional (3-D) stacking [10]–[14]. More recently, chip-scale packages have been demonstrated for gallium

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nitride (GaN) power devices wherein they have been successfully flip-chip bonded onto printed circuit boards (PCBs) to realize ultrahigh switching frequencies in power converters [15], [16]. However, all of these applications have been limited to lower power ranges. In this effort, the benefits of flip-chip packaging have been translated to high-power and higher voltage SiC devices.

This paper is organized into four sections. Section II presents a detailed description of the concept of a flip-chip power device and its implementation in a power electronics system. Section III describes a detailed process flow of converting a commercially available bare die power device to a chip-scale package. Section IV describes the design and fabrication of a flip-chip Schottky diode based on the processes described in Section III, and an evaluation of the electrical characteristics of the flip-chip chip MOSFET. Section V takes the study a step forward with the introduction of a flip-chip MOSFET and a detailed account of a 3-D half-bridge module designed using these novel packages. This section also offers a discussion on the electrical testing results of the module and contrasts it with the performance of two separate half-bridge modules employing discrete devices and wire-bonded die, respectively.

II. Flip-Chip Power Device

Commercially available SiC power devices in bare die form are usually vertical devices. They have a pad on the bottom side of the SiC chip and multiple pads on the top side of the chip, depending on the device type (Schottky diode, MOSFET, or IGBT). Hence, if an SiC bare die is flip-chip bonded on to a substrate, a connection still has to be made to the bottom contact. This may be achieved by using an isolated baseplate or direct bonded copper (DBC) substrate, but it becomes an issue if multiple devices need to share a common baseplate or substrate. Not all devices may share a common signal net for the bottom terminal, and this introduces an additional isolation requirement. The bottom substrate also needs to be a good thermal conductor to facilitate heat removal from the die to the heat sink. Moreover, all bare die power devices are not of the same thickness. Wafer thicknesses differ by manufacturer—and in many cases they also differ by device types from the same manufacturer. For example, a 1200V-rated SiC MOSFET (CPM2-1200-0025B) from Wolfspeed has a nominal thickness of 180 μm, while a 1200-V-rated SiC Schottky diode (CPW5-1200-Z050B) from the same manufacturer has a nominal thickness of 380 μm. Hence, the common substrate for connecting the bottom terminals is often etched to match these height differences. This adds considerable processing complexity and cost.

A solution to this problem is proposed in the form of a chip-scale package. Fig. 1(a) shows a schematic representation of this concept. In this embodiment, a commercially available bare die power device was attached to a metallic bottom connector, thus translating the bottom interconnection of the device to the plane of the top contacts. This makes the resulting chip scale package flip-chip capable. The bottom drain contact also serves as a low thermal-resistance path to a heat sink. Both the top pads of the power device and the bottom connector need to have a solderable finish. The material selection and processes to achieve this are discussed in detail in a subsequent section. The interconnections between the bond pad and the interposer were achieved using solder spheres. Pads for the solder spheres were fashioned on the top surface of the device using solder masking. The dimension of the solder sphere was chosen to cover maximum area on the gate pad. Similar sized solder spheres were used to form a solder ball array on the remaining pads on the die and the bottom connector. The package measures 6.26 mm $\times$ 4.4 mm. The pinout of a flip-chip MOSFET is shown conceptually in Fig. 1(b). The source pad interconnections were achieved using two 2 $\times$ 3 solder sphere arrays on each source pad, and the drain connection was made using a single 4 $\times$ 2 solder sphere array. This has two benefits—it reduces the effective stray inductance (and stray resistance) and it relieves thermomechanical stresses. The specifications of the drain connection and solder ball array have been optimized through finite-element analysis in previously published studies [17], [18]. As mentioned earlier, the reverse side of the metallic bottom connector can be used for heat removal. Fig. 1(c) shows a possible heat removal strategy. Both single-sided, double-sided, and even three-sided cooling (if the substrate is cooled with microchannels) options may now be utilized to achieve efficient thermal management. In the case of high-density integration, low-inductance gate loops, and power loops are realized using 3-D topologies. This is depicted schematically in Fig. 1(d). One of the other major benefits of the proposed approach is that it can easily account for different die thicknesses. This can be achieved by milling different depths on the bottom connector, thus enabling the opportunity of using combinations of different devices to realize the best electrical system design [see Fig. 1(e)].

This chip-scale package may now be seamlessly flip-chip bonded on to a substrate having a matching pad layout. These processes will be described in greater detail in the following section.

III. Fabrication Process

The process flow for fabrication of a typical flip-chip power module follows five major steps:

1) re-metallization of the top pads of the commercial power device in bare die form;
2) attachment of the re-metallized die to the metallic connector;
3) solder masking to expose the pads for attaching solder spheres;
4) attachment of the solder spheres;
5) flip-chip bonding to a patterned interposer or substrate.

The preliminary step in this process was re-metallization. Commercially available SiC power devices are designed for top-side wire bonding. Hence, the top pads of these devices are aluminum. In order to obtain a solderable finish, an electroless nickel plating process was pursued. An electroless nickel-gold (ENIG) finish has been well established as a preferred re-metallization process for aluminum bond pads as described in the literature [19], [20]. The process involved the stripping of the native oxide layer of the aluminum bond pad, followed

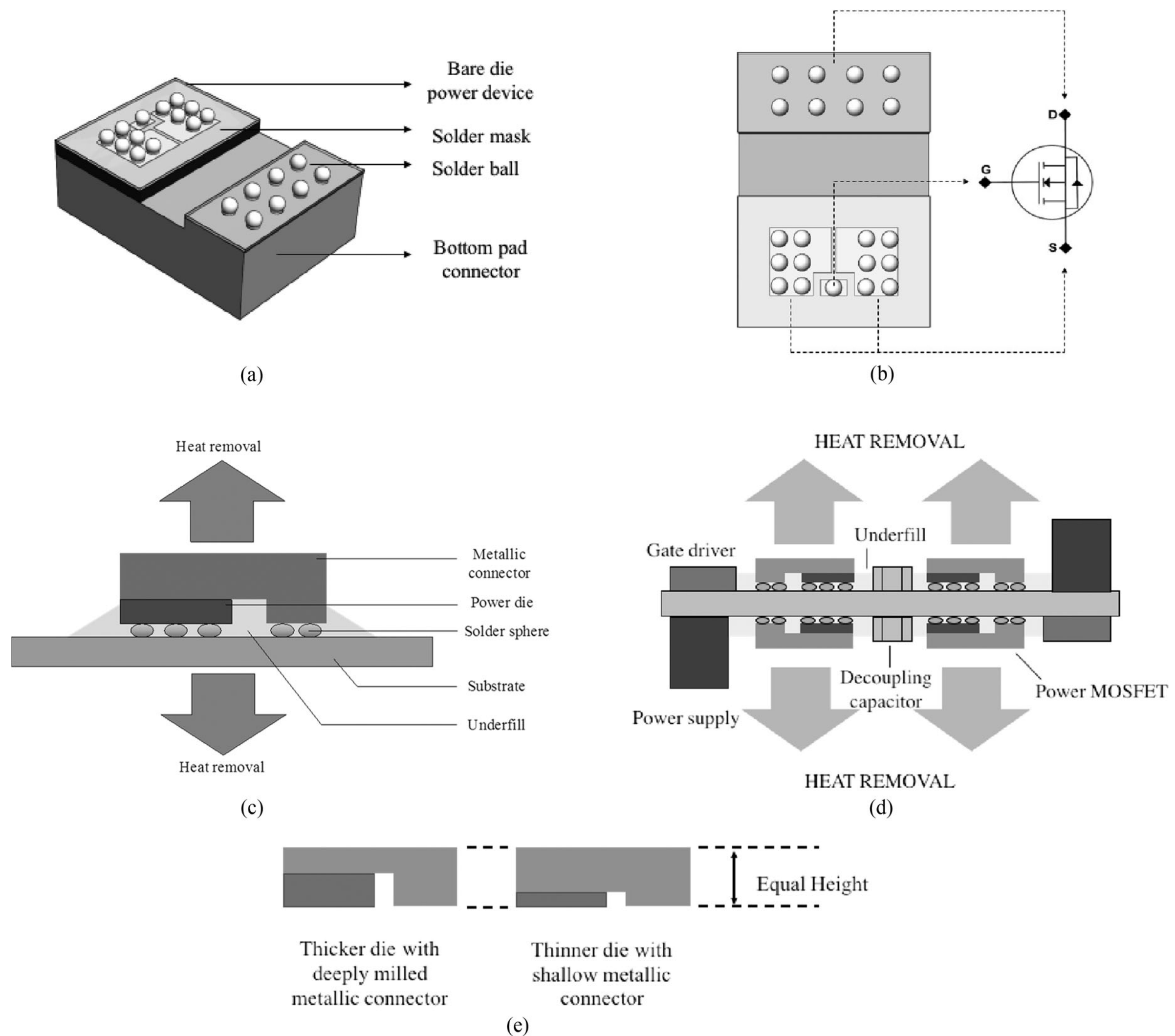
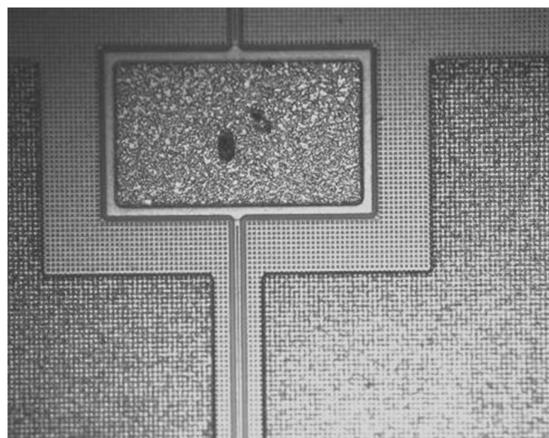


Fig. 1. (a) Schematic showing the concept of a flip-chip power device, (b) a pinout representing the electrical connections to the chip-scale package, (c) a diagram showing the heat removal paths in a back-to-back cell configuration that could be paralleled devices or not depending on the interconnections in the substrate, (d) a diagram of a single cell representation of circuit implementation, and (e) a diagram illustrating the planarization solution to the issue of height variation between different commercial bare die.

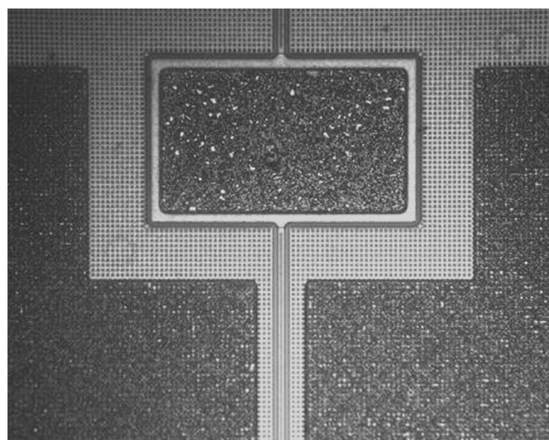
by the deposition of a very thin zinc adhesion layer. The nickel layer was then deposited atop the zinc layer. Fig. 2(a) shows an optical microscope image of the thin zinc layer on the top pads of a bare die ROHM MOSFET. The probe marks on the gate pad were still visible after zinc deposition. Fig. 2(b) shows the optical microscope image of the final 5-μm nickel layer, and the probe marks are barely observable as a result. An interesting feature of choosing electroless plating was the self-patterning nature of the process. No additional photolithography (or masking) step and lift-off process was required—thus reducing the cost and complexity of the process. As can be observed in Fig. 2, no dendritic formations or conductive bridges were found after the metallization steps were completed. During the entire process, the bottom nickel/silver pad of the bare die power device was masked using Kapton tape. After the metallization step, the tape was gently removed using isopropyl alcohol and a pair of tweezers and the sample was thoroughly cleaned to remove organic residues.

The next step in the process involved the attachment of the re-metallized die to the metallic connector. The material chosen for the bottom connector was copper since it provided an inexpensive option without compromising mechanical robustness [18]. The connector was milled out of a 2 mm sheet of copper. The die attach material was SAC305 solder with a peak reflow temperature of 249 °C. This was to maintain a suitable solder hierarchy since the maximum reflow temperature of the solder spheres was around 225 °C. A stencil fashioned from a Kapton sheet was used to hold the die in place during solder reflow. A photograph showing this setup is shown in Fig. 3.

The chip-and-connector assembly was solder-masked using a photo patternable dry film solder resist. The film was laminated onto the surface of the chip-scale package using a desktop thermal laminator. A photolithography step was conducted on the sample through a mask containing the solder ball array pattern. Upon development, pads were exposed on the package surface designating the position of the solder spheres. The sample was



(a)



(b)

Fig. 2. (a) Thin zinc seed layer on the aluminum bond pad, and (b) the thick final layer of nickel.

Fig. 3. Process for die attachment using Kapton film fixturing.

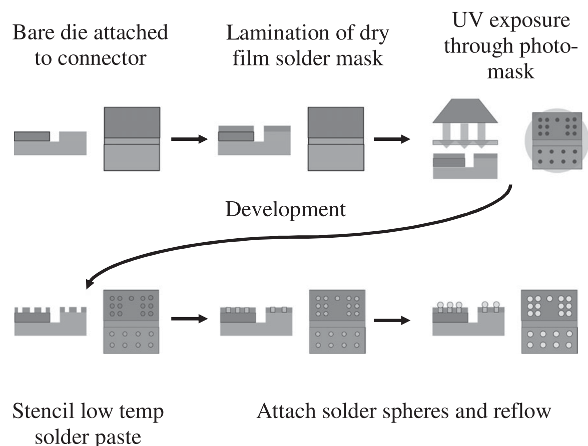


Fig. 4. Schematic depicting the process flow for the solder masking step.

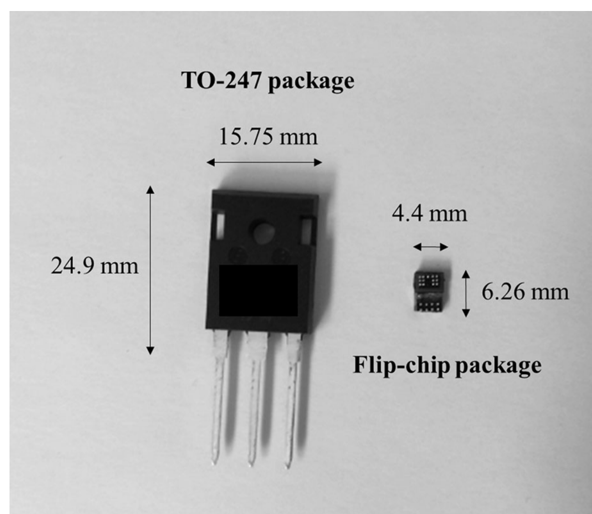


Fig. 5. Ball-bumped sample alongside a TO-247 MOSFET package for comparison.

cured under ultraviolet (UV) light to complete the solder masking process.

Solder sphere attachment was the next step of the process. A squeegee was used to stencil solder paste into the circular open pad areas on the chip scale package. Solder spheres of 15 mil were hand placed onto the wet solder paste. The assembly was reflowed in a Sikama reflow oven. The melting temperature of the attachment solder paste was lower than the solder spheres. Hence, the spheres retained their shape but attached securely to the bond pads on the chip-scale package. The process flow is described in the diagram in Fig. 4.

The assembly is now capable of being flip-chip bonded on to a substrate with matching bond pads, much like a discrete MOSFET. However, the footprint of this device is approximately 14× smaller as compared with a discrete TO-247 device. Fig. 5 shows a photograph comparing the two packages to illustrate this fact.

The final step in the fabrication process was the flip-chip attachment of the chip-scale package on to matching pads on a substrate/interposer. In this study, FR4 was used as the interposer material since it provided a versatile-yet-inexpensive platform for the demonstration of the key benefits of this technology.

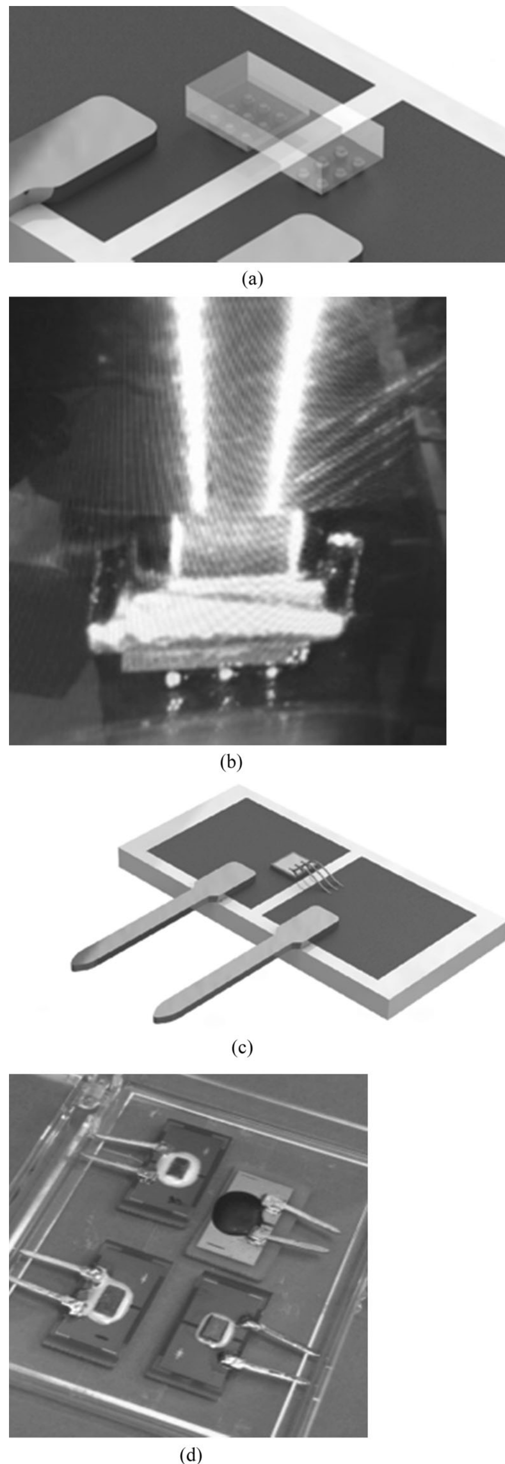


Fig. 6. (a) CAD rendering of the wire bondless flip-chip SBD package, (b) a magnified image of the solder spheres collapsing while reflowing, (c) a CAD rendering of the wire-bonded SBD module, and (d) a photograph showing the finished wire bondless and wire-bonded TO-247 type packages.

IV. Flip-Chip Schottky Barrier Diode

A Schottky barrier diode (SBD) was fabricated using the process flow described in the previous section. The forward I–V characteristics of the samples were measured and compared with a wire-bonded module. The bare die device used for this test was the S6203TCSF from ROHM semiconductor. It is a 650-V-rated SBD measuring 2.3 mm $\times$ 2.3 mm. The copper connector for this package was manufactured by a combination of wet-etching and milling of a 1.5-mm-thick copper sheet. The design justification from a thermomechanical standpoint was described in [18].

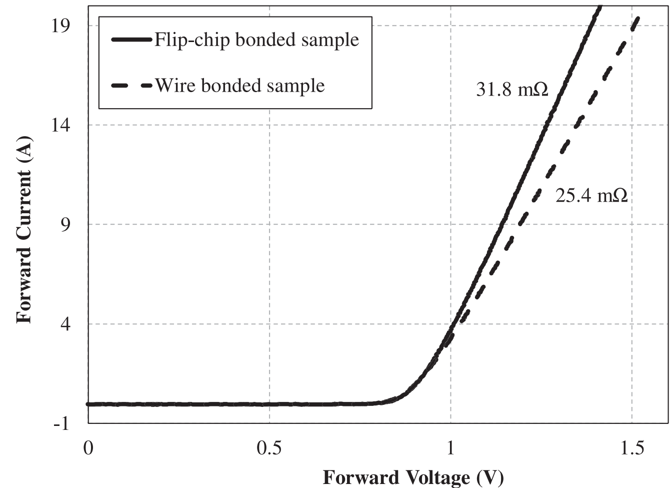
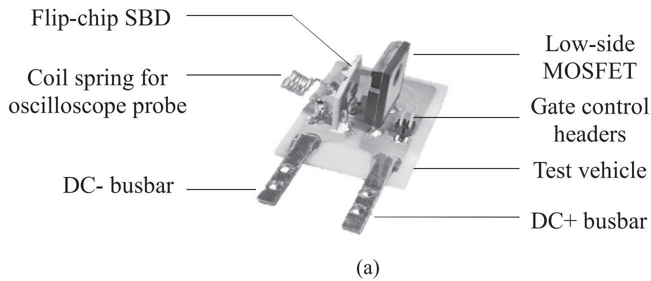


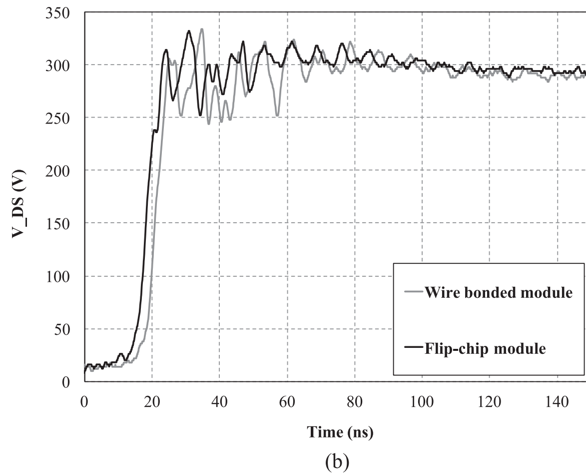
Fig. 7. Forward I–V characteristics of the two TO-247 packages.

The chip-scale SBD package was flip-chip bonded onto an FR4 substrate. The FR4 substrate was also solder masked and patterned in-house with bond pads matching the solder sphere array on the chip-scale SBD package. The flip-chip SBDs were underfilled using Hysol FP4549 for added mechanical support and voltage isolation. Finally, metal leads were soldered on the substrate to cast the package into a TO-247-type footprint. This was to ensure that the sample could be effortlessly mounted and measured using a standard curve tracer. A wire-bonded module was also fabricated, in which the same bare die SBD was soldered and wire bonded to an FR4 substrate of similar dimensions. Fig. 6(a) shows a model for the design of the flip-chip package, and Fig. 6(b) shows a zoomed-in view of the model showing the solder balls underneath the device. Fig. 6(c) shows a magnified photograph of the solder spheres collapsing upon reaching the reflow temperature. Fig. 6(d) shows an artistic rendition of the wire-bonded package used for comparison. A photograph showing a batch of fabricated TO-247-type packages is shown in Fig. 6(e). The samples with a green-solder-masked surface are the flip-chip wire bondless packages with white underfill material [Henkel FP4549], and the wire-bonded sample is the one with a bare copper top surface with a black epoxy glob top isolation.

The samples were measured using a B1505A curve tracer from Keysight and the forward I–V characteristics were plotted. The result of the measurement is shown in Fig. 7. It was observed that the flip-chip-bonded package had a 24% lower on-state resistance as compared with the wire-bonded package. This improvement was observed despite both devices being cast in a TO-247 package, where the inductance and resistance of the package leads dominate. It must be noted that the reduction in the on-state resistance directly translates to a 24% reduction



(a)



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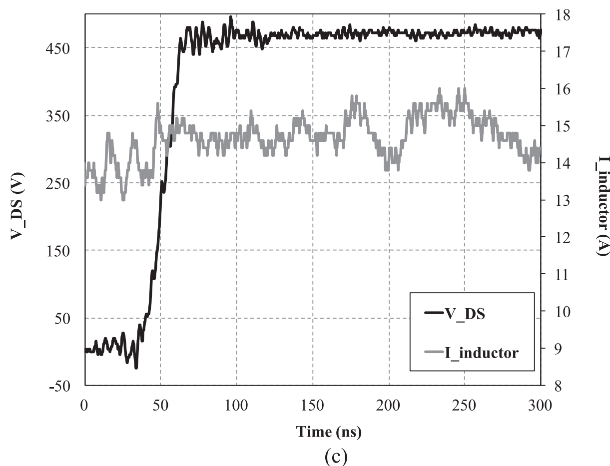

(c)

Fig. 8. (a) Flip-chip SBD package mounted on a double-pulse test fixture, (b) a comparison of the TURN OFF waveform of the double-pulse test, (c) the current and voltage waveforms showing operation at 450 V, 15 A.

in the conduction losses. This greatly reduces the demand on the thermal management, thus potentially increasing the power density of the system. Remarkably, these benefits were made possible through a single impactful shift—by adopting flip-chip wire bondless packaging techniques.

As a next step, the devices were incorporated in a double-pulse test setup. The fabricated flip-chip-bonded sample served as the high-side diode, while a commercially available 1200 V SiC MOSFET was used as the low-side switch. Fig. 8(a) shows a TO-247 flip-chip SBD package mounted on a double pulse test fixture. The double pulse fixture was also manufactured in-house using a two-layer FR4 substrate. The results of the test conducted on the two packages are shown in Fig. 8(b), (c), and (d). As mentioned before, the parasitic inductance of both packages were dominated by the lead inductance. Hence, there was no significant reduction in the voltage overshoot during turn-off. However, upon estimating the loop inductance through the frequency of the ringing in the two waveforms represented in Fig. 8(b), it was observed that the flip-chip solution offered 20.5% lower overall loop inductance as compared with the traditional wire-bonded solution. The time period of the ringing was measured using the oscilloscope cursors, and the related calculations and results are shown in Table I. Fig. 8(c) shows the waveforms for the operation of the flip-chip module at 450 V, 15 A.

TABLE I
MEASURED PARASITIC LOOP INDUCTANCES OF THE TWO MODULES

Output Capacitance of the MOSFET (C_{OSS}) (F)	Time Period of Ringing (ns) (Δt)		Parasitic Loop Inductance (nH) $= \frac{(\frac{\Delta t}{2\pi})^2}{C_{OSS}} \times 10^9$	
	Wire-Bonded	Flip-Chip	Wire-Bonded	Flip-Chip
110e-12	9.2	8.2	19.51	15.5

The experiments described in this section addressed a number of important concerns. Most importantly, it showed that the bare die power devices were electrically functional after they were subjected to the entire process flow. The flip-chip solder bumped approach also showed a lower parasitic loop inductance as compared with wire bonding. However, this was the case of a single device. There are several other factors that affect the switching characteristics of a power device when it is part of a circuit. Also, these experiments did not provide any insight into the switching characteristics and parasitics of the gate-source loop. It was important that a MOSFET be investigated to truly understand the benefits of the proposed approach. This study is described in the following section where flip-chip power MOSFETs were fabricated. A half-bridge was constructed using these novel device packages and the switching performance was evaluated through double pulse tests.

V. 3-D Wire Bondless Half-Bridge Module Using Flip-Chip MOSFETs

The major goal with the electrical design of the flip-chip wire bondless half-bridge module was the minimization of the parasitic inductance in the critical switching loops in the circuit. The flip-chip power MOSFETs were fabricated according to the procedures described in Section III. The chosen bare die power device was the 1200-V-rated S2301UCSF power MOSFET from ROHM Semiconductor. A half-bridge topology was chosen to demonstrate the switching characteristics of the devices. A half-bridge is an integral constituent of a majority of power electronics topologies. Any benefits observed for a half-bridge can translate to benefits for an entire topology. The half-bridge was controlled by an off-board gate drive circuit for these experiments.

In conventional half-bridge modules employing wire-bonded SiC MOSFETs, the power-loop is lateral [see Fig. 9(a)]. Even

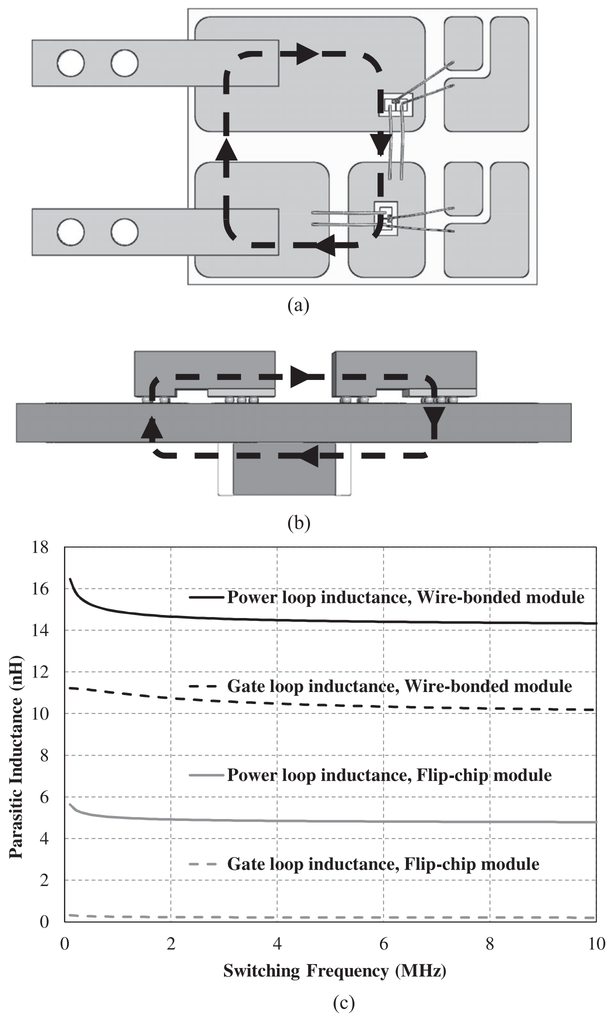

Fig. 9. (a) Conventional lateral wire-bonded power loop, (b) a vertical power loop using flip-chip SiC devices, and (c) a simulation showing the parasitic inductances.

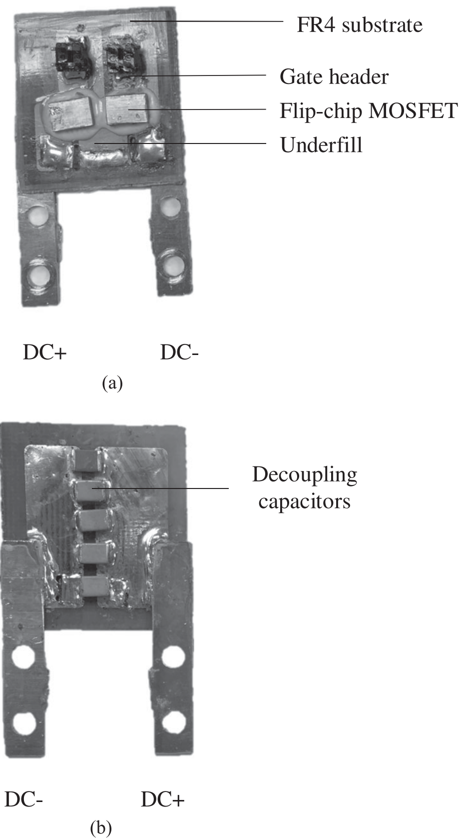

Fig. 10. (a) Top side of the populated flip-chip wire bondless module and (b) the bottom side with the decoupling capacitor bank.

if short wire bonds are used and appropriate clearance rules are obeyed, it usually results in a power-loop of about 14 nH inductance [see Fig. 9(c)]. Even with a wire bondless interconnection method, this lateral loop approach will limit the parasitic inductance benefits.

In previous publications involving gallium nitride (GaN) devices, it was demonstrated that a vertical loop approach outperformed a lateral loop approach in terms of low parasitic inductance [21]. This approach involved placing flip-chip GaN power devices on one side of a printed circuit board (PCB) and dc-link decoupling capacitors directly on the other side of the board. Very low inductance vertical loops were made possible, limited only by the thickness of the PCB. A similar concept for the novel flip-chip SiC MOSFETs is illustrated in Fig. 9(b). It can be observed that due to the opposing current paths in the top and bottom layers, the loop inductance can be highly minimized due to return path cancellation. Fig. 9(c) shows the simulation results confirming this, and the power and gate loop inductances were found to be an order of magnitude lower as compared with the lateral loop design using wire-bonded interconnections.

The next step in this set of experiments was the fabrication of the wire-bondless half-bridge. As in the case of the SBDs, an FR4 substrate was patterned in-house. The substrate was solder masked on the top side with the solder sphere pattern on the flip-chip MOSFETs and pads for attaching the bus bars and gate signal headers. On the reverse side, there were two parallel copper tracks to mount multi-layer ceramic capacitors (MLCCs) in parallel. Photographs of the top and bottom sides of the fabricated half-bridge are shown in Fig. 10. The gate and source connections to each device was established using 4×2 male pin headers. It must be noted that a dedicated Kelvin source connection was provided for the return path of the gate signal. This is standard practice to ensure that the gate-source current path encounters a minimum source inductance. Copper bus bars were used to supply the dc-bus voltage. First, the chip-scale MOSFET packages were aligned and bonded using a flip-chip bonder, followed by an underfill procedure similar to the flip-chip SBDs. The bus bars, pin headers, and dc-link capacitors were soldered as a next step. Five MLCCs measuring 10 nF each were bonded in parallel, resulting in a total capacitance of 50 nF [see Fig. 10(b)].

The gate driver used for these experiments was the IXDN609SI 9A gate driver from IXYS. A 5.1 Ω gate resistor was used with $+20$ and -5 V on and off-state drive voltages.

In addition to the wire bondless module, two other half-bridge were fabricated to serve as baselines for comparison. The first

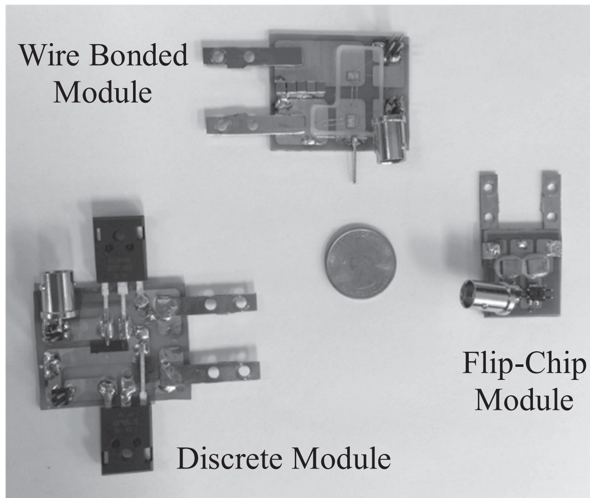

Fig. 11. Three modules fabricated for electrical testing.

half-bridge employed discrete power MOSFETs soldered on a patterned FR4 substrate. The second module for comparison was constructed using wire-bonded power MOSFETs. The wire-bonded module was similar to the schematic shown in Fig. 9(a). The wire-bonded module was encapsulated using an RTV silicone material for supplementing the mechanical durability and electrical isolation. Fig. 11 shows a photograph of the three modules alongside a U.S. quarter for comparison. At first glance, it can be observed that the flip-chip module has a much smaller footprint than the other two modules.

As mentioned earlier, the modules were evaluated using a double-pulse test. The setup was the same as that shown in Fig. 8(a). During all tests, the high-side device was forced to be in the OFF condition by electrically shorting the gate and the source. Hence, the high-side device essentially functioned as a diode. For each sample, the drain-source and gate-source waveforms were measured during the turn-off and turn-on events. The current through the output inductor was also measured. A dc-bus voltage of 300 V was applied across the bus bars of each module at a current of 35 A. A high-bandwidth probe of 600 MHz was used to take switching measurements. A high bandwidth was required to measure transient effects with great accuracy.

The turn-off waveforms of the three modules are shown in Fig. 12(a). While large overshoots were observed in the case of the discrete and wire-bonded half-bridges, respectively, the waveforms for the wire bondless half-bridge were almost free from undesirable overshoots. The output waveforms during the turn-on event are shown in Fig. 12(b). However, there was nothing much to tell the waveforms apart during this event. The low-parasitic advantage was echoed by the gate-source waveforms as well, as can be observed from the waveforms plotted in Fig. 12(c).

Ringing and overshoots in the gate-source voltage during the turn-off event is of great concern in high-frequency power electronic circuits since it often leads to a false turn-on condition in one or more switches resulting in a catastrophic failure. It was found that the gate-source voltage rails for the discrete and wire-bonded modules showed significantly greater disturbances as compared with the wire bondless module. The gate turn-on waveform is shown in Fig. 12(d), and no significant difference was found between the respective waveforms for the three modules. The inductor current was also plotted for during each event and is shown in Fig. 12(e), indicating lower ripple. The rise and fall times for the turn-on and turn-off events ranged between 16 and 20 ns despite using an off-board gate driver. These ultrafast slew rates make megahertz-level switching possible.

The gate and output waveforms of the wire bondless module were virtually distortion-free. This has significant positive implications from the standpoint of a power electronics system. It reduces (and possibly eliminates) the requirement for snubbers and other noise-suppression circuitry. It also potentially eliminates the requirement of the negative voltage rail for the gate drive circuit. The flip-chip interconnection does, in fact, provide extremely low-parasitic interconnections to significantly improve the switching characteristics of the circuit.

The overshoot and distortion in the switching waveforms often increase with an increase in the load current. The width of the first pulse was decreased to provide a current of 15 A. The overshoot and ringing in the voltage across the drain-source and gate-source were compared with the waveforms obtained for a 35 A load current. Fig. 13(a) and (b) shows the waveforms for the discrete module, illustrating the effect of the increased load current on the drain and source voltages, respectively. An increase of nearly 100 V was observed in both the first overshoot and undershoot of the drain-source voltage. The gate voltage overshoot during turn-off was also found to increase significantly under the increased load current. Fig. 13(c) and (d) shows the same set of waveforms for the wire-bonded module. The increase in the drain-source overshoot is significant, but not as drastic as the case of the discrete devices. The gate overshoot, however, does increase considerably. Driving the switch any faster may lead to a false turn-on event. The case for the flip-chip module is presented in Fig. 13(e) and (f). As can be observed from the drain-source waveforms, the overshoot does not show a significant increase even for more than 2× increase in the load current. The overshoot in the gate voltage waveform does increase at 35 A from the flat line at 15 A but is still confined to a level below 0 V. This implies that the switching transitions can be even more aggressive before a false turn-on risk becomes imminent.

The next investigation focused on extracting the actual parasitic loop inductances encountered by the switching currents. A very accurate method to measure this is by measuring the ringing frequency of the drain-source waveform during the turn-off event. During this event, the parasitic loop inductance and the output capacitance of the device resonate to produce ringing. The output capacitance ($C_{\rm OSS}$) of the device for a particular dc-bus voltage is usually provided in the device datasheet, and the time period (Δt) of the ringing may be measured accurately using the oscilloscope cursors. The parasitic loop inductance ($L_{\rm loop}$) may then be estimated using the following relation:

$$L_{\rm loop} = \frac{(\Delta t/2\pi)^2}{C_{\rm OSS}} \times 10^9 \text{ nH}.$$

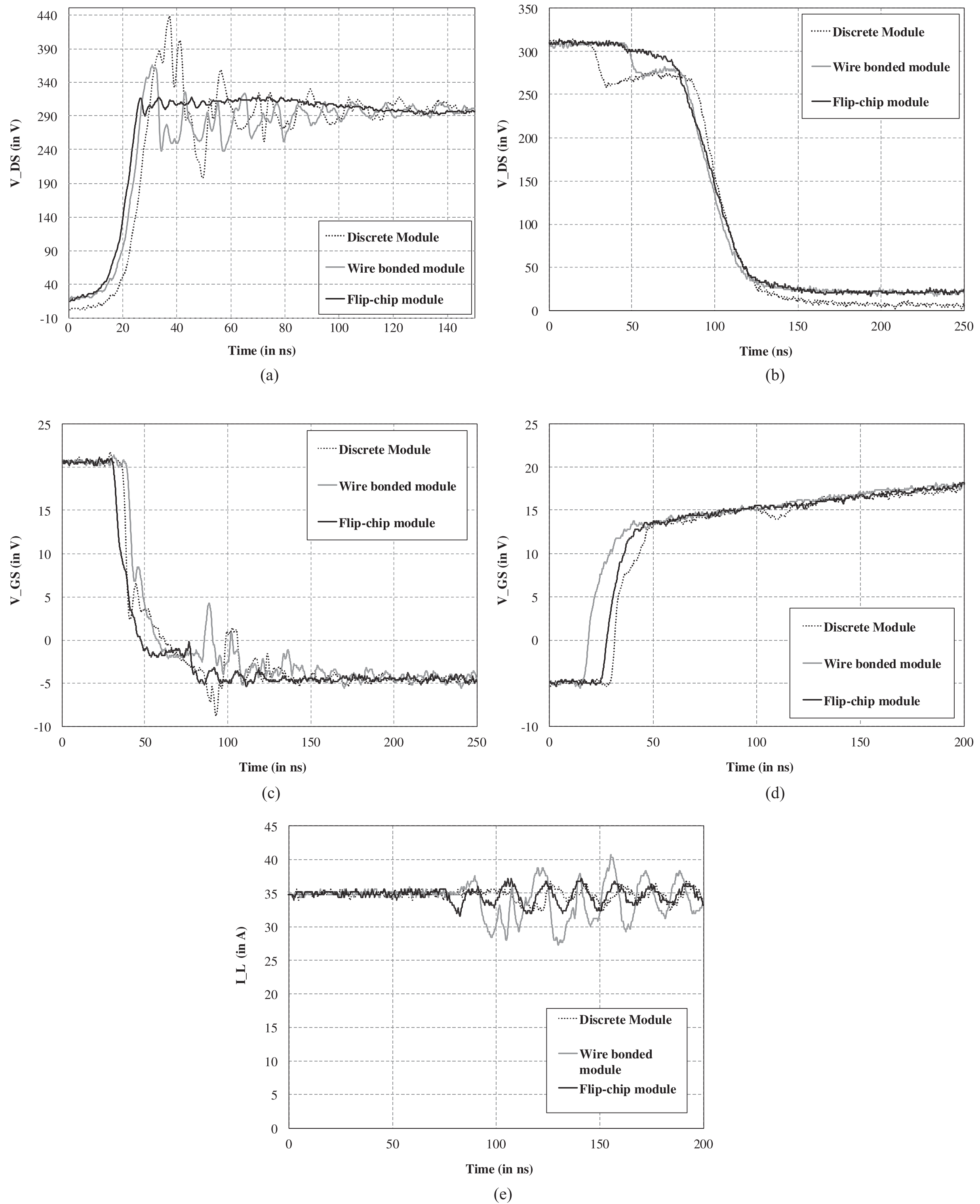

Fig. 12. Plots for the three modules showing the switching characteristics for (a) the output waveforms during turn-off, (b) the output waveforms during turn-on, (c) the gate-source voltage waveforms during turn-off, (d) the gate-source voltage waveforms during turn-on, and (e) waveforms showing the inductor current.

Fig. 14 shows the waveforms of the three modules at a dc-bus voltage of 300 V. It was observed that the frequency of ringing for the flip-chip module was much higher than the discrete and wire-bonded modules. This signified a highly reduced parasitic loop inductance. To quantify this, the loop inductances for the three modules were calculated. The datasheet of the S2301UCSF from ROHM Semiconductor specifies an output capacitance of 110 pF at 300 V. Using this value, the parasitic inductance of the flip-chip half-bridge was calculated to be only 4.88 nH. In comparison, the wire-bonded module offered

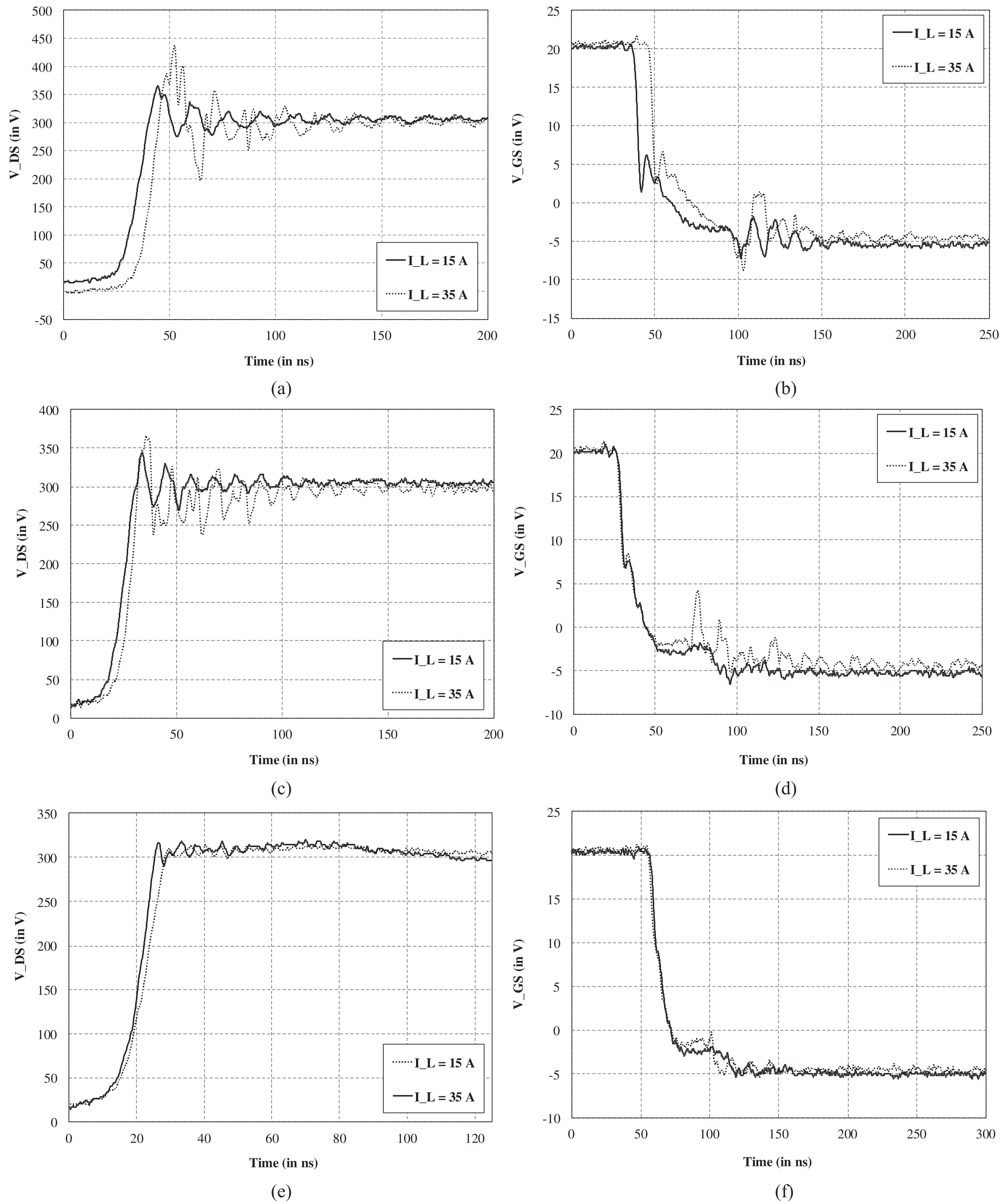

Fig. 13. Waveforms comparing switching characteristics for the three modules showing: (a) the VDS for the discrete module, (b) the VGS for the discrete module, (c) the VDS for the wire-bonded module, (d) the VGS for the wire-bonded module, (e) the VDS for the flip-chip module, and (f) the VGS for the flip-chip module.

TABLE II
CALCULATION OF THE PARASITIC LOOP INDUCTANCES OF THE THREE MODULES UNDER TEST

Output Capacitance of the MOSFET (C_{OSS})	Time Period of Ringing (ns) (Δt)			Parasitic Loop Inductance (nH) $= \frac{(\frac{\Delta t}{2\pi})^2}{C_{\mathrm{OSS}}} \times 10^9$		
	Discrete	Wire-Bonded	Flip-Chip	Discrete	Wire-Bonded	Flip-Chip
110e-12	13	8	4.6	38.96	15.4	4.88

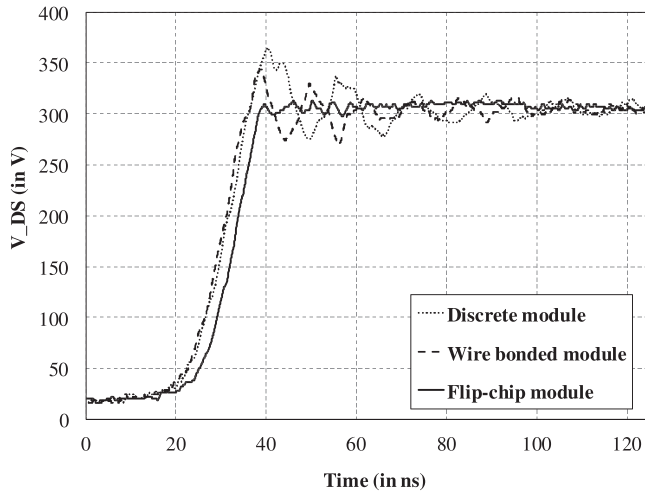

Fig. 14. Waveforms for inductance estimation of the three modules, showing the turn-off waveforms for the drain-source voltage at a bus voltage of 300 V.

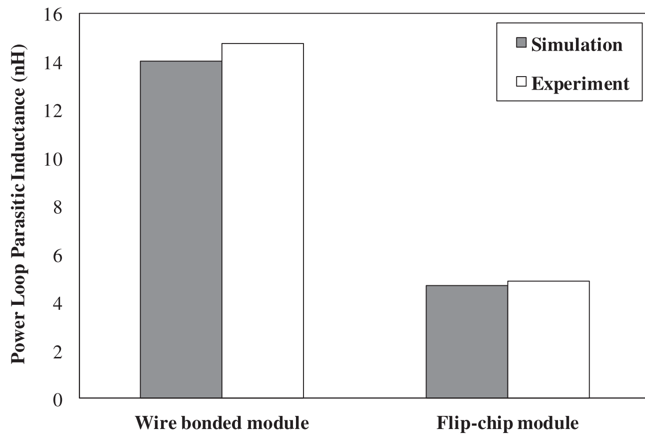

Fig. 15. Bar graph showing a comparison between the simulated and measured values of the parasitic loop inductance for the wire-bonded and flip-chip modules.

a loop inductance of 15.4 nH. Quite predictably, the discrete module offered the most parasitic inductance at 38.96 nH. The calculations are shown in Table II. The low parasitic inductance offered by the flip-chip module was not only encouraging but also matched theoretical predictions closely. Fig. 15 shows a comparison between the predicted and measured values of parasitic inductance for the wire-bonded and flip-chip modules. The discrete module could not be simulated accurately in the absence of details regarding the internal layout and wire bonding scheme. The comparison showed a very close agreement (within 5%) between the predicted and measured values. Additionally, the parasitic resistance of the flip-chip package was 18.41 mΩ, and the corresponding value for the wire-bonded case was estimated to be 49.24 mΩ.

VI. Conclusion

This paper demonstrated a novel flip-chip package for SiC power devices. A process flow for the manufacture of the package was described, along with examples of system implementation using the chip-scale devices. A flip-chip Schottky diode was realized using the wire-bondless power devices and was demonstrated to have 24% lower on-state resistance as compared with a wire-bonded diode. Flip-chip MOSFETs were also fabricated using an identical process flow, and a wire bondless half-bridge module was developed to demonstrate the switching behavior of the MOSFETs. The flip-chip devices with a 3-D vertical power loop managed to reduce the power loop inductance to under 5 nH. This was more than 3$\times$ lower than a custom wire-bonded module. The switching waveforms of the wire bondless module were virtually distortion-free, even at ultrafast rise/fall times of the order of 15–20 ns. These observations make a promising case for the wire bondless packaging of SiC power devices and 3-D power routing to realize ultralow inductances, thus enabling MHz-level switching in SiC power converters.

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