Soft-Switched Interleaved DC/DC Converter as Front-End of Multi-Inverter Structure for Micro Grid Applications

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***Abstract*—An isolated four channel dc/dc converter with zero voltage switching is proposed as the front-end of multiple inverter structures to integrate renewable and other low voltage energy sources to micro grids. The interleaving technique is adopted to connect each module of proposed converter to a common dc source. This dc source can be a fuel cell stack, PV panels, battery, or any other low voltage dc source. All four channels are interleaved and a phase shift of 90° is provided between the gate signals of each channels, which reduces the input current ripple. The output port of the proposed converter provide four isolated and regulated dc voltages. These isolated dc sources can be connected in series or parallel or series-parallel manner to obtain required dc-link voltage of various inverter structure. Issues like capacitor voltage balancing of diode clamped multilevel inverters can overcome through the proposed converter. By incorporating a coupled inductor for isolation and energy storage along with voltage multiplier circuit, the proposed converter can achieve higher voltage step up with lower turns ratio and lower voltage stress at moderate duty ratio. Hence, MOSFETs of low voltage rating (low R_{DS}(ON)) can be utilized to reduce conduction loss. A 2 kW prototype of the proposed interleaved dc/dc converter is developed and tested with diode clamped three-level inverter, five-level inverter, and three-phase two-level inverter to verify the design.**

***Index Terms*—Active clamp, coupled inductor, DC–DC converter, high voltage gain, interleaving, zero voltage switching (ZVS).**

I. Introduction

RAPID industrialization and globalization leads to the exploitation of nonrenewable fossil fuels. Fossil fuels are, thus, at verge of exhaustion. Moreover, these fuels cause carbon emission, global warming, climate changes, and atmospheric pollution. Increasing day by day demand for electric energy of growing population is a major concern for power sector. Aforementioned facts leads to the development of clean and renewable energy sources such as solar photovoltaic (PV), fuel cells, wind energy, and tidal energy. For efficient extraction of energy from these intermitted sources, power electronics converters are required [1], [2]. Output voltage of single PV module and fuel cells are very low and required to step up before connecting to the utility. DC-link voltage of 380–400 V is required for a single phase grid connected inverter system [3]. In case of grid connected three phase full bridge inverter or diode clamped multilevel inverters, dc-link voltage of 760 V or more is preferred [3].

In centralized PV systems, number of PV panels are connected in series to form a string to obtain high-dc voltage. Multiple strings of PV then connected in parallel to realize required power. However, this PV architecture suffers from losses due to partial shading, panel mismatches, poor efficiency of maximum power tracking, and hot spot effects [4]–[6]. To overcome these issues, parallel connected PV structure, multi string structure, and modular PV systems are introduced in [7]–[10]. However, these PV structures produce low voltage dc output, which needs to be step up efficiently. Hence, efficient high voltage gain dc/dc converters is an essential requirement. To overcome the drawbacks of basic boost converter for high voltage step up applications, numerous high voltage gain dc/dc converters are presented in [9], [11]–[18]. Converters in [11] incorporate voltage multiplier circuit in basic boost converter structure to achieve high voltage step up with lower stress. Here, further enhancements of voltage gain require addition of more number of basic voltage multiplier circuits, which increases component count and cost. Use of coupled inductor for high step applications is a good solution [9], [12], [13]. However, care should be taken to deal with leakage inductance and associated voltage spike on switches. Converters in [14] and [15] make use of boost integration technique where a boost converter is integrated with a flyback converter to achieve step up voltage. Here, boost converter acts as a lossless clamping circuit, which recycles the leakage energy of flyback transformer. To enhance the voltage step up gain further, coupled inductor in association with switched capacitor voltage multiplier cells are presented in [16]. These converters are easily able to achieve high voltage

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conversion gain without extreme duty ratio and voltage stress. Soft-switching techniques are incorporated to coupled inductor converters in [17] and [18] to enhance efficiency and power density. All these converters are found to be good choice in medium power level. However, all these converters are nonisolated and do not meet the requirement of galvanic isolations laid down by regulating authorities and industries.

In isolated converters, transformer turns ratio can be adjusted to obtain high voltage step up gain. However, voltage fed converters require large turns ratio, which increases the size as well as leakage inductance of the transformer. Higher voltage stress on output diodes of voltage fed converters force to use high voltage rated diodes or external voltage clamping circuits, which increases the cost. Modular converter scheme is proposed for high voltage gain application in [19]. Here, three or more converters are connected in parallel at input side and in series at output side. Series connection of output terminals of the converter enhance the overall voltage gain. Similarly, input series and output parallel modular dc/dc converter structure and its control is presented in [20]. Flyback converter, which is derived from the buck boost converter is widely used for PV micro inverters in lower power levels [21], [22]. Flyback transformer transfer energy to output during only one switching state. Hence, for high voltage step up, large magnetic core is required, which increases the volume and weight. Isolated coupled inductor and voltage multiplier circuits are incorporated in [23] for high voltage gain. The converter in [23] make use of dual voltage doubler circuit, which reduce voltage stress on output diodes. Passive lossless clamp circuits, which consist of a capacitor, two power diodes and an additional inductor is used to alleviate voltage stress on switches and recycle the leakage energy. Input current ripple is very high in this converter. In addition to this switches are hard switched in [23]. Need of an efficient dc/dc converter system having low input current ripple, high voltage gain, good power density, modularity, and flexibility to use as a front end of multiple inverter structure to interface low voltage energy sources is in demand.

This paper proposes an isolated four channel high step up dc/dc converter with soft switching for low output voltage dc sources. Proposed converter can easily interface with commonly used inverter structures such as single phase inverter, three-phase inverter, diode clamped three level, and five level inverters. Proposed converter produces four isolated and regulated dc voltages. Each of this dc output can be connected in parallel, series or series parallel combination to realize required dc-link voltage of aforementioned inverter structure. At the input side of the converter, all four channels are connected in parallel and interleaving of converters is adapted to minimize the input current ripple. Capacitor voltage balancing of diode clamped inverters is a well known issue. Isolated dc sources can be used as front end active balancing circuit in diode clamped inverters [24] to overcome the voltage balancing problems. Proposed converter provides four isolated and regulated output, which act as the front end of three and five level diode clamped inverters and overcome the capacitor voltage balancing problems. Proposed converter makes use of isolate coupled inductor along with dual voltage multiplier circuits to realize high voltage step up with lower voltage

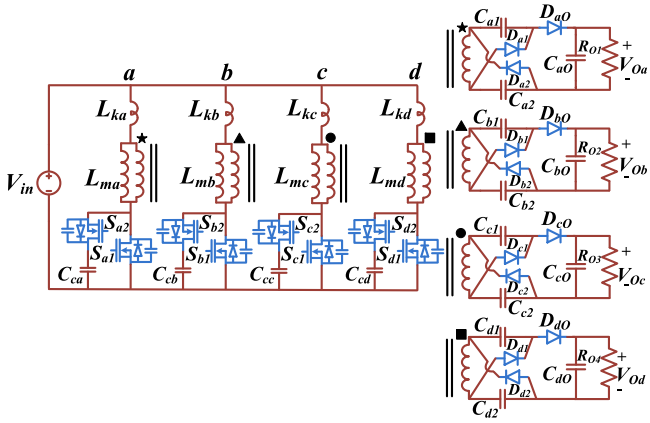

Fig. 1. Proposed interleaved dc/dc converter.

stress. Instead of passive clamp circuit of [23], which requires external inductor and more passive components, proposed converter incorporate active clamp circuits to alleviate the voltage stress due to leakage inductance. The active clamp circuit is originally proposed by Harada and Sakamoto [25]. This clamp circuit is widely used to alleviate voltage spike on MOSFET switches of both forward and flyback converters [26]–[28]. Apart from voltage spike alleviation of switches, active clamp circuit can provide zero voltage turn on of MOSFETs to reduces the switching losses. Hence, high frequency operation is possible, which reduces the size of magnetic components and filter capacitor.

II. Circuit Description and Operation of Proposed Converter

Proposed four channel interleaved converter is shown in Fig. 1. Basic module of each channel (a, b, c, and d) are represented by its equivalent circuit model. Coupled inductor of each channel is represented by its magnetizing inductance (L_{ma}, L_{mb}, L_{mc}, and L_{md}) and leakage inductance (L_{ka}, L_{kb}, L_{kc}, and L_{kd}), respectively. Switches S_{a1}, S_{b1}, S_{c1}, and S_{d1} are the main switches of each channel. Switches S_{a2}, S_{b2}, S_{c2}, S_{d2}, and capacitors C_{ca}, C_{cb}, C_{cc}, C_{cd} form active clamp circuit of each channel, respectively. Coupling references for each channel are represented by symbols "★, ▲, ●, ■." For channel a, voltage multiplier circuit of secondary side consisting of diodes and switched capacitors, which are represented by D_{a1}, D_{a2}, C_{a1}, C_{a2}, respectively. Similar notation is used for other channels also. Diodes D_{a0}, D_{b0}, D_{c0}, and D_{d0} are the output diode of each channel. Main and clamp switch of all channels are operating at same frequency. However, gate signals for each channel is phase shifted by 90° between one another. Each converters output voltage is regulated to its nominal value (200 V) for input voltage and output power variations by voltage mode controller. Due to the symmetry of converter structure, operational principle of converter is explained by considering two channels only. Key waveforms of operations are given in Fig. 2. Operating state of converter during each modes are shown in Fig. 3.

Mode 1 (t_0–t_1): During this mode, main switch S_{a1} of phase *a* and clamp switch S_{b2} of phase *b* are in conduction. At secondary

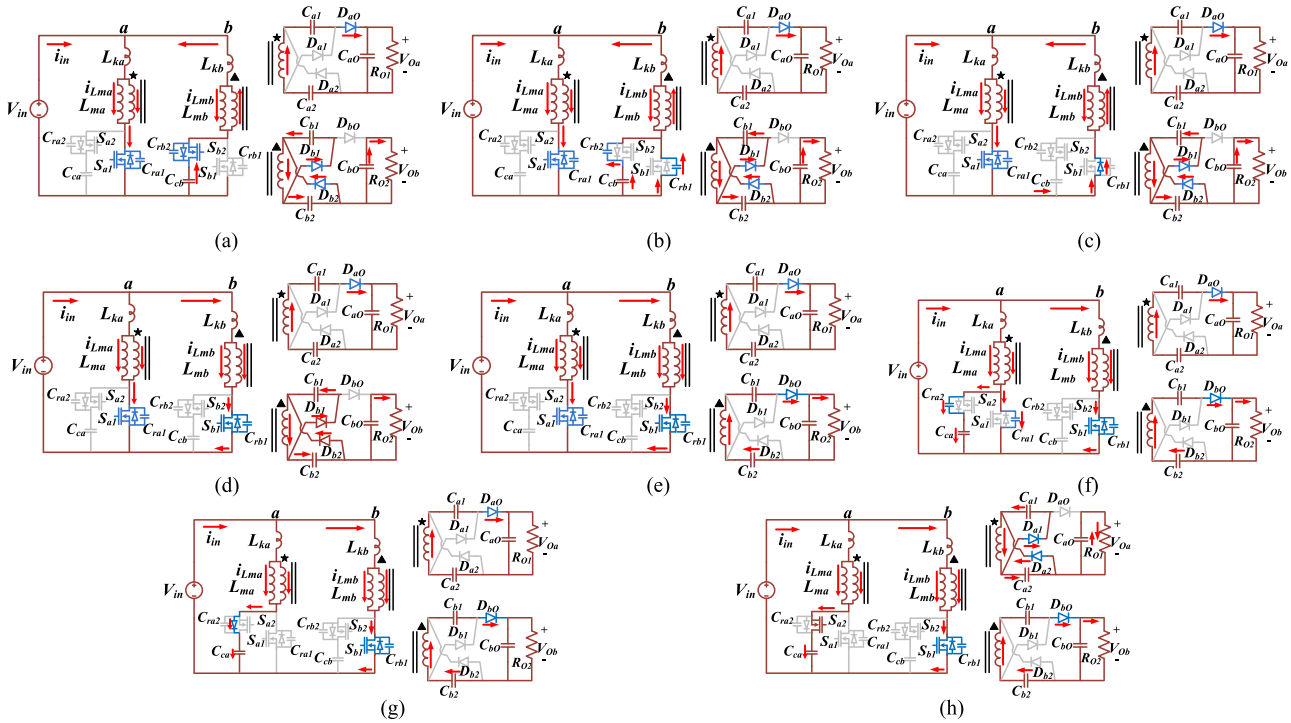

Fig. 3. Different modes of operation of the converter. (a) Mode 1 (t_0–t_1). (b) Mode 2 (t_1–t_2). (c) Mode 3 (t_2–t_3). (d) Mode 4 (t_3–t_4). (e) Mode 5 (t_4–t_5). (f) Mode 6 (t_5–t_6). (g) Mode 7 (t_6–t_7). (h) Mode 8 (t_7–t_8).

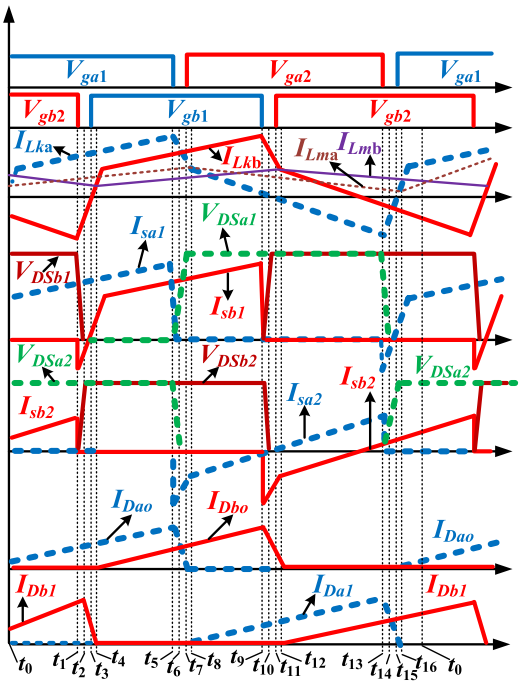

Fig. 2. Key waveforms of the converter.

side of phase a, energy of secondary winding and the capacitors C_{a1} and C_{a2} are transferred to the load through diode D_{a0}. In case of phase b, diode D_{b0} is reverse biased. Secondary winding of phase b, transfer its energy to capacitor C_{b1} and C_{b2} through diodes D_{b1} and D_{b2}.

Mode 2 (t_1–t_2): At t_1, gate signal for clamp switch S_{b2} is withdrawn. Now primary current of phase b charge the output capacitor (C_{rb2}) of S_{b2} and discharge C_{rb1} of S_{b1}.

Mode 3 (t_2–t_3): At t_2, output capacitor C_{rb1} of switch S_{b1} completely discharged. Now primary current of phase b start conducting through the body diode of switch S_{b1}. The clamp switch S_{b2} is in off state. Operation of phase a is same as that of mode 1.

Mode 4 (t_3–t_4): While body diode of S_{b1} is conducting, gate signal to S_{b1} is applied at $t = t_3$. Hence, main MOSFET (S_{b1}) of phase b turn on with soft switching [zero voltage switching (ZVS)]. The primary current of phase b is start to increase linearly.

Mode 5 (t_4–t_5): At t_4, polarity of secondary winding of phase b reverse biases the diodes D_{b1}, D_{b2}, and forward bias output diode D_{b0}. Now reflected voltage at the secondary winding of phase b and stored energy of capacitors C_{b1} and C_{b2} transfer their energy to load in series.

Mode 6 (t_5–t_6): At t_5, gate signal for the main switch S_{a1} of phase a is withdrawn. Now primary current of phase a charges the output capacitor (C_{ra1}) of S_{a1} and discharge the output capacitor (C_{ra2}) of S_{a2}. At secondary side, both phase a and phase b are transferring energy to their respective loads.

Mode 7 (t_6–t_7): The output capacitor (C_{ra2}) of Switch S_{a2} is discharged to zero at t_6. Now body diode of clamp switch S_{a2} is conducting the primary current of phase a where main switch S_{a1} is in off state.

Mode 8 (t_7–t_8): At t_7, gate signal to clamp switch S_{a2} is applied. Clamp switch S_{a2} turn on with ZVS. The output diode (D_{a0}) of phase a is reverse biased. Now secondary winding of phase a charges the capacitors C_{a1} and C_{a2} through diodes D_{a1}

and D_{a2}, respectively. Secondary winding of phase b continue to transfer its energy to the load trough diode D_{b0}.

There are 16 modes of operation for the converter. However, due to the symmetry of converter, remaining eight modes are very similar to that of aforementioned modes and, hence, not discussed in detail.

III. Mathematical Analysis and Design of Proposed Converter

Steady state analysis of the converter is done with following assumptions.

1) Leakage inductance and its effect are not considered for this analysis.
2) Only average voltage across the capacitors are considered (ripple componets are neglected).
3) All semiconductor devices are considered to be ideal.
4) Modes having very small time intervals are neglected including the dead time interval between the MOSFETs.
5) Only one phase (Phase a) is considered due to symmetry.

A. Voltage Conversion Ratio (M) of the Converter

When the main switch S_{a1} of phase a is ON, voltage across the magnetizing inductance is given by

$$V_{L_{ma}}^{\mathrm{ON}} = V_{\mathrm{in}} \tag{1}$$

$$V_{oa} = V_{Ca1} + V_{Ca2} + V_{\mathrm{sec}-a}^{\mathrm{ON}} \tag{2}$$

$$V_{\mathrm{sec}-a}^{\mathrm{ON}} = NV_{\mathrm{in}}. \tag{3}$$

Let

$$V_{Ca1} = V_{Ca2} = V_{Ca} \tag{4}$$

$$V_{Ca} = \frac{V_{oa} - NV_{\mathrm{in}}}{2}. \tag{5}$$

When main switch S_{a1} is turned OFF

$$V_{\mathrm{sec}-a}^{\mathrm{OFF}} = -V_{Ca2} = -V_{Ca} \tag{6}$$

$$V_{L_{ma}}^{\mathrm{OFF}} = \frac{-V_{Ca}}{N}. \tag{7}$$

Over one switching period, applying volt-second balance of magnetizing Inductance we yield

$$DV_{\mathrm{in}} + (1-D)\frac{-V_{Ca}}{N} = 0. \tag{8}$$

From (1) to (8), Ideal voltage conversion gain (M) of proposed converter is obtained as

$$M_{(\mathrm{ideal})} = \frac{V_{oa}}{V_{\mathrm{in}}} = \frac{N(1+D)}{1-D}. \tag{9}$$

Here, N stands for the turn ratio and D is the duty ratio. The leakage inductance of the converter cause duty cycle loss, and thus, reduces the voltage conversion gain. The duty cycle loss due to the leakage inductance can be obtained from the idealized leakage inductance current as shown in Fig. 4.

$$D_{\mathrm{eff}} = D - \Delta D. \tag{10}$$

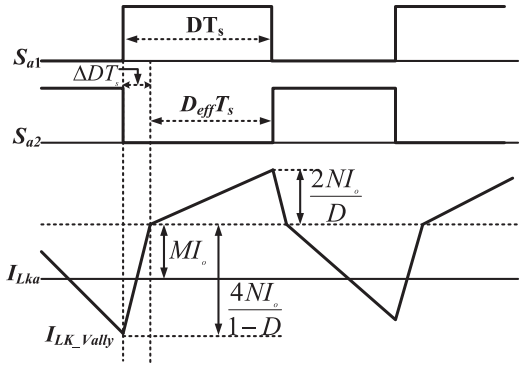

Fig. 4. Idealized current waveform to calculate effective duty cycle due to leakage inductance effect.

Expression for the voltage across the leakage inductance is given by

$$V_{Lk} = L_k \frac{dI_{Lk}}{dt}. \tag{11}$$

Hence, expression for duty cycle loss is obtained as

$$\Delta D = \frac{k.4N^2(1+D)}{(1-D)}. \tag{12}$$

Where $k = \frac{L_k f_s}{R_o}$. From (9), (10), and (12), voltage gain of the converter by considering the leakage inductance effect is obtained as

$$M_{(\mathrm{leakage})} = \frac{V_{oa}}{V_{\mathrm{in}}} = \frac{N(1+D_{\mathrm{eff}})}{(1-D_{\mathrm{eff}})}. \tag{13}$$

B. Voltage Across Various Elements

From (4) and (5), voltage across the capacitors C_{a1} and C_{a2} is obtained as

$$V_{Ca1} = V_{Ca2} = \frac{\mathrm{NDV_{in}}}{1-D} = \frac{DV_{oa}}{1+D}. \tag{14}$$

Voltage stress across the main switch S_{a1} and clamp switch S_{a2} is obtained by

$$V_{DSa1} = V_{DSa2} = V_{\mathrm{in}} - V_{L_{ma}}^{\mathrm{OFF}} = V_{\mathrm{in}} + \frac{V_{Ca}}{N}. \tag{15}$$

Hence, voltage stress across the MOSFETs switches of proposed converter is given by

$$V_{DSa1} = V_{DSa2} = \frac{V_{\mathrm{in}}}{1-D}. \tag{16}$$

Voltage stress on the output diode D_{ao}, voltage multiplier diodes D_{a1} and D_{a2} is obtained as

$$V_{Da1} = V_{Da2} = V_{Da0} = \frac{V_o}{1+D}. \tag{17}$$

C. Design of Coupled Inductor

The peak ripple current of magnetizing inductance is given as

$$\Delta i_{\mathrm{L_{ma}}} = \frac{V_{\mathrm{L_{ma}}} D}{L_m f_s}. \tag{18}$$

Proposed converter is designed to operate in continuous conduction mode (CCM). At boundary between continuous and discontinuous conduction mode (BCM), average value of the converter's input current is half of the peak magnetizing current. Therefore

$$I_{\text{in}} = \frac{\Delta i_{\text{L-ma}}}{2}. \tag{19}$$

At steady state, assuming no losses

$$\frac{V_{oa}}{V_{\text{in}}} = \frac{I_{\text{in}a}}{I_{oa}} = M. \tag{20}$$

Hence

$$\frac{I_{oa}N(1+D)}{1-D} = \frac{V_{\text{in}}D}{2L_{ma}f_s}. \tag{21}$$

Therefore, magnetizing inductance of coupled inductor required to operate the converter in CCM is derived as

$$L_{ma} > \frac{R_{O_{\text{BCM}}}D(1-D)^2}{2f_sN^2(1+D)^2}. \tag{22}$$

D. Selection of Switched Capacitors C_{a1} and C_{a2}

Switched capacitors C_{a1} and C_{a2} are selected as follows:

$$C_{a1} = C_{a2} \geq \frac{2P_{\max}}{V_{Ca}^2 f_s} \tag{23}$$

where $P_{\max}$ is the maximum power that can be delivered to load by individual converter.

E. Selection of Clamp Capacitor C_{ca}

Value of clam capacitor is calculated based on resonant period between clamp capacitor C_{ca} and leakage inductance L_{ka} and is obtained as

$$C_{ca} \geq \frac{(1-D_{\min})^2}{\pi^2 L_{ka} f_s^2}. \tag{24}$$

F. Selection of Output Capacitor

The output voltage of the converter should be ripple free (ideally pure dc voltage). The output capacitor of proposed converter need to reduce the output voltage ripple as minimum as possible. Hence, main criteria for the section of output capacitor is output voltage ripple (ΔV_o). When main switch of the proposed converter is in off state, the load is supported by the stored energy of output capacitor. Hence, the change in output voltage is expressed as

$$\Delta V_o = \frac{Q}{C_o} = \frac{I_o(1-D)T_s}{C_o} \tag{25}$$

where Q is the stored energy in the output capacitor. The expression for output capacitance of proposed converter is obtained as

$$C_o \geq \frac{I_o(1-D_{\min})}{\Delta V_o f_s}. \tag{26}$$

In proposed converter, output voltage ripple is taken as 0.1% of the output voltage ($\Delta V_o = 0.2$ V). The output capacitor value is calculated for minimum duty cycle and obtained as 98.75 μF. To reduce the equivalent series resistance (ESR) of output capacitor, higher value of capacitance (200 μF) is selected. Two 100 μF, electrolytic capacitors are connected in parallel to reduce the ESR effect.

TABLE I
COMPARISON BETWEEN THE ACTIVE CLAMP FLYBACK CONVERTER, CENTER TAP HALF-BRIDGE CONVERTER, AND PROPOSED SOFT-SWITCHED CONVERTER

Parameter	Active clamp flyback Converter	Center tap half-bridge converter	Proposed soft-switch converter
MOSFETs	2	2	2
Diodes	1	2	3
Magnetic component	1	2	1
Voltage gain	$\frac{ND}{1-D}$	ND	$\frac{N(1+D)}{1-D}$
Voltage stress on MOSFET	$\frac{V_o}{ND}$	$\frac{V_o}{ND}$	$\frac{V_o}{N(1+D)}$
Voltage stress on output diode	$\frac{V_o}{D}$	$\frac{V_o}{D}$	$\frac{V_o}{1+D}$
Soft switching of MOSFETs	ZVS	hard switch	ZVS

Proposed converter topology is derived from flyback converter. However, the transformer polarities are similar to forward type converter. The coupled inductor of conventional active clamp circuit transfer energy to output only at one switching instant. Thus, conventional flyback converter requires large magnetic core. In proposed converter, coupled inductor transfer its energy to secondary side during both switch ON and OFFinstant, and thus, have better magnetic utilization compared to the flyback topology. Another two switch converter commonly used is half-bridge converter with center tap output rectifier. For high voltage step up application, half-bridge converter need large turns ratio. This will increase the required core size of the isolation transformer. In addition to this, large turn ratio increases the leakage inductance of the isolation transformer. Leakage inductance cause voltage stress on the MOSFETs, and thus, snubber circuits are required to alleviate voltage stress on the switches. Comparison of active clamp and center tap half-bridge converter with proposed soft-switch converter is shown in Table I. For high step up applications, voltage stress on output diode of both flyback and half-bridge converter is much higher than the output voltage. Thus, diodes of high voltage rating are needed in half-bridge and flyback converters when used for voltage step-up applications. High voltage rated diodes adversely affect the switching performance, and thus, high frequency operation is not preferable. The leakage inductance of the transformer forms a resonance with parasitic capacitance of the output rectifier diodes. This resonance causes voltage ringing across the diodes. Hence, lossy resistor, capacitor, diode (RCD) snubber or external active snubbers are required to protect the output diodes from voltage excursion. However, unproposed converter, output diode voltage stress in lower than the output voltage. Hence, no additional snubber is required to protect the diodes. In addition to this, maximum duty cycle operation of half-bridge converter is restricted to be 0.5, which limits the operation for a wide input voltage variation. Both the switches of half-bridge converters are hard switched and cause switching losses. Soft switching of

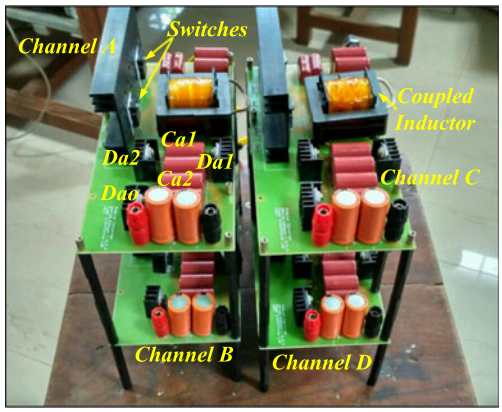

Fig. 5. Photograph of proposed 2 kW interleaved converter.

TABLE II
SPECIFICATIONS OF THE HARDWARE PROTOTYPE

Components	Specifications
Output Power	2 kW
Number of channels	4
Each channel's output power	500 W
Input range	45–65 V
Output voltage of each channel	200 V
MOSFETs	IRFP4227pbf
Diodes	BYC10D600
Switching frequency	100 KHz
Turns ratio	1:2
Switched Capacitors	20 μF (2 $\times$ 10 μF of 250 V)
Output capacitor	200 μF
Magnetizing Inductance	113 μH
Clamp capacitor	9.4 μF (2 $\times$ 4.7 μF)

half-bridge converter can obtain by introducing resonant tank circuits. However, this requires additional inductor and capacitors to be added and also face the voltage regulation problem light load. Compared to half-bridge and flyback converter, the proposed topology has advantages, such as high voltage gain, low voltage stress on output diodes, and soft switching of all MOSFET switches, require lower turns ratio for voltage step-up, no need of additional snubber for output diode protection, etc. Thus, for high voltage step up applications, proposed converter scheme is more suitable than the voltage fed half-bridge, flyback and full bridge topologies.

IV. EXPERIMENTAL VALIDATION OF PROPOSED CONVERTER

An experimental prototype of proposed 2 kW, four channel interleaved converter is fabricated in laboratory. Each individual channels are of 500 W. Photograph of the prototype is shown in Fig. 5. Details of hardware prototypes are given in Table II. E55 core is used for coupled inductor. Structure of the coupled inductor is given in Fig. 6. Primary and secondary winding are wound on the bobbin, which is placed on the middle limb. Litz wires are used to wound the primary and secondary in order to reduce the skin effect. After wounding the primary, masking tapes (insulating paper) is used to separate primary and secondary winding. The winding structure is shown in Fig. 6(b). Finally polymide film tape (Kapton) is wrapped

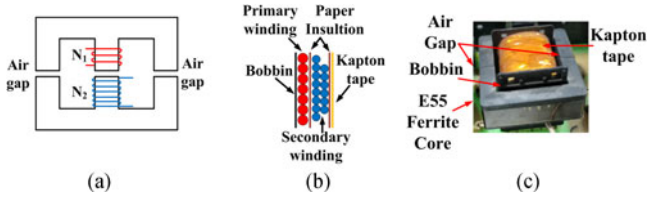

Fig. 6. Structure of coupled inductor. (a) Schematic representation. (b) Winding structure. (c) Actual picture.

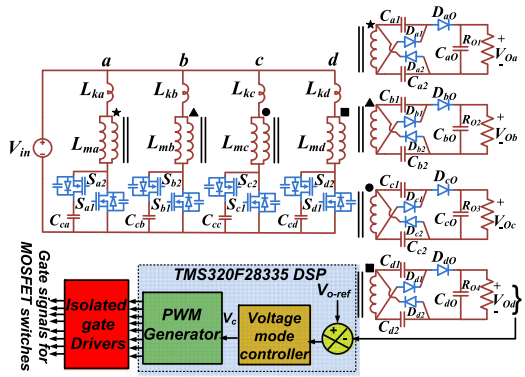

Fig. 7. Controller diagram of proposed converter structure.

around the windings. Polymide tapes have high thermal stability. Primary and secondary winding can be wound in interleaved manner to reduce the leakage inductance. However, in proposed converter, leakage inductance is a blessing in disguise to maintain ZVS of main MOSFETs for wide load variations. Hence, primary and secondary are wound separately and provided insulation in between. Proposed converter have high dc bias current. This dc current will saturate the ferrite core. To alleviate the core saturation, air gap is provided in the magnetic path. Panasonic make metalized Polyester film Capacitors are selected for clamp and switched capacitors. MOSFET IRFP4227pbF having low $R_{ds(\text{on})}$ (21 mΩ) is used for main and clamp switch of each converter. Floating point digital controller (TMS320F28335) is used to control the proposed converter. Voltage mode controller is adopted to control the output voltage of the converter. Since all the converters are identical and constructed with same specification, authors are adopted a single voltage feedback from one channel and used this information to control the output voltage of other channels as shown in Fig. 7. The coupled inductor of each converter is constructed for same turn ratio, magnetizing inductance and leakage inductance. However, even all the cares are taken to make the coupled inductor identical to each other, it is very difficult to obtain the leakage inductance of all the four coupled inductor identical. Thus, leakage inductance of coupled inductor is slightly different for each channel. From (12), the duty cycle loss and, thus, output voltage variation due to leakage inductance can be obtained. The coupled inductor of proposed converter is wound in manner to get close values of leakage inductance between each channel. In experimental prototype, the measured leakage inductances of each channel are $L_{ka} = 1.53\,\mu$H, $L_{kb} = 1.51\,\mu$H, $L_{kc} = 1.495\,\mu$H, and $L_{kd} = 1.503\,\mu$H, respectively. The maximum variation in output voltage between the channels due

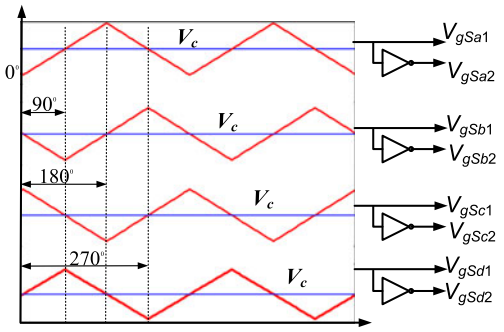

Fig. 8. Schematic of generating 90° phase shifted gate signals for the converter.

to leakage inductance effect is below 0.4%. However, during experimentation, other nonidealities and variation due to temperatures are presented. At full load, for minimum input voltage, the maximum output voltage variations between the channels a and channel c is 1.8 V. This is acceptable for the application point of view where converter is feeding to the dc link capacitors of various inverters. Since magnetizing and leakage inductance of all the four channels are almost identical, the current sharing problem is not severe in proposed converter structure. This can be seen from the experimental result of input current waveforms where all current peaks are nearly same and uniform.

Since the output voltage variation of proposed converter is very small between four output channels, authors implemented simple voltage mode control strategy. Here, output voltage of channel d (whose leakage inductance is very close to the desired designed value of 1.5 μH) is sensed through voltage sensor and feed to TMS20F28335 controller. The voltage controller output signal (V_c) is then feed to the digital pulse width modulation (PWM) modulator (ePWM module in DSP controller), which perform the duty of comparator. To generate phase shift of 90° between each channel, dedicated phase shift registers (TBPHS) are available in ePWM modules of C2000 controllers. Required phase shift value is written in this register. The first ePWM module is acting as a MASTER and remaining three PWM modules are SLAVES. The slave PWM modules are synchronized with the MASTER units and generate the carrier signals of same frequency of master with required phase shift. Master unit generate the synchronization signal for the first slave with the time delay of 90°. The first slave generates synchronization signal for the second slave after a delay of 90° and so on. Thus, the carrier triangular signals are phase shifted by 90° each other. The compare registers of master and slave PWM modules are feed with digital equivalent value of control voltage (V_c). Hence, master and slaves produces the PWM signals of same frequency and duty ratio but phase shifted by 90° each other. The basic operation of generating phase shift of 90° for each channel is depicted in Fig. 8.

Gate signals for main and clamp switches of all channels are of same frequency. In Fig. 9(a), gate signals for the main switches of all four channels are shown. Gate signals of clamp switches are complementary to the main switches of each channels. In Fig. 9(b), gate signal for main and clamp switches of channel a and channel b are depicted. Proposed converter is tested for full load condition. Input currents of individual channels at full load for source voltage of 55 V ($V_{\text{in}} =$ 55 V) is shown in Fig. 9(c). In Fig. 9(d), resultant input current drawn from the input source by interleaving operation of all the four channels is shown. It is clear that resultant input current due to the interleaving operation have less ripple compared to the input currents of individual converters. Drain to source voltage (voltage stress) of main MOSFET of all channels are shown in Fig. 9(e). Clamp circuit successfully alleviated the high voltage spike due to leakage inductance and clamp the voltage stress near to 100 V. Hence, low voltage rated MOSFETs which, have lower $R_{ds(\text{on})}$ can be selected for main and clamp switches, which reduces the conduction loss. All MOSFETs switches of proposed converter turn ON with ZVS. In Fig. 9(f), ZVS turn on of main and clamp switches of channel a is shown. ZVS turn on region is highlighted in Fig. 9(f). The switch currents and input currents of all channels are measured with AP015 current probe. Voltage stress on diodes (D_{a1}, D_{a2}) of voltage multiplier circuits of channel a is shown in Fig. 9(g) along with input current of same channel. In Fig. 9(h), voltage stress on output diode (D_{a0}) and the diode D_{a1} of channel a is depicted. From these results, it is evident that voltage stress on all diodes are well below the output voltage of converter. In addition to this, there is no voltage spike or ringing across the diodes. Therefore, over voltage protection for diodes are not required in proposed converter.

ZVS of main switch (S_{a1}) is load depended and the ZVS characteristic will loss at light load condition. ZVS of main switch mainly depends on the stored energy of leakage inductance. However, for clamp switch (S_{a2}), maintaining ZVS at light load is possible due to the stored energy of both leakage and magnetizing inductance. Hence, irrespective of load condition, clamp switch can maintain ZVS for wide load range. To achieve ZVS of main switch S_{a1}, the energy stored in the leakage inductance (L_{ka}) at time instant t_{13} of Fig. 2 should be sufficiently high to discharge the parasitic capacitance of switch S_{a1} and charge the parasitic capacitance of switch S_{a2}. Thus, the condition for ZVS of main switch S_{a1} is obtained as

$$\frac{1}{2}L_{ka}I_{Lk(t_{13})}^2 \geq \frac{1}{2}C_{r_{(\text{eff})}}V_{\text{Dsa}}^2. \tag{27}$$

Here, $C_{r_{\text{eff}}}$ is the effective parasitic capacitance of S_{a1} and S_{a2}, which can be obtained from the data sheet of MOSFETs. The above relationship can be expressed as

$$L_{ka}\left[\frac{4N}{1-D}\right]^2 I_o^2 \geq C_{r_{(\text{eff})}}V_{\text{Dsa}}^2. \tag{28}$$

The minimum load condition at which ZVS of the main switch is maintained is, thus, obtained as

$$I_{o-\min} = \sqrt{\frac{C_{r_{(\text{eff})}}}{L_{ka}}}\frac{V_{\text{Dsa}}}{\left[\frac{4N}{1-D} - M\right]}. \tag{29}$$

From above relationship, for an input voltage of 65 V, it is found that the ZVS of the main switch can theoretically obtained up to 12% of the full load condition. However, in actual practice,

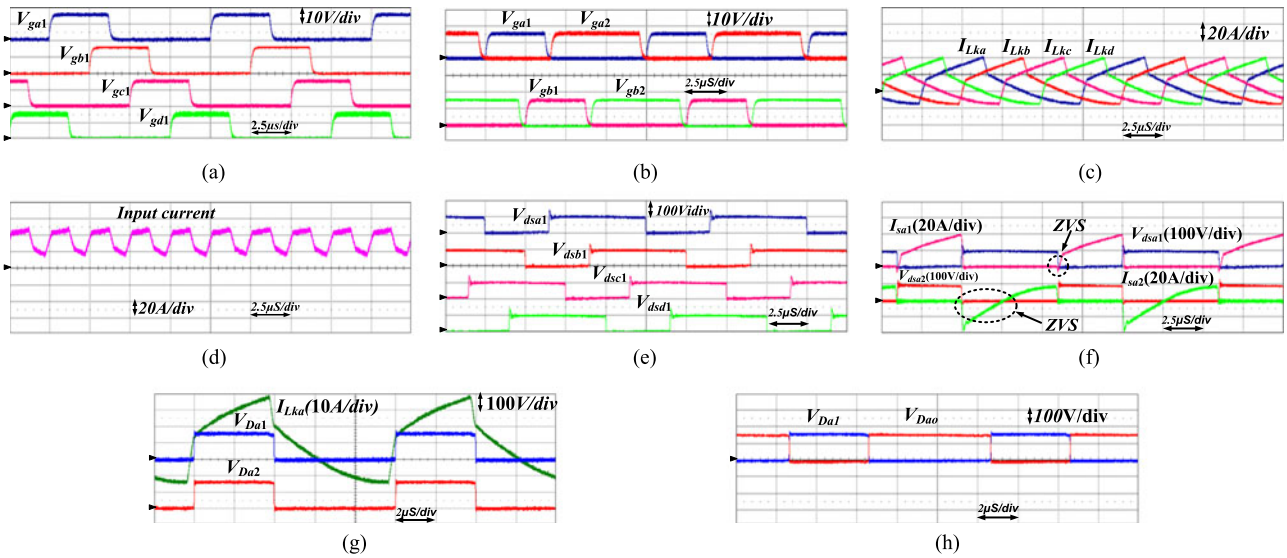

Fig. 9. Experimental results at full load for $V_{\text{in}} = 55$ V. (a) Gate signals for main switches of all four channels which are phase shifted by 90°. (b) Gate signals for main and clamp switches of channel a and channel b. (c) Input current drawn by individual channels at full load. (d) Resultant input current drawn from the input source at full load by interleaving operation of all four channels. (e) Voltage stress across the main switches of all four channels at full load. (f) Soft turn on (ZVS) of main and clamp switches of channel a, ZVS turn on region is highlighted. (g) Voltage stress across the voltage multiplier diodes D_{a1} and D_{a2} of channel a along with input current of same channel. (h) Voltage stress across the output diode D_{a0} of channel a along with voltage stress of diode D_{a1}.

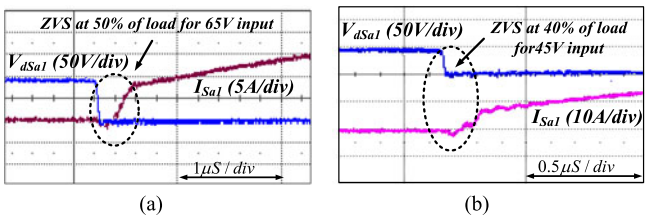

Fig. 10. Experimental results. (a) ZVS turn on of main switch at 50% of full load for an input voltage of 65 V. (b) ZVS turn on of main switch at 40% of full load for an input voltage of 45 V.

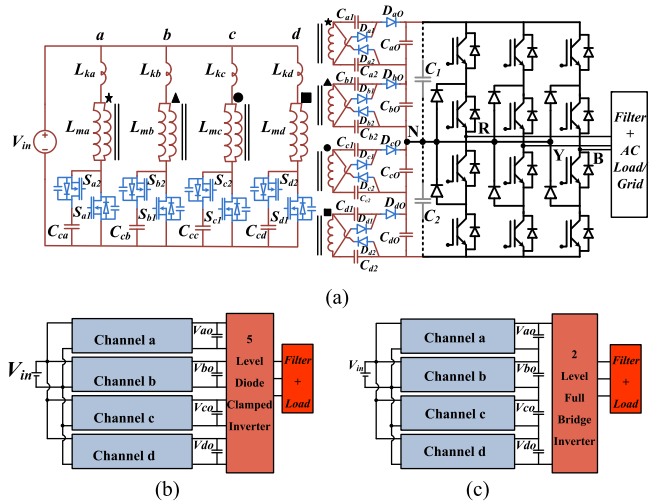

Fig. 11. Schematic of proposed converter feeding to different inverter structures. (a) Proposed converter feeding to a three-phase three-level NPC inverter. (b) Proposed converter connected to a five-level diode clamped inverter. (c) Proposed converter feeding a three-phase two-level inverter structure.

ZVS of the main switch is maintained only up to 28% of the full load. This reduction in ZVS range is due to the PCB track capacitance, large capacitance of transformer winding etc. In Fig. 10(a), zero voltage turn on of main switch of channel a at 50% of the full load is shown. In Fig. 10(b), ZVS turn on of the main switch at 40% of the full load is given when the input voltage is 45 V.

Isolated output port of proposed converter can be connected in series, parallel or combination of series-parallel to obtain required dc-link voltage for various inverter structure. To validate this, proposed converter is tested with three phase, three-level neutral point clamped (NPC) inverter, two level inverter, five level inverter etc. and results are provided. In Fig. 11(a), schematic of proposed converter feeding a three level NPC inverter is shown. Output ports of all the channels are connected in series to obtain dc-link voltage of 800 V (More than 750 V dc voltage is preferred in case of grid connected applications). Neutral point of inverter is connected between the channel b and c. Hence, with respect to neutral point, dc voltage across the capacitors C_1 (V_{C1}) and C_2 (V_{C2}) are +400 V and −400 V, respectively. Capacitor balancing problem is predominant in five level diode clamped inverters. In [24], capacitor voltage balancing of five level diode clamped inverter using a three level dc/dc converter is proposed. In [24], two inner dc link capacitors of five level diode clamped inverter is balanced by the regulated output voltage of three level dc/dc converter. However, for remaining two outer capacitors, additional balancing circuit is required. In [24], balancing circuit of each outer capacitors consist of additional external inductor, MOSFETs, diodes, voltage sensing circuits, and additional control circuits. This makes the system more complex and difficult to control. In proposed converter, each isolated output channels can connected to five-level diode clamped inverter as shown in Fig. 11(b). Each output channels provides regulated dc output voltage, and thus, balance the capacitor voltage of five-level NPC without external balancing

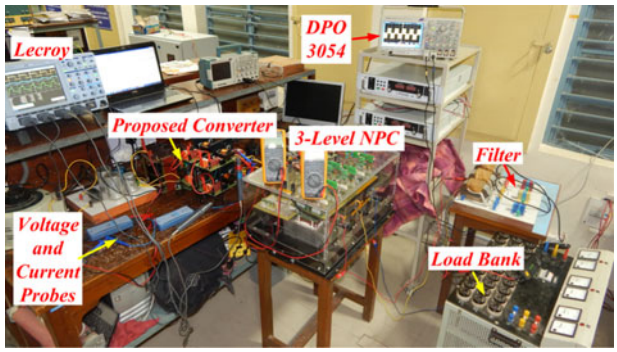

Fig. 12. Experimental set of proposed converter feeding energy to three-phase three-level NPC inverter.

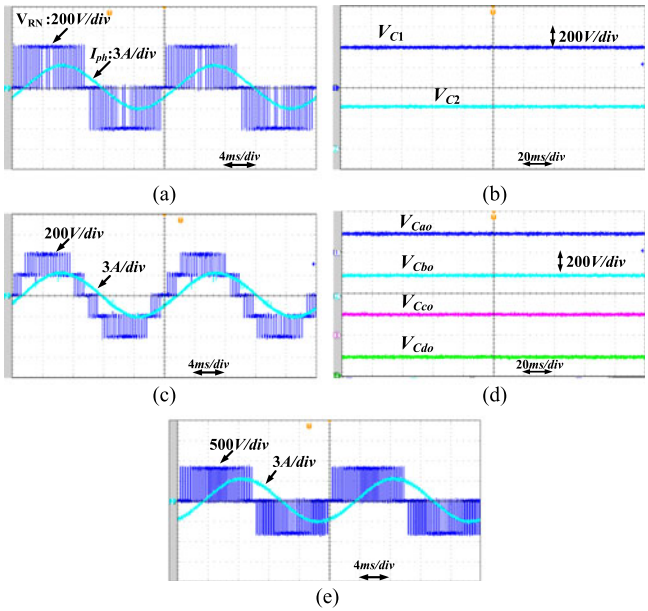

Fig. 13. Experimental results. (a) Phase voltage and current of three level inverter feeding R-L load of 0.85 power factor. (b) Regulated and balanced dc-link voltage of three-level diode clamped inverter. (c) Phase voltage and current of five level diode clamped inverter feeding to R-L load of 0.85 power factor. (d) Balanced dc-link voltage of five level diode clamped inverter, which is regulated by proposed converter. (e) Line voltage and current of two level full bridge inverter feeding R-L load of 0.85 power factor.

circuits. In Fig. 11(c), schematic of proposed converter feeding a three-phase two-level inverter is given.

Feasibility of proposed converter to act as a front end for various inverter structure is experimentally verified. Experimental setup of proposed converter feeding a three-phase three-level NPC inverter is shown in Fig. 12. For experimentation, SEMIKRON made three-level inverter, which is available in the laboratory is used. Capacitors C_1 and C_2 are inbuilt in SEMIKRON inverter. However, by designing the output capacitors C_{a0} to C_{d0}, according to the required power level and voltage ripple, capacitors C_1 and C_2 can be eliminated. Inverter control is done with TMS320F28377d DSP. In Fig. 13(a), phase voltage and current of three-level inverter feeding R-L load of 0.85 power factor is shown. Loads are star connected. Input capacitor voltages V_{C1} and V_{C2} of three-level NPC inverter is constituted by output voltage of proposed converter as mentioned earlier. Balanced dc-link voltages V_{C1} and V_{C2} of three-levels NPC inverter is given in Fig. 13(b). Proposed converter is also tested with five-level diode clamped inverter and two-level inverter structures. Experimental setup is made according to schematic given in Fig. 11(b) and (c) and results are provided for the same load condition of three-level set up. Phase voltage and load current of five-level diode clamped inverter is given in Fig. 13(c). Balanced dc-link voltages of five-level inverter, which is constituted by the regulated and isolated output voltages of proposed converter is shown in Fig. 13(d). As evident from these results, proposed converter's regulated output voltages overcome the capacitor voltage balancing issues of diode clamped inverters. Line voltage and current of three-phase two-level inverter is shown in Fig. 13(e). During all these conditions, proposed converter structure was able to provide balanced and regulated voltages for different inverter structures.

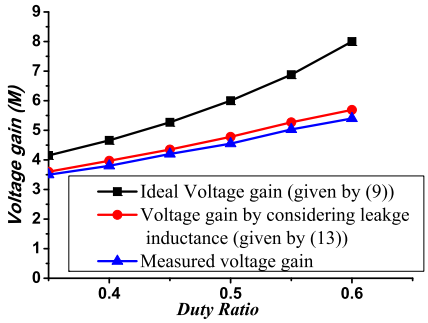

Fig. 14. Steady state curves on theoretical and measured voltage conversion gain of single converter (channel a).

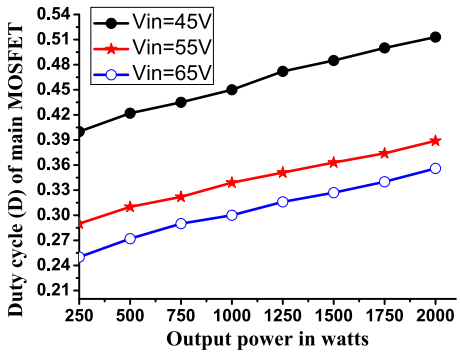

Fig. 15. Output power versus duty cycle of the converter.

Steady state curve for theoretical and measured voltage conversion gain of the converter (channel a) is depicted in Fig. 14. Here, ideal voltage conversion gain of the converter is obtained from the (9) and plotted for duty ratio ranging from 0.35 to 0.6. The leakage inductance of coupled inductor reduces the effective duty cycle of the converter. This duty cycle loss reduces the voltage gain of the converter compared to the ideal one. The voltage gain of the converter considering the effect of leakage inductance is obtained by the (13). Experimentally measured voltage gain of the converter is still less than that of the voltage gain due to the leakage inductance effect. This is due to the voltage drop across the parasitic elements like resistance of coupled inductor, voltage drop across the diodes and MOSFETs etc. In Fig. 15, steady state output power versus

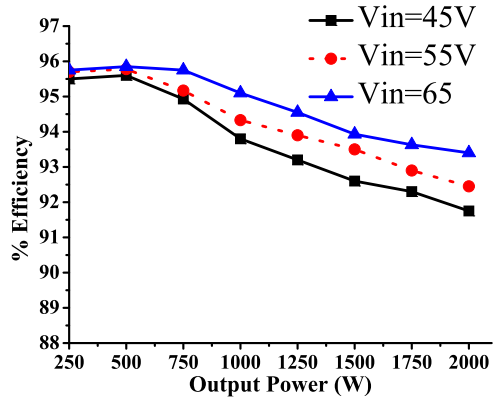

Fig. 16. Efficiency plot of proposed converter for input voltages of 45 V, 55 V, and 65 V.

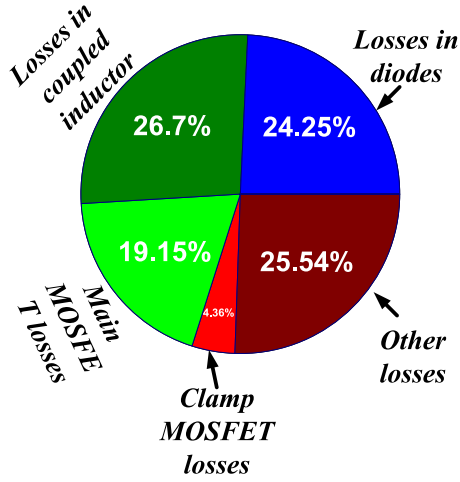

Fig. 17. Measured loss distribution of proposed converter at full load for 45 V input.

duty cycle of the proposed converter is given. Here, all the four converters are connected in interleaved manner to the common input source. The output voltage of all converters is regulated to 200 V through voltage mode controller. The output ports of each converter are connected in series to form 800 V dc bus and then feed to the resistive load bank. The output power versus duty cycle is plotted for an input voltage of 45 V, 55 V, and 65 V. Here, duty cycle D represents the duty cycle of main MOSFET switches of each channels (S_{a1}, S_{b1}, S_{c1}, and S_{d1}). All the four channels are operating at same switching frequency and duty ratio. However, gate pulses are phase shifted by 90° to reduce the input current ripple.

Efficiency of proposed converter is measured for different load and input voltages. Designed input voltage range of proposed converter is 45–65 V. Efficiency of the converter is measured for designed maximum input voltage (65 V), minimum input voltage (45 V) and an intermediate input voltage (55 V). Efficiency curve for above conditions are shown in Fig. 16. Highest efficiency of proposed converter is obtained as 95.83% for the designed maximum input voltage of the converter. Measured lowest efficiency is found to be 91.75% at full load condition where the input voltage is at designed minimum value (45 V). From efficiency plot, it is clear that proposed converter can operate with fairly good efficiency over a wide range of load conditions. Apart from the designed lowest input voltage, efficiency of proposed converter is found to be above 93% for all load conditions. The loss analysis is done for full load condition and designed low input voltage (45 V). The breakup of various losses are shown in Fig. 17. Due to the high RMS input current, losses of coupled inductor constitute 26.7% of total loss of the converter. To reduce the conduction losses in switches, low voltage rated MOSFET having low on-state resistance is selected. The conduction loss of main and clamp switches are 19.15% and 4.36% of total power loss of the converter. The other losses are calculated based on the difference between the measured efficiency of the converter and measured losses of main components. This include, turn-off switching losses of the MOSFETs, losses due to the ESR of switched capacitors, output capacitors, input filter capacitors, losses in driver circuit and auxiliary power supply for the driver circuitry.

V. Conclusion

An isolated four channel interleaved dc/dc converter with soft switching and high voltage step up gain is proposed as a front end of multiple inverter structures. Proposed converter makes use of isolated coupled inductor and dual voltage multiplier circuit to achieve voltage step up with lower voltage stress on devices. Active clamp circuit is used to clamp the voltage spike on MOSFETs and also to provide soft turn on for MOSFET switches. Interleaved operation enhanced the power output and reduces the input current ripple. Modularity of proposed converter is an added advantage. Four isolated output port of proposed converter can be connected in series, parallel or series-parallel combination to obtain required dc-link voltages of multiple commonly used inverter structures such as three-phase two-level inverter, three-level NPC, and five level NPC inverter structures. Proposed converter can overcome the capacitor voltage balancing issues of five-level and three-level NPC inverters without any additional voltage balancing circuits. Feasibility of same is experimentally verified and results are shown. By using MOSFETs of low on state resistance, conduction losses are reduced in proposed converter. A 2 kW prototype of proposed converter is build and results are verified. Maximum efficiency of proposed converter is found to be 95.83%.

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