Single-Phase Six-Switch Dual-Output Inverter Using Dual-Buck Structure

Bang Le-Huy Nguyen, Honnyong Cha, *Member, IEEE*, and Heung-Geun Kim, *Senior Member, IEEE*

***Abstract*—In this paper, a novel six-switch dual-output inverter is proposed. The three-switch leg in the proposed inverter is implemented with the dual-buck structure. Hence, it retains all the benefits of the conventional dual-buck inverter such as improved reliability owing to the absence of short-circuit problems and higher efficiency with the use of power metal–oxide–semiconductor field-effect transistor (MOSFET) without reverse recovery issues on its body diode. In addition, the passive components can be reduced with the high switching frequency operation. A 3.5-kW, 400-V dc input MOSFET-based hardware prototype was built and tested to verify the performance of the proposed inverter and a maximum efficiency of 97% was achieved.**

***Index Terms*—Dual-buck inverter, dual-output, nine-switch converter, reduced-switch-count converters, single-phase inverter, switching cell, three-switch-leg.**

I. Introduction

THE use of active switches, such as the insulated-gate bipolar transistor (IGBT) and metal–oxide–semiconductor field-effect transistor (MOSFET), requires a gate-driver circuit and gate-driver power supply, which undesirably increase the cost, weight, volume, and failure probability of the entire system. Therefore, the reduced-switch-count power converter topologies have been receiving increasing attention.

In dual-output inverters or ac–dc–ac power converter systems, the switch count reduction can be achieved using three well-known methods: split-capacitor leg [1], sharing phase leg [2], and three-switch leg [3]. Among them, the three-switch leg has been intensively employed through various applications, such as dual-output inverter [3]–[5], ac/ac nine-switch converter [6], dual-output Z-source inverter [7], dual-output indirect matrix converter [8], back-to-back converter for doubly fed induction generator [9], drives for six-phase motor [10], power conditioner [11], online uninterrupted power supply (UPS) [12], energy systems for distributed generation [13], multi-input converters [14], and solid-state variable capacitor [15].

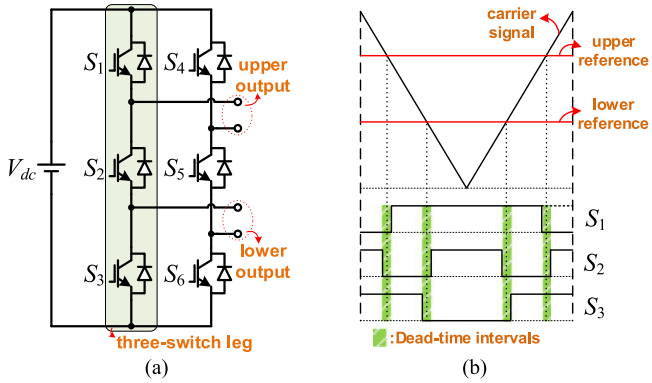

Fig. 1. Conventional dual-output six-switch inverter [3]. (a) Circuit topology. (b) Modulation scheme for three-switch leg.

Fig. 1(a) shows the dual-output six-switch inverter topology introduced in [3]. This topology can independently supply two single-phase ac loads. The reduction of switch count is achieved by sharing the middle switches (S_2, S_5) between the upper and lower outputs. Fig. 1(b) shows the modulation of each three-switch phase leg. The upper reference should be always greater than the lower reference to avoid short-circuit or open terminal. Under this constraint, the operation of three-switch-leg-based converters is divided into two modes: common frequency (CF) and different frequency (DF) modes. In the CF mode, the two outputs have the same fundamental frequencies and the maximum achievable magnitude of their reference signals is one provided that they are in-phase. However, in the DF mode, the fundamental frequencies of the two outputs are different and their maximum achievable magnitudes are lowered to half or the total magnitudes should be lower than one. Hence, the three-switch-leg-based converter topologies are more suitable for applications in which the two outputs are mainly controlled at CF mode such as online-UPS or the same-speed drives system.

The three-switch leg has already been confirmed as a practical alternative to a four-switch full-bridge module to reduce 25% of the active semiconductor devices used in the system. However, like the two-switch leg, it still suffers from short-circuit risk when all switches in the phase leg being turned ON simultaneously. Generally, a finite pulse-width modulation (PWM) dead time is used at the cost of a distorted output waveform and reduced achievable voltage gain [16], [17]. The dual-buck leg with additional current limiting inductors can alleviate these

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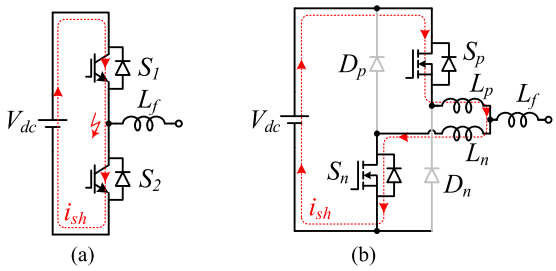

Fig. 2. Comparison of shoot-through paths in (a) conventional and (b) dual-buck phase legs.

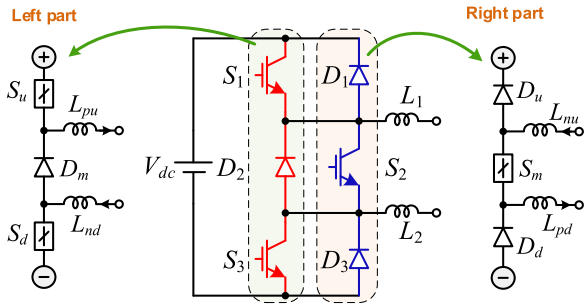

Fig. 3. Decomposition of the conventional three-switch leg.

concerns owing to no short-circuit possibility. Moreover, the use of power MOSFETs and externally selected diodes assist this structure gain higher efficiency, especially at high-switching frequency operation in comparison with conventional IGBT-based topology.

The dual-buck structure was first introduced as a high-performance current regulator in 1990 [18] to the best of our knowledge. This structure is then employed for a range of power converters, such as half-bridge [19], full-bridge [20], three-phase inverter [21], cascaded H-bridge inverter [22], buck, boost, and buck-boost ac–ac choppers without commutation problems [23]–[26]. All of them are extremely reliable and highly efficient.

Follow this trend, a novel three-switch leg using dual-buck structure is proposed in this paper. A discussion on the characteristics of the dual-buck structure and the derivation of the proposed leg are presented in Section II. The operation principle of the proposed leg is analyzed in Section III. In Section IV, the feasibility of the proposed leg is demonstrated by implementing a single-phase six-switch dual-output inverter. The operation modes and carrier-based PWM (CB-PWM) of the proposed inverter is described. In Section V, the experimental results are provided and an efficiency comparison between the proposed and conventional inverters is conducted.

II. Proposed Dual-Buck-Based Three-Switch Leg

A. Dual-Buck Structure

Fig. 2 compares the shoot-through path in the conventional and dual-buck phase legs. As evident in Fig. 2(b), the shoot-through current $i_{\rm sh}$ is restrained by the two current limiting inductors L_p and L_n. During the overlap-time period, $i_{\rm sh}$ increases with a slope of $(V_{\rm dc}/2L_{\rm c})$, where $L_p = L_n = L_c$. Therefore, the dual-buck leg can stand for a certain overlap-time period. This provides sufficient time for the protection circuit to shut down the system to protect the devices when the overlap time lasts longer at fault condition. The system reliability is greatly enhanced.

Additionally, it is well known that the main advantages of power MOSFETs are their fast switching speed and resistive conduction voltage drop, which yield lower switching and conduction losses than IGBTs at a certain current level. However, the large reverse recovery current and the related losses on body diodes often hinder the use of power MOSFETs especially in high-voltage (over 250 V) and hard-switching converters [27].

The dual-buck leg, owing to its unique structure, relieves the reverse recovery issues to a significant extent because the body diodes of MOSFETS do not have a chance to conduct. Instead, the two externally selected fast recovery diodes (D_p and D_n) are used for freewheeling. Sequentially, power MOSFETs can be used and the switching frequency can be increased without severely compromising the converter efficiency. Hence, it leads to lesser filter requirement and avoids acoustic noise. Although two more current limiting inductors are required, the efficiency of the dual-buck leg can be higher than that of the IGBT-based conventional leg [21].

B. Proposed Dual-Buck Three-Switch Leg

The conventional three-switch leg can be decomposed into the left and right parts, as shown in Fig. 3. In the left part, two switches are connected in series with a diode in the middle, whereas in the right part, two diodes are connected in series with a switch in the middle. Inductors are added to each part to limit the current during the overlap-time period.

By recombining the left and right parts while retaining the presence of all the limiting inductors, a novel three-switch leg is formed, as shown in Fig. 4(a). There are no shoot-through worries and the high converter reliability is achieved. Additionally, the external diodes, which can be selected with optimized recovery characteristics and lower voltage drop, reduce the switching and conduction losses significantly.

Although the proposed leg can stand for the overlap-time period, this causes a circulating current $i_{\rm cr}$ flowing through the circuit loops. Fig. 4(b) and (c) shows the shoot through and freewheeling paths when all switches simultaneously being turned ON (overlap-time period) and turned OFF (deadtime period), respectively. The increase of $i_{\rm cr}$ during the overlap-time period $\Delta t_{\rm op}$ is calculated as

$$\frac{\Delta i_{\rm cr}}{\Delta t_{\rm op}} = \frac{V_{\rm dc} - 3i_{\rm cr}r_{\rm ds,on}}{4L_c}. \tag{1}$$

where $V_{\rm dc}$ is the dc-link voltage, $L_{pu} = L_{pd} = L_{nu} = L_{nd} = L_c$ is the inductance of the limiting inductors, and $r_{\rm ds,on}$ is the on-state resistance of power MOSFETs. Conversely, this current reduces during the deadtime period $\Delta t_{\rm dp}$ with the slope of $(V_{\rm dc} - 3V_f)/4L_c$, where V_f is the forward voltage drop on external diodes.

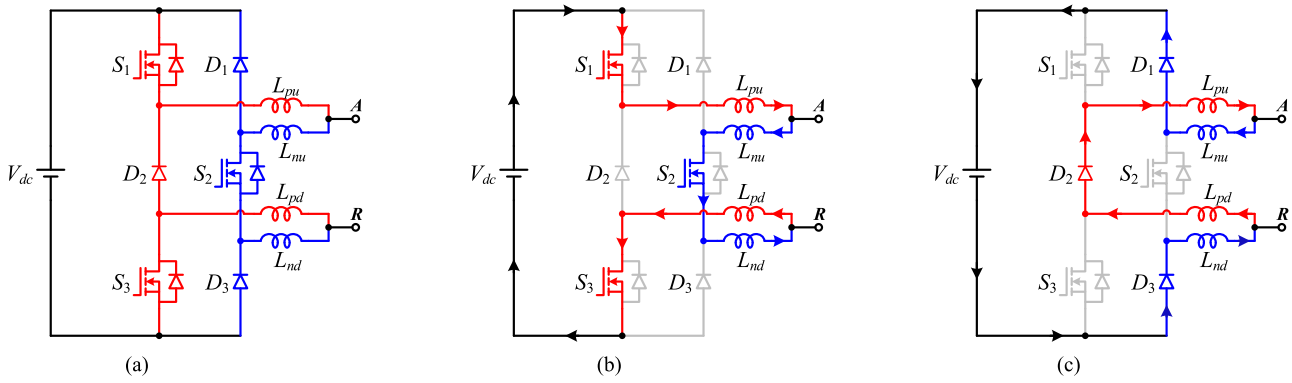

Fig. 4. Proposed three-switch leg. (a) Circuit. (b) Shoot-through path. (c) Freewheeling path.

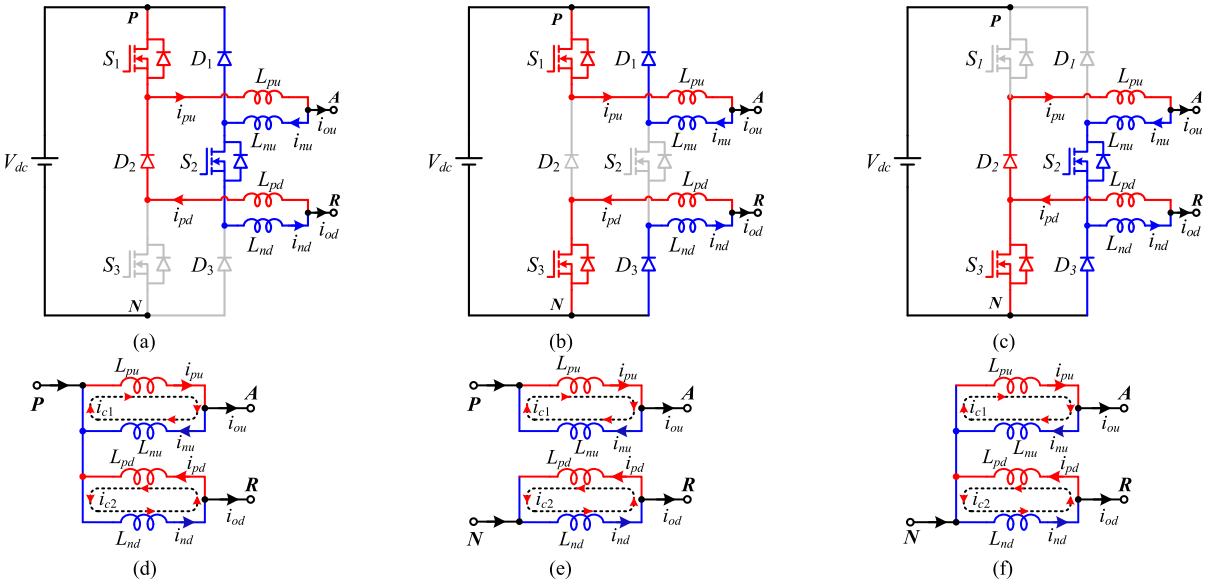

Fig. 5. Switching states and simplified equivalent circuits of the proposed leg. (a), (d) P [110]. (b), (e) Z [101]. (c), (f) N [011].

Hence, the $i_{\rm cr}$ can be approximated as

$$i_{\rm cr} = \frac{V_{\rm dc}}{4L_c}\left(\sum t_{\rm op} - \sum t_{\rm dp}\right) \geq 0. \tag{2}$$

In (2), the voltage drops on semiconductor devices (V_f and $i_{\rm cr} r_{\rm ds,on}$) are neglected; $\Sigma t_{\rm op}$ and $\Sigma t_{\rm dp}$ are the accumulated time of deadtime and overlap-time intervals, respectively. When $\Sigma t_{\rm dp} \geq \Sigma t_{\rm op}$, the i_{cr} is retained at zero. Thus, the $i_{\rm cr}$ can be minimized by adding more deadtime than overlap time. Nonetheless, more deadtime leads to more distortion in outputs and reduction of dc-source utilization. In this paper, a deadtime of approximately 0.2 μs is inserted. Therefore, the $i_{\rm cr}$ can be neglected.

III. Operation Principle of the Proposed Leg

A. Switching State

Similar to the conventional three-switch leg, the proposed leg also has three switching states for switches [S_1, S_2, S_3] listed as P [110], Z [101], and N [011]. Fig. 5 shows the schematics and the simplified equivalent circuits of the three switching states with the voltage drops across semiconductor devices are neglected. Where i_{c1} and i_{c2} represent the freewheeling of limiting inductor currents through the circuit loops if it occurs. The relationship between the switching states and voltages across the limiting inductors can be determined as described in Table I. As can be seen in Fig. 5, in each switching state, the output terminals A and R are connected to the source terminals P and N through current limiting inductors (L_{pu}, L_{nu}, L_{pd}, and L_{nd}).

TABLE I
Relationship Between Switching States and Inductor Voltages

States	Devices						Inductor Voltages	
	S_1	D_1	S_2	D_2	S_3	D_3	v_{Lpu}, v_{Lnu}	v_{Lpd}, v_{Lnd}
P [110]	ON	FB	ON	FB	OFF	RB	v_{PA}	v_{PR}
Z [101]	ON	FB	OFF	RB	ON	FB		v_{NR}
N [011]	OFF	RB	ON	FB	ON	FB	v_{NA}	

* FB: forward-biased, RB: reverse-biased

B. Evaluation of Currents in Devices

By involving limiting inductors, the currents flowing inside the proposed dual-buck three-switch leg are different from those

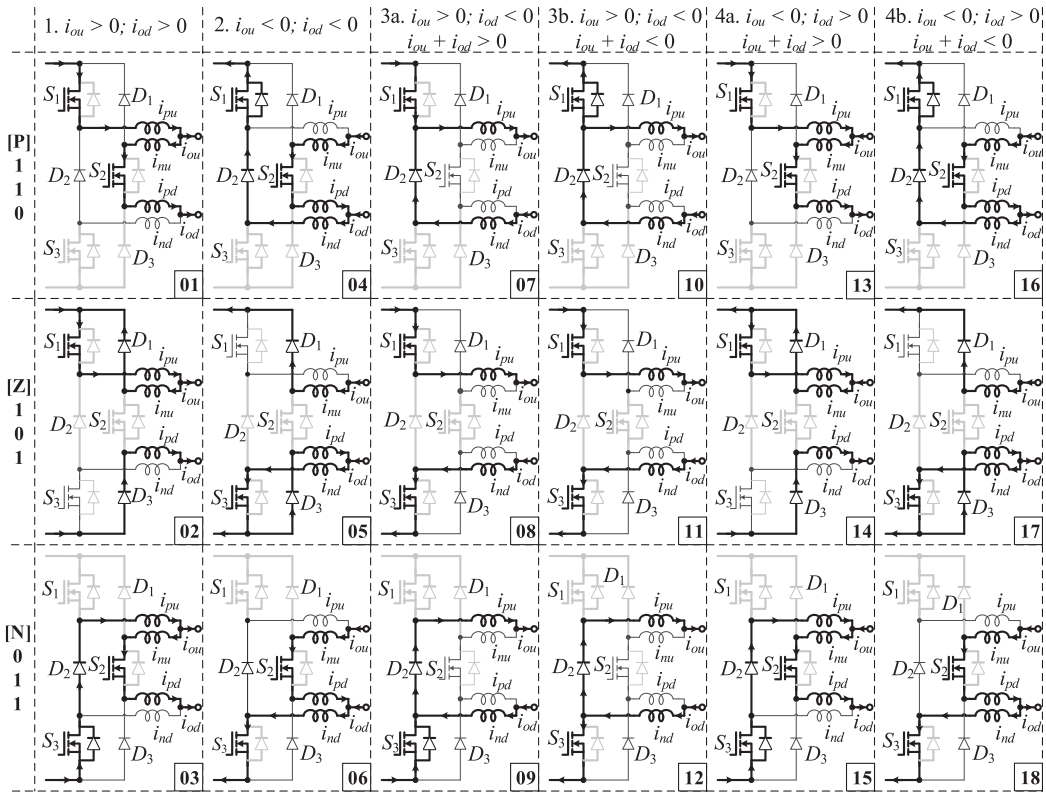

Fig. 6. Current paths of the proposed leg for each switching state.

TABLE II
CURRENTS IN LIMITING INDUCTORS

Cases	Output current polarities		Currents in limiting inductors			
			L_{pu}	L_{nu}	L_{pd}	L_{nd}
1	$i_{ou} > 0$, $i_{od} > 0$		i_{ou}+i_{od}	i_{od}	i_{od}	0
2	$i_{ou} < 0$, $i_{od} < 0$		0	-i_{ou}	-i_{ou}	-i_{ou}- i_{od}
3	$i_{ou} > 0$, $i_{od} < 0$		i_{ou}	0	0	-i_{od}
4(a)	$i_{ou} < 0$, $i_{od} > 0$	(i_{ou}+ i_{od}) > 0	i_{ou}+ i_{od}	i_{od}	i_{od}	0
4(b)		(i_{ou}+ i_{od}) < 0	0	-i_{ou}	-i_{ou}	-i_{ou}- i_{od}

of conventional one since inductor current cannot change immediately. Fig. 6 shows the current paths for each switching state. In Fig. 6, for the sake of simplicity, the currents in limiting inductors are assumed to be a fixed value during a switching period.

For example, let us consider the case when the two output currents are positive. Begin with the switching state P [110], the switch S_1 and the inductor L_{pu} conduct the total output currents $(i_{ou} + i_{od})$, whereas the switch S_2 and inductors L_{nu}, L_{pd} conduct the lower output current (i_{od}), as shown in mode 01 of Fig. 6. In this case, the inductor L_{nd} does not conduct any currents. Thus, the i_{c1} and i_{c2} are zero.

Changing to the switching state Z [101], the current $(i_{nu} = i_{od})$ in L_{nu} freewheels through the loop of $L_{nu} - D_1 - S_1 - L_{pu}$. Thus, S_1 and L_{pu} still conduct the total output currents $(i_{ou} + i_{od})$, the i_{c1} is i_{nu}. While the lower output current (i_{od}) freewheels through D_3 and L_{pd} as shown in mode 02, the i_{c2} is zero.

Changing to switching state N [011], the current $(i_{pu} = i_{ou} + i_{od})$ in L_{pu} freewheels through S_3 and D_2, whereas S_2 and inductors L_{pd} and L_{nu} conduct the lower output current, as shown in mode 03. The i_{c1} and i_{c2} are zero.

Other modes in Fig. 6 clarify how output currents flowing inside the proposed leg for the remained cases when output currents are both negative or have different polarities. Totally, there are 18 modes of six cases for three switching sates. As can be seen in Fig. 6, the i_{c1} only appears in modes 02 and 14, the i_{c2} only appears in modes 05 and 17.

The currents in semiconductor devices and limiting inductors are listed in Tables II and III, respectively.

C. Reverse Recovery Issues

In conventional dual-buck two-switch leg in Fig. 2(b), the body diodes of MOSFETs do not have a chance to conduct owing to the unidirectional currents in limiting inductors [21]. Obviously, there is no reverse recovery problems. However, in the proposed dual-buck three-switch leg, the body diode of S_1 may conducts in modes 04, 10, and 16 for the switching state P [110]; the body diode of S_3 may conducts in modes 03, 09, and 15 for the switching state N [011], as can be seen Fig. 6. In these cases, when S_1 or S_3 is forced to be turned OFF, the reverse recovery process occurs.

To assess the reverse recovery problem, the transitions between these modes to other modes are considered. First, when the switching state changes from P [110] or N [011] to Z [101], the switches S_1 and S_3, respectively, are maintained being turned ON. Therefore, the reverse recovery does not occur in this case. Second, when the switching state changes between P [110] and N [011], for example, from mode 03 to mode 01 in

TABLE III
CURRENTS IN SEMICONDUCTOR DEVICES

Output current polarities		Currents in semiconductor devices												
		P [110]				Z [101]				N [011]				
		S_1	D_1	S_2	D_2	S_1	D_1	S_3	D_3	S_2	D_2	S_3	D_3	
$i_{ou} > 0, i_{od} > 0$		$i_{ou}+i_{od}$	0	i_{od}	0	$i_{ou}+i_{od}$	i_{od}	0	i_{od}	i_{od}	$i_{ou}+i_{od}$	$-i_{ou}-i_{od}$*	0	
$i_{ou} < 0, i_{od} < 0$		$i_{ou}+i_{od}$*	0	$-i_{ou}$	$-i_{ou}-i_{od}$	0	$-i_{ou}$	$-i_{ou}-i_{od}$	$-i_{ou}$	$-i_{ou}$	0	$-i_{ou}-i_{od}$	0	
$i_{ou} > 0$,	$(i_{ou}+i_{od}) > 0$	$i_{ou}+i_{od}$	0	0	$-i_{od}$	i_{ou}	0	$-i_{od}$	0	0	i_{ou}	$-i_{ou}-i_{od}$*	0	
$i_{od} < 0$	$(i_{ou}+i_{od}) < 0$	$i_{ou}+i_{od}$*	0	0	$-i_{od}$	i_{ou}	0	$-i_{od}$	0	0	i_{ou}	$-i_{ou}-i_{od}$	0	
$i_{ou} < 0$,	$(i_{ou}+i_{od}) > 0$	$i_{ou}+i_{od}$	0	i_{od}	0	$i_{ou}+i_{od}$	i_{od}	0	i_{od}	i_{od}	$i_{ou}+i_{od}$	$-i_{ou}-i_{od}$*	0	
$i_{od} > 0$	$(i_{ou}+i_{od}) < 0$	$i_{ou}+i_{od}$*	0	$-i_{ou}$	$-i_{ou}-i_{od}$	0	$-i_{ou}$	$-i_{ou}-i_{od}$	$-i_{ou}$	$-i_{ou}$	0	$-i_{ou}-i_{od}$	0	

* The current may flow through the body diodes of MOSFETs

Fig. 6, the S_3 is first turned OFF. Then, during 0.2 μs deadtime, its body diode conducts the current. When the S_1 is turned ON, the body diode of S_3 is forced to turned OFF and thus requires a reverse current to recombine the charge stored during its conduction time. Fortunately, during this transition, the diode D_2 is being forward biased. Hence, it prevents occurring of the shoot through. The reverse current should flow through the limiting inductors.

In comparison with the conventional three-switch leg configuration in Fig. 1, the reverse current in the diode recovery process flows through the turned ON switches in a low-impedance path. Therefore, this results in overshoot, especially when the dc-voltage is high. Since the proposed leg does not possess any low-impedance paths, there is no overshoot concerns.

D. Limiting Inductor Design

As mentioned in [21], to reduce the total inductance or in the case of motor drives where the filter inductor is not necessary, the limiting inductors should be designed only for the protection against abnormal operating conditions such that the protection circuit has sufficient time to shut down the system before the shoot-through current reaches the threshold value.

There are four limiting inductors in the shoot-through path; hence, the inductance value of each inductor can be reduced by half while retaining the same slope of the shoot-through current compared with a dual-buck two-switch phase leg.

IV. SINGLE-PHASE SIX-SWITCH DUAL-OUTPUT INVERTER

A. Switching Modes

Fig. 7(a) shows the configuration of a single-phase six-switch dual-output inverter, which consists of two proposed legs. The three-phase inverter can also be obtained by using three proposed legs, as shown in Fig. 7(b). According to the three switch states (P, Z, N) of each phase leg, the proposed inverter has nine switching modes (PP, ZZ, NN, PN, PZ, ZP, ZN, NP, and NZ). The upper and lower circuits of the proposed inverter can be considered independently as the two equivalent circuits shown in Fig. 8. The switching voltages (v_u, v_d) in each equivalent circuit are determined based on the switching modes depicted in Table IV.

For simplicity, the operation of the proposed leg can be considered the same as that of the conventional dual-output inverter with an additional limiting inductor (L_c). The output current

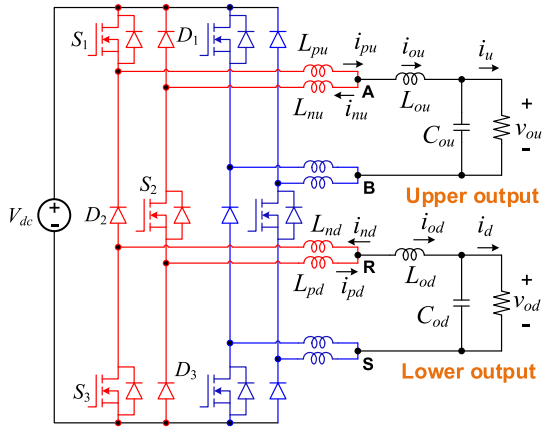

Fig. 7. Proposed dual-output inverters. (a) Single phase. (b) Three phase.

ripples can be derived from the equivalent circuits in Fig. 8 as follows:

$$\Delta i_{oi} = \frac{(V_{\rm dc} - v_{oi})\, D_i T_s}{L_c + L_{oi}}; i = u \text{ or } d. \tag{3}$$

The current ripples (Δi_{ou} and Δi_{od}) of the limiting inductors should be half of the output currents when they are continuous

$$\Delta i_{pi} = \Delta i_{ni} = 0.5 \Delta i_{oi} \tag{4}$$

where i refers to the upper (u) or lower (d) output; D_i is the time ratio of $v_i = V_{\rm dc}$; L_c is the equivalent limiting inductor; L_{oi} and C_{oi} are the filtering inductor and capacitor of the output, respectively; and T_s is the switching period.

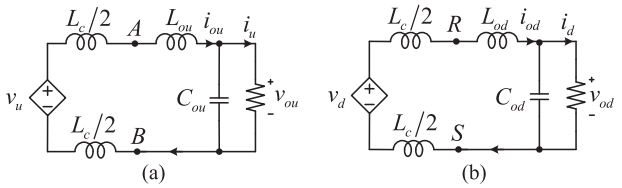

Fig. 8. Equivalent circuits of the proposed single-phase inverter. (a) Upper output. (b) Lower output.

TABLE IV
SWITCHING MODES OF THE PROPOSED INVERTER

Switching voltage	Switching modes								
	PP	ZZ	NN	PN	PZ	ZP	ZN	NP	NZ
v_u	0	0	0	$V_{\rm dc}$	0	0	$V_{\rm dc}$	$-V_{\rm dc}$	$-V_{\rm dc}$
v_d	0	0	0	$V_{\rm dc}$	$V_{\rm dc}$	$-V_{\rm dc}$	0	$-V_{\rm dc}$	0

B. Carrier-Based PWM With Offset Functions

The sinusoidal references which are transferred to the scale of [0; 1] can be expressed as follows:

$$\begin{cases} v_{Au} = 0.5 + 0.5m_u \sin(2\pi f_u t) \\ v_{Bu} = 0.5 + 0.5m_u \sin(2\pi f_u t + \pi) \end{cases} \quad (5)$$

$$\begin{cases} v_{Rd} = 0.5 + 0.5m_d \sin(2\pi f_d t) \\ v_{Sd} = 0.5 + 0.5m_d \sin(2\pi f_d t + \pi) \end{cases} \quad (6)$$

where v_{Au} and v_{Bu} are the modulating references for upper terminals (A and B), while v_{Rd} and v_{Sd} are the modulating references for lower terminals (R and S) of the first and second legs, respectively. Hence, the references for the upper and lower ac outputs ($v_{AB}^{\rm ref}$ and $v_{RS}^{\rm ref}$) can be determined as

$$\begin{aligned} v_{AB}^{\rm ref} &= v_{Au} - v_{Bu} = m_u \sin(2\pi f_u t) \\ v_{RS}^{\rm ref} &= v_{Rd} - v_{Sd} = m_d \sin(2\pi f_d t). \end{aligned} \quad (7)$$

According to the control constraint of the three-switch leg, the upper reference is always larger or equal to the lower reference ($v_{Au} \geq v_{Rd}$, $v_{Bu} \geq v_{Sd}$). To ensure this condition, a positive offset function ($v_{{\rm off}u}$) is added to the upper references, whereas a negative offset function ($v_{{\rm off}d}$) is added to the lower references. The boundaries of the offset functions are expressed as follows:

$$1 - \max_u \geq v_{{\rm off}u} \geq v_{{\rm off}d} \geq -\min_d \quad (8)$$

where $\max_u = \max(v_{Au}, v_{Bu})$ and $\min_d = \min(v_{Rd}, v_{Sd})$. The value of $v_{{\rm off},\max} = 1 - \max_u$ and $v_{{\rm off},\min} = -\min_d$ represents the maximum and minimum offsets, respectively. The discontinuous PWM methods that reduce the switching loss can be achieved by adding the maximum offset ($v_{{\rm off},\max}$) to the upper references and the minimum offset ($v_{{\rm off},\min}$) to the lower references. The gate drive signal generation scheme of switches S_1–S_6 is shown in Fig. 9.

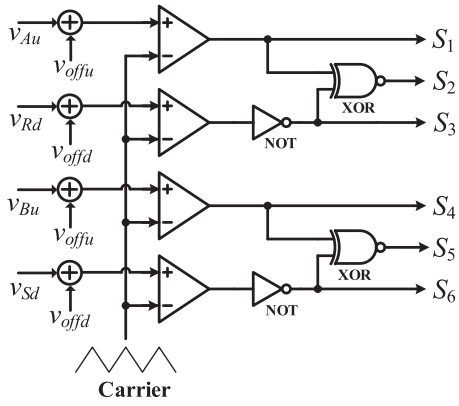

Fig. 9. Gate signal generation scheme with offset functions.

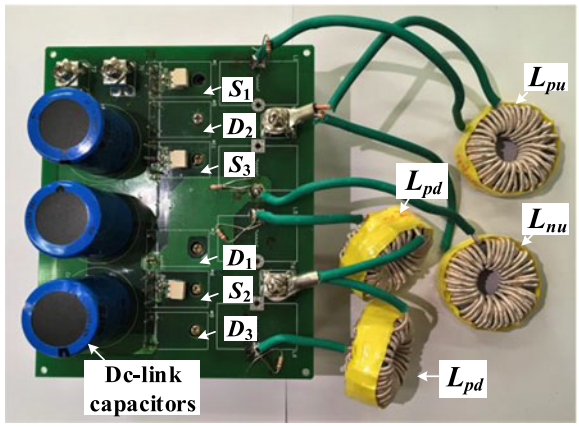

Fig. 10. Prototype photo of the proposed leg.

TABLE V
EXPERIMENTAL PARAMETERS

Input voltage ($V_{\rm dc}$)	400 V
Switching frequency ($f_{\rm sw}$)	30 kHz
MOSFET (S)	47N60CFD
Diode (D)	RHRG3060
Limiting inductors (L_c)	0.2 mH
Filter inductors (L_{oi})	0.74 mH
Filter capacitors (C_{oi})	6 μF

V. EXPERIMENTAL RESULTS

A 3.5-kW prototype of a single-phase six-switch dual-output inverter was built and tested. Fig. 10 shows the prototype photo of the proposed leg. The experimental parameters are shown in Table V. In the CF mode, two outputs are modulated using the additional offsets ± 0.06 with the modulation indices ($m_u = 0.6$, $m_d = 0.8$), respectively, at same fundamental frequencies of 60 Hz, whereas in the DF mode, the modulation indices ($m_u = 0.4$, $m_d = 0.45$) and the additional offsets ± 0.25 are used, the fundamental frequency of upper and lower outputs are 60 Hz and 120 Hz, respectively.

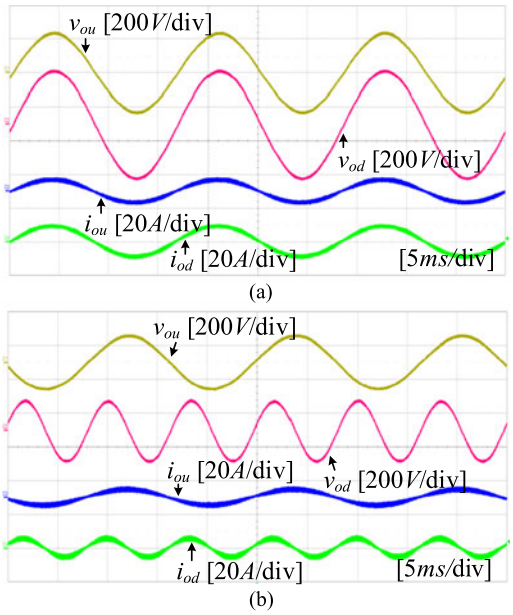

Fig. 11. Output voltages and currents in (a) CF and (b) DF modes.

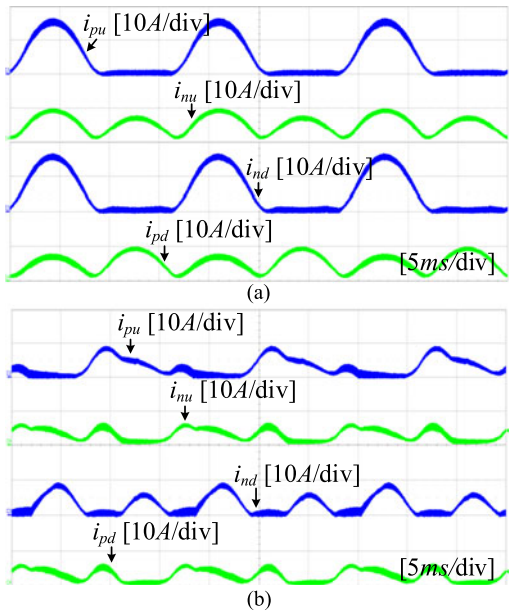

Fig. 12. Limiting inductor currents in (a) DF and (b) CF modes.

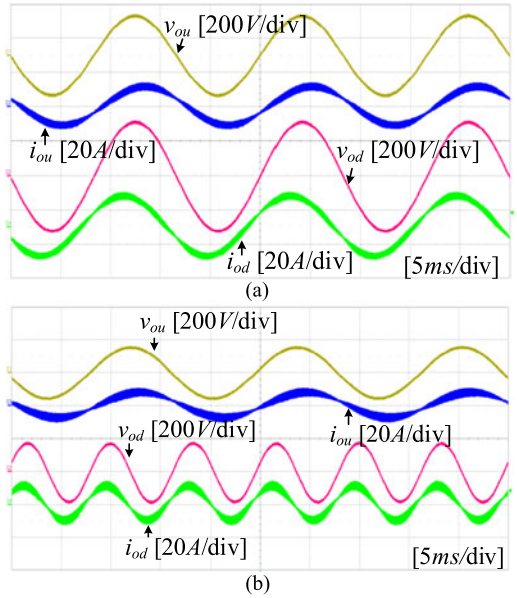

Fig. 13. Output voltages and currents of *RL* and *RC* loads in (a) CF and (b) DF modes.

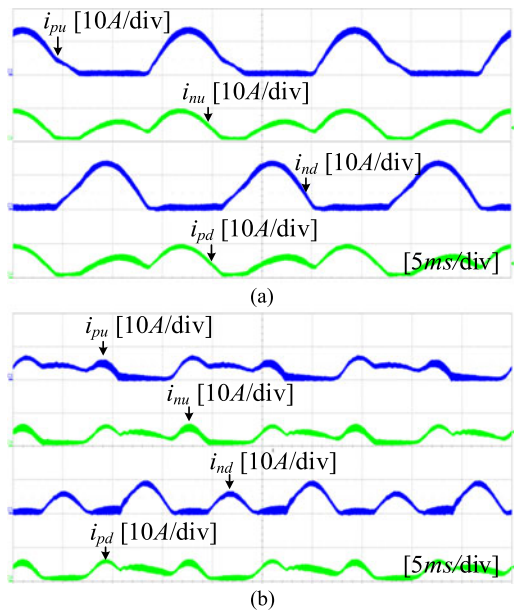

Fig. 14. Limiting inductor currents of *RL* and *RC* loads in (a) CF and (b) DF modes.

A. *Resistive Loads*

First, two outputs are connected to the resistive loads of 35 Ω. Fig. 11 shows the output voltage and current waveforms in CF and DF modes. The currents in the limiting inductors (L_{pu}, L_{nu}, L_{nd}, L_{pd}) in each mode are shown in Fig. 12. As can be seen in the figures, the two outputs can operate independently either at the same or different frequencies; the currents in limiting inductors are the same as analyzed in Table III.

B. *Inductive, Capacitive, and Nonlinear Loads*

Second, experiments are conducted with the inductive load ($R = 35\,\Omega$ and $L = 50$ mH in series) and the capacitive load ($R = 35\,\Omega$ and $C = 200\,\mu$F in series) connected to the upper and lower outputs, respectively. Fig. 13 shows the output voltage and current waveforms obtained at CF and DF modes, respectively. The currents in the limiting inductors of this test are also shown in Fig. 14.

Next, a nonlinear load that consists of a diode bridge rectifier followed by a capacitor of 560 μF and a load resistance of 100 Ω is connected to the lower output, whereas the upper one feeds to the resistive load of 35 Ω. Fig. 15 shows the output voltage and current waveforms obtained at CF and DF modes.

The currents in the limiting inductors are also shown in Fig. 16. As shown, the independency is ensured under either

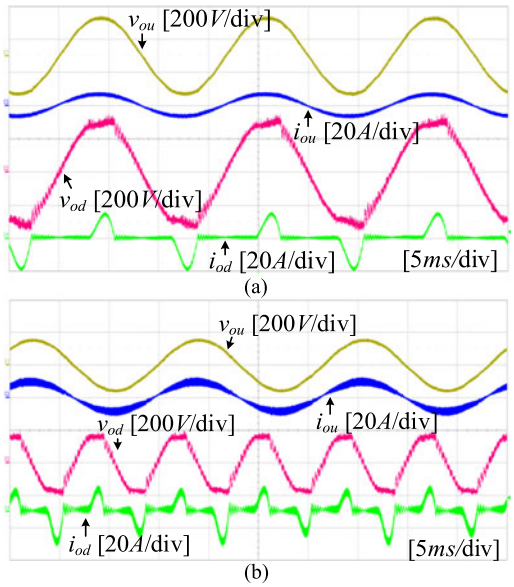

Fig. 15. Output voltages and currents of the resistive and nonlinear loads in (a) CF and (b) DF modes.

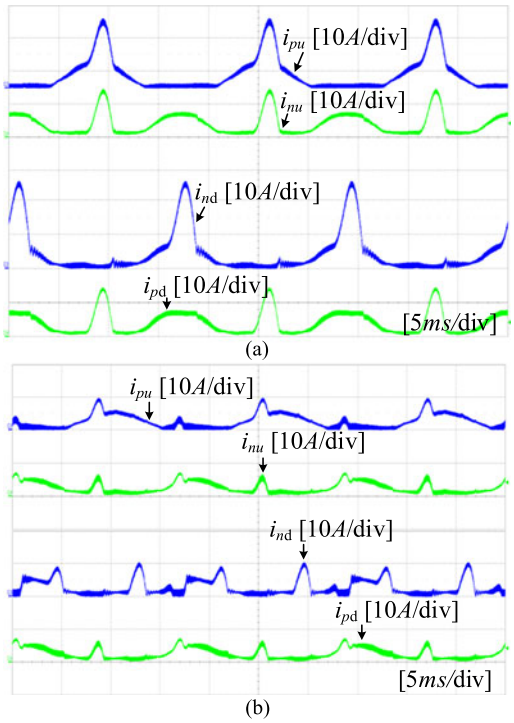

Fig. 16. Limiting inductor currents of the resistive and nonlinear loads in (a) CF and (b) DF modes.

the difference in power factor of two outputs or the nonlinear operation.

C. Step-Load Response

Experiments for the transient response are conducted with the resistive loads. Fig. 17(a) shows the step-load response when only the lower load changed from no load to 35 Ω at CF mode, whereas Fig. 17(b) shows the transient response when both

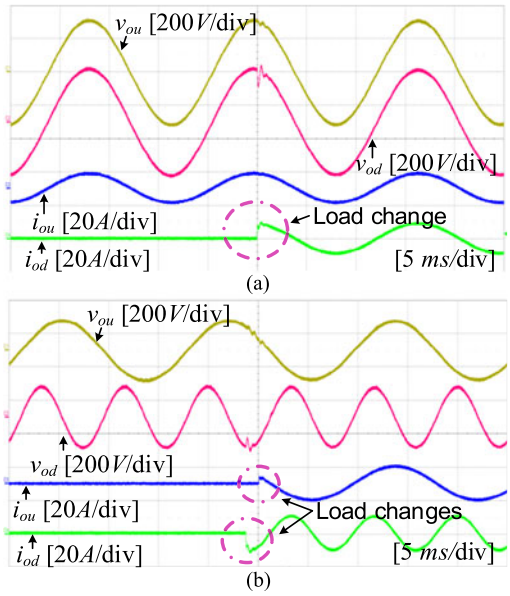

Fig. 17. Step-load responses of output voltages and currents in (a) CF and (b) DF mode.

upper and lower loads changed from no load to 35 Ω at DF mode. Notably, the responses of two outputs are decoupled, i.e., they do not affect each other.

D. Efficiency Comparison

The efficiencies are first compared between DF and CF modes with both continuous and discontinuous, as shown in Fig. 18(a).

Apparently, the discontinuous CB-PWM results in higher efficiency owing to the reduction of switching loss. The DF mode also gain higher efficiency conversion compared with the CF mode owing to only the subtraction of output currents flowing through the components as in cases 3 and 4 listed in Table II. The peak efficiency achieved was 97%.

The efficiency comparison is made between the conventional six-switch inverter [3] and the proposed inverter, as shown in Fig. 18(b). Same as the proposed inverter, the conventional inverter was also built using power MOSFETs. Both inverters are tested under the same parameters as listed in Table V except that the dc-link voltage $V_{\rm dc}$ is reduced to 250 V and a 2 μs deadtime interval is added for safe operation. The switching frequency is 30 kHz. The high-voltage and hard commutation of the conventional MOSFET-based six-switch inverter results in significant reverse-recovery loss, the efficiency of the conventional inverter then peaks at only 90.3%. Moreover, the shoot-through which occurs in reverse recovery process severely reduces the converter reliability [27]. However, under the same operating condition, the efficiency of the proposed inverter can achieve more than 95% with high reliability.

The basic features of the conventional dual-output six-switch inverter (6SWI) [3], proposed dual-buck six-switch inverter (DB-6SWI), two separated conventional full-bridge inverters (2FBI), and two separated dual-buck full-bridge inverters (2DB-FBIs) [20] are summarized in Table VI.

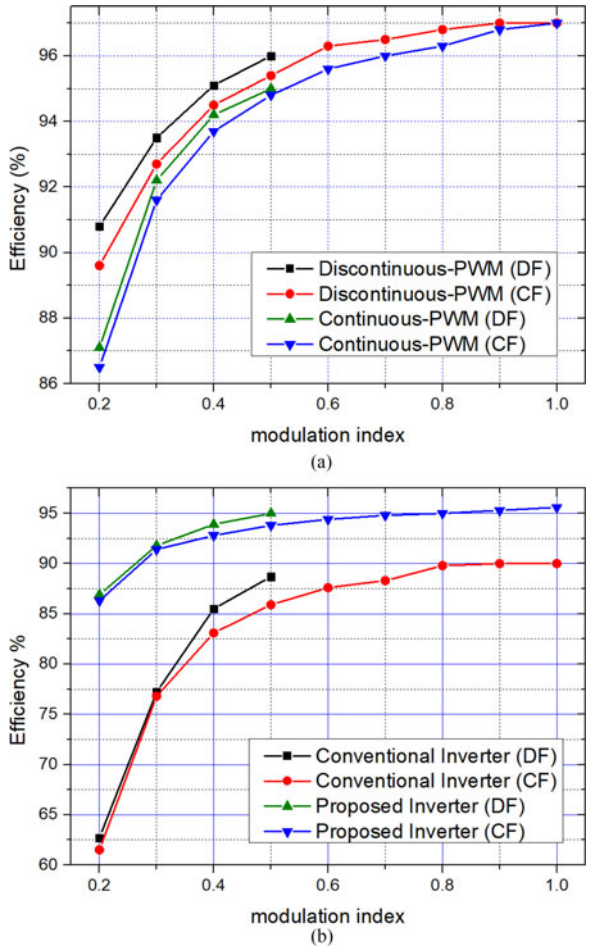

Fig. 18. Efficiency comparison.

TABLE VI
COMPARISON OF SEPARATED FULL-BRIDGE AND SIX-SWITCH INVERTERS

Parameters	Inverters			
	6SWI	DB-6SWI	2FBIs	2DB-FBIs
No. of switches	6	6	8	8
No. of external diodes	–	6	–	8
No. of limiting inductors	–	8	–	8
Maximum modulation index at DF mode	0.5	0.5	1	1
Shoot-through possibility	yes	no	yes	no
Reverse recovery problem on MOSFET's body diode	yes	no	yes	no
Switch for high-voltage hard-commutation	IGBT	MOSFET	IGBT	MOSFET
Switching frequency	low	high	low	high
Efficiency	low	high	low	high

VI. CONCLUSION

In this paper, a novel dual-buck-based three-switch leg is proposed as an alternative to the conventional three-switch leg for the aforementioned power converters. Same as the many recently developed dual-buck converters, system reliability in the proposed converter is greatly enhanced owing to no shoot-through worries in the proposed leg. The single-phase six-switch dual-output inverter is implemented as a typical application. It can supply independently two single-phase motors or other ac loads. Experimental results and efficiency comparison agree with the theoretical analysis.

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