Reconfigurable Multilevel Inverter With Fault-Tolerant Ability

Hossein Khoun Jahan, Farhad Panahandeh, Mehdi Abapour, and Sajjad Tohidi

***Abstract*—The cascaded H-bridge multilevel inverter (CMI) is one of the most popular converters, especially in renewabale energy applications. Beyond offering some significant benefits, this inverter suffers from the drawback of employing great number of components which reduces the reliability of the inverter. Thus, designing a scheme to enhance reliability in this kind of inverter is of crucial importance. In this paper, a fault-tolerant structure for the cascaded H-bridge multilevel inverter is designed. Failure rates of the switches and diodes are calculated. Then, by using the Markov method, reliability and mean time to failure (MTTF) of the mentioned inverter, before and after employing the suggested scheme, are evaluated. In order to prove proper performance of the suggested scheme, a laboratory built prototype is employed. The results show that employing the suggested scheme significantly enhances reliability and MTTF of the inverter.**

***Index Terms*—Fault-tolerant scheme, multilevel inverter, reliability.**

I. Introduction

IT IS commonly acknowledged that semiconductors in power electronic devices possess low reliability. Due to this reality and considering the fact that power electronic based converters are, mostly, based on semiconductors, designing fault-tolerant structures which improve the reliability and the availability of the system would be of high importance. Although higher reliability postulates higher cost, it leads to continuous energy conversion. So far, reliability evaluation of different kinds of converters is considered in the literature [1]–[3]. To the end of enhancing reliability of different converters, various methods are put forth by different research works. In some cases, new structures with higher reliability are presented [4]–[9]. In the others, redundant switch structures, parallel configuration, and standby configuration are analyzed [10]. There are also some research works which deal with the emphatic factors that affect the reliability of components utilized in converters. Such factors are junction temperature, ambient temperature, power range, etc. [5].

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One of the most popular converters which takes part in state-of-the-art technologies is multilevel inverter. The main advantages attributed to multilevel inverters are as [11], [12] follows.

1) Lower voltage and power rating of components.
2) Lower $\frac{dv}{dt}$ of output voltages.
3) Staircase ac voltage of improved quality and minimized total harmonic distortion.
4) No need for bulky and slow filter.
5) Fast dymanic response.
6) Lower electromagnetic interference.
7) Lower common mode voltage.
8) Lower switching frequency and hence, lower switching power loss.

Depite the mentioned advantages, such converters suffer from drawback of requiring an extra number of components. Besides the increased cost, complexity, and volume, the main demerit of using extra components is reducing reliability. Hence, this problem requires a cautious inspection in multilevel inverters [13]–[16].

Flying capacitors, diode-clamped converter, and cascaded H-bridge cells multilevel inverter (CMI) are three main topologies of multilevel inverters. Among such topologies, CMI stands out for its modular and simple structure. This feature makes this topology more popular and in-demand. Hence CMI is of a preveling topic in power elecrtonic based converter. Owing to employing higher number of components, CMI is also considered from reiability point of view. In this regard, some fault-tolerant structures and control strategies have been put forth to enhance the reliability of this multilevel inverter [7], [17]–[19]. In [7], reliability of a seven-level CMI in improved by using a fault-tolerant scheme. The suggested structure owns four relays in each module and when a fault occurs in a module, its dc source is transferred to the other module through the related relays, where it connects to the existing dc sources in series. By changing switching patterns, the inverter keeps functioning without being affected by the fault. The main drawback of the mentioned fault-tolerant scheme is the high voltage stress that is exerted to the remained healthy switches. In [17], a fault-tolerant method is suggested to ehance the reliabilty of CMIs. In the suggested method, the faulty modules are bypassed though some bypassing contuctors. The suggested method is simple and easy to implement. However, the main demerit of this method is that bypassing the faulty module decreases power and voltage capacity of the protected converter. Similar to the suggested method in [17], the suggested fault-tolerant method in [18] improves the relaibility of a CMI through bypassing the faulty module.

In this reference, a redundant module is considered to preserve the voltage and power capacity of the fault-tolerant CMI. Since after a fault the voltages of sources in the healthy modules need boosting, the method presented in this reference is only suitable for static compensator (STATCOM) application.

Since CMIs need some separated dc sources, they are very compatible devices to be employed in photovoltaic (PV) applications [20], [21]. Considering various applications of PV, such as transportation and aerospace systems, enhancing CMI's reliability is of high importance.

In this paper, a fault-tolerant structure for the cascaded multilevel inverters is proposed. The proposed structure employs two relays to remove the failed sections from the converter. When occurring a fault in the considered inverter, the full-bridge cells change to the half-bridge cells through the relays conductors. Thus, the inverter continues to perform its task without being affected by the fault. In order to assess the suggested scheme, a cascaded H-bridge inverter, which comprises three H-bridge cells, is considered and failure rates of its semiconductor switches are analyzed. Furthermore, the reliability and mean time to failure (MTTF) of the considered inverter, with and without the proposed scheme, are compared. Additionally, using computer aid simulated model and a laboratory built prototype the feasibility and viability of the proposed scheme are proven.

This paper is organized as following: In Section II, the proposed fault-tolerant scheme and the way it works will be explained. The fault diagnosis method designed for the proposed fault-tolerant scheme is also available in this section. The feasibility and viability of the proposed scheme are proved through some simulation and experimental results presented in Section III. In Section IV by using the Markov approach, failure rate analysis and reliability evaluation of the conventional and the proposed structure will be discussed. In Section V, numerical results of reliability and MTTF are presented. In Section VI, the proposed scheme is compared with the schemes suggested in [7] and [18]. Finally, the overall work will be concluded in Section VII.

II. Proposed Fault-Tolerant Scheme and Fault Diagnosing Method

A. Conventional CMI

Depending on the desired output voltage features, a CMI inverter could be synthesized with several H-bridge cells. The voltage values of dc sources in each cell could be chosen to be symmetric or asymmetric. In a CMI with symmetric cells, all the cells comprise the same dc source. Therefore, all the components in the cells are the same in physical and electrical characteristics. Although this type of CMI offers an output voltage of fewer level and lower quality than asymmetric CMIs, it has a modular configuration and easy to be designed and constructed. On the contrary, asymmetric CMIs use dc sources with different voltage values in different cells. In the most common asymmetric configurations, the voltage values of the dc sources in different cells could be chosen to be binary (2^m where m is the number of the cell) or trinary (3^m). Between these two, the configuration with trinary voltage values offers output voltage of higher levels and quality. On the contrary, it suffers from higher voltage stress on the components. Among the mentioned three configurations, the binary configuration could be counted as a tradeoff configuration. A typical three-cell CMI is shown in Fig. 1.

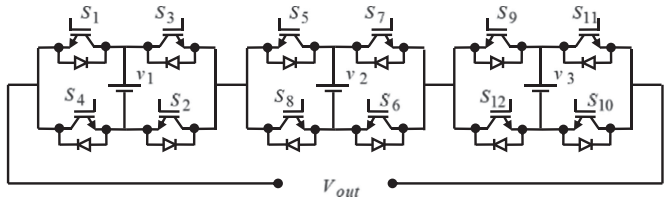


Fig. 1. Typical three-cell CMI.

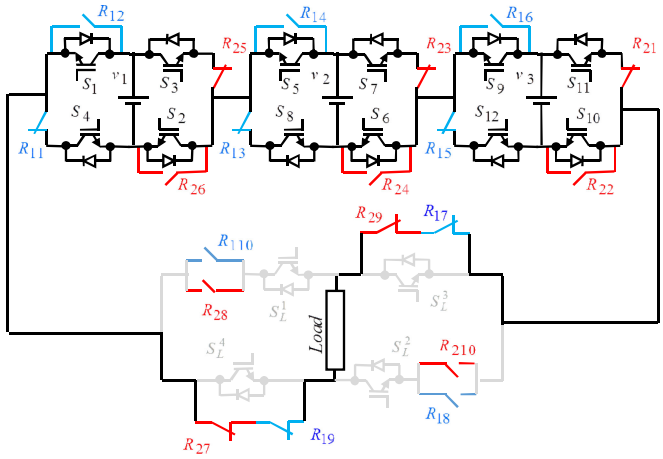


Fig. 2. Proposed fault-tolerant CMI.

B. Proposed Fault-Tolerant Scheme and Fault Diagnosing Method

The basic principal of the proposed fault-tolerant scheme is a reconfiguration of CMI from the cascaded full-bridge cells to the cascaded half-bridge cells when the first fault occurs and also a reconfiguration of it from the cascaded half-bridge cells to a series-connected dc-sources when the second fault occurs. The mentioned scheme is realized through employing two relays along with a reserved load-side H-bridge cell. The proposed scheme could be employed in a CMI of several H-bridge cell. The CMI could either be synthesized with symmetric H-bridge cells or asymmetric cells with binary dc sources. However, for the sake of simplicity, a CMI of three cells which is equipped with the proposed fault-tolerant scheme is analyzed. It is worth mentioning that the utilized relays must includes one normally open and one normally close conductor for each cell and also they must include two normal-open and two normal-close conductors for the load-side H-bridge cell. A three-cell CMI equipped with the proposed scheme is shown in Fig. 2. In this figure, the conductors related to right-side relay (R_1) are colored in red and the conductors related to the left-side relay (R_2) are colored in blue.

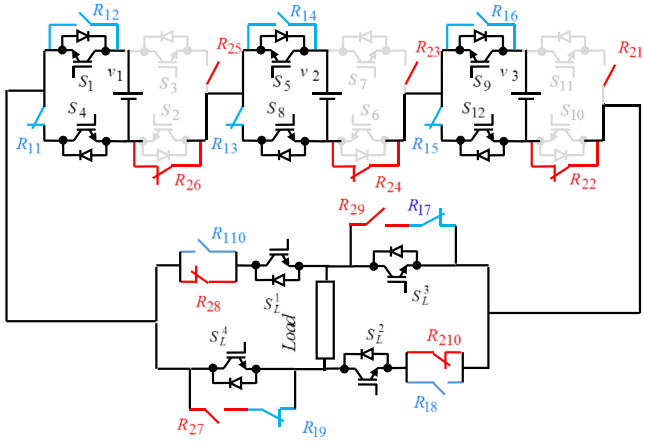


Fig. 3. Configuration of the proposed scheme after a fault in the components on the right side of the cells.

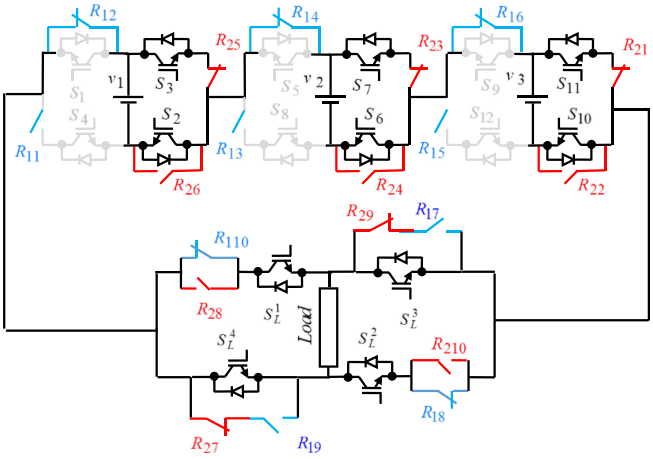


Fig. 4. Configuration of the proposed scheme after a fault in the components on the left side of the cells.

Fault could happen in either the right-side switches or the left-side switches of an H-bridge cell. When the fault is diagnosed to happen in one of the right-side switches of any of the H-bridge cells, the right-side relay will start functioning. Thus, when this relay acts, the related normal-open conductors will be closed and the normal-close conductors will be opened. As a result, the faulted component will be removed from the inverter and the load-side bridge will join to the circuit. The resultant configuration is shown in Fig. 3.

The same process take place when a fault occurs in the left-side switches. The only difference is that instead of the right-side relay, the left-side relay shoulders the responsibility of removing the failed components and joining the load-side bridge to the configuration. The configuration after a fault occurring in the left-side switches is depicted in Fig. 4.

When the second fault happens, since one of the relays is in the functioning state, the remaining relay starts functioning. When the two relays are in the functioning state, all the existing dc sources connect to each other to form a set of series-connected dc sources. The obtained configuration is a simple three-level

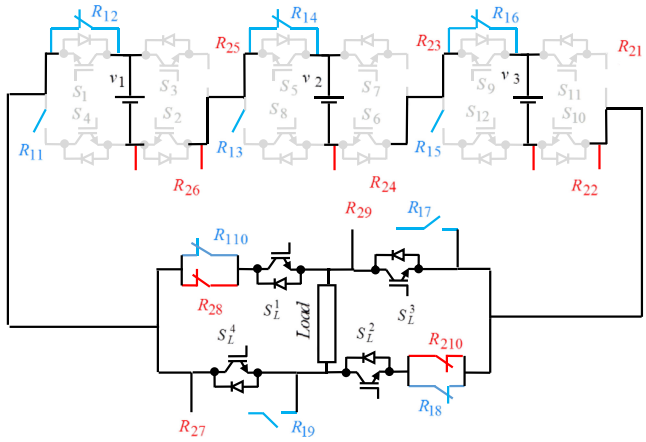


Fig. 5. Configuration of the proposed scheme after experiencing the second fault.

TABLE I
SWITCHING PATTERN OF SYMMETRIC CMI

Level	Voltage (p.u)	Healthy mode	Fault in right side	Fault in left side
		$S_1,S_4,S_5,S_8,S_9,S_{12}$, $S_3,S_2,S_7,S_6,S_{11},S_{10}$,	$S_1,S_4,S_5,S_8,S_9,S_{12}$, $S^1{}_L,S^2{}_L,S^3{}_L,S^4{}_L$	$S_3,S_2,S_7,S_6,S_{11},S_{10}$, $S^1{}_L,S^2{}_L,S^3{}_L,S^4{}_L$
1	0	[101010101010]	[0101011100]	[1010101100]
2	1	[101010011010]	[1001011100]	[0110101100]
3	2	[101010010110]	[1010011100]	[0101101100]
4	3	[101010010101]	[1010101100]	[0101011100]
5	-1	[011010101010]	[1001010011]	[0110100011]
6	-2	[010110101010]	[1010010011]	[0101100011]
7	-3	[010101101010]	[1010010011]	[0101010011]

inverter, as shown in Fig. 5. It is to be mentioned that when the first fault happens and the configuration of the system changes to Figs. 3 or 4, the shape of output voltage remains unchanged. But, when the second fault occurs and the configuration of Fig. 5 is realized, the number of levels of output voltage reduces to three. However, a pulse width modulation (PWM) switching method guarantees the fundamental value of the output voltage.

Switching patterns of the studied CMI with symmetric cells in the healthy mode and under two fault conditions are tabulated in Table I. Similarly, the switching patterns of the asymmetric CMI under normal and fault conditions are presented in Table II. Furthermore, switching pattern of the CMI with symmetric and asymmetric cells when the second fault occurs is shown in Table III

C. Fault Diagnosing Method

An elaborate fault-tolerant structure always calls for a precise fault diagnosing method [22], [23]. The simpler the fault diagnosing methods, the more reliable the whole fault-tolerant structure. The fault diagnosing method, designed for the proposed structure, is solely based on watching out the output voltage situations and checking its levels to be according to the related switching patterns. When a fault happens, it will affect the output voltage and will bring about a mismatch to appear between the

TABLE II
SWITCHING PATTERN OF ASYMMETRIC CMI

Level	Voltage (p.u)	Healthy mode	Fault in right side	Fault in left side
		S_1,S_4,S_5,S_8,S_9,S_{12}, S_3,S_2,S_7,S_6,S_{11},S_{10},	S_1,S_4,S_5,S_8,S_9,S_{12}, $S^1{}_L$,$S^2{}_L$,$S^3{}_L$,$S^4{}_L$	S_3,S_2,S_7,S_6,S_{11},S_{10}, $S^1{}_L$,$S^2{}_L$,$S^3{}_L$,$S^4{}_L$
1	0	[101010101010]	[0101011100]	[1010101100]
2	1	[101010011010]	[1001011100]	[0110101100]
3	2	[101010100110]	[0110011100]	[1001101100]
4	3	[101010010110]	[1010011100]	[0101101100]
5	4	[101010101001]	[0101101100]	[1010011100]
6	5	[101010011001]	[1001101100]	[0110011100]
7	6	[101010100101]	[0110101100]	[1001011100]
8	7	[101010010101]	[1010101100]	[0101011100]
9	-1	[011010101010]	[1001010011]	[0110100011]
10	-2	[100110101010]	[0110010011]	[1001100011]
11	-3	[010110101010]	[1010010011]	[0101100011]
12	-4	[101001101010]	[0101100011]	[1010010011]
13	-5	[011001101010]	[1001100011]	[0110010011]
14	-6	[100101101010]	[0110100011]	[1001010011]
15	-7	[010101101010]	[1010100011]	[0101010011]

TABLE III
SWITCHING PATTERN OF SYMMETRIC AND ASYMMETRIC CMI AFTER SECOND FAULT

	Voltage (p.u.)		
Level	Symmetric	Asymmetric	$S_L^1, S_L^2, S_L^3, S_L^4$
1	0	0	[1010]
2	3	7	[1100]
3	–3	–7	[0011]

existing output voltage level and the related switching pattern. Thus, the fault will be diagnosed. According to Tables I and II, when the voltage level changes, only two state changes occur in two switches of a certain side. Thereupon, when a fault occurs, it is highly probable that the switches which their states have been changed at the last moment to experience the fault. Therefore, after realizing the mismatch between the existing voltage level and the executed switching pattern, which leads to the fault to be diagnosed, the second stage is to find out the position of the fault. After diagnosing the fault the operation command is sent to the relay that is related to the side of two switches which their states are changed at the last moment. However, there is also probability of fault happening on the other side which includes the switches that are in stand still positions in the last switching action. Therefore after turning ON the relay related to the side including switches that take part in the last switching action, the new situation must be checked. In the case that the available output voltage level is according to its related switching pattern in the next mode, the system keeps working in this new situation. if a mismatch exists between the mentioned factors, the system sends operation command to the second relay and turn the previous relay OFF. In the case of the second fault, since one of the relays is in the functioning state, the operation command is sent to the other relay. Thus, the inverter goes to the third mode and the switching pattern of this mode is executed. Fig. 6(a) shows a three-cell CMI equipped with the proposed fault-tolerant scheme. Meantime, the flowchart in Fig. 6(a) shows the process of the fault diagnosing method and the strategy of removing the faulty components.

It is worth to briefly explain the presented flowchart. For the sake of simplicity, the three-cell CMI, depicted in Fig. 2, is considered in the flowchart presented in Fig 6(b). Depending on the selected values for the voltages of the dc sources, a three-cell CMI can be employed either as a seven-level symmetric CMI or as a 15-level asymmetric CMI. It is to be noted that i in this flowchart is indicative of voltage levels. So, the maximum value of this parameter is considered seven for the assumed symmetric CMI, and 15 for the asymmetric one. According to the presented flowchart, in the initial stages values of the output and reference voltages, in the newly generated level, are compared. Meantime, states of the left-side and right-side switches ($S_1, S_3, S_5, S_7, S_9, S_{11}$) in the new and previous levels are processed through a XOR ($\oplus$) operation. When the output voltage mismatches the reference voltage the system understands that a fault has emerged. Thereafter, the system should diagnose the location of the fault. Since two locations are possible for the first fault (left-side fault (Fault *L*) and right-side fault (Fault *R*)), the system easily finds out the location of the first fault only through checking the last switching action of the switches in a particular side. (The task of finding out of the last switching action is possible through checking out the result of the XOR operation). In the flowchart this side is considered to be the left-side switches (S_1, S_5, S_9). In the other words, because for any change in the voltage level there is only one switching action in a certain side, the system does not need to check all the switching actions in both sides. What is more, since the lower switches in each side have comlementary states respect to the upper switches [for instance, according to Tables I and II, the lower switches in the left-side (S_4, S_8, S_{12}) have always complemetary states respect to the upper switches (S_1, S_5, S_9) in the same side] it is not required to check the lower switches states as well. If the result of XOR process of the switching pattern of that particular side is logically true, it is understood that the last state change (switching action) has happened. Henec, fault is highly probable to happen in these switches so the operation command should be sent to the relay related to that particular side. However, if the result of XOR process of switching pattern for the mentioned side is logically false (zero), the fault is highly probable to happen in the other side and the operation command should be sent to other relay. In the suggested flowchart, R_1, R_2, Fault *L*, and Fault *R* are, respectively, relay 1(relay assigned for the left-side switches), relay 2 (relay assigned for the right-side switches), fault in the left-side switches, and fault in the right-side switches.

It is interesting to mention that according to Fig. 6(a) and (b), there is no need to recognize the sort of the fault. Hence there is no need to continously checking the status of all the switches. Therefore, whether the switch fault is of short- or open-circuit sort, the system will act properly.

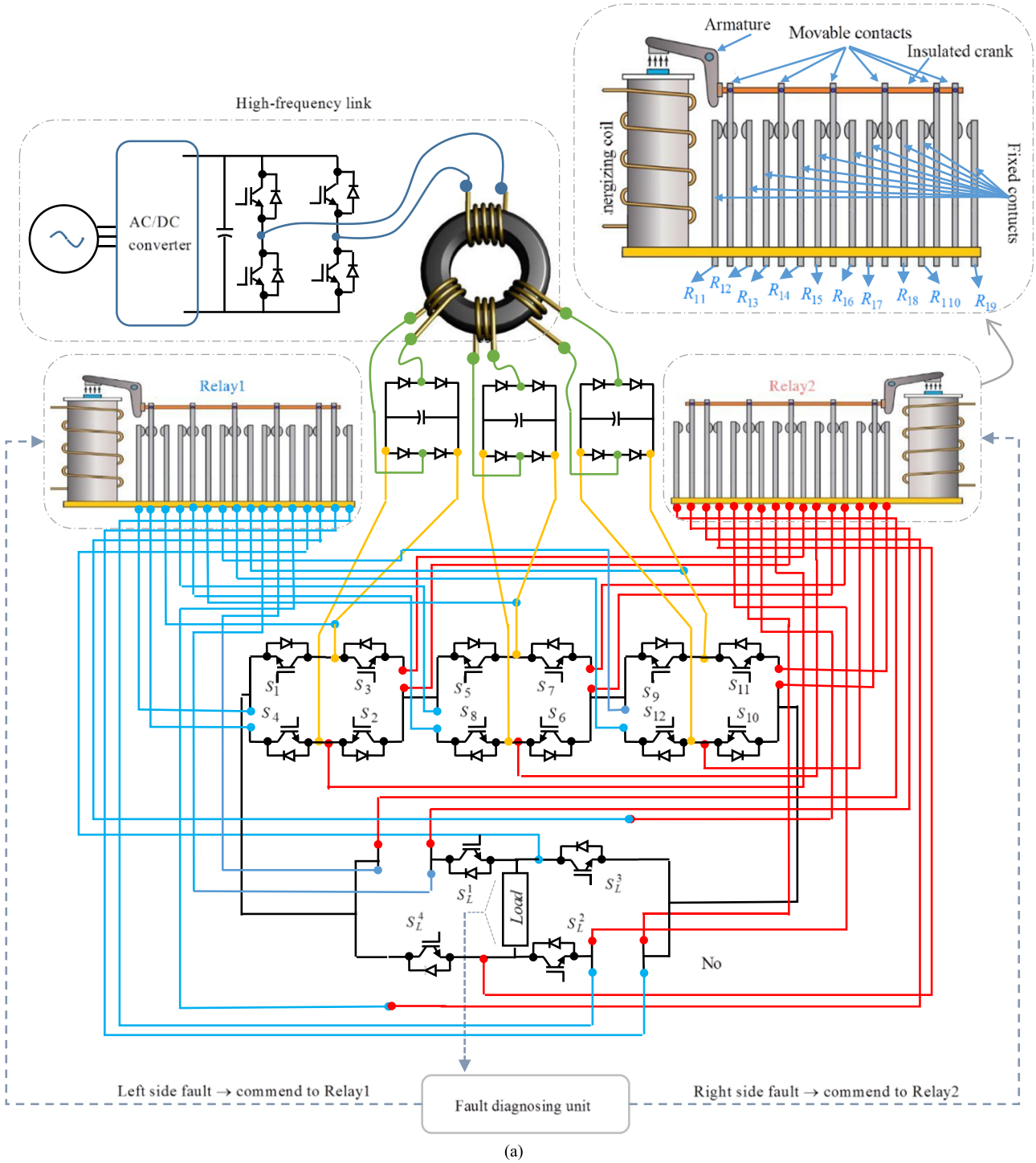
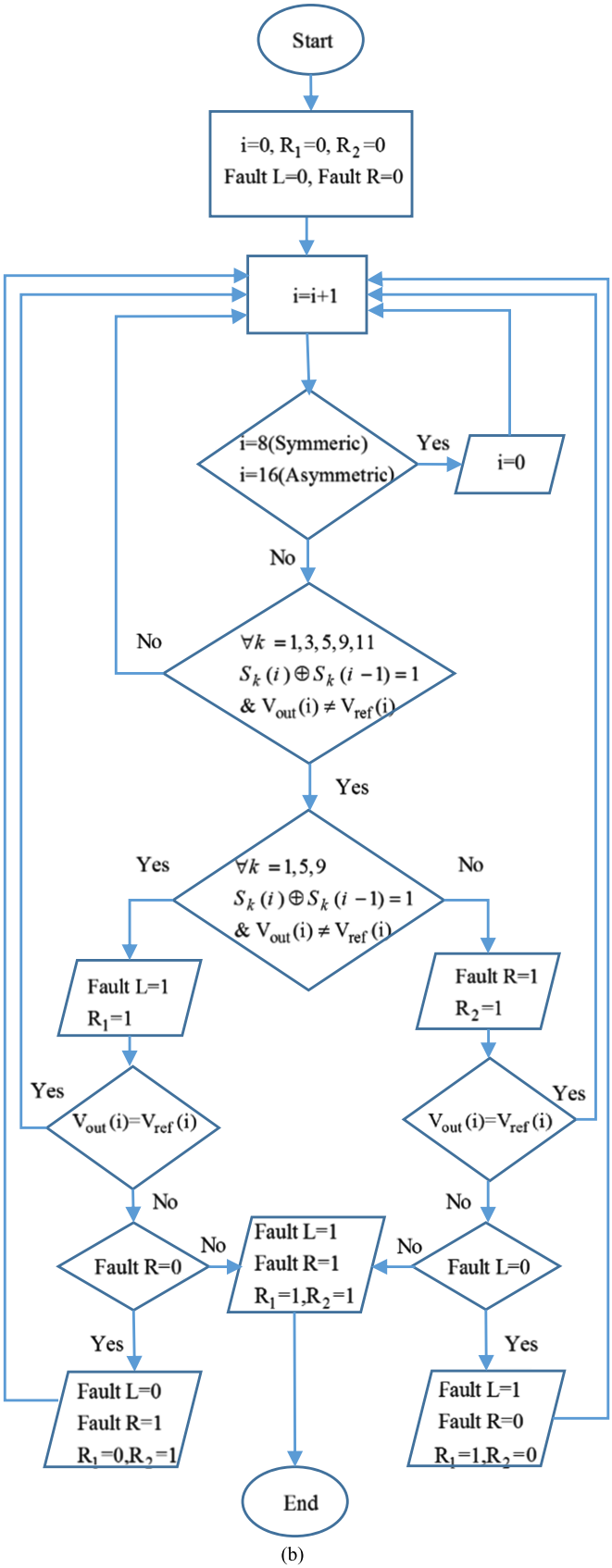


Fig. 6. (a) Typical three-cell CMI equipped with the proposed fault-tolerant structure.

III. Simulation and Experimental Result

In order to investigate the feasibility and viability of the suggested fault-tolerant scheme, the simulation results along with the experimental results are provided in this section. The simulation results are carried out using Matlab/Simulink. In addition, a laboratory prototype is employed to extract the experimental results. The employed prototype is depicted in Fig. 7. In the prototype, DSP-TMS320F28335 is adopted in order to compute the switching signals of the switches as well as to execute the fault diagnosing program. Characteristics of the components used in the studied model are listed in Table IV.

The assumed CMI is a three-cell multilevel inverter with symmetric sources (seven-level) and also 15-level with asymmetric sources (15-level). The desired output voltage is a sinusoidal voltage with the peak value of $220 \times \sqrt{2}$ V and the frequency of 50 Hz. A series-connected R–L impedance of $155\,\Omega + 370$ mH



(b)

Fig. 6. *(Continued)*. (b) Fault diagnosing and removing flowchart.

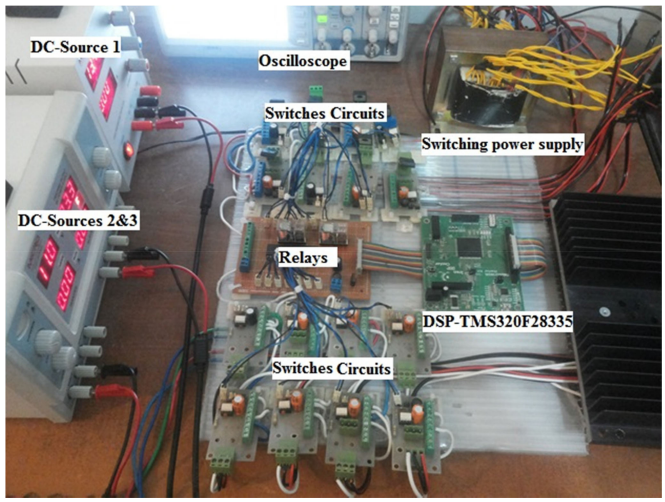


Fig. 7. Laboratory built prototype.

TABLE IV
TYPE OF COMPONENTS OF PROTOTYPE SETUP

Component	Type
Switches	MTD20N06HDL and IRFP250
Optocoupler	TLP250
Relay	Omron

is taken into consideration, which is connected to the terminals of the inverter as a load. In order to evaluate the performance of the suggested scheme under faulty conditions, two faults are considered to take place in the switches which are on the right and left sides of the cells (in the topology shown in Fig. 1). First, the symmetric inverter is considered. Fig. 8(a) shows the overall output voltage before and after happening of the above-mentioned two faults. The output voltage along with the load current after the first and the second faults are shown in Fig. 9(b) and (c), respectively. As observed, as the first fault takes place in one of the switches, the related relay starts operating and takes the inverter into the second mode. This is, also, the case when the second fault happens. The only difference is that, in the second fault, the second relay takes the inverter to the third mode. As shown, in the second mode the inverter resumes operating without altering the shape of output voltage. It is worth mentioning that since it takes about 0.02 s for the relays to reconfigure the topology of the inverter, one cycle of the output voltage disappears. Moreover, the experimental results of output voltage with the load current before and after the first fault are shown in Fig. 9(a).

If the second fault which takes place in one of the switches in the remained switches on the healthy side of the cells, the switches on the healthy side of the cells are removed from the circuit and all the sources are connected to each other in series through the second relay. Thus, the CMI topology will be reconfigured to a full-bridge cell containing one united dc

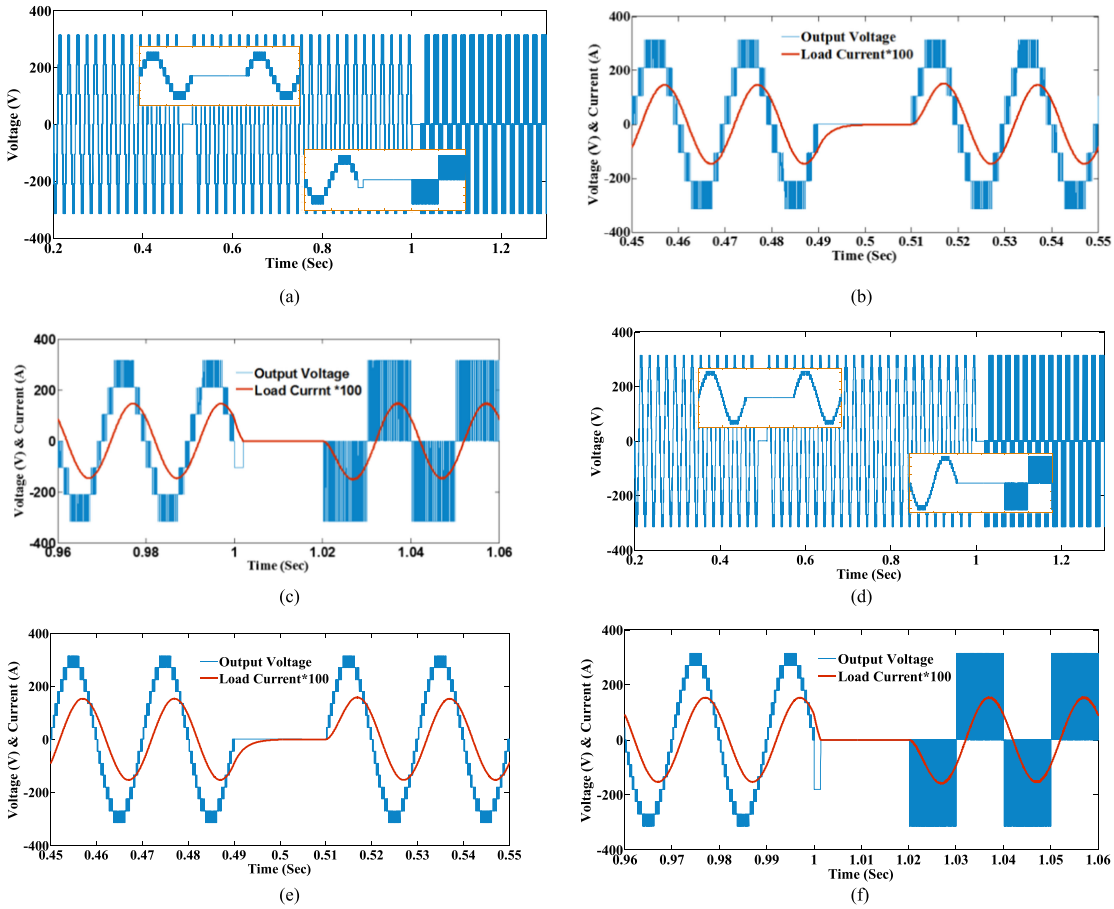


Fig. 8. Simulation results. (a) Overall output voltage of the symmetric topology. (b) Close view of the output voltage and load current in the first fault instance (symmetric topology). (c) Close view of the output voltage and load current in the second fault instance (symmetric topology). (d) Overall output voltage of the asymmetric topology. (e) Close view of the output voltage and load current in the first fault instance (asymmetric topology). (f) Close view of the output voltage and load current in the second fault instance (asymmetric topology).

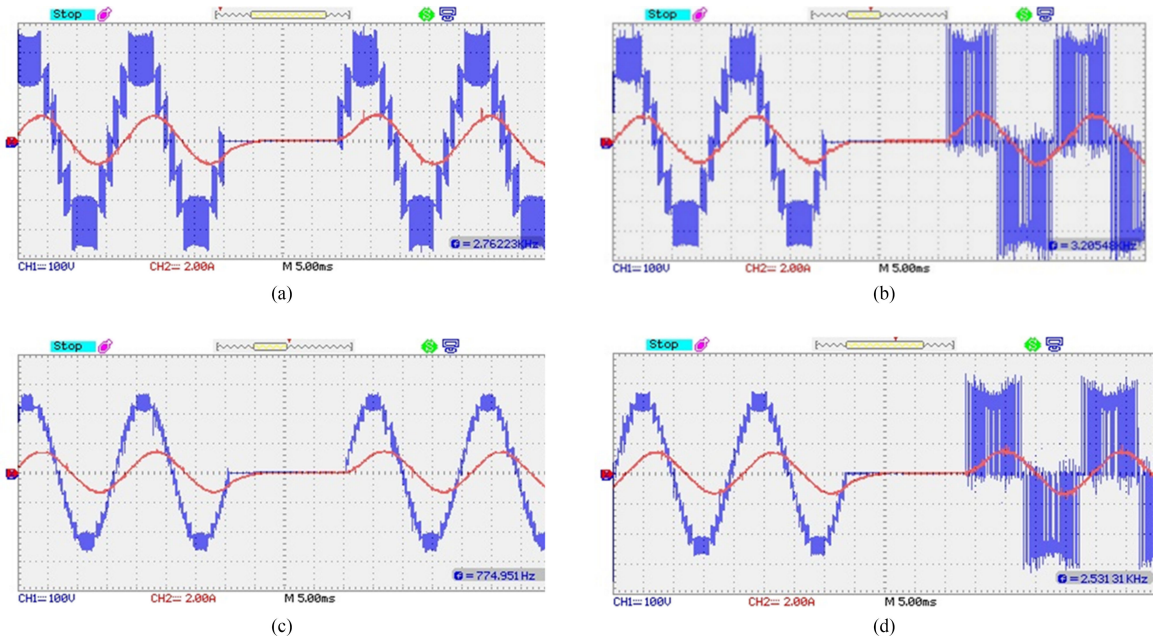


Fig. 9. Experimental results. (a) Output voltage and load current in the first fault instance (symmetric topology). (b) Output voltage and load current in the second fault instance (symmetric topology). (c) Output voltage and load current in the first fault instance (asymmetric topology). (d) Output voltage and load current in the second fault instance (asymmetric topology).

source. Thereupon, the shape of output voltage will change to a three-level voltage. However, in this mode, the PWM-based switching guarantees the fundamental shape of output voltage. The experimental results of inverter experiencing the second fault are depicted in Fig. 9(b). As mentioned earlier, due to slow response of the relay, about one cycle of the output voltage will vanish. According to the simulation and experimental results, since the load is resistive–inductive, the load current remains sinusoidal under any conditions.

The same scenarios and condition, described for the symmetric inverter in the previous paragraph, is considered for asymmetric CMI. Fig. 8(d) shows the simulation results of the overall output voltage realized by the three-cell asymmetric CMI. As shown, the inverter is exposed to the two independent faults. As depicted, the fault-tolerant scheme for the asymmetric inverter performs similar to the symmetric inverter. The close views of the output voltage and the load current in the fault instances are shown in Fig. 8(e) and (f), respectively.

In the experimental result, the magnitude of desired output voltage in the considered asymmetric topology is 234 V. Hence, the used dc voltages have the amplitude of 34, 68, and 136 V. The experimental results under different conditions are shown in Fig. 9(c) and (d). It goes without saying that the same procedure, which is described for the symmetric topology, is resorted when a fault takes place in the asymmetric inverter.

IV. Reliability Evaluation

A. Reliability Evaluation of the Conventional CMI

In this section, reliability evaluation of the CMI equipped with the suggested scheme is presented. To this end, following sequence is accomplished.

1) Failure rate analysis of the components.
2) Analyzing states of the system under different fault conditions and sketching Markov chain of the whole plot.
3) Reliability and MTTF evaluation by using the sketched Markov chain.

According to [24] and [25], as shown in Fig. 10, hazard rates of power electronic components can be investigated in three different phases. Phase I which is known as debugging phase is mainly related to manufacturing errors. Phase II is known as useful life period and characterized by approximately constant rate. Phase III shows wear out or fatigue phase of the components. For the sake of compactness and owing to the fact that power electronic devices are employed in their useful life, only the useful life period are considered to figure out the components failure rates.

For the sake of providing a more realistic reliability analysis for a practical CMI, the dc sources are considered to be provided by a high-frequency link according to [26] and [27]. In order to employ the Markov approach, it is necessary to obtain Markov chain and calculate all the possible Markov transition of the branches. In this paper, symmetric and asymmetric CMI inverters, which are synthesized with three H-bridge cells, are under consideration. Markov chain for this inverter is shown in Fig. 11. Each cell is synthesized with four switches and four diodes that realize an H-bridge. Without using the proposed fault-tolerant

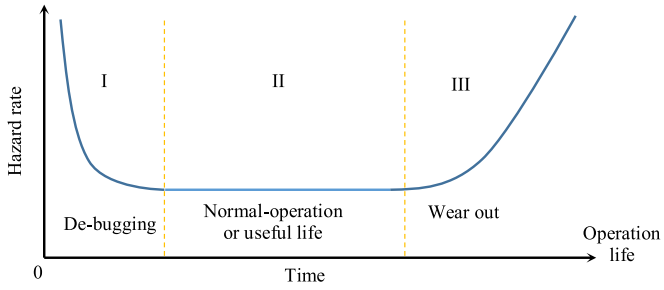


Fig. 10. Typical electronic component hazard rate as a function of age.

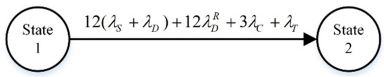


Fig. 11. Markov chain of conventional CMI.

scheme, one or more faults occurred in any component will cease the whole system to operate. Under such conditions there are only two states. In the first state, all the components are healthy and hence the inverter performs its tasks properly. This state is the healthy mode. In the second state, which is called the failure mode, at least one component fails and hence the inverter fails to operate. Taking into consideration that a failure in any of the remaining components causes the whole system to break down, in reliability evaluation, in this mode the system is considered as a series connected system. Considering that the inverter is synthesized with 12 power switches and 12 diodes, Markov transition chain is $\lambda_{12} = 12(\lambda_S + \lambda_D) + 12\lambda_D^R + 3\lambda_C + \lambda_T$, where λ_S and λ_D are failure rates of switches and diodes, respectively. λ_D^R and λ_C are failure rates of diodes and capacitors of rectifiers and λ_T is failure rate of high-frequency transformer.

According to Fig. 11, the differential equation (state-space equation) of the probability of being in any state for a seven-level (symmetric) or 15-level (asymmetric) CMI is stated in the following equation. Since there is no fault-tolerant scheme, the second state is assumed to be the absorbing state (1) shown at the bottom of the next page. where $P_1(t)$ and $P_2(t)$ are the probability of the healthy and failure modes, respectively.

In order to evaluate reliability, the initial state is required to be ascertained. Generally, all the systems are most likely to be in the healthy mode when they start to operate. Therefore, the initial condition is

$$P(0) = \begin{bmatrix} 1 & 0 \end{bmatrix}. \tag{2}$$

From (1) and (2), reliability of the conventional CMI inverter is

$$R(t) = P_1(t) = e^{-(12(\lambda_S+\lambda_D)+12\lambda_D^R+3\lambda_C+\lambda_T)t}. \tag{3}$$

To calculate the MTTF, a stochastic matrix (P) is expressed as (4) shown at the bottom of the next page.

By omitting columns and rows related to the absorbing state, the probability of not being in the absorbing state (Q) is obtained as

$$Q = \left[1 - (12(\lambda_S + \lambda_D) + 12\lambda_D^R + 3\lambda_C + \lambda_T)\right]. \tag{5}$$

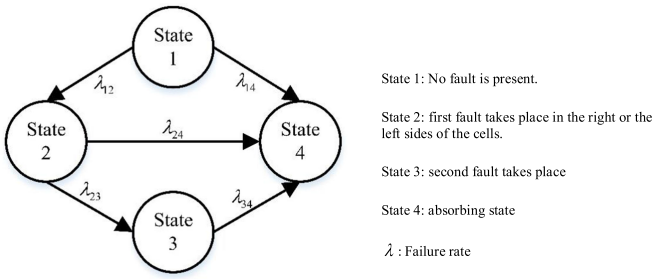


Fig. 12. Markov chain of the proposed fault-tolerant CMI scheme.

MTTF can also be obtained as

$$\mathrm{MTTF} = \int_0^\infty R(t)dt = [I - Q]^{-1} \tag{6}$$

$$\mathrm{MTTF} = \frac{1}{12(\lambda_S + \lambda_D) + 12\lambda_D^R + 3\lambda_C + \lambda_T}. \tag{7}$$

B. Reliability Evaluation of CMI Equipped with the Proposed Fault-Tolerant Scheme

The proposed fault-tolerant scheme for a three-cell CMI is depicted in Fig. 2. In this part, the conditional probability is used to evaluate reliability of the proposed scheme. The first condition is the proper operation of switches and diodes on the main cells and the second condition is the existence of a failure in one of the switches or diodes on the load-side module. Markov chain of the proposed scheme is shown in Fig. 12. It should be mentioned that improper operation of two relays could result in operation of the inverter in the absorbing state. Probability of each state is calculated as stated in (8)–(11)

$$d/dt\left[P_1(t)\ P_2(t)\ P_3(t)\ P_4(t)\right] = \left[P_1(t)\ P_2(t)\ P_3(t)\ P_4(t)\right] \times \begin{bmatrix} -(\lambda_{12}+\lambda_{14}) & \lambda_{12} & 0 & \lambda_{14} \\ 0 & -(\lambda_{23}+\lambda_{24}) & \lambda_{23} & \lambda_{24} \\ 0 & 0 & -\lambda_{34} & \lambda_{34} \\ 0 & 0 & 0 & 0 \end{bmatrix}. \tag{8}$$

Failure rates of each branch in Markov chain are

$$\begin{cases} \lambda_{12} = 12(\lambda_S + \lambda_D).P_r \\ \lambda_{14} = 12(\lambda_S + \lambda_D).(1 - P_r) + 12\lambda_D^R + 3\lambda_C + \lambda_T \\ \lambda_{23} = 6(\lambda'_S + \lambda'_D).P_r \\ \lambda_{24} = 6(\lambda'_S + \lambda'_D).(1 - P_r) + 4(\lambda_{\mathrm{SL}} + \lambda_{\mathrm{DL}}) \\ \qquad +12\lambda_D^R + 3\lambda_C + \lambda_T \\ \lambda_{34} = 4(\lambda'_{\mathrm{SL}} + \lambda'_{\mathrm{DL}}) + 12\lambda_D^R + 3\lambda_C + \lambda_T \end{cases} \tag{9}$$

where P_r is the probability of the proper operation of the two relays. Since P_1, P_2, and P_3 are the up state of this structure, the reliability is equal to

$$R(t) = \sum_{i=1}^{3} P_i(t). \tag{10}$$

The healthy mode is assumed to be the initial state

$$P(0) = \begin{bmatrix} 1\ 0\ 0\ 0 \end{bmatrix}. \tag{11}$$

Probability of each state is also

$$P_1(t) = e^{-(\lambda_{12}+\lambda_{14})t} \tag{12}$$

$$P_2(t) = \frac{\lambda_{12}}{\lambda_{23} + \lambda_{24} - \lambda_{12} - \lambda_{14}}\left[e^{-(\lambda_{12}+\lambda_{14})t} - e^{-(\lambda_{23}+\lambda_{24})t}\right] \tag{13}$$

$$P_3(t) = \frac{\lambda_{12}\lambda_{23}}{(\lambda_{12}+\lambda_{14}-\lambda_{34})(\lambda_{23}+\lambda_{24}-\lambda_{34})}e^{-\lambda_{34}t} + \frac{\lambda_{12}\lambda_{23}}{(\lambda_{34}-\lambda_{12}-\lambda_{14}).(\lambda_{23}+\lambda_{24}-\lambda_{12}-\lambda_{14})}e^{-(\lambda_{12}+\lambda_{14})t} + \frac{\lambda_{12}\lambda_{23}}{(\lambda_{34}-\lambda_{23}-\lambda_{24}).(\lambda_{12}+\lambda_{14}-\lambda_{23}-\lambda_{24})}e^{-(\lambda_{23}+\lambda_{24})t}. \tag{14}$$

Stochastic matrix (*P*) is expressed as

$$P = \begin{bmatrix} 1-(\lambda_{12}+\lambda_{14}) & \lambda_{12} & 0 & \lambda_{14} \\ 0 & 1-(\lambda_{23}+\lambda_{24}) & \lambda_{23} & \lambda_{24} \\ 0 & 0 & 1-\lambda_{34} & \lambda_{34} \\ 0 & 0 & 0 & 1 \end{bmatrix}. \tag{15}$$

In order to evaluate the MTTF, probability of not being in the absorbing state (*Q*) is required to be calculated. *Q* is obtained by truncating the columns and rows of *P* which are related to the absorbing state

$$\mathrm{MTTF} = [I - Q]^{-1} = \begin{bmatrix} \lambda_{12}+\lambda_{14} & -\lambda_{12} & 0 \\ 0 & \lambda_{23}+\lambda_{24} & \lambda_{23} \\ 0 & 0 & \lambda_{34} \end{bmatrix}. \tag{16}$$

C. Failure Rate Analysis of the Components

In this part, failure rates of power electronic components are calculated according to the method given in [28]. The failure rate of each component is obtained by multiplication of different factors

$$\lambda_{\mathrm{component}} = \lambda_b \sum_{i=1}^{n} \pi_i \quad (\mathrm{failure}/10^6\mathrm{h}) \tag{17}$$

$$d/dt\left[P_1(t)\ P_2(t)\right] = \left[P_1(t)\ P_2(t)\right] \begin{bmatrix} -12(\lambda_S+\lambda_D) + 12\lambda_D^R + 3\lambda_C + \lambda_T & 12(\lambda_S+\lambda_D) + 12\lambda_D^R + 3\lambda_C + \lambda_T \\ 0 & 0 \end{bmatrix} \tag{1}$$

$$P = \begin{bmatrix} 1-(12(\lambda_S+\lambda_D) + 12\lambda_D^R + \lambda_C + \lambda_T) & (12(\lambda_S+\lambda_D) + 12\lambda_D^R + \lambda_C + \lambda_T) \\ 0 & 1 \end{bmatrix} \tag{4}$$

TABLE V
TEMPERATURE AND OTHER EFFECTIVE FACTORS OF THE COMPONENTS [28]

Element	Effective factors	Temperature factor
MOSFET	$\lambda_S = \lambda_b \pi_T \pi_A \pi_Q \pi_E$	$\pi_T = \exp[-1925(\frac{1}{T_j+273} - \frac{1}{298})]$
Diode	$\lambda_D = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E$	$\pi_T = \exp[-3091(\frac{1}{T_j+273} - \frac{1}{298})]$
Transformer	$\lambda_T = \lambda_b \pi_T \pi_Q \pi_E$	$\pi_T = \exp[-1276(\frac{1}{T_{\rm HS}+273} - \frac{1}{298})]$
Capacitor	$\lambda_C = \lambda_b \pi_T \pi_V \pi_{\rm Cap} \pi_Q \pi_E$	$\pi_T = \exp[5.09(\frac{T_a+273}{358})^5]$

where n is the number of factors affecting the component failure rate and λ_b is the basic failure rate of component which is related to the component quality and its performance at a given temperature. In order to evaluate the influence of temperature, it is necessary to calculate the power loss of component. Temperature factor along with the other effective factors of components are included in Table V.

π_E: Effect of the environment which is equal to 1 for the component operating on the ground.

π_Q: Quality factor of the component which is equal to 1 [29].

π_A: Application factor of a MOSFET which depends on its power.

π_C: Contact construction factor which is equal to 1 for a metallurgically bonded diode, and it is equal to 2 for a nonmetallurgical bonded diode.

π_S: Electrical stress factor of a diode which is calculated by the following equation where V_S is the voltage stress ratio and is ratio of the applied voltage to the rated voltage [28]:

$$\pi_S = V_S^{2.43}. \tag{18}$$

π_V: Electrical stress factor of a capacitor. This factor is defined as follows in which V_C^M is maximum applied voltage and $V_C^{\rm Rated}$ is rated voltage of a capacitor:

$$\pi_V = \left[\left(\frac{V_C^M / V_C^{\rm Rated}}{0.5}\right)^3 + 1\right]. \tag{19}$$

$\pi_{\rm Cap}$: Capacity factor of a capacitor which is related to the material of the capacitor according to [28] and for a specific kind of capacitor is calculated as

$$\pi_{\rm Cap} = 0.34 C^{0.18}. \tag{20}$$

T_j: The junction temperature of a diode or power switch which is calculated as [28]

$$T_j = T_c + \theta_{\rm jc} P_D \tag{21}$$

$$T_c = T_a + \theta_{\rm ca} P_D. \tag{22}$$

These two equations are applicable for both MOSFETs and diodes. T_a is the environment temperature and assumed to be 25 °C. P_D is the average power loss of component. The power loss of MOSFET consists of two parts: switching power loss and directional power loss (conductor loss). According to Hajiesmaeili *et al.* [7], power loss equations for MOSFET and diode are presented as

$$P_D = \frac{1}{T}\left[\int_0^T \left(R_d i_S^2(t) + V_f i_D(t)\right) dt\right] \tag{23}$$

$$P_{D_{\rm SW,av}} = P_{\rm CL} + P_{\rm SL} = \frac{1}{T}\left[\int_0^T \left(R_{\rm DS,on} i_S^2(t) + V_T i_S(t)\right) dt\right] + \left[C^\circ f_s V_{\rm DS}^2\right]. \tag{24}$$

Also, the hotspot temperature $(T_{\rm HS})$ of a transformer is calculated as follows [28]:

$$T_{\rm HS} = T_a + \frac{125 \times 1.1 \times P_{\rm Loss}^{\rm Transformer}}{A} \tag{25}$$

where A is the radiating surface of the transformer. The power loss equation for transformer is presented as follows:

$$P_{\rm Transformer}^{\rm Loss} = \frac{1}{T_s}\left[\int_0^{Ts} R_T i_T^2(t) dt\right]. \tag{26}$$

To calculate power loss equations of the components, it is necessary to evaluate the currents of CMI switches and diodes. These currents for both symmetric and asymmetric configurations are presented as

$$\begin{cases} i_{S_n} = S_n i_S, & \text{sgn}(i_S) = \text{sgn}(v_{\rm SW_n}), \quad S_n \in \{0,1\} \\ i_{D_n} = S_n i_S, & \text{sgn}(i_S) \neq \text{sgn}(v_{\rm SW_n}), \quad n \in \{1,2,\ldots,14\} \end{cases} \tag{27}$$

where i_{S_n}, i_{D_n}, i_S, S_n, $\text{sgn}(i_S)$, $\text{sgn}(v_{\rm SW_n})$, and n are the current of nth switch, the current of nth diode, sign of load current, sign of the voltage over nth switch, the state of the nth switches, and the number of switches, respectively.

The mentioned parameters for employed components are presented in Table VI. The considered components are assumed to be commercially available and the parameters are extracted from datasheets.

V. NUMERICAL RESULTS

In this section, the numerical results of reliability and MTTF calculations are presented. Parameters and effective factors of MOSFETs and diodes are available in Table VI. Output power is considered to be equal to $P_{\rm Load} = 200$ W at the lagging power factor of 0.8. The output frequency is equal to 50 Hz. The maximum output voltage value is 315 V. Thus, in the symmetric CMI, the dc sources are equal to each other and they are considered to be $V_1 = V_2 = V_3 = 105$ V. But in the binary asymmetric configuration, those are equal to be $V_3 = 2V_2 = 4V_1 = 180$ V.

TABLE VI
REQUIRED PARAMETERS TO EVALUATE RELIABILITY OF THE PROPOSED SCHEME

Parameters	Explanations		Quantity	Parameters	Explanations		Quantity
V_{Out}^{Max}	RMS load voltage		220 (v)	C	Capacitance of capacitors used in rectifiers		4700 (μF)
V_{Out}	Max. load voltage		315 (v)	V_C^{rated}	Rated voltage of the capacitors used in rectifiers		200 (v)
P_o	load power		200 (W)	λ_b	Basic failure rate of MOSFET		0.06
$P.F$	Power factor of the load		0.8		Basic failure rate of Diode		0.0038
V_i	Sources in symmetric mode	$V_1=V_2=V_3$	105 (v)		Basic failure rate of Transformer		0.049
V_i	Sources in asymmetric mode	V_1	45 (v)		Basic failure rate of Capacitor		0.00254
				π_Q	Quality factor		1
		V_2	90 (v)	π_C	Contact construction factor		1
		V_3	180 (v)	π_E	Environment factor		1
f_S	Switching frequency		5 (kHz)	π_A	Application factor		8
A	Radiating surface of transformer		0.2 (in^2)	C_o	Capacitance of MOSFET out capacitor		330 (pF)
f_T	Transformer frequency		20 (kHz)	T_a	Ambient temperature		25 (°C)
$R_{DS,on}$	MOSFET conductive resistance		0.55 (Ω)	θ_{JC}	Junction to case temperature	Diode	1.5 ($^{\circ C}/_{W}$)
V_T	Threshold voltage of MOSFET		0.5 (v)			MOSFET	1 ($^{\circ C}/_{W}$)
V_f	Forward voltage of diode		0.5 (v)	θ_{CA}	Case to ambient temperature	Diode	63 ($^{\circ C}/_{W}$)
R_D	Diode conductive resistance		0.2 (Ω)			MOSFET	72 ($^{\circ C}/_{W}$)

TABLE VII
TEMPERATURE FACTOR OF COMPONENTS IN SYMMETRIC AND ASYMMETRIC CONFIGURATIONS

		Healthy mode			After first fault						After second fault		
		Source-side components			Source-side components			Load-side components			Load-side components		
Configuration	Component	P_D (W)	T_j (°C)	π_T	P_D (W)	T_j (°C)	π_T	P_D (W)	T_j (°C)	π_T	P_D (W)	T_j (°C)	π_T
Symmetric	MOSFET	0.77	73.51	2.47	0.77	73.51	2.47	0.91	82.33	.83	1.15	97.45	3.54
	Diode	0.44	57.78	2.79	0.44	57.78	2.79	0.44	57.78	2.79	0.59	68.95	3.79
Asymmetric	MOSFET	0.8	75.62	2.56	0.8	75.62	2.56	0.91	82.33	2.83	1.15	97.45	3.54
	Diode	0.44	57.78	2.79	0.44	57.78	2.79	0.44	57.78	2.79	0.59	68.95	3.79

TABLE VIII
EFFECTIVE FACTORS ON RELIABILITY OF COMPONENTS IN HIGH-FREQUENCY LINK

	Component								
	Diodes			Capacitors			Transformer		
Configuration	P_D (W)	T_j (°C)	π_T	π_V	π_{Cap}	π_T	P_{Loss}^T (W)	T_{HS} (°C)	π_T
Symmetric	0.52	63.74	3.3	2.16	1.56	7.65	20	13750	66.08
Asymmetric	0.6	69.7	3.43	6.83					

The calculated power losses, junction temperatures, and temperature factors in different states of operation for MOSFETS and diodes of the proposed CMI scheme are listed in Table VII. The effective factors of components in the high-frequency link are provided in Table VIII.

The failure rates of components, MTTF, and reliability of the inverter in both symmetric and asymmetric structure are listed in Table IX.

In the proposed fault-tolerant scheme, because of the high reliability of relays, healthy operation probability of the two relays

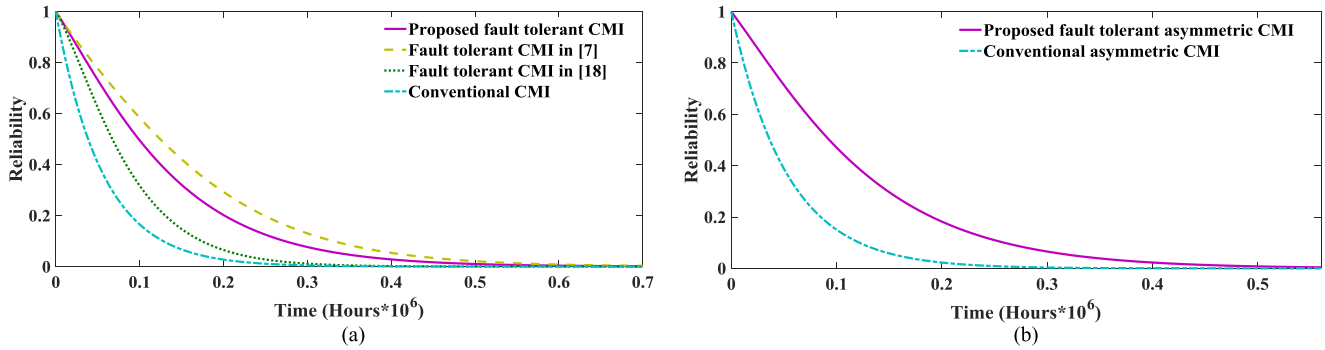


Fig. 13 (a) Reliability comparison of a three-cell symmetric CMI equipped with the proposed scheme and the schemes presented in [7] and [18], as well as the conventional CMI without using fault-tolerant structure. (b) Reliability comparison of a three-cell asymmetric CMI with and without employing the proposed scheme.

TABLE IX
NUMERICAL RESULTS FOR THE CONVENTIONAL CMI

Index	Symmetric	Asymmetric
λ_S	1.19	1.23
λ_D	0.011	0.011
λ_D^R	0.012	0.013
λ_C	0.066	0.21
λ_T	3.24	3.24
MTTF	0.0555×10^6 (h)	0.0528×10^6 (h)
$R(t)$	e^{-18t}	$e^{-18.93t}$

TABLE X
FAILURE RATES IN THE PROPOSED SCHEME

Failure rates (failure/10^6h)	λ_{12}	λ_{14}	λ_{23}	λ_{24}	λ_{34}
Symmetric mode	12.97	5.02	6.48	9.79	10.43
Asymmetric mode	13.41	5.52	6.7	10.26	10.88

assumed to be equal to $P_r = 0.9$. Failure rates are presented in Table X.

Probability of each state of the symmetric and asymmetric structures are calculated by using (12)–(14) and are tabulated in Table XI.

Reliability equations for the proposed fault-tolerant CMI with symmetric and asymmetric configurations are, respectively, shown in the following equations:

$$R(t) = 1.9e^{-10.43t} - 0.83e^{-16.27t} - 0.08e^{-18t} \quad (28)$$

$$R(t) = 1.84\ e^{-10.88t} - 0.69e^{-16.96t} - 0.15e^{-18.93t}. \quad (29)$$

By using (6), MTTF of symmetric and asymmetric configurations are obtained

$$\text{MTTF} = \int_0^\infty R(t) = 0.12671 \times 10^6\ (h) \quad (30)$$

$$\text{MTTF} = \int_0^\infty R(t) = 0.12051 \times 10^6\ (h). \quad (31)$$

VI. COMPARISON

In order to provide a comprehensive assessment, the proposed fault-tolerant scheme is compared with the schemes suggested in [7] and [18]. To this end, a three-cell CMI is taken into consideration and different effective parameters on it are considered. Furthermore, reliabilities of these three schemes along with the CMI without employing any fault-tolerant structure are depicted in Fig. 13. Since the schemes given in [7] and [18] are not adoptable in asymmetric CMIs, only the reliabilities of an asymmetric CMI with and without being equipped with the proposed fault-tolerant structure are considered. The results are tabulated in Table XII.

In the fault-tolerant CMI presented in [7], when a fault occurs in one of the H-bridge cells, the dc source in that cell is transferred to one of the intact modules and all the switches in the faulty cell become deactivated. This is accomplished through some relays. Four relays and one voltage sensor are required for each cell in the fault-tolerant structure presented in [7]. High number of sensors and relays make the sensing and fault diagnosing scheme complex and difficult to be implemented and executed. In [18], Song and Huang employ one redundant H-bridge cell to enhance reliability of CMIs. When a fault emerges in one of the CMI cells, the cell is bypassed through a relay and the other healthy cells take over the bypassed cell task. Therefore, the switches should tolerate an extra voltage. Similar to the structure in [7], each cell in the fault-tolerant CMI in [18] calls for one voltage sensor. However, unlike fault-tolerant CMI in [7], the fault-tolerant scheme in [18] needs only one relay for each H-bridge cell. This makes the scheme in [18] easier to be controlled than that in [7]. Nevertheless, the scheme in [7] offers higher reliability than that in [18].

Unlike the fault-tolerant scheme in [7] and [18], the sensing and fault diagnosing/removing scheme in the proposed scheme in this work does not require a complex process, because this scheme requires only one voltage sensor to watch out the output voltage and totally two relays to rid the CMI of faulty conditions. However, compared with the structure in [7], the proposed structure needs four extra switches (load-side switches). The other demerit of structures in [7] and [18] is that all the switches in the CMI equipped with the suggested fault-tolerant schemes

TABLE XI
PROBABILITY OF EACH STATE BY ASSUMING INTACT OPERATION OF LOAD-SIDE CELL

	Symmetric	Asymmetric
$P_1(t)$	e^{-18t}	$e^{-18.93t}$
$P_2(t)$	$7.54 \times (e^{-16.27t} - e^{-18t})$	$6.81 \times (e^{-16.96t} - e^{-18.93t})$
$P_3(t)$	$1.9e^{-10.43t} + 6.46e^{-18t} - 8.37e^{-16.27t}$	$1.84e^{-10.88t} + 5.66e^{-18.93t} - 7.5e^{-16.96t}$

TABLE XII
COMPARISON OF DIFFERENT FAULT-TOLERANT SCHEMES

Scheme	Proposed scheme	[7]	[18]
Number of Power Switches	16	12	16
Number of Relays	2	12	4
Number of Sensors	1	6	4
Number of elements designed for working in Max. voltage stress	4	12	14
Control difficulty	Easy	Difficult	Moderate
Ability to work in asymmetric mode	Yes	No	No
Reliability	$R(t) = 1.9e^{-10.43t} - 0.83e^{-16.27t} - 0.08e^{-18t}$	$R(t) = 5.09e^{-10.43t} + 1.49e^{-18t} - 5.55e^{-13.43t}$	$R(t) = 4.23e^{-18.83t} - 3.23e^{-22.92t}$
MTTF	0.12671×10^6 h	0.15707×10^6 h	0.08359×10^6 h

should tolerate higher voltage under the worst faulty conditions. In this term, only the four load-side switches of the proposed scheme have to tolerate the maximum output voltage. Hence, the switches of main cells are not required to be of high voltage rating. They are only required to tolerate the dc voltage of dc sources in the H-bridge cells. In addition, the suggested schemes in [7] and [18] are not applicable for asymmetric CMI, whereas the scheme under discussion can be adopted in both symmetric and asymmetric CMI without needing any extra component. According to Fig. 13, in terms of reliability, the suggested scheme in [7] surpasses others, whereas the proposed scheme provides higher reliability than that in [18].

VII. CONCLUSION

In this paper, in order to enhance reliability of the CMIs, a fault-tolerant structure is proposed. A CMI equipped with the proposed fault-tolerant structure features a flexible topology which can be reconfigured when different faults occur. The reconfiguration is accomplished through two relays. It is noteworthy that the proposed structure is applicable to both symmetric and asymmetric CMIs. Additionally, a simple fault diagnosing scheme is proposed for the suggested structure. This scheme is based on watching out the output voltage circumstance and comparing it with the voltage according to the executed switching pattern. This is an interesting feature owing to the fact that it only requires one sensor. Since there is no need to recognize the type fault of the switches (short circuit or open circuit), there is no need to check out situations of the switches. Furthermore, different operating modes of the proposed fault-tolerant CMI are modeled and the related Markov chain is obtained. By using the obtained Markov model, reliability of the studied CMI is assessed. Finally, by using Matlab/Simulink environment and also a laboratory prototype, viability and feasibility of the suggested structure are validated.

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