Quasi-Square-Wave Modulation of Modular Multilevel High-Frequency DC Converter for Medium-Voltage DC Distribution Application

Yu Wang, Qiang Song, *Member, IEEE*, Biao Zhao, *Member, IEEE*, Jianguo Li, Qianhao Sun, and Wenhua Liu

***Abstract*—In a direct current (dc) distribution network, the modular multilevel high-frequency dc converter (MDCC) can achieve electrical isolation, voltage conversion and power transmission between the low- and medium-voltage dc buses. In this paper, quasi-square-wave (QSW) modulation, which avoids the dv/dt stress problem and maintains a high dc voltage utilization, is applied in MDCC, and the mathematical model of QSW modulation with a dual-phase-shift (DPS) scheme is established. Based on the model, the influences of staircase rising and falling process in QSW modulation on MDCC performance, including the power characteristic, current stress, switching characteristic, and efficiency characteristic, are analyzed. The influences of QSW modulation under DPS scheme on MDCC performance are also investigated. Moreover, to achieve a comprehensive optimization of MDCC performance, a multiobjective optimized control strategy based on QSW modulation under DPS scheme is proposed. Finally, a MDCC prototype is set up and the experimental results verify the correctness and effectiveness of the analysis and proposed strategy.**

***Index Terms*—DC distribution network, modular multilevel high-frequency dc converter, multiobjective optimized dual-phase-shift (DPS) strategy, quasi-square-wave (QSW) modulation.**

I. Introduction

COMPARED with the alternating current (ac) distribution network, the direct current (dc) distribution network can reduce the use of power converters, thereby decreasing power consumption and component cost. Besides, the dc distribution network has higher power conversion efficiency, and its transmission power quality can be improved effectively [1], [2]. Moreover, with the development of dc distributed power sources, energy storage devices, and electrical equipment, the dc distribution network has considerable potential for application [3], [4]. Current studies on the improvement of the dc distribution network not only focus on low-voltage dc (LVDC) distribution network but extends to medium-voltage dc (MVDC) and high-voltage dc (HVDC) distribution networks [5], [6].

DC/DC converters are crucial to dc distribution networks for converting voltage and interconnecting links of different voltage levels. High-frequency (HF) dc/dc converters are expected to be the trend in next-generation power conversion because of their advantages, such as low volume, low cost, lightweight, low power conversion noise, high efficiency, and high power density [7]. Among the various topologies of HF dc/dc converters, the recently emerging modular multilevel dc/dc converter (M2DC) based on modular multilevel converter (MMC) topology on both sides provides a possible solution for MVDC and HVDC distribution networks [8]–[16]. The single-phase MMC structure is employed on both sides of M2DC to increase the voltage level, and its scalable architecture enables a large operating voltage and power rating by stacking the requisite number of half-bridge submodules (SMs) in cascade. Meanwhile, redundancy can be implemented by installing additional SMs. Moreover, dc breakers are unnecessary as its bidirectional fault blocking feature is similar to a dc circuit breaker, thereby presenting a secure solution for dc grids [15], [16]. However, the MMC topology of M2DC on the LVDC side has low voltage utilization and a complicated implementation process. Thus, M2DC becomes unsuitable for connecting the LVDC distribution network with the MVDC and HVDC distribution networks. Moreover, M2DC also has only one high-frequency-link (HFL) transformer, thereby limiting its power capability and applications.

Therefore, a modular multilevel HF dc converter (MDCC) is proposed to connect LVDC distribution network with the MVDC and HVDC distribution networks [17], as shown in Fig. 1. Similar to M2DC, a single-phase MMC structure exists on the MVDC side, and the advantages of MMC structure are retained. In contrast to M2DC, the LVDC side of MDCC is composed of full bridges, which are connected in parallel to increase the current level, and the number of full bridges changes with the current and power levels in practical application. In addition, the HFL transformers in the MDCC are not integrated transformers as those in M2DC, but are constituted of several independent HFL transformers in series with lower voltage and power levels. Therefore, the power capacity of each single HFL isolated transformer in MDCC will be decreased, thereby reducing manufacturing difficulty of HFL transformer, and altering the power capacity of MDCC effectively

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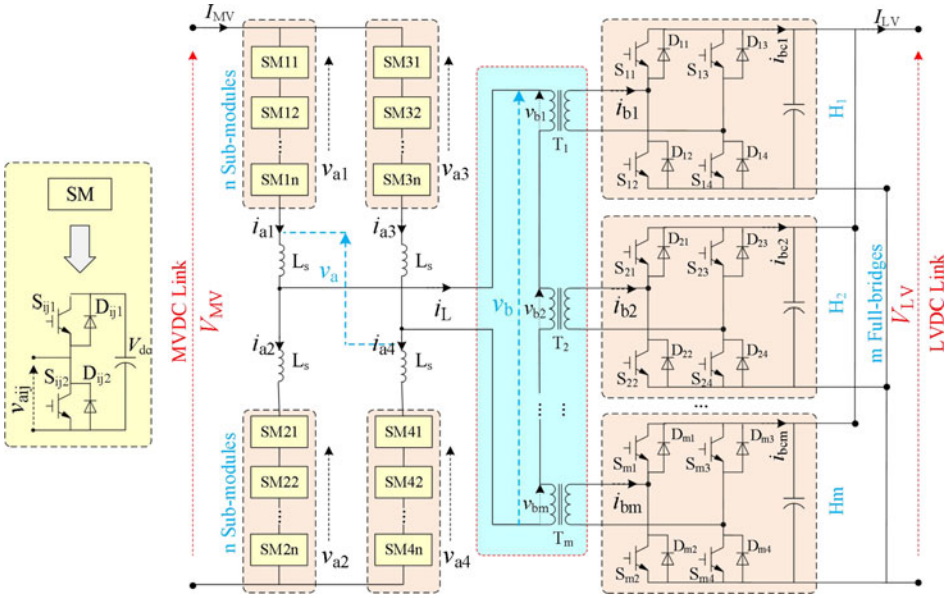

Fig. 1. Topology of modular multilevel high-frequency-link dc converter.

according to the requirement. Similar architectures of dc/dc converter covering the direct connection and transformer-interfaced are found in [18], [19]. Different from MDCC, these dc/dc converters realize voltage conversion by varying the magnitude of SM stack voltage. The direct connection architecture cannot provide galvanic isolation, and the transformer-interfaced architecture cannot achieve the bidirectional power transmission, which are the requirements of dc distribution application.

Generally, because a square wave (SW) has higher dc voltage utilization ratio and power transfer capability than a sinusoidal wave with the same amplitude, the SW modulation is preferred for HFL modulation in dc/dc converters such as dual-active-bridge (DAB), M2DC, MDCC, etc. [20], [21]. However, the SW modulation suffers from *dv/dt* stress problem because it produces a destructive *dv/dt* stress upon transformer insulation, in which the dc voltage is instantly switched, particularly in the HVDC system [22]. Trapezoidal and sinusoidal modulations are applied to alleviate the *dv/dt* stress on the transformer and decrease the harmonic content in HFL voltage [23], [24]. Nevertheless, the power transmission capability under trapezoidal and sinusoidal modulations is smaller than that under SW modulation [15], [20]. Therefore, the quasi-SW (QSW) modulation, in which the small phase shift between the adjacent SMs generates the quasi-square HFL voltages to approximate the SW modulation, is proposed in [25]. dv/dt of HFL voltages will be reduced significantly by applying QSW modulation, and the high dc voltage utilization ratio and power transfer capability are preserved. However, the staircase rising and falling process in HFL voltages makes QSW modulation different from SW modulation, and the influence of voltage staircase during the rising and falling process in QSW modulation on converter performance has not been discussed yet.

When the voltages on two sides of dc/dc converter do not match, the current stress and circuiting current become large. This situation leads to larger power loss and lower efficiency, thereby hindering the application of dc/dc converters. The dual-phase-shift (DPS) scheme, which has been investigated and applied effectively in DAB converter, has been proven effective in solving these problems [26], [27]. However, the mathematical model of QSW modulation under DPS scheme is still absent, and the influence of QSW modulation under DPS scheme to dc/dc converter performance has not been investigated yet. In addition, the DPS scheme in existing literature only optimizes a single characteristic, such as the current stress, power characteristic, efficiency characteristic or switching characteristic [28]–[31], and the multiobjective optimization scheme has not been considered yet.

In this paper, the QSW modulation is applied in MDCC to reduce the dv/dt stress and maintain the power transfer capability, and the mathematical model of QSW modulation under DPS scheme is established. Based on the model, the influences of voltage staircase during the rising and falling process in QSW modulation on MDCC performance including power characteristic, current stress, switching characteristic, and efficiency characteristic are analyzed. Besides, the influences of DPS scheme under QSW modulation on MDCC performance are also investigated. Moreover, a multiobjective optimized DPS strategy is proposed to achieve a multiobjective optimization of power transfer capacity, current stress, and power loss in MDCC.

II. Quasi-Square-Wave Modulation With Dual-Phase-Shift Control for MDCC Performance

The topology configuration of MDCC is shown in Fig. 1. $V_{\rm MV}$ and $V_{\rm LV}$ are the MVCD and LVDC voltages, while $I_{\rm MV}$ and $I_{\rm LV}$ are the MVCD and LVDC currents, respectively. $i_{\rm L}$ is the HFL current. The MMC topology connected to MVCD side is composed of four arms in a bridge arrangement, and each arm contains n SMs and inductor L_s. Each SM comprises a capacitor, a half-bridge with power switches and diodes. In addition, each SM generates square voltage $v_{aji,}$ and the positive and negative

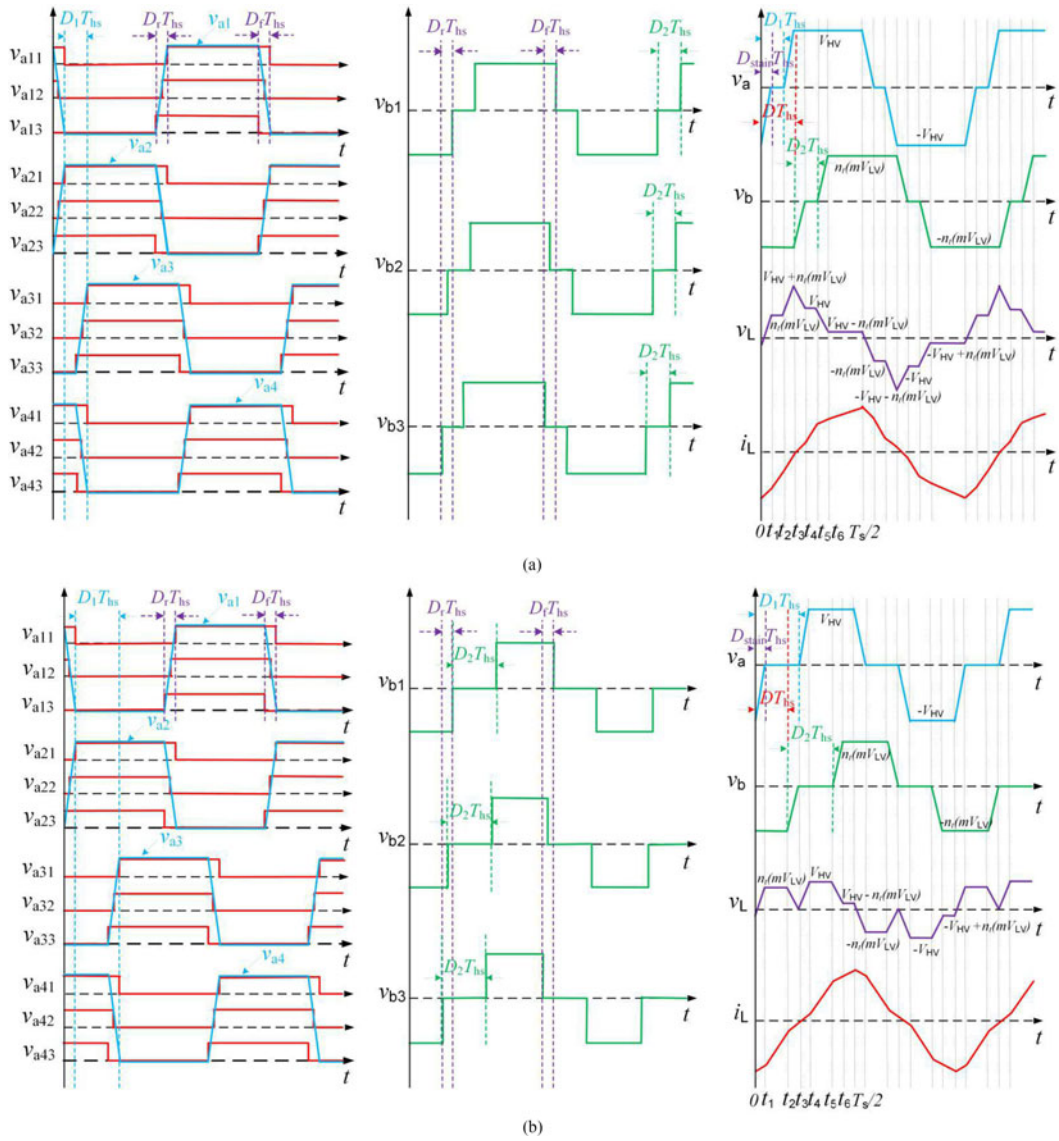

Fig. 2. QSW modulation waveforms under DPS scheme in MDCC: (a) when $0 \le D_1 = D_2 = d \le D \le 1$ and (b) when $0 \le D \le D_1 = D_2 = d \le 1$.

voltages in each SM are $V_{\rm dc}$ and 0, respectively. $v_{a1} - v_{a4}$ and $i_{a1} - i_{a4}$ are, respectively, the voltages and the currents of arms in MMC topology. The LVDC side is composed of m full bridges, which connect in parallel to increase the current level. $v_{b1} - v_{bm}$ and $i_{b1} - \mathrm{i}_{bm}$ are the voltages and the currents in full bridges, respectively.

The QSW modulation is employed in MDCC to alleviate the voltage derivative dv/dt stress on transformers and ensure higher dc voltage utilization ratio and power transfer capability. $k = V_{\rm MV}/n_{\rm T} m V_{\rm LV}$ is defined as voltage conversion ratio, and the modulation waveforms when $k > 1$ under DPS based on QSW with $n = m = 3$ are shown in Fig. 2. The modulation waveforms when $k > 1$ are discussed, and the modulation waveforms when $k < 1$ can be analyzed similarly. The SMs in each arm in MMC topology insert or bypass one by one during the voltage rising or falling transition, and a modulation time difference exists between the adjacent SMs. By doing so, the height of each voltage stair is limited to one SM or full-bridge capacitor voltage, thereby reducing the dv/dt stress. Therefore, the HFL voltage v_a on the MVDC side is a QSW with a voltage staircase during the voltage transition. A modulation time difference also occurs between adjacent full bridges on the LVDC side. Thus, the HFL voltage v_b on the LVDC side is also a QSW with a staircase voltage during voltage rising or falling transition. The voltage rising and falling times during staircase transition are equal to reduce control difficulty, and the arms on the MVDC side and the full bridges on the LVDC side have the same voltage changing times during staircase transition.

In Fig. 2, v_{a1}, v_{a2}, v_{a3}, and v_{a4} are the arm voltages in MMC on the MVDC side. v_{b1}, v_{b2}, and v_{b3} are the equivalent HFL voltages from full bridges voltages on the LVDC side. D is the duty ratio of outer phase-shift angle between HFL voltages. D_1 and D_2 are the duty ratios of the inner phase-shift angle on MVDC and LVDC sides, and the control scheme becomes DPS when $D_1 = D_2 = d$. The D_r and D_f are the duty ratios of voltage staircase during rising and falling transitions,

respectively, and assume that $D_r = D_f = D_{\text{stair}}.T_s$ is the periodic time and T_{hs} is a half of periodic time where $T_{hs} = T_s/2$. The f_s is switching frequency. When $0 \le d \le D \le 1$, $t_1 = D_{\text{stair}}\,T_{hs}, t_2 = dT_{hs}, t_3 = (d + D_{\text{stair}})\,T_{\text{hs}}$, $t_4 = D\,T_{hs}$, $t_5 = (D + D_{\text{stair}})\,T_{hs}$, $t_6 = (D + d)T_{hs}$, $t_7 = (D + d + D_{\text{stair}})T_{hs}$, and $t_8 = T_s/2$. When $0 \le D \le d \le 1$, $t_1' = D_{\text{stair}}\,T_{hs}$, $t_2' = DT_{hs}$, $t_3' = (D + D_{\text{stair}})\,T_{hs}$, $t_4' = d\,T_{hs}$, $t_5' = (d + D_{\text{stair}})\,T_{hs}$, $t_6' = (D + d)T_{hs}$, $t_7' = (D + d + D_{\text{stair}})T_{hs}$, and $t_8' = T_s/2$. Since the phase differences between adjacent SMs and adjacent full bridges are small in QSW modulation, the voltage staircase during rising and falling process are very similar to oblique lines, especially in the case of a large number of SMs and full bridges. To simplify the mathematical analysis and calculation, the voltage staircase during rising and falling process in QSW modulation are simplified into oblique lines [32].

A. Transfer Power Characterization

According to Fig. 2, when $0 \le d \le D \le 1$ and $0 \le D \le d \le 1$, the HFL voltages v_a and v_b can be described as

$$v_a(t) = \begin{cases} \frac{V_{\text{MV}}}{D_{\text{stair}}T_{hs}}t - V_{\text{MV}}, & t \in [0, t_1] \\ 0, & t \in [t_1, t_2] \\ \frac{V_{\text{MV}}}{D_{\text{stair}}T_{hs}}(t - dT_{hs}), & t \in [t_2, t_3] \\ V_{\text{MV}}, & t \in [t_3, T_s/2] \end{cases}$$

$$v_b(t) = \begin{cases} -n_t m V_{\text{LV}}, & t \in [0, t_4] \\ \frac{n_t m V_{\text{LV}}}{D_{\text{stair}}T_{hs}}(t - DT_{hs}) - n_t m V_{\text{LV}}, & t \in [t_4, t_5] \\ 0, & t \in [t_5, t_6] \\ \frac{n_t m V_{\text{LV}}}{D_{\text{stair}}T_{hs}}(t - DT_{hs} - dT_{hs}), & t \in [t_6, t_7] \\ n_t m V_{\text{LV}}, & t \in [t_7, T_s/2] \end{cases}$$

$$0 \le d \le D \le 1 \quad (1)$$

$$v_a(t) = \begin{cases} \frac{V_{\text{MV}}}{D_{\text{stair}}T_{hs}}t - V_{\text{MV}}, & t \in [0, t_1'] \\ 0, & t \in [t_1', t_4'] \\ \frac{V_{\text{MV}}}{D_{\text{stair}}T_{hs}}(t - dT_{hs}), & t \in [t_4', t_5'] \\ V_{\text{MV}}, & t \in [t_5', T_s/2] \end{cases}$$

$$v_b(t) = \begin{cases} -n_t m V_{\text{LV}}, & t \in [0, t_2'] \\ \frac{n_t m V_{\text{LV}}}{D_{\text{stair}}T_{hs}}(t - DT_{hs}) - n_t m V_{\text{LV}}, & t \in [t_2', t_3'] \\ 0, & t \in [t_3', t_6'] \\ \frac{n_t m V_{LV}}{D_{\text{stair}}T_{hs}}(t - DT_{hs} - dT_{hs}), & t \in [t_6', t_7'] \\ n_t m V_{\text{LV}}, & t \in [t_7', T_s/2] \end{cases}$$

$$0 \le D \le d \le 1. \quad (2)$$

The power conversion of MDCC can be viewed as the power exchange between HFL voltage sources v_a and v_b through the equivalent inductor L, and the average current of inductor over one switching period should be zero in the steady state. Therefore, the HFL current i_L can be expressed as

$$i_L(t) - i_L(0) = \int_0^t \frac{v_a(t) - v_b(t)}{L} dt. \quad (3)$$

Substituting (1) and (2) into (3), the HFL current i_L in the condition of $0 \le d \le D \le 1$ can be described as (4) shown at the bottom of this page.

The HFL current i_L at 0, $D_{\text{stair}}T_{hs}$, dT_{hs}, $(d + D_{\text{stair}})\,T_{hs}$, DT_{hs}, $(D+D_{\text{stair}})T_{hs}$, $(D+d)T_{hs}$, $(D+d+D_{\text{stair}})T_{hs}$, and $T_s/2$ is given by (5) as shown at the bottom of this page.

Similarly, the HFL current i_L in condition of $0 \le D \le d \le 1$ can be described as (6) as shown at the bottom of the next page, where the HFL current i_L at $t' = 0, D_{\text{stair}}\,T_{hs}, DT_{hs}$, $(D + D_{\text{stair}})\,T_{hs}$, $d\,T_{hs}$, $(d + D_{\text{stair}})\,T_{hs}$, $(D + d)T_{hs}$, $(D + d + D_{\text{stair}})\,T_{hs}$, and $T_s/2$ is given by (7) as shown at the bottom of the next page.

$$i_L(t) = \begin{cases} I_L(0) + \frac{n_t m V_{\text{LV}}}{L}[\frac{k}{2D_{\text{stair}}T_{hs}}t^2 + (1-k)t], & t \in [0, t_1] \\ I_L(D_{\text{stair}}T_{hs}) + \frac{n_t m V_{\text{LV}}}{L}(t - D_{\text{stair}}T_{hs}), & t \in [t_1, t_2] \\ I_L(dT_{hs}) + \frac{n_t m V_{\text{LV}}}{L}[\frac{k}{2D_{\text{stair}}T_{hs}}(t - dT_{hs})^2 + (1 - \frac{kd}{D_{\text{stair}}})(t - dT_{hs})], & t \in [t_2, t_3] \\ I_L(dT_{hs} + D_{\text{stair}}T_{hs}) + \frac{n_t m V_{\text{LV}}}{L}(k+1)(t - dT_{hs} - D_{\text{stair}}T_{hs}), & t \in [t_3, t_4] \\ I_L(DT_{hs}) + \frac{n_t m V_{\text{LV}}}{L}[-\frac{(t-DT_{hs})^2}{2D_{\text{stair}}T_{hs}} + (k + 1 + \frac{D}{D_{\text{stair}}})(t - DT_{hs})], & t \in [t_4, t_5] \\ I_L(DT_{hs} + D_{\text{stair}}T_{hs}) + \frac{n_t m V_{\text{LV}}}{L}k[t - (D + D_{\text{stair}})T_{hs}]\}, & t \in [t_5, t_6] \\ I_L(DT_{hs} + dT_{hs}) + \frac{n_t m V_{\text{LV}}}{L}\{-\frac{[t-(D+d)T_{hs}]^2}{2D_{\text{stair}}T_{hs}} + (k + \frac{D+d}{D_{\text{stair}}})[t - (D+d)T_{hs}]\}, & t \in [t_6, t_7] \\ I_L(DT_{hs} + dT_{hs} + D_{\text{stair}}T_{hs}) + \frac{n_t m V_{\text{LV}}}{L}(k-1)(t - (D + d + D_{\text{stair}})T_{hs}), & t \in [t_7, T_s/2] \end{cases} \quad (4)$$

$$\begin{cases} I_L(0) = \frac{n_t m V_{LV}\,T_{hs}}{2L}[(k-1)D_{\text{stair}} - 4D + (2k-2)d + 1 - k] \\ I_L(D_{\text{stair}}T_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[D_{\text{stair}} - 4D + (2k-2)d + 1 - k] \\ I_L(dT_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[-D_{\text{stair}} - 4D + 2kd + 1 - k] \\ I_L(dT_{hs} + D_{\text{stair}}T_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[(1+k)D_{\text{stair}} - 4D + 1 - k] \\ I_L(DT_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[-(1+k)D_{\text{stair}} + (2k-2)D - (2k+2)d + 1 - k] \\ I_L(DT_{hs} + D_{\text{stair}}T_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[kD_{\text{stair}} + 2kD - (2k+2)d + 1 - k] \\ I_L(DT_{hs} + dT_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[-kD_{\text{stair}} + 2kD - 2d + 1 - k] \\ I_L(DT_{hs} + dT_{hs} + D_{stair}T_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[(k-1)D_{\text{stair}} + (2k+2)D + 1 - k] \\ I_L(T_{hs}) = \frac{n_t m V_{\text{LV}}\,T_{hs}}{2L}[(1-k)D_{\text{stair}} + 4D + (2-2k)d + k - 1] \end{cases} \quad (5)$$

The average transferred power of MDCC can then be expressed as follows:

$$P = \frac{1}{T_{hs}} \int_0^{T_{hs}} v_a(t) \bullet i_L(t) dt. \tag{8}$$

Substituting (1)–(7) into (8), the transferred power of MDCC can be derived as

$$P = \begin{cases} \frac{V_{\mathrm{MV}}\, n_t\, m V_{\mathrm{LV}}}{2 f_s L} \\ \quad \times \left[2D(1-2D) - 2d^2 - \frac{D_{\mathrm{stair}}^2}{6}\right], & 0 \le d \le D \le 1 \\ \frac{V_{\mathrm{MV}}\, n_t\, m V_{\mathrm{LV}}}{2 f_s L} \\ \quad \times \left[2D(1-2d-D) - \frac{D_{\mathrm{stair}}^2}{6}\right], & 0 \le D \le d \le 1 \end{cases}. \tag{9}$$

The normalized transferred power under DPS based on QSW modulation can be described as

$$p = \frac{P}{P_N} = \begin{cases} 4\left[2D(1-2D) - 2d^2 - \frac{D_{\mathrm{stair}}^2}{6}\right], & 0 \le d \le D \le 1 \\ 4\left[2D(1-2d-D) - \frac{D_{\mathrm{stair}}^2}{6}\right], & 0 \le D \le d \le 1 \end{cases} \tag{10}$$

where P_N is the maximum transferred power with a conventional single-phase-shift (SPS) scheme and $P_N = V_{\mathrm{MV}}\, n_t\, m V_{\mathrm{LV}}/(8\, f_s\, L)$.

From (10), we conclude that the normalized transferred power can be regulated by the outer phase-shift angle D, the inner phase-shift angle d, and the voltage staircase duty ratio D_{stair}. Compared with the normalized transferred power under DPS with SW modulation, the expression of normalized transferred power under DPS with QSW modulation has a similar structure, and the only difference is the appearance of negative term $-D_{\mathrm{stair}}^2/6$, which is caused by the voltage staircase rising and falling process in QSW modulation. Apparently, the negative term $-D_{\mathrm{stair}}^2/6$ reduces the total transferred power and the dc voltage utilization in converter. The curves of normalized transferred power under the DPS based on QSW modulation are shown in Fig. 3. The figure shows that with different inner phase-shift angles in $0 \le d \le D \le 1$ and $0 \le D \le d \le 1$, the normalized transferred power decreases with the increase in voltage staircase ratio D_{stair}. Therefore, the voltage staircase ratio D_{stair} in QSW modulation should be a small value to solve the *dv/dt* problem and maintain the transferred power simultaneously.

B. Current Stress Characterization

Fig. 2 depicts that the HFL currents are symmetrical during a switching cycle. From (5) and (7), the current stress $I_{\max}$ in MDCC under the DPS scheme based on QSW modulation in both $0 \le d \le D \le 1$ and $0 \le D \le d \le 1$ situation can be described as

$$I_{\max} = \max\{|i_L(t)\}| = |i_L(T_{hs})| = \frac{n_t m V_{\mathrm{LV}}}{4 f_s L}[(1-k)D_{\mathrm{stair}} + 4D + (2-2k)d + k - 1]. \tag{11}$$

The normalized current stress $G_{\max}$ under the SPS and DPS control schemes can be derived as follows:

$$G_{\max} = \frac{I_{\max}}{I_N} = \begin{cases} 2[(1-k)D_{\mathrm{stair}} + 4D + (2-2k)d + k - 1], & \text{DPS} \\ 2[(1-k)D_{\mathrm{stair}} + 4D + k - 1], & \text{SPS} \end{cases} \tag{12}$$

where I_N is the current at maximum transmission power P_N under the SPS scheme and $I_N = P_N/V_{\mathrm{MV}} = n_t\, m V_{\mathrm{LV}}/8\, f_s\, L$.

$$i'_L(t) = \begin{cases} I'_L(0) + \frac{n_t m V_{\mathrm{LV}}}{L}\left[\frac{k}{2D_{\mathrm{stair}} T_{hs}} t^2 + (1-k)t\right], & t \in [0, t'_1] \\ I'_L(D_{\mathrm{stair}} T_{hs}) + \frac{n_t m V_{\mathrm{LV}}}{L}(t - D_{\mathrm{stair}} T_{hs}), & t \in [t'_1, t'_2] \\ I'_L(DT_{hs}) + \frac{n_t m V_{\mathrm{LV}}}{L}\left[-\frac{1}{2D_{\mathrm{stair}} T_{hs}}(t - DT_{hs})^2 + (1 + \frac{D}{D_{\mathrm{stair}}})(t - DT_{hs})\right], & t \in [t'_2, t'_3] \\ I'_L(DT_{hs} + D_{\mathrm{stair}} T_{hs}), & t \in [t'_3, t'_4] \\ I'_L(dT_{hs}) + \frac{n_t m V_{\mathrm{LV}}}{L}\left[\frac{k}{2D_{\mathrm{stair}} T_{hs}}(t - dT_{hs})^2 - \frac{kd}{D_{\mathrm{stair}}}(t - dT_{hs})\right], & t \in [t'_4, t'_5] \\ I'_L(dT_{hs} + D_{\mathrm{stair}} T_{hs}) + \frac{n_t m V_{\mathrm{LV}}}{L} k[t - (d + D_{\mathrm{stair}}) T_{hs}]\}, & t \in [t'_5, t'_6] \\ I'_L(dT_{hs} + DT_{hs}) + \frac{n_t m V_{\mathrm{LV}}}{L}\{-\frac{[t-(d+D)T_{hs}]^2}{2D_{\mathrm{stair}} T_{hs}} + (k + \frac{d+D}{D_{\mathrm{stair}}})[t - (d+D)T_{hs}]\}, & t \in [t'_6, t'_7] \\ I'_L(dT_{hs} + DT_{hs} + D_{\mathrm{stair}} T_{hs}) + \frac{n_t m V_{\mathrm{LV}}}{L}(k-1)[t - (d + D + D_{\mathrm{stair}}) T_{hs}], & t \in [t'_7, T_s/2] \end{cases} \tag{6}$$

$$\begin{cases} I'_L(0) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[(k-1)D_{\mathrm{stair}} - 4D + (2k-2)d + 1 - k] \\ I'_L(D_{\mathrm{stair}} T_{hs}) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[D_{\mathrm{stair}} - 4D + (2k-2)d + 1 - k] \\ I'_L(DT_{hs}) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[-D_{\mathrm{stair}} - 2D + (2k-2)d + 1 - k] \\ I'_L(dT_{hs}) = I'_L(DT_{hs} + D_{\mathrm{stair}} T_{hs}) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[(2k-2)d + 1 - k] \\ I'_L(dT_{hs} + D_{\mathrm{stair}} T_{hs}) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[kD_{\mathrm{stair}} - 2d - k + 1] \\ I'_L(dT_{hs} + DT_{hs}) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[-kD_{\mathrm{stair}} + 2kD - 2d - k + 1] \\ I'_L(dT_{hs} + DT_{hs} + D_{\mathrm{stair}} T_{hs}) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[(k-1)D_{\mathrm{stair}} + (2k+2)D - k + 1] \\ I'_L(T_{hs}) = \frac{n_t m V_{\mathrm{LV}} T_{hs}}{2L}[(1-k)D_{\mathrm{stair}} + 4D + (2-2k)d + k - 1] \end{cases} \tag{7}$$

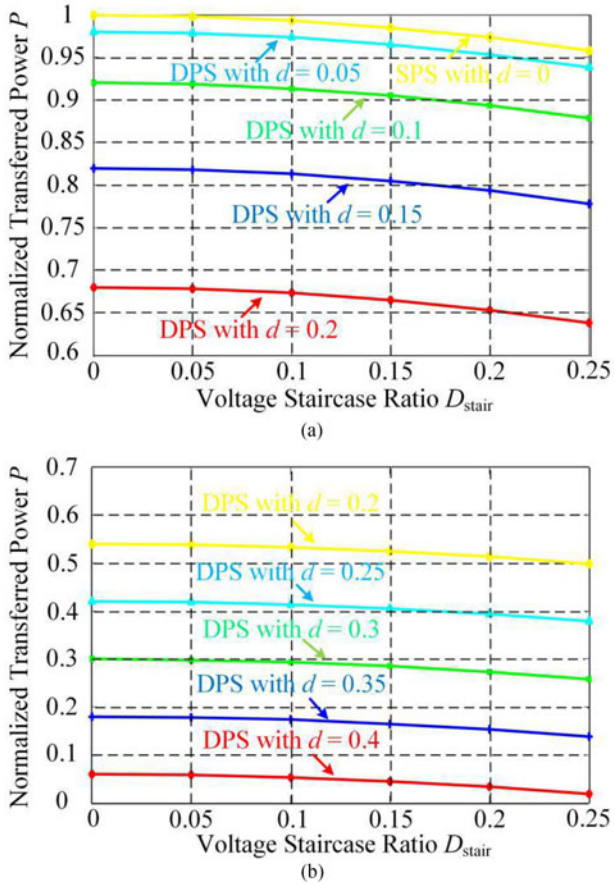

Fig. 3. Transferred power under DPS based on QSW modulation: (a) $0 \leq d \leq D \leq 1$ and (b) $0 \leq D \leq d \leq 1$.

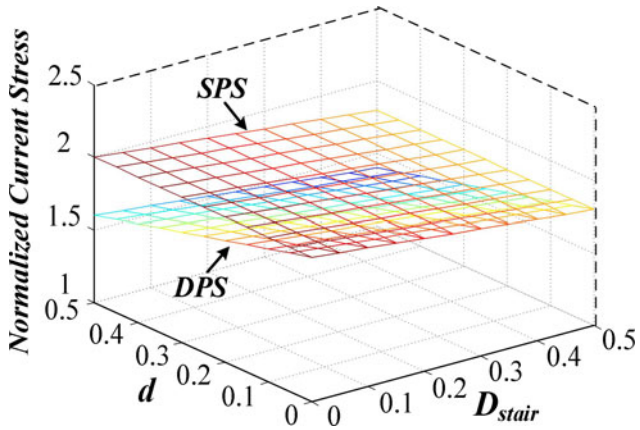

Fig. 4. Normalized current stress under SPS and DPS schemes based on QSW modulation.

From (12), the normalized current stress $G_{\max}$ can be regulated by the outer phase-shift angle D, the inner phase-shift angle d, and the voltage staircase ratio D_{stair}. The normalized current stress with varied inner phase-shift angles and voltage staircase ratios in QSW modulation is presented in Fig. 4. The figure demonstrates that the normalized current stresses under DPS are smaller than those under SPS, and the normalized current stress decreases with the increase in inner phase-shift angle d. Therefore, the DPS scheme is an effective method to

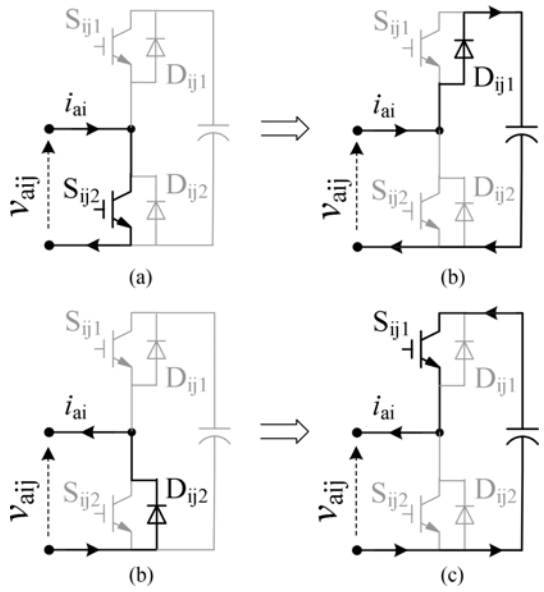

Fig. 5. Transition from bypass state to insert state for SMs on MVDC side: (a) $i_{ai} > 0$, bypassed state; (b) $i_{ai} > 0$, inserted state; (c) $i_{ai} < 0$, bypassed state; and (d) $i_{ai} < 0$, inserted state.

reduce current stress. Moreover, the normalized current stress also decreases with the increase of voltage staircase ratio D_{stair}. However, the effect of obtaining a small current stress by increasing voltage staircase ratio D_{stair} is less evident than that by increasing inner phase-shift angle d.

C. Soft-switching Characterization

In MDCC, soft-switching behavior is different between the SMs on the MVDC side and the full bridges on the LVDC side

1) Soft-Switching for SMs on the MVDC Side: Each SM on the MVDC side mainly has two switching behaviors: transiting from bypassed state to inserted state and transiting from inserted state to bypassed state, as shown in Figs. 5 and 6, respectively. The figures present that when the SM transits from bypass state to insert state, SM current i_{ai} should flow into SM to guarantee the zero-voltage turn on of S_{ij1} and zero-voltage turn off of S_{ij2}. When the SM transits from insert state to bypass state, the SM current i_{ai} should flow out the SM to guarantee the zero-voltage turn on of S_{ij2} and zero-voltage turn off of S_{ij1}.

The currents flowing through the SM in each arm of MMC are composed of the HFL current i_L and circulating current i_{cir}

$$\begin{cases} i_{a1} = i_{a4} = \frac{i_L}{2} + \frac{i_{\text{cir}}}{2} = \frac{i_L}{2} + \frac{P}{2V_{\text{MV}}} \\ i_{a2} = i_{a3} = -\frac{i_L}{2} + \frac{i_{cir}}{2} = -\frac{i_L}{2} + \frac{P}{2V_{\text{MV}}} \end{cases} \tag{13}$$

where P is the transfer power described in (9).

Fig. 2 and the previously presented analysis show that during the time interval $[0,\ dT_{hs} + D_{\text{stair}}T_{hs}]$, v_{a2} and v_{a3} are in voltage rising transition and the SMs in arms a_2 and a_3 transit from bypass state to insert state one by one. Meanwhile, v_{a1} and v_{a4} are in voltage falling transition and SMs in arms a_1 and a_4 transit from insert state to bypass state one by one. To realize ZVS for the switches in SMs, the arm currents i_{a1} and

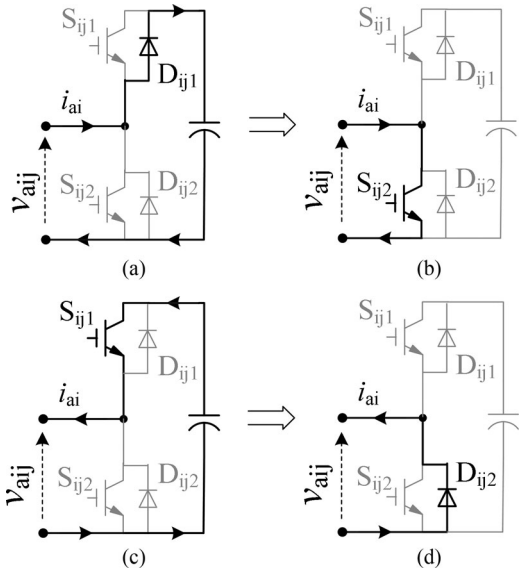

Fig. 6. Transition from insert state to bypass state for SMs on MVDC side: (a) $i_{\rm ai} > 0$, inserted state; (b) $i_{\rm ai} > 0$, bypassed state; (c) $i_{\rm ai} < 0$, inserted state; and (d) $i_{\rm ai} < 0$, bypassed state.

i_{a4} should flow out from SMs, and the arm currents i_{a2} and i_{a3} should flow into SMs. Besides, i_{a1} and i_{a4} increase, whereas $i_{\rm a2}$ and $i_{\rm a3}$ decrease during $[0,\ d{\rm T}_{hs} + D_{\rm stair}T_{hs}]$. Therefore, the following equations can be obtained to realize ZVS for the switches in SMs:

$$\begin{cases} I_{a1}(dT_{hs} + D_{\rm stair}T_{hs}) = I_{a4}(dT_{hs} + D_{\rm stair}T_{hs}) \\ \quad = \frac{I_L\,(dT_{hs}+D_{\rm stair}T_{hs})}{2} + \frac{P}{2V_{\rm MV}} \le 0 \\ I_{a2}(dT_{hs} + D_{\rm stair}T_{hs}) = I_{a3}(dT_{hs} + D_{\rm stair}T_{hs}) \\ \quad = -\frac{I_L\,(dT_{hs}+D_{\rm stair}T_{hs})}{2} + \frac{P}{2V_{\rm MV}} \ge 0. \end{cases} \tag{14}$$

Moreover, (14) can be the ZVS condition during $[{\rm T}_{hs},\ (1 + d + D_{\rm stair})T_{hs}]$ because of the symmetry of HFL voltage and current waveforms. Thus, substituting (5), (7), and (9) into (14), the ZVS condition for switches in SMs on MVDC side in a switching period can be expressed as

$$\begin{cases} d \ge \sqrt{-\frac{D_{\rm stair}^2}{12} + \frac{1+k}{4}D_{\rm stair} + 2D + \frac{k-1}{4}}, \quad 0 \le d \le D \le 1 \\ d \le \frac{1}{1-4D}\Big[-\frac{D_{\rm stair}^2}{6} - \frac{k}{2}D_{\rm stair} \\ \qquad\qquad + 2D(1-D) + \frac{k-1}{2}\Big], \quad 0 \le D \le d \le 1. \end{cases} \tag{15}$$

2) Soft-Switching for Full Bridges on the LVDC Side: Each full-bridge on the LVDC side mainly has two switching behaviors: transiting from $v_{bi} < 0$ state to $v_{bi} > 0$ state, and transiting from $v_{bi} > 0$ state to $v_{bi} < 0$ state, as shown in Figs. 7 and 8, respectively. It can be concluded from figures that, when full-bridge transits from $v_{bi} < 0$ to $v_{bi} > 0$ state, full-bridge current should be $i_{\rm bi} > 0$ to guarantee the zero-voltage turn on of S_{i1} and S_{i4}. When a full-bridge transits from $v_{bi} > 0$ to $v_{bi} < 0$ state, the full-bridge current should be $i_{bi} < 0$ to guarantee the zero-voltage turn on of S_{i2} and S_{i3}.

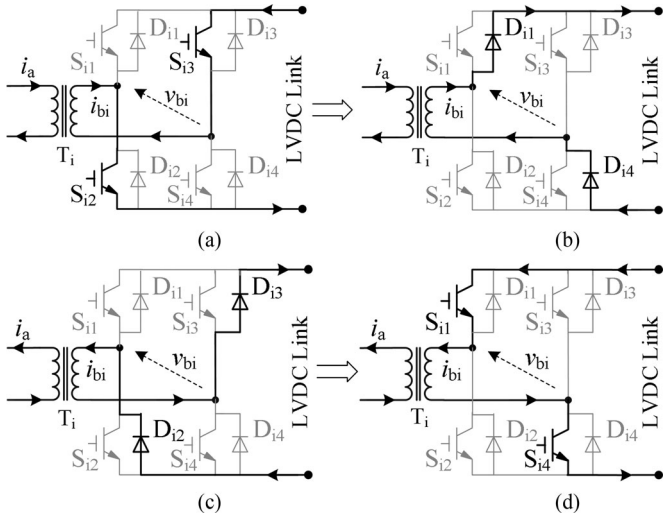

Fig. 7. Transition from $v_{\rm bi} < 0$ to $v_{\rm bi} > 0$ state for full bridges on LVDC side: (a) $i_{ai} > 0$, $v_{bi} < 0$, (b) $i_{ai} > 0$, $v_{bi} > 0$, (c) $i_{ai} < 0$, $v_{bi} < 0$, and (d) $i_{ai} < 0$, $v_{bi} > 0$.

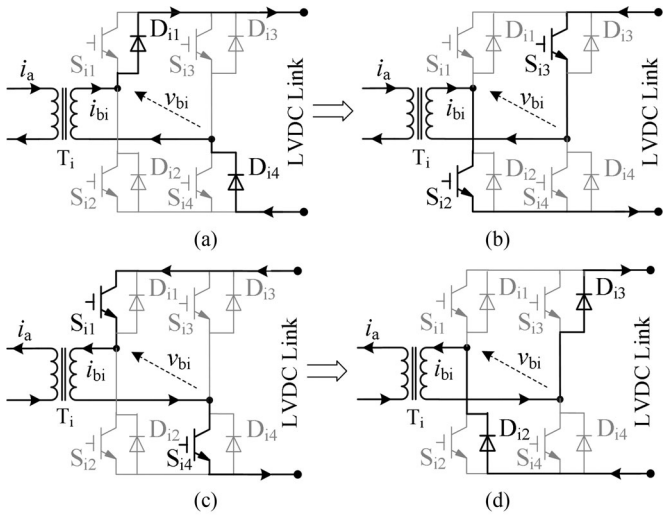

Fig. 8. Transition from $v_{bi} > 0$ to $v_{bi} < 0$ state for full bridges on the LVDC side: (a) $i_{bi} > 0$, $v_{bi} > 0$, (b) $i_{bi} > 0$, $v_{bi} < 0$, (c) $i_{bi} < 0$, $v_{bi} > 0$, and (d) $i_{bi} < 0$, $v_{bi} < 0$.

According to Fig. 2, the currents in full bridges are equal to the HFL current

$$i_{b1} = i_{b2} = i_{b3} = i_{b4} = i_L. \tag{16}$$

Fig. 2 also illustrates that the time intervals $[D{\rm T}_{hs},\ (D + d + D_{\rm stair})T_{hs}]$ and $[(1 + D)T_{hs},\ (1 + D + d + D_{\rm stair})T_{hs}]$ are the voltage rising and falling transitions of v_b, respectively. To realize ZVS for all the switches in full bridges, the current i_{bi} should be greater than 0 during $[D{\rm T}_{hs},\ (d + D + D_{\rm stair})T_{hs}]$ and less than 0 during $[(1 + D)T_{hs},\ (1 + d + D + D_{\rm stair})T_{hs}]$. Given the symmetry of HFL voltage and current waveforms, the following equations are obtained to realize ZVS for switches in full bridges:

$$I_L(DT_{hs}) \ge 0. \tag{17}$$

Substituting (5) and (7) into (17), the ZVS condition for switches in full bridges can be derived as

$$\begin{cases} -(1+k)D_{\rm stair}+(2k-2)D \\ \quad -(2k+2)d+1-k\geq 0, \quad 0\leq d\leq D\leq 1 \\ -D_{\rm stair}-2D+(2k-2)d \\ \quad +1-k\geq 0, \quad 0\leq D\leq d\leq 1. \end{cases} \tag{18}$$

Thus, the ZVS condition for switches in full bridges on the LVDC side in a switching period can be expressed as

$$\begin{cases} d\leq \frac{-(1+k)D_{\rm stair}+(2k-2)D+1-k}{2k+2}, & 0\leq d\leq D\leq 1 \\ d\geq \frac{D_{\rm stair}+2D+k-1}{2k-2}, & 0\leq D\leq d\leq 1. \end{cases} \tag{19}$$

3) Soft-Switching for All Switches in SMs and Full Bridges

From (15) and (19), the ZVS condition for all switches in SMs and full bridges in a switching period can be derived as

$$\begin{cases} \sqrt{-\frac{D_{\rm stair}^2}{12}+\frac{1+k}{4}D_{\rm stair}+2D+\frac{k-1}{4}} \\ \quad \leq d\leq \frac{-(1+k)D_{\rm stair}+(2k-2)D+1-k}{2k+2}, & 0\leq d\leq D\leq 1 \\ \frac{D_{\rm stair}+2D+k-1}{2k-2}\leq d\leq \frac{1}{1-4D} \\ \quad \left[-\frac{D_{\rm stair}^2}{6}-\frac{k}{2}D_{\rm stair}+2D(1-D)+\frac{k-1}{2}\right], & 0\leq D\leq d\leq 1. \end{cases} \tag{20}$$

From (20), the increase in the voltage staircase ratio $D_{\rm stair}$ reduces the range of adjustable inner phase-shift angle to achieve soft-switching for switches. Therefore, the voltage staircase ratio $D_{\rm stair}$ in QSW modulation should be a small value to avoid reducing the soft-switching range.

D. Power Loss Characterization

Similar to the HFL dc/dc converter, the power losses in MDCC are conduction loss $P_{\rm CON}$, switching loss $P_{\rm SW}$ and transformer and auxiliary inductor loss $P_{\rm TA}$. Thus, the total power loss $P_{\rm LOSS}$ in MDCC can be calculated as

$$P_{\rm LOSS}=P_{\rm CON}+P_{\rm SW}+P_{\rm TA}. \tag{21}$$

1) Conduction Loss: The switches and diodes are assumed to have the same voltage drop $V_{\rm CE}$. The *n* voltage drops will always occur in each arm because the arm current in MMC structure always flow through one switch or diode in each SM. In addition, the current on the LVDC side will always flow through 2*m* switches or diodes. Thus, the average conduction loss in one switching cycle can be divided into the conduction loss in SMs on the MVDC side calculated from the average value of arm currents and the conduction loss in full bridges on LVDC side calculated from the average value of HFL currents

$$\begin{aligned} P_{\rm CON}&=P_{\rm CON-SM}+P_{\rm CON-FB} \\ &=\frac{nV_{\rm CE}}{T_s}\left[\int_0^{T_s}i_{a1}dt+\int_0^{T_s}i_{a2}dt+\int_0^{T_s}i_{a3}dt\right. \\ &\quad \left.+\int_0^{T_s}i_{a4}dt\right]+\frac{2mV_{\rm CE}}{T_s}\int_0^{T_s}i_L dt. \end{aligned} \tag{22}$$

Substituting (13) and (16) into (22), the conduction loss of MDCC can be derived as

$$\begin{aligned} &P_{\rm CON-SM} \\ &=\begin{cases} \frac{nV_{\rm CE}n_t mV_{\rm LV}}{f_s L} \\ \left[2D(1-2D)-2d^2-\frac{D_{\rm stair}^2}{6}\right], & 0\leq d\leq D\leq 1 \\ \frac{nV_{\rm CE}n_t mV_{\rm LV}}{f_s L} \\ \left[2D(1-2d-D)-\frac{D_{\rm stair}^2}{6}\right], & 0\leq D\leq d\leq 1 \end{cases} \end{aligned} \tag{23}$$

$$\begin{aligned} &P_{\rm CON-FB} \\ &=\frac{mV_{\rm CE}n_t mV_{\rm LV}}{4f_s L}\left\{[(1-2d)+(k+2kd+8D-2)]+D_{\rm stair}\right. \\ &\quad \left.\times\left[\frac{2(1-k)}{3}D_{\rm stair}+(2-2k)d-4D+1-k\right]\right\} \\ &\quad 0\leq d\leq D\leq 1 \quad \text{and} \quad 0\leq D\leq d\leq 1. \end{aligned} \tag{24}$$

From (23) and (24), the normalized conduction losses in SMs $P_{\rm CON-SM}$ and full bridges $P_{\rm CON-FB}$ for MDCC with varied inner phase-shift angles and voltage staircase ratios under QSW modulation are shown in Figs. 9 and 10, respectively. The conduction losses in SMs and full bridges are normalized by $P_{\rm CON-SM}=nV_{\rm CE}\,n_{\rm t}\,mV_{\rm LV}/f_{\rm s}\,L$ and $P_{\rm CON-FB}=mV_{\rm CE}\,n_{\rm t}\,mV_{\rm LV}/4f_{\rm s}\,L$, respectively. The figures present that in both $0\leq d\leq D\leq 1$ and $0\leq D\leq d\leq 1$ situations, the normalized conduction losses in SMs and full bridges under DPS scheme are smaller than those under SPS scheme and decrease with the increase of inner phase shift d. The normalized conduction losses in SMs and full bridges also decrease with the increase in voltage staircase ratio $D_{\rm stair}$. However, compared with the reduction in normalized conduction loss obtained by increasing inner phase-shift angle *d*, the reduction in normalized conduction loss realized by increasing voltage staircase ratio $D_{\rm stair}$ is less evident, and the reduction obtained by increasing voltage staircase ratio is more evident on the conduction loss in full bridges than that in SMs.

2) Switching Loss: As discussed in the extant literature, the switching loss is smaller than the conduction loss and the transformer and auxiliary inductor loss. The switching loss is generally approximately one-fourth of conduction loss. However, the switching loss can be reduced effectively by reducing the switching frequency or using the silicon carbide devices. Moreover, a very small switching loss exists when the soft-switching behavior is achieved. In that case, the switching loss makes up a small percentage of the total power loss in dc/dc converter, and it can be neglected in the simple power loss model [33]. Therefore, the switching loss is neglected in power loss to simplify the analysis and calculation in this paper.

3) Transformer and Auxiliary Inductor Loss: The power loss in the transformer and auxiliary inductor can be divided into copper loss $P_{\rm COPP}$ and core loss $P_{\rm CORE}$. The HFL inductor current always flows through the auxiliary inductor and the transformer in the entire switching cycle. The winding resistances of the transformer and auxiliary inductor are assumed as

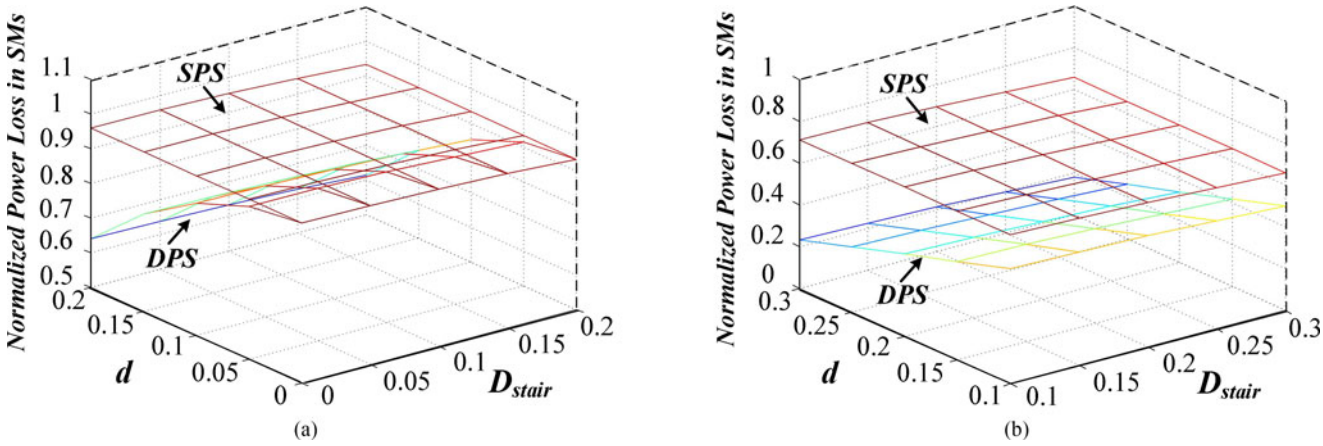

Fig. 9. Normalized conducting loss in SMs under QSW modulation: (a) $0 \le d \le D \le 1$ and (b) $0 \le D \le d \le 1$.

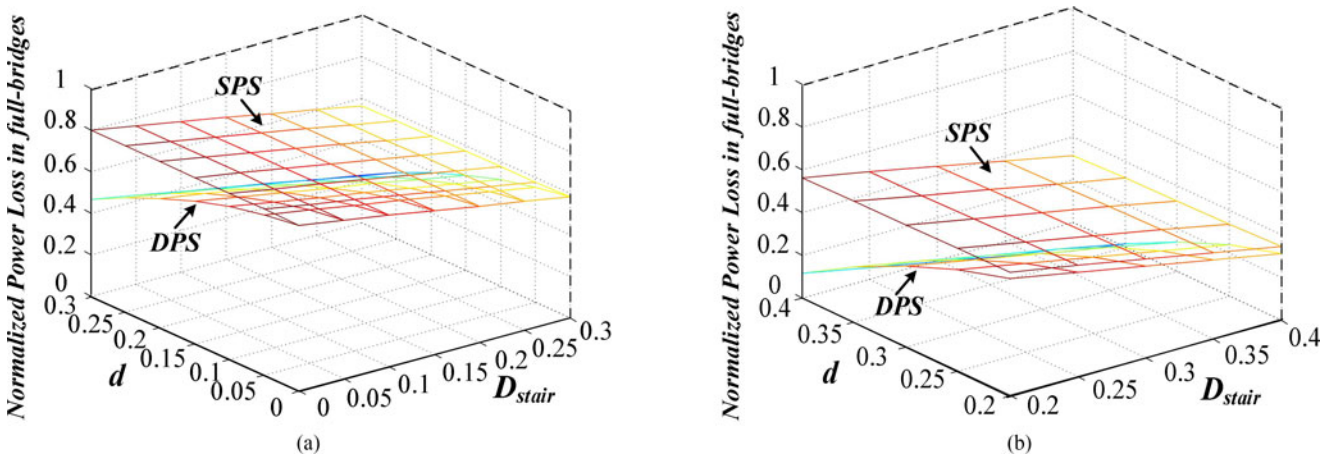

Fig. 10. Normalized conducting loss in full bridges under QSW modulation: (a) $0 \le d \le D \le 1$ and (b) $0 \le D \le d \le 1$.

constants, and the copper loss P_{COPP} can be calculated from the root-mean-square (rms) value of the HFL inductor current $I_{L-\mathrm{rms}}$. To simplify the calculation of core loss, a sinusoidal current with the rms value of HFL current $I_{L-\mathrm{rms}}$ is assumed to be responsible for the core loss P_{CORE} in the transformer and auxiliary inductor. The loss P_{TA} in the transformer and auxiliary inductor can be calculated as

$$\begin{aligned} P_{\mathrm{TA}} &= P_{\mathrm{COPP}} + P_{\mathrm{CORE}} \\ &= \left(R_{tr} + R_{au} + \frac{2cf_s\mu_0^2N^2V_e}{g^2}\right) I_{L-\mathrm{rms}}^2 \end{aligned} \tag{25}$$

where R_{tr} and R_{au} are the winding resistances of the transformer and auxiliary inductor, respectively. Besides, c is the coefficient, μ_0 is the permeability of vacuum, g is the air gap, N is the turn number, V_e is the effective volume, and the rms value $I_{L-\mathrm{rms}}$ can be derived as

$$I_{L-\mathrm{rms}} = \sqrt{\frac{1}{T_{hs}}\int_0^{T_{hs}} (i_L(t))^2 dt}. \tag{26}$$

Substituting (13) and (15) into (26), the normalized transformer and the auxiliary inductor loss of MDCC can be obtained

$$P_{\mathrm{TA}} = \begin{cases} (k-1)^2(1+2d)(1-d)^2 - 4kD^2 \\ \quad \times (3d+D-3) + 4k(d-D)^3 \\ \quad + D_{\mathrm{stair}}^2\left[\frac{2(1-k)}{3}D_{\mathrm{stair}} + (2\right. \\ \quad \left. -2k)d - 4D + 1 - k\right]^2, & 0 \le d \le D \le 1 \\ (k-1)^2(1+2d)(1-d)^2 \\ \quad - 4kD^2(3d+D-3) \\ \quad + D_{\mathrm{stair}}^2\left[\frac{2(1-k)}{3}D_{\mathrm{stair}} + (2\right. \\ \quad \left. -2k)d - 4D + 1 - k\right]^2, & 0 \le D \le d \le 1. \end{cases} \tag{27}$$

From (27), the normalized transformer and auxiliary inductor loss P_{TA} with varied inner phase-shift angles and staircase voltage ratios are presented in Fig. 11. In both $0 \le d \le D \le 1$ and $0 \le D \le d \le 1$ conditions, the normalized transformer and auxiliary inductor loss under DPS scheme are smaller than that under SPS scheme and decreases with the increase of inner

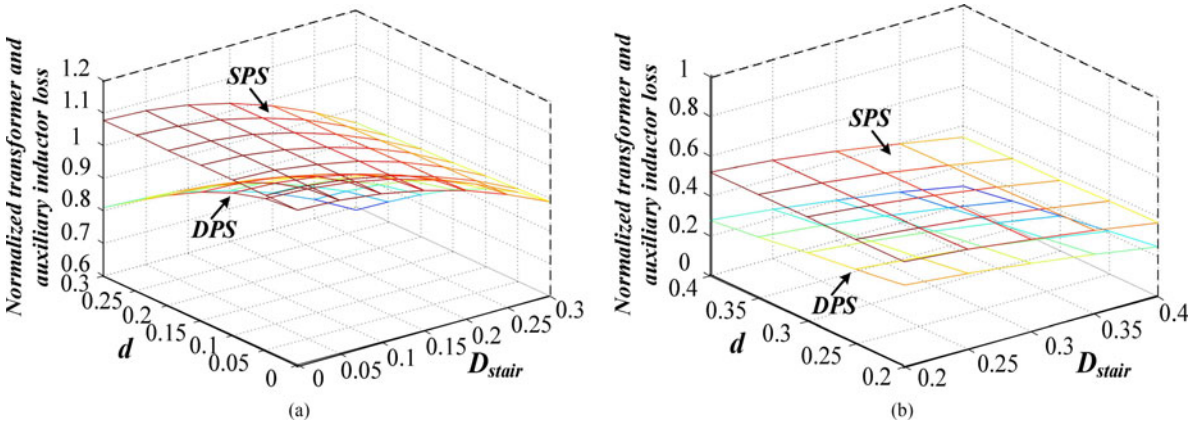

Fig. 11. Normalized transformer and auxiliary inductor loss under QSW modulation: (a) $0 \le d \le D \le 1$ and (b) $0 \le D \le d \le 1$.

phase-shift d. Moreover, the normalized transformer and auxiliary inductor loss also decreases with the increase of voltage staircase ratio $D_{\rm stair}$.

4) Overall Power Loss: According to the earlier analysis, since the switching loss is neglected in simple power loss model in this paper, the conduction loss and the normalized transformer and auxiliary inductor loss account for approximately two-thirds and one-third of the overall power loss in MDCC, respectively. The normalized overall power loss $P_{\rm LOSS}$ in MDCC with varied inner phase-shift angles and staircase voltage ratios is presented in Fig. 12. In both $0 \le d \le D \le 1$ and $0 \le D \le d \le 1$ conditions, the overall power loss under DPS scheme is smaller than that under SPS scheme and decreases with the increase of inner phase shift d. The overall power loss also decreases with the increase of voltage staircase ratio $D_{\rm stair}$.

III. Multiobjective Optimized Modulation Strategy

According to the preceding analysis, power characteristic, current stress, soft-switching and efficiency characteristic of MDCC can be optimized by DPS scheme based on QSW modulation. To obtain the optimization for power characteristic, current stress and efficiency characteristic simultaneously, an optimized DPS scheme based on QSW modulation is proposed.

From (12), to achieve the minimum value of normalized current stress, a Lagrangian objective function and its constraints for minimum value solution are derived as

$$\begin{cases} L(d,D,\lambda) = G_{\max}(d,D) + \lambda(P(d,D) - P_{0N}) \\ \frac{dL}{dd} = 0, \frac{dL}{dD} = 0, \frac{dL}{dD_{\rm stair}} = 0, \frac{dL}{d\lambda} = 0 \end{cases} \tag{28}$$

where λ is the function coefficient and P_{0N} is the specified normalized transmit power for MDCC.

Substituting (10) and (12) into (28), the constraint solutions when $0 \le d \le D \le 1$ and $0 \le D \le d \le 1$ can be derived as (29) as shown at the bottom of this page.

Similarly, from (22) and (25), to achieve the minimum value of normalized power loss, a Lagrangian objective function and its constraints for minimum value solution are derived as

$$\begin{cases} L(d,D,\lambda) = P_{\rm Loss}(d,D) + \lambda(P(d,D) - P_0) \\ \frac{dL}{dD_1} = 0, \quad \frac{dL}{dD} = 0, \quad \frac{dL}{dD_{\rm stair}} = 0, \quad \frac{dL}{d\lambda} = 0 \end{cases}. \tag{30}$$

$$\begin{cases} L = 2[(1-k)D_{\rm stair} + 4D + (2-2k)d + k - 1] + \lambda(4[2D(1-2D) - 2d^2 - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N}) \\ \frac{dL}{dd} = (1-k) - 4\lambda d = 0 \ \frac{dL}{dD} = 1 + \lambda(1-4D) = 0 \ 0 \le d \le D \le 1 \\ \frac{dL}{dD_{\rm stair}} = (1-k) - \frac{2}{3}\lambda D_{\rm stair} = 0 \ \frac{dL}{d\lambda} = 4[2D(1-2D) - 2d^2 - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N} = 0 \end{cases}$$

$$\begin{cases} L = 2[(1-k)D_{\rm stair} + 4D + (2-2k)d + k - 1] + \lambda(4[2D(1-2d-D) - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N}) \\ \frac{dL}{dd} = (1-k) - 4\lambda D = 0 \ \frac{dL}{dD} = 1 + \lambda(1-2D) = 0 \ 0 \le D \le d \le 1 \\ \frac{dL}{dD_{\rm stair}} = (1-k) - \frac{2}{3}\lambda D_{\rm stair} = 0 \ \frac{dL}{d\lambda} = 4[2D(1-2d-D) - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N} = 0 \end{cases} \tag{29}$$

$$\begin{cases} L = [(1-2d) + (k + 2kd + 8D - 2) + \frac{4(1-k)}{3}D_{\rm stair}^2] + \lambda(4[2D(1-2D) - 2d^2 - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N}) \\ \frac{dL}{dd} = (1-k) - 8d\lambda = 0 \ \frac{dL}{dD} = 1 + \lambda(1-4D) = 0 \ 0 \le d \le D \le 1 \\ \frac{dL}{dD_{\rm stair}} = (1-k) - \lambda D_{\rm stair} = 0 \ \frac{dL}{d\lambda} = 4[2D(1-2D) - 2d^2 - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N} = 0 \end{cases}$$

$$\begin{cases} L = [(1-2d) + (k + 2kd + 8D - 2) + \frac{4(1-k)}{3}D_{\rm stair}^2] + \lambda(4[2D(1-2d-D) - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N}) \\ \frac{dL}{dd} = (1-k) - 8\lambda D = 0 \ \frac{dL}{dD} = 1 + \lambda(1-2D) = 0 \ 0 \le D \le d \le 1 \\ \frac{dL}{dD_{\rm stair}} = (1-k) - \lambda D_{\rm stair} = 0 \ \frac{dL}{d\lambda} = 4[2D(1-2d-D) - \frac{D_{\rm stair}^2}{6}] - P_{0\rm N} = 0 \end{cases} \tag{31}$$

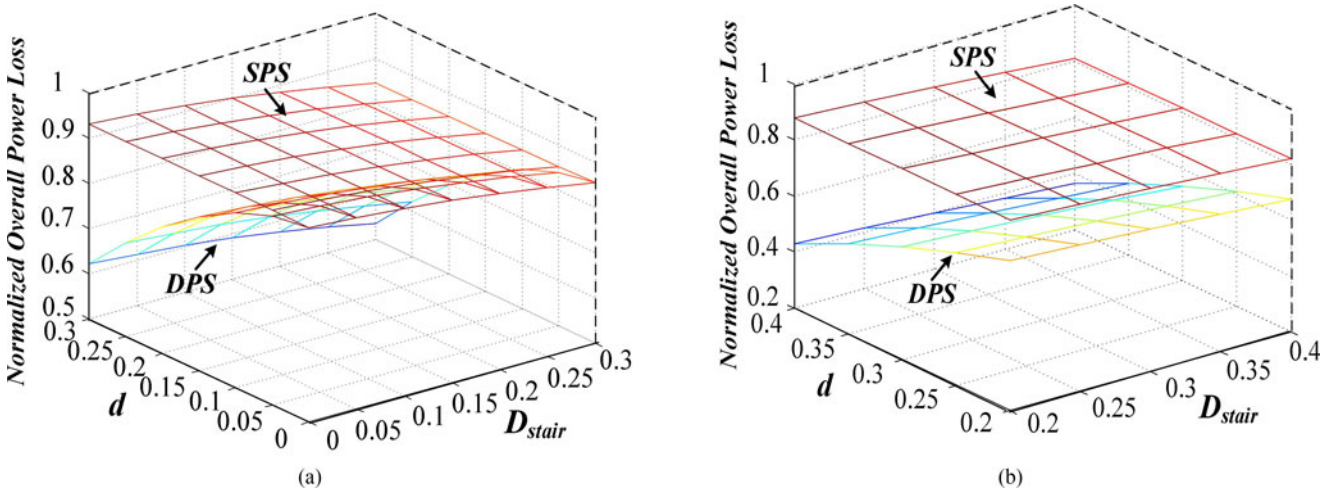

Fig. 12. Normalized overall power loss under QSW modulation: (a) $0 \le d \le D \le 1$ and (b) $0 \le D \le d \le 1$.

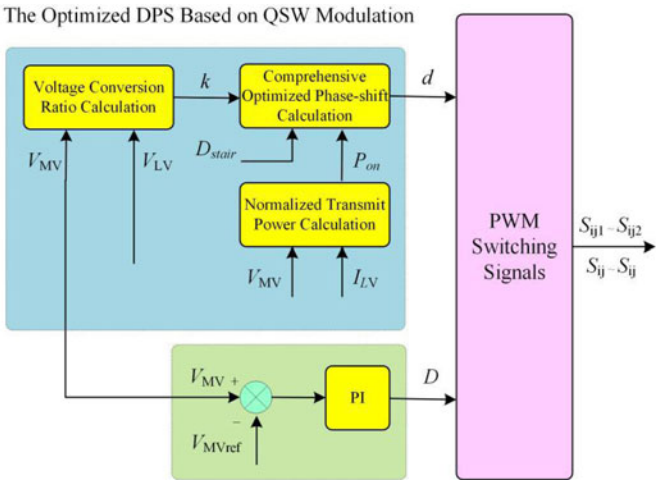

Fig. 13. Optimized modulation scheme for MDCC based on DPS strategy.

Substituting (23), (24), and (27) into (30), the constraint solutions when $0 \le d \le D \le 1$ and $0 \le D \le d \le 1$ can be obtained as (31) shown at the bottom of the previous page.

The common solution for (28) and (30) can then be obtained as follows:

$$d = \begin{cases} \sqrt{D(1-2D) - \frac{D_{\text{stair}}^2}{12} - \frac{P_{0N}}{8}}, & 0 \le d \le D \le 1 \\ 1 - D + \frac{1}{4D}\left(\frac{P_{0N}}{2} + \frac{D_{\text{stair}}^2}{3}\right), & 0 \le D \le d \le 1. \end{cases} \tag{32}$$

With normalized transmission power P_{on}, staircase voltage ratio D_{stair} and outer phase-shift D, the optimized inner phase-shift angle d can be obtained according to (32). With the optimized inner phase-shift angle d, the minimum value of current stress and the minimum value of power loss in MDCC can be obtained simultaneously, and the multiobjective optimized DPS strategy based on QSW modulation can be achieved.

The control block of optimized DPS scheme based on QSW modulation is shown in Fig. 13. In the scheme, the outer phase-shift D is regulated by a proportional–integral (PI) controller to control the required voltage or power transferred by converter, and the inner phase shift d is calculated according to an optimized model. The proposed strategy optimizes the current stress and power loss characteristics simultaneously, thereby improving MDCC efficiency.

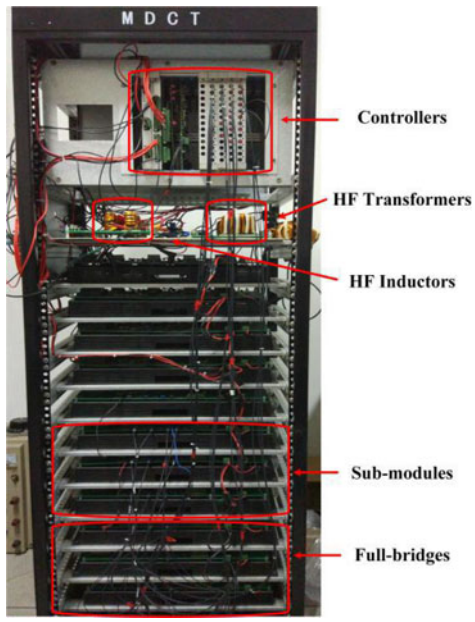

Fig. 14. MDCC prototype in laboratory.

IV. Experimental Verification

To verify the theoretical analysis and the proposed optimal modulation strategy, a MDCC prototype is constructed in laboratory, as shown in Fig. 14. The main parameters of experiment are: the MVDC and LVDC voltages are $V_{\text{MV}} = 310\,\text{V}$ and $V_{\text{LV}} = 110 - 150\,\text{V}$, respectively, the transformer ratio is $n_t = 4:5$, the numbers of SMs and full bridges are $n = m = 3$, the arm inductor is $L_{\text{s}} = 30\,\mu\text{H}$, the dc-link capacitance is $C_{\text{dc}} = 450\,\mu\text{F}$, and the switching frequency is $f_s = 20\,\text{kHz}$.

The steady-state voltage and current waveforms on the MVDC and LVDC sides with the proposed strategy are shown in Fig. 15. The LVDC voltage V_{LV} is 125 V, and the MVDC

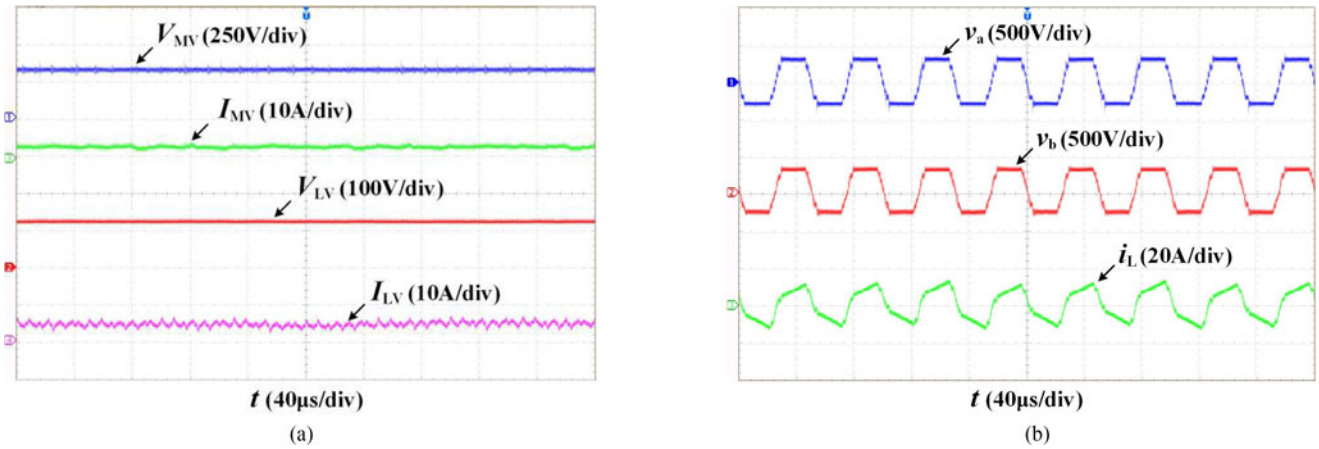

Fig. 15. Steady-state voltages and currents of MDCC with proposed DPS strategy. (a) Voltages and currents on the MVDC and LVDC side. (b) HFL voltages and current.

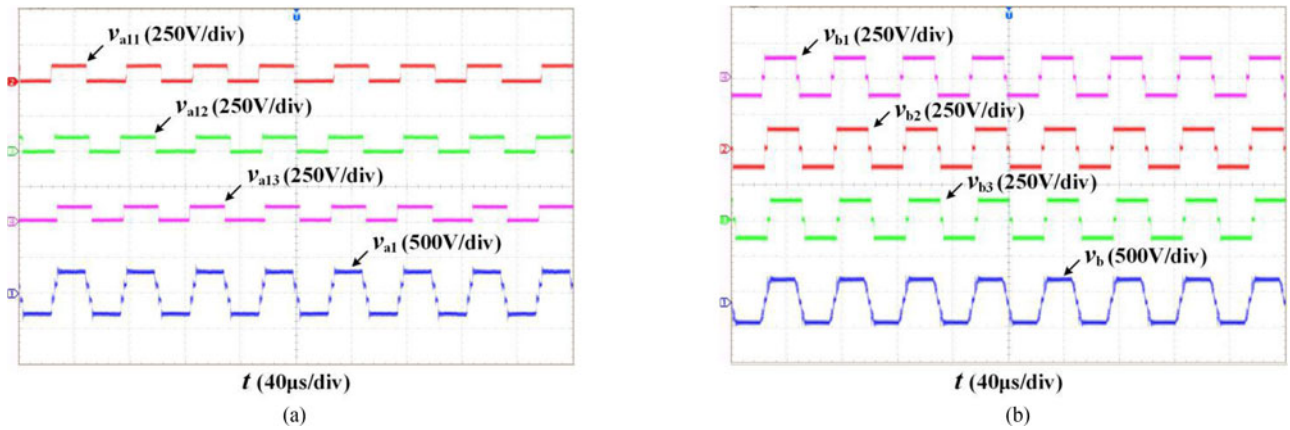

Fig. 16. Voltage waveforms of SMs on the MVDC and full bridges on the LVDC side with QSW modulation: (a) SMs on the MVDC side and (b) full bridges on the LVDC side.

voltage V_{MV} is controlled at the preset 310 V. The HFL voltages v_a and v_b are quasi-square waveforms, and the frequencies of HFL voltages v_a and v_b and current i_L are all 20 kHz.

The voltages of SMs on the MVDC side and full bridges on the LVDC side are shown in Fig. 16. According to Fig. 16(a), the SMs in one arm of MMC structure produce square voltages v_{a11}, v_{a12}, and v_{a13} with equivalent amplitude. The positive and negative voltages of square voltage are V_{dc} and 0, respectively, and the voltage waveforms vary alternately. The phase-shift angle exists between adjacent SM square voltages and forms the staircase rising and falling process in arm voltage v_{a1}. Similarly, each full-bridge produces square voltages v_{b1}, v_{b2}, and v_{b3}, with the inner phase-shift angle and voltage waveforms varying alternately, and the phase-shift angle also exists between adjacent full-bridge voltages. The voltage levels of full-bridge voltages are $-V_{\mathrm{dc}}$, 0 and V_{dc}, and full-bridge voltages directly compose the HFL multilevel quasi-square voltage v_b on the LVDC side, as shown in Fig. 16(b). The results indicate that, with the modulation strategy, the SMs and full bridges on each side operate in balance, and MDCC achieves the voltage conversion and power transmission accurately.

The steady-state HFL voltage and current waveforms under DPS scheme with different voltage staircase ratios D_{stair} in QSW modulation are shown in Fig. 17. The figure shows that under DPS scheme with same inner phase-shift angle, the current stress is reduced by increasing the voltage staircase ratio D_{stair} in QSW modulation. Especially, when the voltage staircase ratio increases to $D_{\mathrm{stair}} = 1$, the HFL voltage turns into the staircase wave modulation, as shown in Fig. 17(c), and current stress achieves the lowest value. The results also indicate that the current stress under staircase wave modulation is smaller than that under QSW modulation.

The steady-state HFL voltage and current waveforms under SPS scheme, DPS scheme and proposed optimized DPS strategy are shown in Fig. 18. With the same voltage staircase ratio, the current stress under the DPS scheme is smaller than that under the SPS scheme, which indicates that current stressis optimized by applying DPS scheme. The current stress under the proposed optimized DPS strategy is smaller than that under conventional DPS strategy; thus, the current stress can be further optimized under the proposed DPS strategy with QSW modulation.

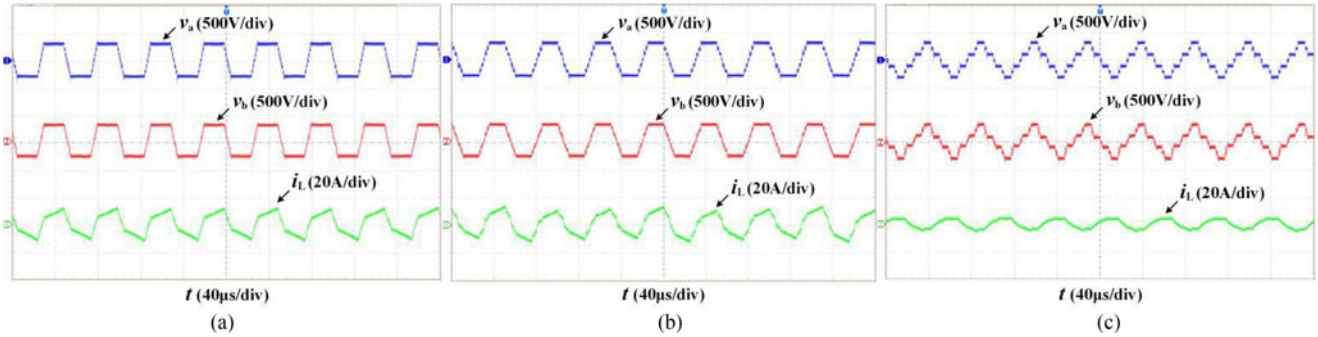

Fig. 17. Steady-state waveforms of v_a, v_b, and i_L under DPS strategy based on QSW modulation with different voltage staircase ratio $D_{\rm stair}$: (a) with voltage staircase ratio $D_{\rm stair} = 0.1$, (b) with voltage staircase ratio $D_{\rm stair} = 0.2$, and (c) with voltage staircase ratio $D_{\rm stair} = 1$.

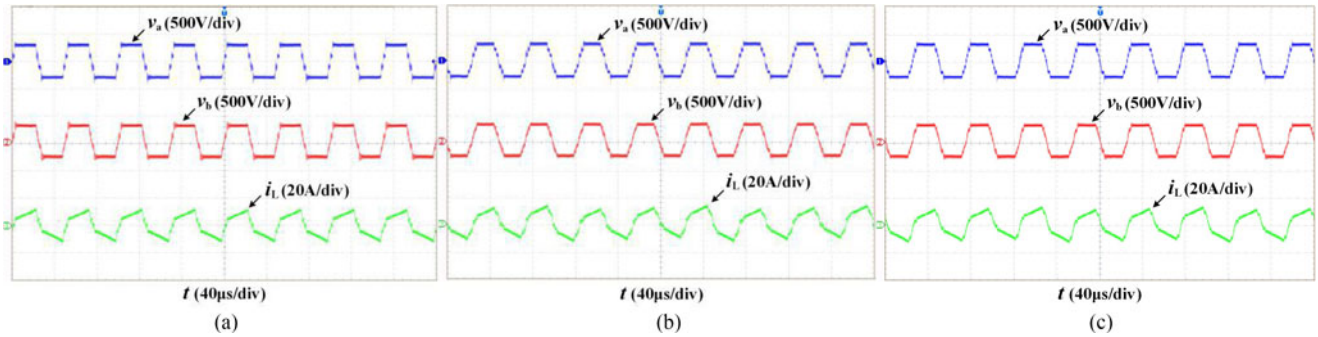

Fig. 18. Steady-state waveforms of v_a, v_b, and i_L under SPS, DPS, and proposed optimized DPS strategy based on QSW modulation: (a) SPS with $d = 0$, (b) conventional DPS with $d = 0.15$, (c) the proposed DPS with optimized $d = 0.12$.

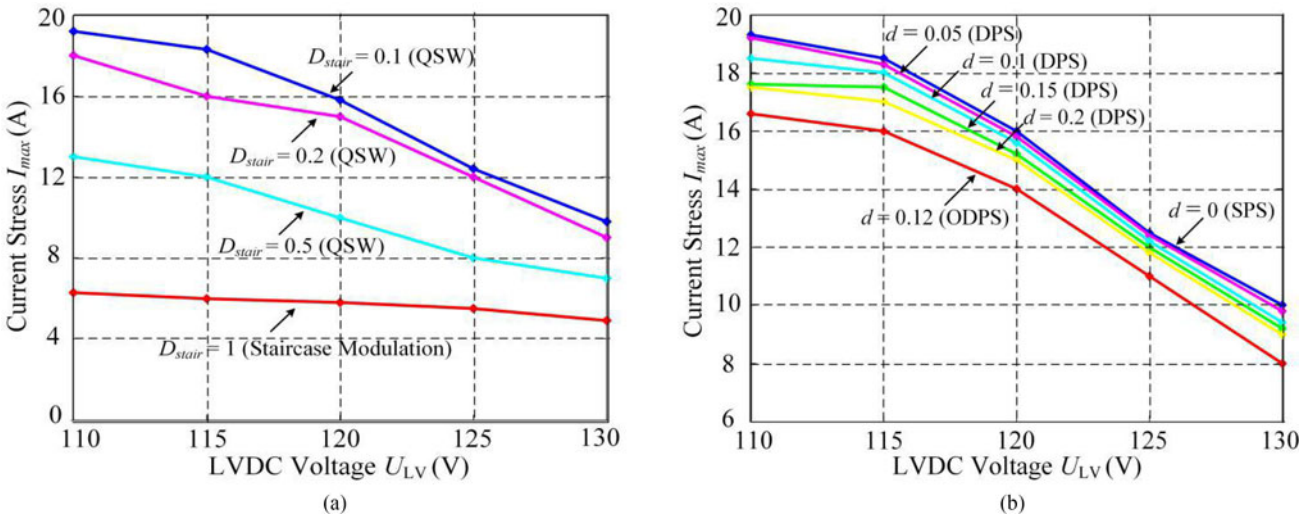

Fig. 19. Experimental current stress values with varied LVDC voltage $U_{\rm LV}$ under the SPS, DPS, and proposed DPS strategy based on QSW modulation: (a) with different staircase transition angle $D_{\rm stair}$ and (b) with different inner phase-shift angle d.

For further verification, the experimental current stress values with varied LVDC voltages, different staircase transition angle and inner phase-shift angle are presented in Fig. 19. The results in Fig. 19(a) indicate that the current stress decreases with the increase of staircase transition angle $D_{\rm stair}$. When the voltage staircase ratio increases to $D_{\rm stair} = 1$, the HFL voltage becomes staircase wave modulation, and the current stress achieves the lowest value. The results in Fig. 19(b) imply that the current stress reduces with the increase of inner phase-shift angle d. Compared with conventional DPS strategy, the proposed optimized DPS strategy generates the smallest current stress across the entire range.

With the same transfer power, the experimental values of MDCC power loss and efficiency with varied LVDC voltages

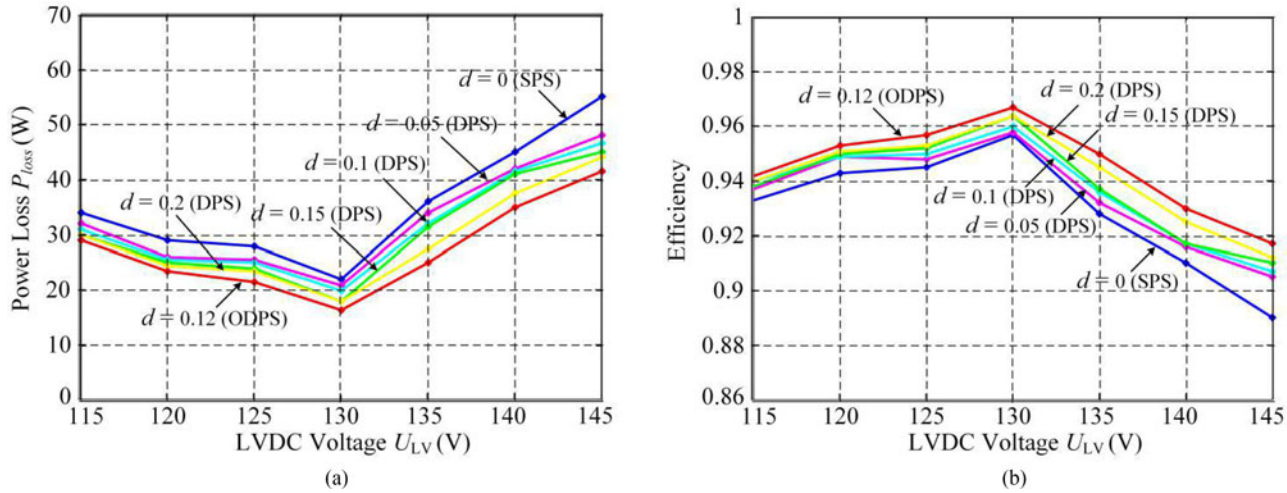

Fig. 20. Experimental power loss and efficiencies of MDCC with varied LVDC voltage U_{LV} under varied inner phase-shift angle d based on QSW modulation: (a) power loss and (b) efficiencies.

under the SPS, DPS and proposed DPS strategy are shown in Fig. 20. When the LVDC voltage $V_{\mathrm{LV}} = 130$ V, which indicates that the voltage conversion ratio $M = 1$, the MDCC achieves the lowest power loss and highest efficiency. Once the LVDC voltage V_{LV} changes and the voltage conversion ratio $M \neq 1$, the power loss becomes larger and the efficiency declines consequently. The power loss in MDCC with DPS scheme is smaller than that with SPS scheme, and a higher efficiency is also achieved. In addition, the lower power loss along with higher efficiency can be obtained when the inner phase-shift d increases. Moreover, with the proposed optimized DPS strategy, the lowest power loss and highest efficiency of MDCC can be achieved across the entire range.

The previously presented experimental results present that the inner phase-shift angle d and staircase transition angle D_{stair} in QSW modulation both affect the transferred power, current stress and power loss in MDCC, thereby affecting the converter efficiency. With the proposed optimized DPS strategy based on QSW modulation, the SMs and full bridges on each side operate in balance, and MDCC realizes the voltage conversion and power transmission accurately. Compared with the SPS and conventional DPS, the proposed DPS strategy based on QSW modulation reduces the current stress and power loss simultaneously, and the higher efficiency of MDCC can be achieved.

V. Conclusion

In this paper, the QSW modulation is applied in MDCC and the mathematical model of QSW modulation with DPS scheme is established. Other HFL phase-shift scheme such as SPS, EPS, and TPS under QSW modulation can be analyzed similarly based on the derived mathematical model, thereby facilitating further analysis in HFL characteristics and optimization of modular multilevel dc/dc converter. The influences of DPS scheme under QSW modulation on MDCC performance including the power characteristic, current stress, switching characteristic, and efficiency characteristic are investigated based on this model, which provides a practical reference for the design and application of QSW modulation. The following conclusions are obtained through the analysis and experimental verification. With the increase in voltage staircase ratio in QSW modulation, the transferred power decreases, and the range of adjustable inner phase-shift angle to achieve soft-switching for switches are also reduced. Therefore, the voltage staircase ratio in QSW modulation should be small. The current stress and power loss under DPS are smaller than those under SPS and decreases with the increase in inner phase shift. Therefore, the DPS scheme is an effective method to reduce the current stress and power loss. With the increase in voltage staircase ratio in QSW modulation, the current stress and the power loss also decrease. These conclusions have a reference value on the application of DPS scheme under QSW modulation in MDCC and other converters such as M2DC, DAB based dc/dc converter, etc. Besides, a multiobjective optimized DPS strategy based on QSW modulation is proposed in this paper. The transferred power, current stress and power loss can be optimized simultaneously by achieving the optimized inner phase-shift angle in DPS scheme, thereby improving the efficiency and extending the applicability of MDCC and other dc/dc converters. The proposed concept and strategy can also be applied in other modular multilevel dc/dc converters.

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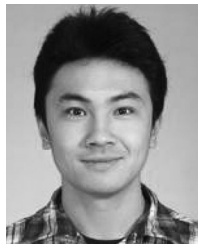

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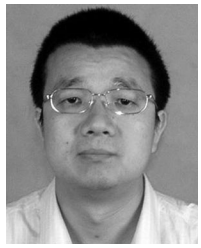
His current research interests include high-frequency dc–dc converters and flexible dc transmission and distribution systems.



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