Parallel of Two Unidirectional AC–DC–AC Three-Leg Converters to Improve Power Quality

Nady Rocha, *Member, IEEE*, André Elias Lucena da Costa, and Cursino Brandão Jacobina, *Fellow, IEEE*

***Abstract*—A unidirectional single-phase ac–dc–ac converter is proposed and analyzed in this paper. It is composed of paralleled rectifiers and inverters sharing two legs with two dc-link capacitor voltages. Models and a control strategy of the systems including circulating currents are developed. Compared to the conventional four-leg and three-leg (4L and 3L) single-phase ac–dc–ac converters, the proposed topology allows the decreasing of the current and power ratings of the power switches, the harmonic distortion, and semiconductors power losses. And compared to the unidirectional three-leg ac–dc–ac converter, it allows us to decrease the current and power ratings of the power switches and the harmonic distortion. In addition, a modified interleaved pulse width modulation (PWM) strategy using four-carrier PWM is presented, ensuring five-level voltage at the input and output sides of the converter. Simulation and experimental results are also presented to demonstrate the viability of the proposed circuit.**

***Index Terms*—AC–DC–AC converter, circulating current, single-phase converter, unidirectional converter.**

I. Introduction

IN ORDER to reduce the cost of the converter, topologies in which the front-end rectifier is half-controlled has been proposed in the technical literature. These converters replace controlled switches with uncontrolled switches, for instance, insulated gate bipolar transistor (IGBT) by diodes. Half-controlled or semicontrolled rectifiers may be used for dc-motor drives, dc-power supplies, for generating the dc-link of inverters, in telecommunications, aerospace, industrial, commercial, and military applications [1]–[7]. In the last decade the interest of half-controlled rectifiers have been increased for applications in wind generation systems and battery charging for plug-in hybrid electric vehicles [8]–[13]. The main features of the topologies with semicontrolled rectifier are as follows:

1) cheaper switches and less amount of gate drives, lower cost of the converter when compared to full controlled rectifier;
2) reduction in switching losses, resulting in more efficient converters when compared to the full controlled rectifier;
3) high power density and low conduction losses when compared with boost rectifier converter;
4) a better performance and dc-link voltage control when compared to a diode rectifier;
5) the front-end rectifiers are unidirectional.

In some applications, the grid and load belong to the single-phase type, such as universal active power filters and uninterruptible power supplies (UPS) that can be built from single-phase ac–dc–ac converters. In this case, it is possible to utilize single-phase ac–dc–ac full-bridge topology with four legs as shown in Fig. 1(a) [14], [15]. Other interesting single-phase to single-phase topology is based on a three-leg converter, in which one of the legs is shared between grid and load sides, as illustrated in Fig. 1(b) [16]–[18].

A unidirectional single-phase ac–dc–ac component minimized converter was discussed in [19]. It is composed of one unidirectional rectifier and one bidirectional inverter, using only four controlled switches, as shown in Fig. 1(c). Compared to a three-leg converter (3L converter) and a four-leg converter (4L converter), the unidirectional three-leg converter (denominated here as 3L2D converter) is more efficient and cheaper. Its weakness is the increase in harmonic distortion. In [20], three unidirectional 3L2D converters are combined in series to three-phase application. This converter ensures reduction in harmonic distortion in the grid currents and load voltages, due to multilevel voltage in input and output of the converter. While in [21] proposes a single-phase ac–dc–ac converter composed of two unidirectional 3L2D converters connected in series, reducing the voltage on the switches and the harmonic distortion. A bridgeless three-level rectifier, with a diode leg and a neutral-point clamped leg, was proposed in [22]. This rectifier reduces the power losses and harmonic distortion in the grid currents.

A common solution to improve the reliability and high-quality power source is to adopt the use of parallel converters with interleaved technique, the parallel converters not only satisfy the two initial requirements, but also reduce converter power losses and the size and loss of the inductor filter without increasing the harmonic content [23], [24]. Several novel topologies and control strategies have been presented to improve the performance of parallel converters [25]–[47]. In [43], a control scheme for parallel three-phase rectifiers under unbalanced operating conditions with the suppression of the circulating currents between the parallel modules was

Manuscript received May 24, 2017; revised September 25, 2017; accepted October 26, 2017. Date of publication November 7, 2017; date of current version June 22, 2018. Recommended for publication by Associate Editor D. Xu. *(Corresponding author: Nady Rocha.)*

N. Rocha and A. E. L. da Costa are with the Department of Electrical Engineering, Federal University of Paraíba Cidade Universitária, João Pessoa 58051-900, Brazil (e-mail: nadyrocha@cear.ufpb.br; andre.costa@cear.ufpb.br).

C. B. Jacobina is with the Department of Electrical Engineering, Federal University of Campina Grande, Campina Grande 58109-970 Brazil (e-mail: jacobina@dee.ufcg.edu.br).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2771464

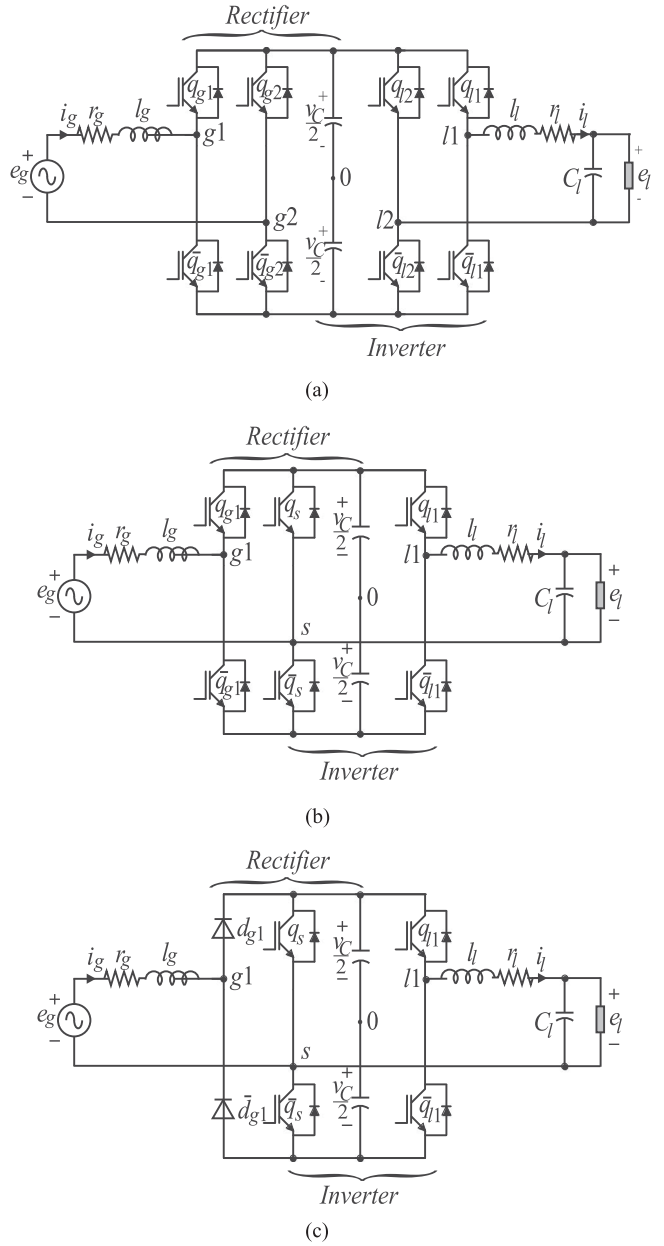

Fig. 1. Conventional single-phase to single-phase ac–dc–ac converters. (a) Four-leg converter (4L). (b) Three-leg converter (3L). (c) Unidirectional three-leg converter (3L2D).

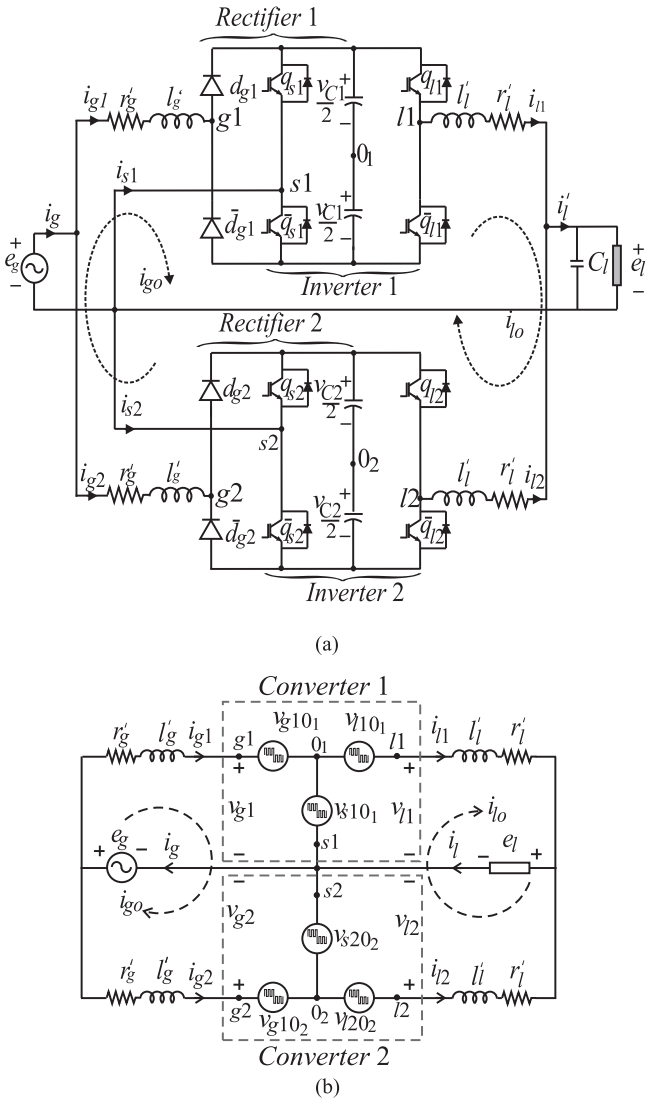

Fig. 2. Proposed unidirectional single-phase to single-phase converters with two dc-link voltages (6L4D). (a) System configuration. (b) Simplified model.

presented. In [44], two parallel converters are used to achieve high current rating in MW-level wind energy conversion system. In this paper, different modulation schemes were evaluated in order to reduce the size and loss of the inductance filters.

In this paper, one parallel single-phase to single-phase dc-link converter is proposed. This topology has been conceived from two three-leg converters with an uncontrolled leg connected in parallel without an isolation transformer, as shown in Fig. 2(a). The proposed converter is suitable for applications addressing single phase ac–dc–ac converters in a wide range of power levels. Generally, single-phase systems require load with power less than 10 kVA [48]. Compared to 4L and 3L converters [see Fig. 1(a) and (b)], proposed configuration, called 6L4D [see Fig. 2(a)], permits the decreasing of the current and the power rating processed by the rectifier and inverter switches, the harmonic content at the input and output sides of the proposed converter and the total switch losses. When compared with 3L2D converter, the proposed configuration permits the decreasing of the power rating processed by the switches and the total harmonic distortion (THD). A synchronization technique between input and output converter voltages is proposed for the 6L4D converter. The technique allows the reduction of the shared-leg current and eliminates the distortion of the grid current in the zero-crossing distortion without hysteresis control. Besides the proposed topology, another important contribution of this paper is a modified interleaved pulse width modulation (PWM) technique that ensures five-level voltage at the input and at output side of the proposed converter, which decrease the inductance filter size and the THD. Simulation and experimental results show the viability of the proposed parallel unidirectional ac–dc–ac converter.

The paper introduces the system model of the proposed topology in Section II. Then, Section III presents the control strategies, including PWM strategy and control scheme, while Section IV shows the analysis of the harmonic distortion, including the modified carrier interleaved PWM. The study of dc-link voltage is presented in Section V. The semiconductor power loss is presented in Section VI. Simulation and experimental results to illustrate the correct operation of the proposed converter are presented in Sections VII and VIII, respectively. Finally, Section IX presents the conclusions with the main advantages of the proposed configuration.

II. System Model

The proposed configuration is made up of the parallelism of two unidirectional three-leg converters, inductor and capacitor filters (C_l, r'_g, l'_g, r'_l, and l'_l) and two dc-link capacitor voltages. The controlled legs of the converters are composed of top controlled switches q_{sk} and q_{lk}, with $k = 1, 2$ and complementary bottom controlled switches $\overline{q}_{sk}$ and $\overline{q}_{lk}$ and the two uncontrolled legs are constituted by top diodes d_{gk} and complementary bottom diodes $\overline{d}_{gk}$.

From the simplified model of the system, shown in Fig. 2(b), the following equations can be derived:

$$e_g = r'_g i_{gk} + l'_g \frac{di_{gk}}{dt} + v_{gk} \tag{1}$$

$$i_g = i_{g1} + i_{g2} \tag{2}$$

$$e_l = -r'_l i_{lk} - l'_l \frac{di_{lk}}{dt} + v_{lk} \tag{3}$$

$$i_l = i_{l1} + i_{l2} \tag{4}$$

with

$$v_{gk} = v_{gk0_k} - v_{sk0_k} \tag{5}$$

$$v_{lk} = v_{lk0_k} - v_{sk0_k} \tag{6}$$

where e_g is the grid voltage, i_g is the grid current, i_{gk} are the input currents of the rectifiers, v_{gk} are the voltages generated by the rectifiers, v_{lk} are the voltages generated by the inverters, e_l is the load voltage, i_l is the load current, i_{lk} are the output currents of the inverters, v_{gk0_k}, v_{lk0_k}, and v_{sk0_k} are the converter pole voltages, r'_g and l'_g represent the resistances and inductances of the input filter, respectively, r'_l and l'_l represent the resistances and inductances of the output filter, respectively.

The mathematics model of rectifiers 1 and 2 is represented by (1). Summing the equations of the rectifier 1 ($k = 1$) with that of the rectifier 2 ($k = 2$) and using (2), the equivalent model for the grid voltage (rectifiers 1 and 2) can be obtained as following:

$$e_g = \frac{r'_g}{2} i_g + \frac{l'_g}{2} \frac{di_g}{dt} + v_g \tag{7}$$

$$v_g = \frac{v_{g1} + v_{g2}}{2}. \tag{8}$$

In like manner, from (3) and (4), the equivalent load voltage is written as

$$e_l = -\frac{r'_l}{2} i_l - \frac{l'_l}{2} \frac{di_l}{dt} + v_l \tag{9}$$

$$v_l = \frac{v_{l1} + v_{l2}}{2}. \tag{10}$$

From (7) and (9), neglecting the coil resistance and considering l_g the filter inductance of the conventional 3L converter, it should be notice that in order to achieve the same harmonic distortion, without interleaved operation, the inductance l'_g of the unidirectional 6L4D converter is two times the inductance l_g of the 3L converter. However, (8) and (10) show that the voltages v_g and v_l are three-level voltages when interleaved technique is used, which can reduce the inductance value, as shown in [44].

The previous model can also be expressed by using the circulating currents i_{go} and i_{lo} (rectifier and inverter sides, respectively) introduced by

$$i_{g1} = \frac{i_g}{2} + i_{go} \tag{11}$$

$$i_{g2} = \frac{i_g}{2} - i_{go} \tag{12}$$

$$i_{l1} = \frac{i_l}{2} + i_{lo} \tag{13}$$

$$i_{l2} = \frac{i_l}{2} - i_{lo}. \tag{14}$$

From (1) and (3), it turns out that

$$0 = 2r'_g i_{go} + 2l'_g \frac{di_{go}}{dt} + v_{g1} - v_{g2} \tag{15}$$

$$0 = -2r'_l i_{lo} - 2l'_l \frac{di_{lo}}{2} + v_{l1} - v_{l2}. \tag{16}$$

In this case, the complete system model is given by (7), (9), and

$$v_{go} = 2r'_g i_{go} + 2l'_g \frac{di_{go}}{dt} \tag{17}$$

$$v_{lo} = -2r'_l i_{lo} - 2l'_l \frac{di_{lo}}{dt} \tag{18}$$

with

$$v_{go} = -v_{g1} + v_{g2} \tag{19}$$

$$v_{lo} = -v_{l1} + v_{l2} \tag{20}$$

where v_{go} and v_{lo} are the circulating voltages at the rectifier and inverter side, respectively. The negative effects of the circulation currents can be minimized through coupled inductor, which provides a high inductance to the circulating current. The advantage of this solution is the possibility to reduce the inductor filter size and thus, improving efficiency. The design of inductor can be made in similar way as presented in [44] and [49].

A. System Model to Eliminate Zero-Crossing Distortion

From Fig. 2(a), two operation conditions can be highlighted to obtain a sinusoidal grid current without zero crossover distortion:

Case 1: $i_g \geq 0$

In this case, the diodes d_{g1} and d_{g2} conduct the currents i_{g1} and i_{g2}, respectively, and then

$$v_{gk0_k} = \frac{v_{Ck}}{2}. \tag{21}$$

From (5), (6), and (21), the pole voltages of controlled legs are defined by

$$v_{sk0_k} = \frac{v_{Ck}}{2} - v_{gk} \tag{22}$$

$$v_{lk0_k} = \frac{v_{Ck}}{2} + v_{lk} - v_{gk}. \tag{23}$$

Since $v_{C1} = v_{C2} = v_C$, the rectifier pole voltages v_{sk0_k} and v_{lk0_k} have two limit values $-v_C/2$ and $v_C/2$, from (22) and (23), it can be obtained that $0 \leq v_{gk} \leq v_C$, and $v_{lk} \leq v_{gk}$.

Case 2: $i_g < 0$

In this case, the diodes $\bar{d}_{g1}$ and $\bar{d}_{g2}$ conduct the currents i_{g1} and i_{g2}, respectively, and then

$$v_{gk0_k} = -\frac{v_{Ck}}{2}. \tag{24}$$

From (5), (6), and (24), the pole voltages of controlled legs are defined by

$$v_{sk0_k} = -\frac{v_{Ck}}{2} - v_{gk} \tag{25}$$

$$v_{lk0_k} = -\frac{v_{Ck}}{2} + v_{lk} - v_{gk}. \tag{26}$$

From (25) and (26), it can be obtained that $-v_C \leq v_{gk} \leq 0$ and $v_{lk} \geq v_{gk}$.

The operation of the converter without low order harmonics must satisfy the limit voltage restrictions and the grid current i_g and inverter voltage v_l must have the same phase angle as voltage v_g.

III. Control Strategies

A. PWM Strategy

The circulation current at the rectifier side (i_{go}) can be controlled in two ways: 1) from the control of rectifier currents (i_{g1} and i_{g2}) or 2) from the control of grid current (i_g) and its own circulating current i_{go}. Fig. 3 exemplifies these two possibilities. First option (Scheme 1), the control of the currents i_{g1} and i_{g2} determines the reference voltages v^*_{g1} and v^*_{g2}, as shown in Fig. 3(a). On the other hand, in the second option (Scheme 2), the grid current i^*_g and circulating current i_{go} are controlled. At the output of these controllers, the voltages v^*_g and v^*_{go} are defined, respectively.

Considering the first option (Scheme 1), the voltages v^*_{g1}, v^*_{g2}, v^*_l, and v^*_{lo} are the reference voltages provided by the controllers (see Section III-B). Then from (5), (10), and (20), it follows that

$$v^*_{gk} = v^*_{gk0_k} - v^*_{sk0_k} \tag{27}$$

$$v^*_l = \frac{1}{2}\left(v^*_{l10_1} - v^*_{s10_1} + v^*_{l20_2} - v^*_{s20_2}\right) \tag{28}$$

$$v^*_{lo} = -v^*_{l10_1} + v^*_{s10_1} + v^*_{l20_2} - v^*_{s20_2}. \tag{29}$$

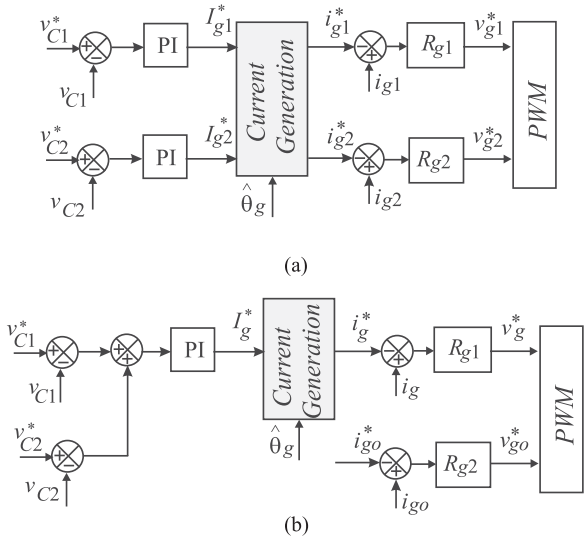

Fig. 3. Circulating current control. (a) Scheme 1. (b) Scheme 2.

There are four reference voltages v^*_{g1}, v^*_{g2}, v^*_l, and v^*_{lo}, and only four reference pole voltages $v^*_{s10_1}$, $v^*_{s20_2}$, $v^*_{l10_1}$, and $v^*_{l20_2}$ to be determined, since the pole voltages $v^*_{g10_1}$ and $v^*_{g20_2}$ depend on the current direction.

From (27) to (29), the reference pole voltages can be written

$$v^*_{sk0_k} = -v^*_{gk} + v^*_{gk0_k} \tag{30}$$

$$v^*_{l10_1} = v^*_l + v^*_{g10_1} - v^*_{g1} + \frac{1}{2}v^*_{lo} \tag{31}$$

$$v^*_{l20_2} = v^*_l + v^*_{g20_2} - v^*_{g2} - \frac{1}{2}v^*_{lo}. \tag{32}$$

The voltages $v^*_{gk0_k}$ are defined from (33) and (34)

Case 1: $i_g \geq 0$

$$v^*_{gk0_k} = \frac{v^*_{Ck}}{2}. \tag{33}$$

Case 2: $i_g < 0$

$$v^*_{gk0_k} = -\frac{v^*_{Ck}}{2}. \tag{34}$$

When v^*_{gk} is not synchronized to v_{lk} the reference pole voltages $v^*_{sk0_k}$ and $v^*_{lk0_k}$ are higher than the maximum and minimum limits ($v_C/2$ and $v_C/2$). This operation condition causes over-modulation and introduces low-order harmonic in the grid current and in the load voltage, consequently increases the harmonic distortion. In order to obtain the gating signals, a comparison of the pole voltages with one, two, or four high-frequency triangular carrier signals (called here single, double, or four carrier-based PWM) is performed [50]–[53].

B. Control Strategy

Fig. 4 presents the control block diagram for the proposed configuration. The dc-link capacitor voltages v_{C1} and v_{C2} are adjusted to their reference values v^*_{C1} and v^*_{C2} by using the conventional proportional–integral type controllers. The reference dc-link voltages are equal to v^*_C, i.e., $v^*_{C1} = v^*_{C2} = v^*_C$.

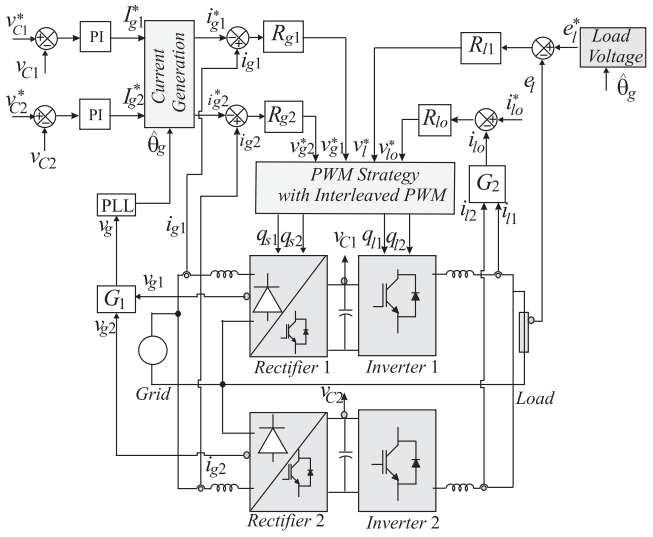

Fig. 4. System block control diagram for proposed configuration.

TABLE I
PARAMETER OF WTHD ANALYSES

Parameter	Value	Parameter	Value
Grid voltage	1.0 p.u.	DC-link voltage	1.55 p.u.
Inductor (l_g/l'_g)	0.1 p.u./0.2 p.u.	Load power	1.0 p.u.
Resistor (r_g/r'_g)	0.01 p.u./0.02 p.u.	Load voltage	0.9 p.u.
Switching frequency	10 kHz	N_h	1000

TABLE II
WTHD OF THE VOLTAGES v_g AND v_l FOR ALL TOPOLOGIES ANALYZED

	WTHD				
Voltage	4L	3L	3L2D	Proposed	
				SC	DC
v_g	0.155%	0.155%	0.308%	0.308%	0.082%
v_l	0.204%	0.248%	0.290%	0.290%	0.163%

Such controllers provide the amplitude of the reference of the rectifier currents i^*_{g1} and i^*_{g2}, respectively. To control the input currents, the instantaneous reference currents i^*_{g1} and i^*_{g2} are synchronized (via blocks phase lock loop scheme) with the rectifier voltage v_g ensuring the elimination of zero crossover distortion in grid current. From the measurements of the voltages v_{g1} and v_{g2}, the rectifier voltage v_g is obtained from (8), represented by block G_1.

The control of the rectifier currents (i_{g1} and i_{g2}) are implemented by using the controllers R_{g1} and R_{g2}. This paper used double-sequence controller [54]. The current controllers define the input reference voltages v^*_{g1} and v^*_{g2}.

Despite the dc-link capacitor voltage and rectifier current controls, another control goal of the proposed converters is the regulation of the circulating current. The circulating current at the inverter side is obtained from (13) and (14), represented in Fig. 4 by block G_2. The control of the i_{lo} is implemented with the controller indicated by block R_{lo} that determines the voltage v^*_{lo}. The load voltage control defines the reference voltage v^*_l. In this block, v^*_l must be synchronized with v_g to eliminate the zero crossover distortion in the grid current. In addition, this synchronization also causes a decrease of current in the shared leg.

IV. HARMONIC DISTORTION

A. Weighted THD (WTHD)

The WTHD factor has been used to evaluate the distortion of the voltages generated at the input and output of the converter [55]. In order to calculate the value of the WTHD, the harmonics of the converter voltages are weighted with the number of harmonics frequency, hence the WTHD is more interesting than the THD in the analysis of the modulated voltages [56]. The WTHD was computed by using

$$\text{WTHD} = \frac{100}{a_1}\sqrt{\sum_{h=2}^{N_h}\left(\frac{a_h}{h}\right)^2} \tag{35}$$

where a_1 is the amplitude of the fundamental component, a_h is the amplitude of hth component harmonic and N_h is the number of harmonics taken into consideration.

The WTHD was evaluated considering the parameters and conditions shown in Table I. In this paper, four topologies are compared: conventional 4L and 3L converters, unidirectional 3L2D converter, and proposed unidirectional converter (6L4D). In order to ensure the proper operation of the unidirectional converter, the load voltage must be less than the grid voltage. Then, all the topologies were evaluated considering that the grid voltage equals 1.0 p.u. and the load voltage equals 0.9 p.u. To ensure the same dc-link voltage among all topologies, the output voltage was synchronized with the input voltage in the converters with shared-leg (3L, 3L2D, and 6L4D converters).

Table II shows the WTHD of the voltages generated by the rectifier [$v_g = (v_{g1} + v_{g2})/2$ for the proposed configuration, $v_g = v_{g10} - v_{g20}$ for the conventional 4L converter, and $v_g = v_{g10} - v_{s0}$ for the 3L and unidirectional 3L2D converters] and voltages generated by the inverter [$v_l = (v_{l1} + v_{l2})/2$ for the proposed configuration, $v_l = v_{l10} - v_{l20}$ for the conventional 4L converter and $v_l = v_{l10} - v_{s0}$ for the 3L and the unidirectional 3L2D converters]. The switching frequency is equal to 10 kHz. Voltages v_g and v_l are responsible for controlling i_g and e_l. This means that the WTHD of these voltages determines the harmonic distortion of the utility grid current and load voltage. In this paper, the study of harmonic distortion for the proposed topology is carried out by using the interleaved technique in the PWM strategy. The results with single-carrier-based PWM (SC) and double-carrier-based PWM (DC) are presented in Table II.

Applying a single-carrier-based PWM (SC) the WTHD of the voltages v_g and v_l are equal to WTHD of unidirectional 3L2D topology and greater than the conventional 4L and 3L converters. However, by using a double-carrier-based PWM (DC) the proposed system guarantees the lowest value of WTHD for input and output voltage. Considering the proposed topology with double-carrier-based PWM the improvement of WTHD of the

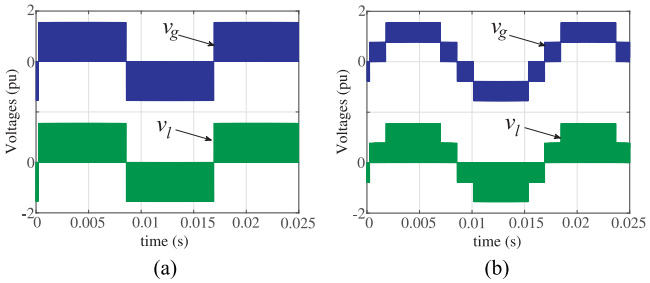

Fig. 5. Voltages v_g and v_l. (a) 4L, 3L, and 3L2D topologies and 6L4D topology with single-carrier PWM. (b) 6L4D topology with double-carrier PWM.

voltages v_g and v_l is, respectively, close to 47% and 20%, when compared to the conventional 4L topology, 47% and 35% when compared to the conventional 3L topology and 73% and 44% when compared to the unidirectional 3L2D topology.

The explanation for the WTHD behavior in Table II can be obtained from Fig. 5, which depicts the rectifier and inverter voltages (v_g and v_l) obtained considering the cases presented in Table II. It is worth mentioning that, using single-carrier-based PWM the voltage v_g generated by the proposed topology is similar to voltages v_g and v_l of the conventional topologies [see Fig. 5(a)]. However, using double-carrier-based PWM [see Fig. 5(b)], the number of levels of voltage v_g is higher. On the other hand, the outline of the voltage v_l is not distributed as well because the five levels are not well defined, which means a higher value of WTHD.

B. Modifier-Carrier Interleaved PWM (MC)

As shown in Fig. 5(b), the waveform of the output voltage v_l of the proposed topology has not the five levels of voltages well defined. In this section, a modifier interleaved-carrier PWM is presented in order to improve the harmonic distortion in the load voltage, while ensuring the same harmonic distortion in the front-end converter.

In this strategy, the gating signals of the two shared legs are obtained by comparison of the pole voltages with the double-carrier PWM v_{t1} and v_{t2}. The interleaving angle of the triangular carrier signals is 180° [see Fig. 6(a)]. On the other hand, the gating signals of the two inverter legs are obtained by comparison of the pole voltages (v_{l10_1} and v_{l20_2}) with the four-carrier PWM. The triangular carrier signals v_{t3} and v_{t4} have the interleaving angle equal to 90° and 270°, respectively [see Fig. 6(a)]. When the gating signals of the two inverter legs (l_1 and l_2) are obtained from v_{t3} and v_{t4}, there is a change in the vector switching sequences applied to generate the gate signals, as shown in Fig. 7(a). Notice that from 7(a), the voltage levels are well defined when $v_l > v_C/2$ or $v_l < -v_C/2$, but for $-v_C/2 < v_l < v_C/2$, the voltage levels are not well defined. This happens because for $v_l > v_C/2$ or $v_l < -v_C/2$ the nearest switching vector sequences are applied to generate the gate signals, otherwise more distant vector switching sequences are used. In this way, in the proposed strategy, when v_l^* is higher or equal to $v_C/2$ or less than or equal to $-v_C/2$, the pole voltages v_{l10_1} and v_{l20_2} are compared to v_{t3} and v_{t4}, respectively.

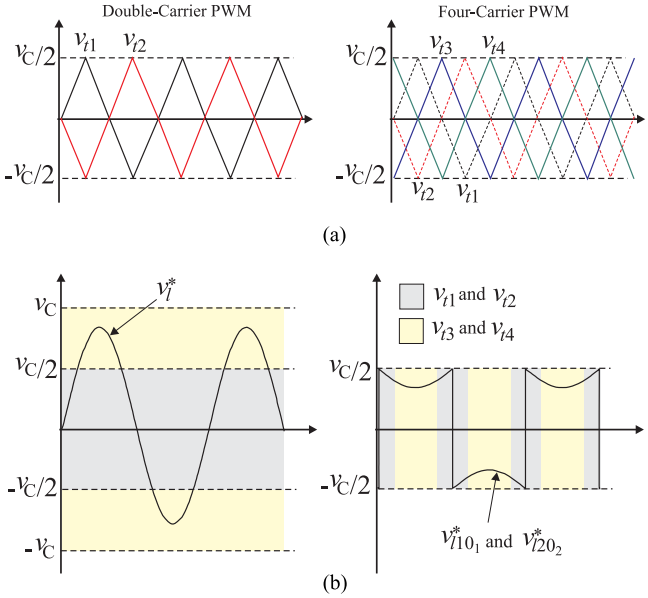

Fig. 6. Modified PWM strategy. (a) Double-carrier PWM (left) and four-carrier PWM (right). (b) Choice of carrier based on v_l^* (left) and reference pole voltages (right).

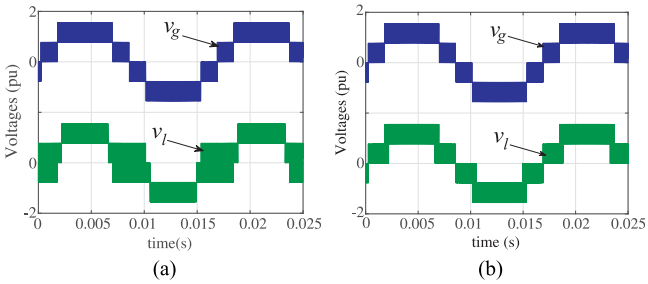

Fig. 7. Voltages v_g and v_l. (a) 6L4D topology with four-carrier PWM. (b) 6L4D topology with modified PWM strategy.

Otherwise, the pole voltages v_{l10_1} and v_{l20_2} are compared to v_{t1} and v_{t2}, respectively. This PWM strategy is illustrated in Fig. 6(b). This ensures that the switching vector sequence to generate the voltage v_l will be carried out by nearest vectors, which allows a reduction of the harmonic distortion.

Fig. 7(b) presents the waveform of voltages v_g and v_l of the investigated converter with the proposed modified-carrier interleaved PWM strategy. It can be seen from the figure that the voltages v_g and v_l have the five well-defined voltage levels. The WTHD of voltages v_g and v_l are equal to 0.082% and 0.088%, respectively. The decreased value of WTHD in output voltage (v_l) is nearly 46% when compared to proposed topology with double-carrier PWM. Whereas, compared to conventional 4L, 3L, and 3L2D topologies the reduction is about 57%, 65%, and 70%, respectively.

C. Total Harmonic Distortion

This section presents the harmonic distortion analysis of the grid, load, and internal currents (i_g, i_l, and i_{g1}). In this case, the

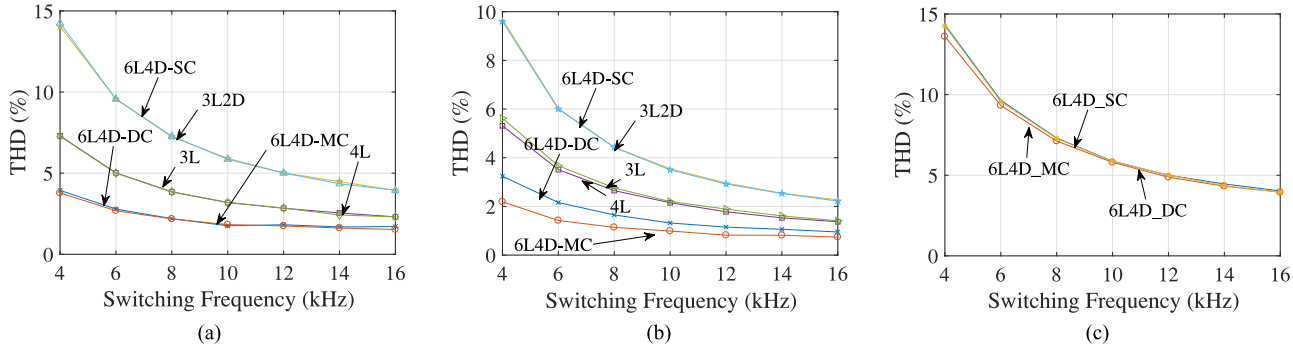

Fig. 8. THD comparison for different topologies and switching frequencies. (a) Grid current (i_g). (b) Load current (i_l). (c) Internal current (i_{g1}).

THD is better than the WTHD. It can be defined as

$$\text{THD} = \frac{\sqrt{\sum_{h=2}^{N_h} a_h^2}}{a_1}. \tag{36}$$

The same conditions and parameter were considered in the THD analysis. The THD value curves of the currents i_g, i_l, and i_{g1} across the switching frequency range are plotted in Fig. 8. The results have been obtained with parameters shown in Table V. The inductance l_g of the conventional converters was half of the proposed topology to achieve the same equivalent inductance. From Fig. 8, it can be seen that the THD values of the grid and load currents of the proposed topology with single-carrier PWM (6L4D-SC) are equal to the unidirectional 3L2D topology. On the other hand, the THD values of the grid and load currents of the proposed topology with modifier-carrier interleaved PWM (6L4D-MC) are much lower than the conventional 3L2D. The THD improvement of the proposed topology with modifier-carrier PWM is due to the multilevel input and output converter voltages. As a result of the comparison, it is clear that using the modifier-carrier PWM, the proposed converter has the lowest value of THD in the grid and load currents among all the conventional topologies. In order to achieve the same THD value, when compared to 4L and 3L topologies the switching frequency of the 6L4D-MC topology can be reduced by half, while compared with 3L2D topology the switching frequency can be reduced by one-quarter.

Fig. 8(c) illustrates the THD value of the internal currents of the unidirectional 6L4D converter (i_{g1}). The THD value of the i_{g2} is equal to i_{g1}, and is also equal to the THD value of the grid current (i_g) when the single-carrier PWM is applied. Moreover, the internal current (i_{g1}) has the same value of the harmonic distortion, independent of the PWM strategies applied (single, double, or modified-carrier PWM), as shown in Fig. 8(c). Similar analysis is found with currents i_{l1} and i_{l2}.

V. DC-Link Capacitor Voltage Specification

Neglecting the oscillations on the dc-link capacitor voltage and considering the balanced system, i.e., inductors with same values, from pole voltages (30)–(32), the minimum voltage $v_C^* = v_{C1}^* = v_{C2}^*$ is given by

$$v_C^* \geq \left|\hat{V}_g\right| \tag{37}$$

$$v_C^* \geq \left|\hat{V}_l\right| \tag{38}$$

$$v_C^* \geq \left|\hat{V}_g - \hat{V}_l\right|. \tag{39}$$

In order to apply the input voltage with amplitude V_g and the output voltage with amplitude V_l, the minimum dc-link voltage must satisfy (37)–(39). Considering that $\hat{V}_g = V_g e^{-j\theta_g}$ and $\hat{V}_l = V_l e^{-j(\theta_g+\varepsilon)}$ and ε the angle between the voltages $\hat{V}_g$ and $\hat{V}_l$,

Jacobina *et al.* [57] shows that the three-leg converter can have the same dc-link voltage of the 4L converter when $-60^\circ \leq \varepsilon \leq 60^\circ$. The amplitude of $\hat{V}_g - \hat{V}_l$ has a value near the amplitude of $\hat{V}_g$ when $\varepsilon = 60^\circ$. On the other hand, whenever $\varepsilon > 60^\circ$ the dc-link voltage of the three-leg converters is higher than that of the 4L converter, once the minimum dc-link voltage is determined by (39), as shown in [57].

However, to insure proper function of the proposed topology, the voltage v_g^* must be synchronized with v_l^* and grid and the load frequencies must be equal (e.g., line voltage regulators and uninterruptible power supplies). These conditions define the minimum dc-link voltage v_C^* demanded by proposed topology, which is equal to the conventional 4L converter. For different grid and load frequency, the dc-link voltages of the 3L converter is twice the value of conventional 4L converter.

The capacitance of the dc-link voltage can be obtained using the procedure outlined in [23] and [58]. Since the flux power through converter is half of total power flux, the capacitor size can be reduced to half, when compared to conventional 4L converter [58].

VI. Converter Losses

The loss estimation is obtained by using the technique presented in [59] and [60]. The following losses are included in the model: IGBT and diode conduction, IGBT turn-on energy losses, IGBT turn-off energy losses, and diode turn-off energy losses (reverse recovery).

Fig. 9 shows the semiconductor power losses (normalized by load power) in each leg of the converter. The results have been obtained by using the same switching frequency (10 kHz), load

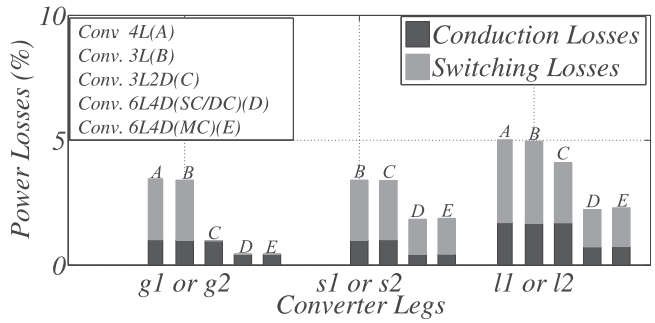

Fig. 9. Power losses of the converter legs.

TABLE III
SEMICONDUCTOR LOSSES ESTIMATION WITH SAME SWITCHING FREQUENCY

Load Power	4L	3L	3L2D	6L4D	
				SC/DC	MC
500 VA	18.94%	13.52%	9.44%	11.33%	11.55%
1000 VA	16.96%	11.77%	8.46%	9.02%	9.15%
2000 VA	15.27%	9.95%	7.51%	8.11%	8.07%

TABLE IV
RMS CURRENT THROUGH THE SEMICONDUCTOR OF TOPOLOGIES 4L, 3L, 3L2D, AND 6L4D

	4L	3L	3L2D	6L4D
Switch current				SC/DC/MC
i_{dgk} or i_{qgk}	0.67	0.67	0.67	0.337
i_{qsk}	–	0.67	0.67	0.33
i_{qlk}	1.0	1.0	1.0	0.499

power equal to 1000 VA and power factor equal to 0.8. Notice that, because of the reduction of currents, for the proposed configuration the power loss of each leg is always lower than that of the conventional 4L, 3L, and 3L2D converters, as shown in Fig. 9. Although the power loss of each leg of the proposed topology are lower than the 3L2D topology, the total power loss is still high, as shown in Table III. In addition, notice that, the proposed topology has the same performance for different carrier PWM (single, double, and modified-carrier PWM).

Table IV shows the root-mean-square (rms) current through the semiconductor of topologies 4L, 3L, 3L2D, and 6L4D with output power equal to 1000 VA normalized across the load current of the 4L converter. Topologies 4L, 3L, and 3L2D have the same current stress, which is expected since all of them operate with same values of i_g and i_l. The semiconductors of the proposed converter have the lowest current stress, because the legs operate with reduced amplitude of the grid ($i_g/2$) and load current ($i_l/2$). Consequently, the proposed topology allows the use of low-cost semiconductors. The losses of the 3L2D topology are smaller than those of the 3L and 4L topologies, because of the diode leg and of the PWM strategy. Despite the fact that the current in each leg of the 6L4D topology has been reduced about 50%, the reduction of the power loss was less than 50%, this is due to the nonlinear model of loss [61]. Since the proposed topology has double of switches of the 3L2D topology, the power losses are slightly greater.

TABLE V
PARAMETERS EMPLOYED ON THE SIMULATION RESULTS

Parameter	Value	Parameter	Value
r_g and r_l	0.2 Ω	V_g (rms)	127 V
l_g and l_l	5 mH	v_{C1} and v_{C2}	221.3 V
f_{sh}	10 kHz	C	2200 μF
V_l (RMS)	114 V	Cl	5 μF

Table III lists the total semiconductor power losses obtained with all topologies with three different power loads (500 VA, 1000 VA, and 2000 VA and power factor equal to 0.8) and same switching frequency. The 3L2D topology is more efficient than the proposed 6L4D topology for all cases analyzed; however, the performance in harmonic distortion is much worse than the proposed 6L4D topology. This means that for the same value of THD the 6L4D topology will be more efficient than 3L2D. On the other hand, the power losses of the proposed 6L4D topology are lower than conventional 3L and 4L topologies. The total power loss, for the proposed topology, is almost 45% and 22% lower than the conventional 4L and 3L topologies, respectively.

VII. SIMULATIONS RESULTS

The proposed system was simulated by using the parameters presented in Table V. Steady-state operation mode was considered in the simulation tests. Simulation results using single, double, and modifier-carrier PWM are shown in Figs. 10–12.

Notice that all control requirements demanded by the configuration were established, i.e., the control guarantees sinusoidal grid current waveform without zero crossover distortion and grid current synchronized by voltage v_g [see Figs. 10(a), 11(a), and 12(a)], dc-link voltages under control [see Figs. 10(e), 11(e), and 12(e)] and load voltage sinusoidal and under control [see Figs. 10(f), 11(f), and 12(f)]. Also, the control guarantees the output circulating currents close to zero [see Figs. 10(d), 11(d), and 12(d)]. Furthermore, as expected, the proposed configuration provides current reduction in the shared-leg since i_{s1} is lower than the i_{g1}, i_{g2}, i_{l1}, and i_{l2}. Compared to single and double-carrier PWM, the modified-carrier PWM ensures five-level voltages at the input and output side of the proposed converter (v_g and v_l) as shown in Fig. 12(a) and (b).

VIII. EXPERIMENTAL RESULTS

The proposed system was implemented in the laboratory. Steady-state operation mode was considered in the experimental tests. The experimental setup used in the experimental tests is based on a digital signal processor TMS320F28335 equipped with appropriate plug-in boards and sensors as illustrated in Fig. 13. In the experimental tests, the load was obtained using an *RL* load plus a single-phase motor (127 V, 60 Hz, 1 kW, and

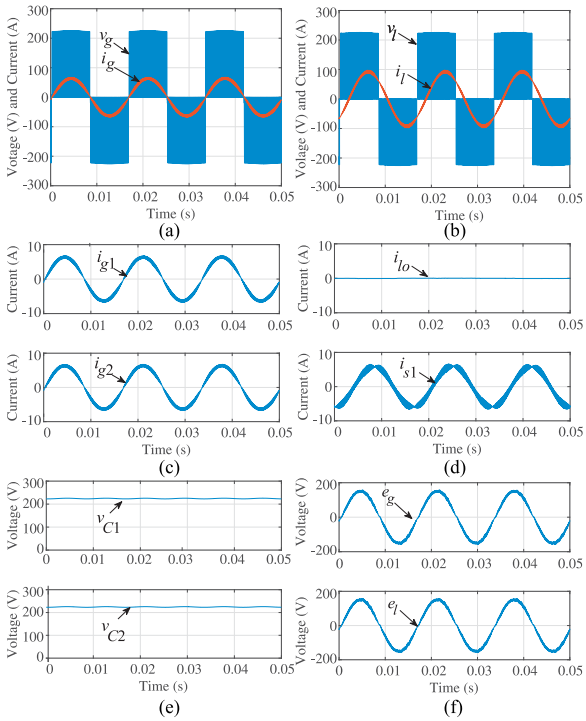

Fig. 10. Simulation results using single-carrier PWM. (a) Voltage of the rectifier (v_g) and current of the grid (i_g). (b) Voltage of the inverter (v_l) and current of the load (i_l). (c) Input currents in rectifiers 1 and 2 (i_{g1} and i_{g2}). (d) Circulating current (i_{lo}) and shared-leg current (i_{s1}). (e) DC-link voltages (v_{C1} and v_{C2}). (f) Grid and load voltages (e_g and e_l).

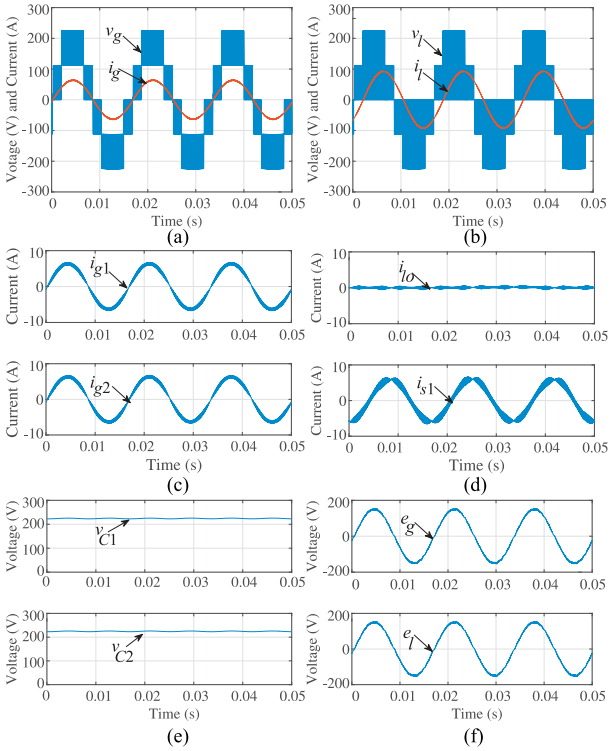

Fig. 11. Simulation results using double-carrier PWM. (a) Voltage of the rectifier (v_g) and current of the grid (i_g). (b) Voltage of the inverter (v_l) and current of the load (i_l). (c) Input currents in rectifiers 1 and 2 (i_{g1} and i_{g2}). (d) Circulating current (i_{lo}) and shared-leg current (i_{s1}). (e) Dc-link voltages (v_{C1} and v_{C2}). (f) Grid and load voltages (e_g and e_l).

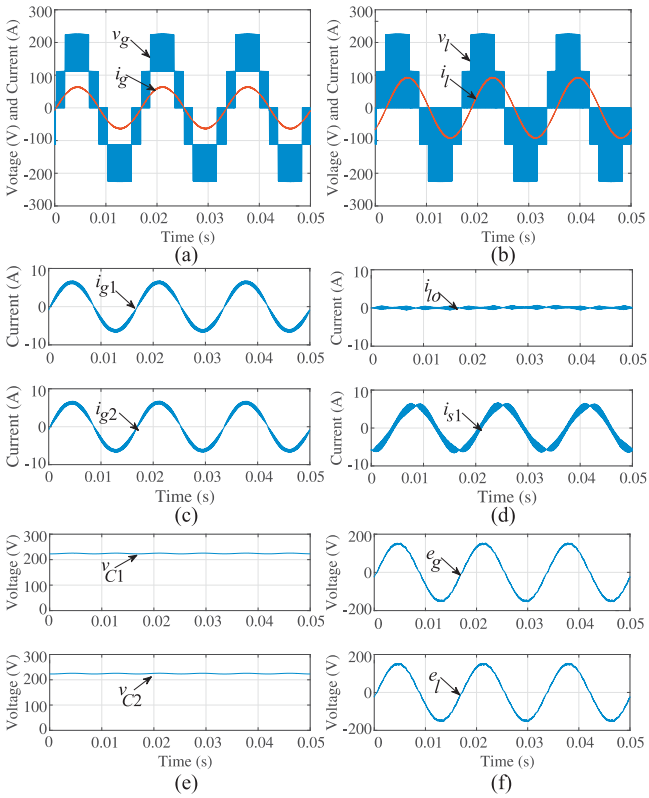

Fig. 12. Simulation results using modifier-carrier PWM. (a) Voltage of the rectifier (v_g) and current of the grid (i_g). (b) Voltage of the inverter (v_l) and current of the load (i_l). (c) Input currents in rectifiers 1 and 2 (i_{g1} and i_{g2}). (d) Circulating current (i_{lo}) and shared-leg current (i_{s1}). (e) DC-link voltages (v_{C1} and v_{C2}). (f) Grid and load voltages (e_g and e_l).

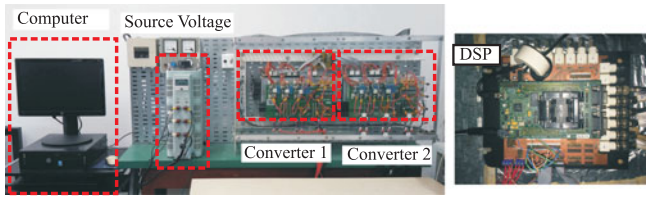

Fig. 13. Photo of the experimental setup.

TABLE VI
PARAMETERS EMPLOYED ON THE EXPERIMENTAL TESTS

Parameter	Value	Parameter	Value
r'_g and r'_l	0.33 Ω	V_g (rms)	120 V
l'_g and l'_l	6 mH	v_C	210 V
f_{sh}	10 kHz	C	2200 μF
V_l (rms)	108 V	R and L	8.54 Ω and 12 mH

1750 r/min). The detailed system parameters employed on the experimental tests are listed in Table VI.

Experimental results using single-carrier PWM are shown in Fig. 14(a). Fig. 14(a)–(I) shows that the grid current is sinusoidal and it is synchronized with the rectifier voltage v_g, this guarantees grid current without zero-cross over distortion.

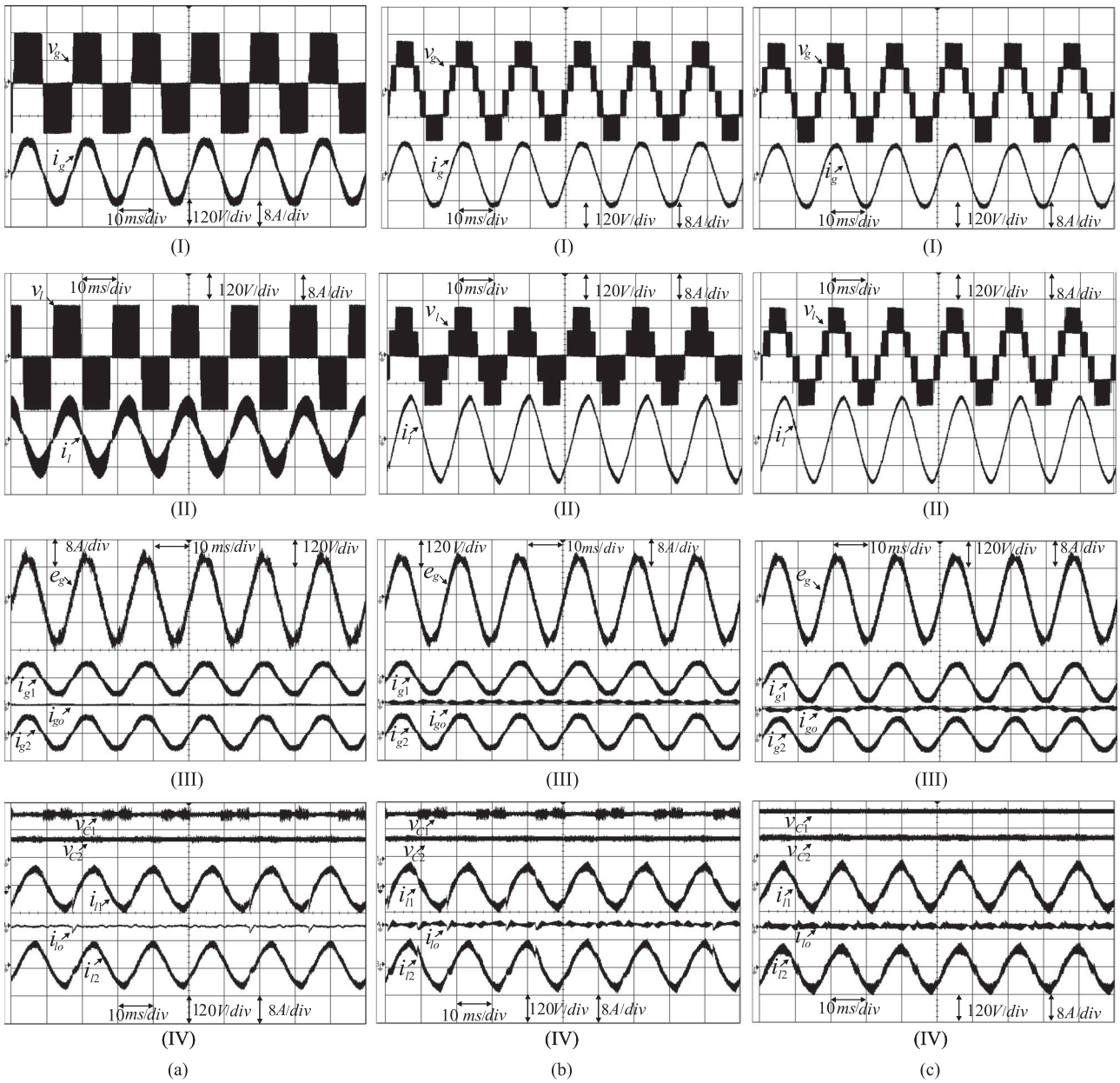

Fig. 14. Experimental results of the Conf. 6L4D. (a) Using single-carrier PWM. (b) Using double-carrier PWM. (c) Using Modified-Carrier PWM. (I) Input converter voltage (v_g) and grid current (i_g). (II) Output converter voltage (v_l) and load current (i_l). (III) Grid voltage (e_g), input circulating current (i_{go}) and internal currents (i_{g1} and i_{g2}). (IV) Dc-link voltages (v_{C1} and v_{C2}), internal currents (i_{l1} and i_{l2}) and output circulating current (i_{lo}).

The dc-link voltages are under control [see Fig. 14(a)–(I)] with voltages equal to 210 V. Fig. 14(a)-(I) and (a)-(II) shows the three-level voltages v_g and v_l because single-carrier PWM is applied. Fig. 14(a)-(III) and (a)-(IV) shows that the circulating currents (i_{go} and i_{lo}) are close to zero. Furthermore, as expected, the parallel converter provides current reduction of each leg of the converter as shown in Fig. 14(a)-(III) and (a)-(IV).

Fig. 14(b) presents another set of experimental results using double-carrier PWM. Fig. 14(b)-(I) and (b)-(II) illustrates a reduction in the ripple of the grid and load currents when double-carrier PWM is applied. These figures also show the five-level voltages at the grid and load side, with the level of the voltage at the grid side well defined. On the other hand, circulating currents are null and they have a larger ripple when compared to the circulating current with single-carrier PWM.

Fig. 14(c) presents the experimental results using the modified-carrier PWM. Fig. 14(c)-(I) and (c)-(II) shows the five-level voltages at the grid and load sides, with the level of the voltage at the grid and load side well defined. Verify that the proposed converter with modified-carrier PWM strategy provides high power quality at the input and output voltage converter (v_g and v_l). The behavior of voltages and currents is in agreement with the simulation results presented.

Table VII shows the THD measured of the proposed 6L4D topology and conventional 4L and 3L2D converters. The THD

TABLE VII
EXPERIMENTAL THD FOR 4L, 3L2D, AND 6L4D TOPOLOGIES

	4L	3L2D	Proposed		
			SC	DC	MC
i_g	4.45%	5.15%	5.37%	3.04%	2.71%
i_{g1}	–	–	5.49%	5.29%	4.96%

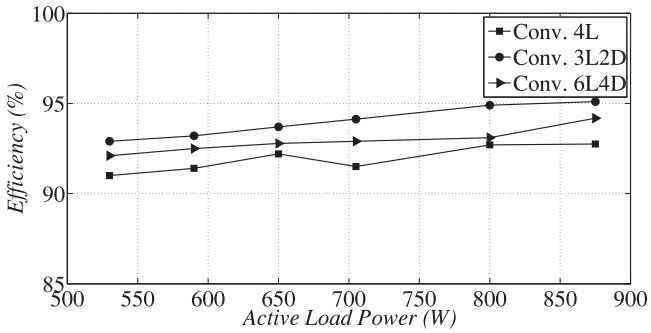

Fig. 15. Measured converter efficiencies of the 6L4D, 3L2D, and 4L configurations for different load conditions.

values are measured with $l_g = l'_g/2$ and $l_l = l'_l/2$. For proposed topology, the three PWM strategies were applied. The best result was obtained for proposed topology with modified carrier PWM. The grid current (i_g) and the internal current (i_{g1}) THD values are noticed as 2.71% and 4.96%, respectively. As expected, the higher THD value was measured to unidirectional 3L2D and 6L4D (with single-carrier PWM) topologies, a similar value was calculated for these topologies. Compared to 4L and 3L2D topologies the improvement of harmonic distortion content was 39% and 48%, respectively.

The efficiency of converters 4L, 3L2D, and 6L4D for different load conditions can be seen in Fig. 15. In order to obtain these results, only *RL* load was applied. The efficiency was obtained considering the same conditions for all the converters. The highest efficiency was obtained for 3L2D converter and the lowest for converter 4L, as expected. The proposed converter presented the highest efficiency of 94.18% at full load conditions and the lowest efficiency of 92.30% at 60.6% of full load conditions. It should be noticed that if the same harmonic distortion is considered for topologies 4L, 3L2D, and 6L4D, the efficiency of the proposed converter will be the highest, since it is necessary to increase the switching frequency of 4L and 3L2D topologies to achieve the same harmonic distortion of the 6L4D topology.

IX. CONCLUSION

A unidirectional parallel single-phase ac–dc–ac converter has been proposed in this paper. It is composed of a single-phase load fed by two parallel single-phase three-leg ac–dc–ac converters with minimized controlled switches without an isolation transformer. In order to improve the performance of the proposed configuration, a modified interleaved PWM technique is presented. The technique ensures five-level voltages at the input and on the output side of the proposed converter, which decreases the THD. It has been demonstrated that, when compared to conventional 4L, 3L, and 3L2D, the proposed converter allows the reduction of the current and the power ratings processed by the power switches and the THD. Also, when compared with topologies 4L and 3L, the proposed topology has reduced semiconductors power losses and, consequently, has better efficiency. These characteristics make the proposed converter suitable for applications such as universal active power filters and UPS. Experimental and simulation results validate the operation of the proposed converter.

REFERENCES

[1] S. K. Biswas, B. Basak, and M. M. Swamy, "A three-phase half-controlled rectifier with pulse width modulation," *IEEE Trans. Ind. Electron.*, vol. 38, no. 2, pp. 121–125, Apr. 1991.
[2] S. Manias, "Novel full bridge semicontrolled switch mode rectifier," *Proc. Inst. Elect. Eng. B—Elect. Power Appl.*, vol. 138, no. 5, pp. 252–256, Sep. 1991.
[3] R. Martinez and P. N. Enjeti, "A high-performance single-phase rectifier with input power factor correction," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 311–317, Mar. 1996.
[4] J. Kikuchi, M. D. Manjrekar, and T. A. Lipo, "Performance improvement of half controlled three phase PWM boost rectifier," in *Proc. 30th Annu. IEEE Power Electron. Spec. Conf. Rec.*, Aug. 1999, vol. 1, pp. 319–324.
[5] A. Karaarslan and I. Iskender, "Analysis and comparison of current control methods on bridgeless converter to improve power quality," *Int. J. Elect. Power Energy Syst.*, vol. 51, pp. 1–13, 2013.
[6] J. C. Pelicer, F. J. M. de Seixas, A. C. de Loureno, and L. d. S. d. C. e Silva, "Novel isolated multi-pulse rectifiers with low current distortion using three-phase half-controlled boost converters," in *Proc. IEEE 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf.*, Nov. 2015, pp. 1–5.
[7] L. Huang, F. Chen, W. Yao, and Z. Lu, "Flexible mode bridgeless boost PFC rectifier with high efficiency over a wide range of input voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3513–3524, May 2017.
[8] D. S. Oliveira, Jr, M. M. Reis, C. E. A. Silva, L. H. S. C. Barreto, F. L. M. Antunes, and B. L. Soares, "A three-phase high-frequency semicontrolled rectifier for PM WECS," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 677–685, Mar. 2010.
[9] Y. Wang, D. Panda, and T. A. Lipo, "Application of a dual-half-controlled-converter in a PMSG wind turbine," in *Proc. 2010 Power Electron. Elect. Drives Autom. Motion*, Jun. 2010, pp. 673–677.
[10] Y. Wang, T. A. Lipo, and D. Pan, "Half-controlled-converter-fed open-winding permanent magnet synchronous generator for wind applications," in *Proc. 14th Int. Power Electron. Motion Control Conf.*, Sep. 2010, pp. T4-123–T4-126.
[11] M. M. Amin and O. A. Mohammed, "Development of a grid-connected wind generation system utilizing high frequency-based three-phase semi-controlled rectifier-current source inverter," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2011, pp. 645–652.
[12] M. M. Amin and O. A. Mohammed, "A three-phase high frequency semi-controlled battery charging power converter for plug-in hybrid electric vehicles," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2011, pp. 2641–2648.
[13] H. Nian and Y. Zhou, "Investigation and suppression of current zero crossing phenomenon for a semicontrolled open-winding PMSG system," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 602–612, Jan. 2017.
[14] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 5–22, Feb. 2005.
[15] I. S. de Freitas, C. B. Jacobina, and E. C. dos Santos Jr, "Single-phase to single-phase full-bridge converter operating with reduced AC power in the dc-link capacitor," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 272–279, Feb. 2010.
[16] H. W. Park, S. J. Park, J. G. Park, and C. U. Kim, "A novel high-performance voltage regulator for single-phase AC sources," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 554–562, Jun. 2001.

[17] J.-H. Choi, J.-M. B. Kwon, J.-H. Jung, and B.-H. Kwon, "High-performance online UPS using three-leg-type converter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 889–897, Jun. 2005.

[18] Y. Lu, G. Xiao, X. Wang, F. Blaabjerg, and D. Lu, "Control strategy for single-phase transformerless three-leg unified power quality conditioner based on space vector modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2840–2849, Apr. 2016.

[19] C. B. Jacobina, N. Rocha, N. S. M. L. Marinus, and E. C. Santos, "AC-AC single-phase dc-link converter with four controlled switches," in *Proc. IEEE 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 1927–1932.

[20] N. S. de Moraes Lima Marinus, C. B. Jacobina, N. Rocha, and E. C. dos Santos, "AC-DC-AC three-phase converter based on three three-leg converters connected in series," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3171–3181, Jul. 2016.

[21] N. B. de Freitas, C. B. Jacobina, N. S. Marinus, and N. Rocha, "AC-DC-AC single-phase multilevel six-leg converter with reduced number of controlled switches," *IEEE Trans. Power Electron.*, 2017, to be published.

[22] J. S. Kim, S. H. Lee, W. J. Cha, and B. H. Kwon, "High-efficiency bridgeless three-level power factor correction rectifier," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1130–1136, Feb. 2017.

[23] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, F. Blaabjerg, and G. Danfoss, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, Mar. 2008.

[24] R. Ramos, D. Biel, E. Fossas, and F. Guinjoan, "Interleaving quasi-sliding-mode control of parallel-connected buck-based inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 11, pp. 3865–3873, Nov. 2008.

[25] Y.-T. Chen, R.-S. Jiang, and R.-H. Liang, "Analysis and design of zero-voltage-switching parallel interleaved current-doubler converters with coupled output inductors," *IET Power Electron.*, vol. 5, no. 4, pp. 467–476, Apr. 2012.

[26] V. Chunkag and U. Kamnarn, "Parallelling three-phase ac to dc converter using CUK rectifier modules based on power balance control technique," *IET Power Electron.*, vol. 3, no. 4, pp. 511–524, Jul. 2010.

[27] S.-Y. Tseng and C.-Y. Hsu, "Interleaved step-up converter with a single-capacitor snubber for PV energy conversion applications," *Int. J. Elect. Power Energy Syst.*, vol. 53, no. 1, pp. 909–922, Dec. 2013.

[28] Z. Ye, D. Boroyevich, J.-Y. Choi, and F. C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 609–615, Sep. 2002.

[29] D. M. Vilathgamuwa, C. J. Gajanayake, and P. C. Loh, "Modulation and control of three-phase paralleled z-source inverters for distributed generation applications," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 173–183, Mar. 2009.

[30] C.-T. Pan and Y.-H. Liao, "Modeling and control of circulating currents for parallel three-phase boost rectifiers with different load sharing," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2776–2785, Jul. 2008.

[31] J. Wang, "Design a parallel buck derived converter system using the primary current droop sharing control," *IET Power Electron.*, vol. 4, no. 5, pp. 491–502, May 2011.

[32] R. P. Singh and A. M. Khambadkone, "Current sharing and sensing in n-paralleled converters using single current sensor," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1212–1219, May/Jun. 2010.

[33] R. M. Cuzner, D. J. Nowak, A. Bendre, G. Oriti, and A. L. Julian, "Mitigating circulating common-mode currents between parallel soft-switched drive systems," *IEEE Trans. Ind. Appl.*, vol. 43, no. 5, pp. 1284–1294, Sep./Oct. 2007.

[34] R. Li and D. Xu, "Parallel operation of full power converters in permanent-magnet direct-drive wind power generation system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1619–1629, Apr. 2013.

[35] Y.-J. Ko, K.-B. Lee, D.-C. Lee, and J.-M. Kim, "Fault diagnosis of three-parallel voltage-source converter for a high-power wind turbine," *IET Power Electron.*, vol. 5, no. 7, pp. 1058–1067, Aug. 2012.

[36] C.-C. Hou, "A multicarrier PWM for parallel three-phase active front-end converters," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2753–2759, Jun. 2013.

[37] Z. Xu, R. Li, H. Zhu, D. Xu, and C. Zhang, "Control of parallel multiple converters for direct-drive permanent-magnet wind power generation systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1259–1270, Mar. 2012.

[38] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Interleaving impact on AC passive components of paralleled three-phase voltage-source converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, May/Jun. 2010.

[39] T. Itkonen, J. Luukko, A. Sankala, T. Laakkonen, and R. Pollanen, "Modeling and analysis of the dead-time effects in parallel PWM two-level three-phase voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2446–2455, Nov. 2009.

[40] N. Genc and I. Iskender, "DSP-based current sharing of average current controlled two-cell interleaved boost power factor correction converter," *IET Power Electron.*, vol. 4, no. 9, pp. 1015–1022, Nov. 2011.

[41] Y.-T. Chen, R.-S. Jiang, and R.-H. Liang, "Analysis and design of zero-voltage-switching parallel interleaved current-doubler converters with coupled output inductors," *IET Power Electron.*, vol. 5, no. 4, pp. 467–476, Apr. 2012.

[42] S. Thamizharasana, J. Baskaranb, S. Ramkumarc, and S. Jeevananthan, "A new dual bridge multilevel dc-link inverter topology," *Int. J. Elect. Power Energy Syst.*, vol. 45, no. 1, pp. 376–383, Feb. 2013.

[43] X. Zhang, Z. Fu, Y. Xiao, G. Wang, and D. Xu, "Control of parallel three-phase PWM converters under generalized unbalanced operating conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3206–3215, Apr. 2017.

[44] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Comparative evaluation of modulation schemes for grid-connected parallel interleaved inverters," in *Proc. IEEE PEDG*, Jun. 2016, pp. 1–8.

[45] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Dual-converter-fed open-end transformer topology with parallel converters and integrated magnetics," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4929–4941, Aug. 2016.

[46] J. Lyu, J. Zhang, X. Cai, H. Wang, and J. Dai, "Circulating current control strategy for parallel full-scale wind power converters," *IET Power Electron.*, vol. 9, no. 4, pp. 639–647, 2016.

[47] N. Rocha, C. Jacobina, E. dos Santos Jr, and R. Cavalcanti, "Parallel single-phase AC/DC/AC shared-leg converters: Modelling, control and analysis," *Int. J. Elect. Power Energy Syst.*, vol. 61, pp. 27–38, 2014.

[48] "IEEE recommended practice for emergency and standby power systems for industrial and commercial applications," *IEEE Std 446-1995 [The Orange Book]*, pp. 1–320, Jul. 1996.

[49] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Optimized integrated harmonic filter inductor for dual-converter-fed open-end transformer topology," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1818–1831, Mar. 2017.

[50] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proc. IEEE*, vol. 82, no. 8, pp. 1194–1214, Aug. 1994.

[51] C. B. Jacobina, A. M. N. Lima, E. R. C. da Silva, R. N. C. Alves, and P. F. Seixas, "Digital scalar pulse-width modulation: A simple approach to introduce non-sinusoidal modulating waveforms," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 351–359, May 2001.

[52] V. K. Chinnaiyana, J. Jeromeb, and J. Karpagam, "An experimental investigation on a multilevel inverter for solar energy applications," *Int. J. Elect. Power Energy Syst.*, vol. 47, no. 1, pp. 157–167, May 2013.

[53] A. K. Panda and Y. Suresh, "Research on cascade multilevel inverter with single dc source by using three-phase transformers," *Int. J. Elect. Power Energy Syst.*, vol. 40, no. 1, pp. 9–20, Sep. 2012.

[54] C. B. Jacobina, M. B. de R. Correa, T. M. Oliveira, A. M. N. Lima, and E. R. C. da Silva, "Current control of unbalanced electrical systems," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 517–525, Jun. 2001.

[55] E. Babaeia, S. H. Hosseinia, and G. B. Gharehpetianb, "Reduction of THD and low order harmonics with symmetrical output current for single-phase ac/ac matrix converters," *Int. J. Elect. Power Energy Syst.*, vol. 32, no. 3, pp. 225–235, Mar. 2010.

[56] D. Holmes and T. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice* (IEEE Press Series on Power Engineering). Hoboken, NJ, USA: Wiley, 2003.

[57] C. B. Jacobina, T. M. Oliveira, and E. R. C. da Silva, "Control of the single-phase three-leg AC/AC converter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 467–476, Apr. 2006.

[58] L. Asiminoaei *et al.*, "Parallel interleaved inverters for reactive power and harmonic compensation," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.

[59] M. Cavalcanti, E. da Silva, D. Boroyevich, W. Dong, and C. Jacobina, "A feasible loss model for IGBT in soft-switching inverters," in *Proc. IEEE 34th Annu. Power Electron. Spec. Conf.*, Jun. 2003, vol. 3, pp. 1845–1850.

[60] J. A. A. Dias, E. C. dos Santos, C. B. Jacobina, and E. R. C. da Silva, "Application of single-phase to three-phase converter motor drive systems with IGBT dual module losses reduction," in *Proc. Brazilian Power Electron. Conf.*, Sep. 2009, pp. 1155–1162.

[61] O. Al-Naseem, R. W. Erickson, and P. Carlin, "Prediction of switching loss variations by averaged switch modeling," in *Proc. 15th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2000, vol. 1, pp. 242–248.

Nady Rocha (M'10) was born in So Gabriel, Bahia, Brazil, in 1982. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Campina Grande, Campina Grande, Brazil, in 2006, 2008, and 2010, respectively.

Since 2011, he has been with the Department of Electrical Engineering, Federal University of Paraíba, João Pessoa, where he is currently an Associate Professor in electrical engineering. His research interests include power electronics, renewable energy sources, and electrical drives.

André Elias Lucena da Costa was born in João Pessoa, Brazil, in 1993. He received the B.S. degree in electrical engineering in 2016 from Federal University of Paraíba, João Pessoa, Brazil, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include power electronics and renewable energy sources.

Cursino Brandão Jacobina (S'78–M'78–SM'98–F'14) was born in Correntes, Pernambuco, Brazil, in 1955. He received the B.S. degree in electrical engineering from the Federal University of Paraiba, Campina Grande, Brazil, in 1978, and the Diplôme d'Etudes Approfondies and the Ph.D. degrees in electrical engineering from the Institut National Polytechnique de Toulouse, Toulouse, France, in 1980 and 1983, respectively.

From 1978 to March 2002, he was with the Department of Electrical Engineering, Federal University of Paraba. Since April 2002, he has been with the Department of Electrical Engineering, Federal University of Campina Grande, Campina Grande, Brazil, where he is currently a Professor in electrical engineering. His research interests include electrical drives, power electronics, and energy systems.