

Operation of Three-Level Inverter-Based Shunt Active Power Filter Under Nonideal Grid Voltage Conditions With Dual Fundamental Component Extraction

Yap Hoon , Mohd Amran Mohd Radzi , *Senior Member, IEEE*, Mohd Khair Hassan ,
and Nashiren Farzilah Mailah, *Member, IEEE*

Abstract—In this paper, a new reference current generation method is proposed for effective harmonics mitigation and reactive power compensation of three-level neutral-point diode clamped inverter-based shunt active power filter (SAPF) under nonideal grid voltage conditions. The proposed method is named as dual fundamental component extraction algorithm. In operation, the proposed algorithm extracts at the same time, the desired fundamental current and voltage components for generating reference current and synchronization phases, respectively. As a result, the proposed algorithm is able to generate reference current that ensures in phase operation of SAPF with the operating power system, without depending on any phase-locked loop elements. Besides, the proposed algorithm employs self-tuning filter (STF) for accurate computation of the fundamental components. Design concept and effectiveness of the proposed algorithm are thoroughly studied and evaluated in MATLAB–Simulink. Additionally, a laboratory prototype utilizing TMS320F28335 digital signal processor is built to validate its feasibility. Encouraging findings obtained from both simulation and experimental works demonstrate effectiveness of the proposed algorithm under both ideal and nonideal grid voltage conditions.

Index Terms—Active power filter (APF), clarke transformation, current harmonics, indirect current controlled (ICC), multilevel inverter, self-tuning filter (STF).

I. INTRODUCTION

HIGH current harmonics in power distribution system caused by extensive applications of nonlinear loads is one of the most significant power quality problems that have attracted tremendous research interests. The presence of harmonic currents in the power system not only degrades overall system efficiency (low-power-factor performance), but also causes other associated problems, which include overheating of

equipment, failures of sensitive devices, and capacitor blowing [1]. Therefore, it is compulsory to install mitigating devices to confine and eliminate harmonic currents generated by the nonlinear loads. In fact, various innovative techniques have been proposed in the literature [2] to reduce the impacts of harmonic currents and major research works have been conducted on control algorithm designs [3].

Shunt active power filter (SAPF) is the most effective mitigation tool which has extensively been applied to alleviate current harmonics problems. Presently, for SAPF applications, multilevel inverters are recognized as a better alternative over standard two-level voltage source inverters due to their superior advantages in terms of better output voltage quality with lower harmonic levels and lower power losses [4], [5]. However, the multilevel inverters employed are mostly restricted to three-level inverters, since controller complexity needed to maintain voltage balance of dc-link capacitors while controlling the complex switching operation of SAPF, increases as the number of level increases [6], [7]. For a three-level neutral-point diode clamped (NPC) inverter, voltage across each of its splitting dc-link capacitors has to equally be maintained at half of its overall dc-link voltage.

Effectiveness of SAPF in current harmonics mitigation is strictly dependent on the accuracy of its reference current generation algorithm. By possessing an accurate reference current, the SAPF should be able to effectively alleviate harmonic problems [7], [8]. Although various methods with unique merits have been proposed for generating reference current [3], [9], [10], time-domain-based approaches especially synchronous reference frame (SRF) [11]–[13] and instantaneous power (pq) theory [14]–[16] are still the predominant methods applied due to their simple implementation features that reduce controller complexity and eventually ease the process for practical implementation.

Despite their simplicity as compared to their counterparts classified under frequency domain category such as fast Fourier transform [5] and learning technique category such as artificial neural network [17], they actually suffer from some potential disadvantages that have restricted the capability of SAPF. For instance, one major drawback of SRF algorithm is the necessity

Manuscript received April 13, 2017; revised July 5, 2017 and August 29, 2017; accepted October 12, 2017. Date of publication October 24, 2017; date of current version June 22, 2018. Recommended for publication by Associate Editor H. Li. (*Corresponding author: Yap Hoon.*)

The authors are with the Faculty of Engineering, Department of Electrical and Electronic Engineering, Universiti Putra Malaysia, Selangor 43400, Malaysia (e-mail: davidhoon0304@hotmail.com; amranmr@upm.edu.my; khair@upm.edu.my; nashiren@upm.edu.my).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TPEL.2017.2766268

of synchronization reference phase, particularly obtained from phase-locked loop (PLL) that requires thorough implementation if the source voltages are unbalanced and/or distorted. Besides, PLL requires implementation of proportional-integral (PI) controller that can properly work only with a proper tuning of its gain parameters [18]. This is a tough and time consuming process as the tuning of PI controller is normally obtained via empirical approach.

In contrast, pq theory algorithm does not involve any PLL elements, but it requires additional voltage processing, and active and reactive power calculation process, and thus, increases computation burden of the designed controller. Moreover, both SRF and pq theory algorithms are still relying on numerical filters [either low-pass filter (LPF) or high-pass filter (HPF)] to obtain their respective current and power components for generating reference current. Nevertheless, LPF is more preferred as it provides better harmonic cancellation effects [3]. However, it is revealed in [7], [16] that numerical LPF still cannot provide accurate fundamental component detection where the detected fundamental component is reported to carry high amount of ripples. Hence, reference current generated in this manner will not be accurate. Besides, a typical LPF can only perform well by having a good compromise between its cutoff frequency and the order of filter, which requires careful consideration and is difficult to be attained.

Both SRF and pq theory algorithms are reported to be effective under ideal (balanced and sinusoidal) and nonideal (unbalanced and/or distorted) source voltage conditions [19], [20]. However, to work effectively under nonideal source voltage conditions, additional self-tuning filter (STF) has to be integrated with the algorithms: for SRF algorithm, STF is applied to improve ability of PLL (referred to here as STF-PLL) [19], and meanwhile for pq theory algorithm, STF is integrated directly with the main algorithm (referred to here as STF-pq) [20]–[22]. It is important to note that, presently, STF has only been adapted to SRF and pq theory algorithms. In operation, STF serves as a voltage processing algorithm where it extracts fundamental components of nonideal source voltages before applying them in the process of generating reference current. From here, it is clear that even though STF has been adapted to SRF and pq theory algorithms, it only allows the algorithms work effectively under nonideal source voltage conditions but it does not alleviate the inherent problems of SRF and pq theory algorithms as described previously.

Another weakness of the existing algorithms is related to the characteristic of their generated reference current. The characteristic of the generated reference current actually determines operation of the subsequent current control algorithm [23]–[25]. For instance, if a nonsinusoidal reference current is provided, the current control algorithm will be operated according to direct current control (DCC) scheme. On the other hand, if a sinusoidal reference current is provided, the current control algorithm will be operated according to indirect current control (ICC) scheme. It is worth noting that the existing SRF [11]–[13], pq theory [14], [15], and STF-pq theory [21], [22] algorithms are still producing a nonsinusoidal reference current based on the extracted harmonic current. In this manner, the desired switching pulses

(generated by current control algorithm) meant for controlling mitigation operation of the SAPF will be generated based on DCC scheme.

As reported in [25]–[27], source current is potentially polluted by switching ripples resulted from switching operation of SAPF, thus, quality of the mitigated source current is degraded. However, DCC scheme that generates switching pulses by comparing a measured injection current (SAPF output current) with a nonsinusoidal reference current (obtained from reference current generation algorithm) [23]–[25], does not possess exact information on the characteristics of the actual source current. Therefore, even if the source current is polluted by the generated switching ripples, DCC scheme is unable to alleviate the problems due to lack of essential information. As a result, mitigated source current with higher total harmonic distortion (THD) value is produced.

Although ICC scheme that operates by comparing the actual source current with a sinusoidal reference current (obtained from reference current generation algorithm) has been demonstrated in [16], [23]–[25], [27] to overcome weaknesses of the DCC scheme, there is still no relevant work on the existing SRF, pq theory, or even STF-pq algorithms that have been conducted together with the ICC scheme. Hence, this work is aimed to filling this gap. Unlike DCC scheme, the ICC scheme that possesses exact information on the characteristic of the actual source current is free from switching ripples problems [16], [25], [27] and, thus, providing superior harmonics mitigation performance.

Therefore, based on the described limitations of the existing SRF and pq theory algorithms, this paper proposes a new time domain-based alternative control algorithm named as dual fundamental component extraction (DFCE) algorithm. The newly proposed algorithm is specifically designed to suit requirements of current control algorithm that operates under ICC scheme. It is able to accurately generate the desired reference current and at the same time provides synchronization phases to ensure effective operation of SAPF even under the influence of nonideal source voltages, without using any PLL elements (as required by the existing SRF algorithm), unnecessary power calculations (as required by the existing pq theory algorithm) and any low-pass filtering processes (as required by both the existing SRF and pq theory algorithms). In addition, it adopts the STF technique for effective operation under nonideal source voltage conditions. Simulation study using MATLAB-Simulink and experimental test utilizing digital signal processor (DSP) are performed to verify and validate design concept and effectiveness of the proposed DFCE algorithm. Moreover, comparative analysis with existing approaches is also performed to investigate improvements achieved by the proposed algorithm.

The rest of the paper is organized as follows. In Section II, a brief review on three existing algorithms for generating reference current of SAPF is provided. Next, in Section III, operation of SAPF is briefly described. Particulars of the proposed algorithm are presented in Section IV with clear illustration. Simulation and experimental findings are presented and thoroughly discussed in Section V and VI respectively. Finally, Section VII concludes significant contributions of this work.

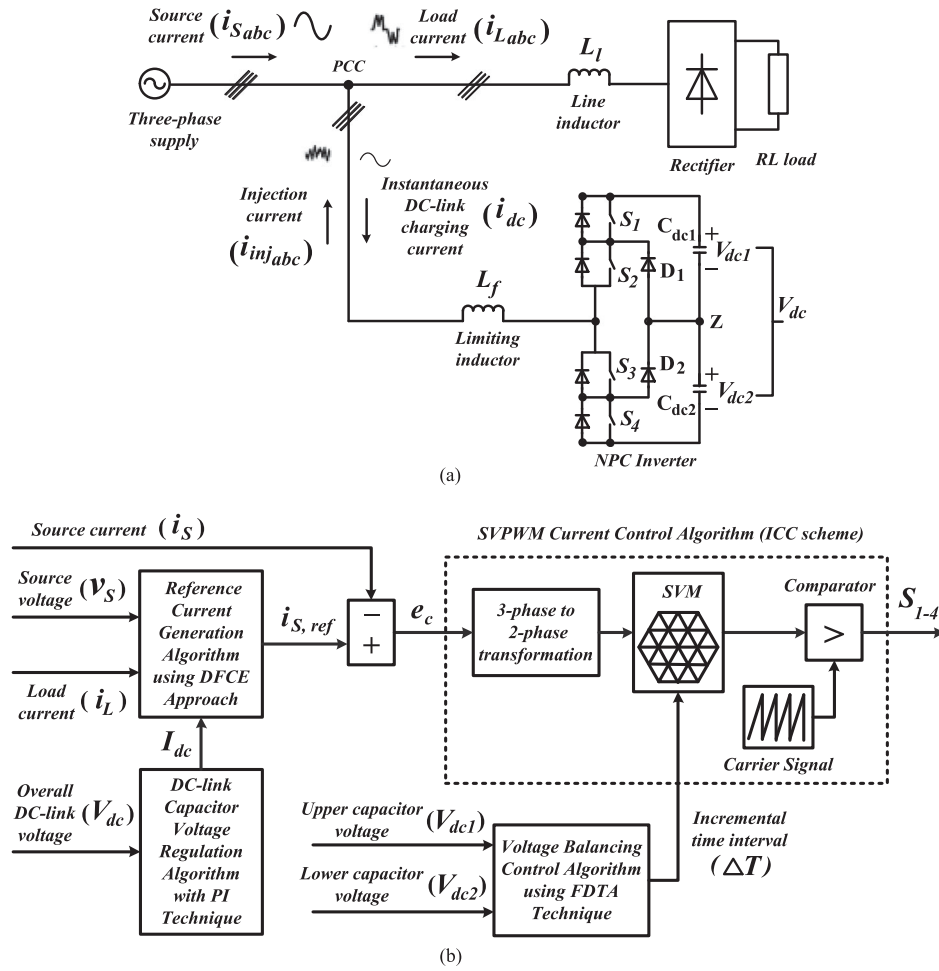


Fig. 1. Three-phase three-level NPC-inverter-based SAPF: (a) circuit configuration and (b) the applied control system showing the reference current generation algorithm and all the other associated algorithms.

II. REVIEW OF TIME DOMAIN-BASED REFERENCE CURRENT GENERATION ALGORITHM

This section briefly reviews three existing time-domain-based reference current generation algorithms of SAPF. The well-known SRF [7], [13] and pq theory [14], [16] algorithms are first described, followed by descriptions of the improved version STF-pq [20], [21] algorithm. The reader is referred to [7], [14], [21] for further details on the described algorithms.

A. SRF Algorithm

SRF is one of the widely applied algorithms in the literature. This algorithm operates based on Park transformation. First, the measured three-phase load currents are transformed into their respective two-phase dq -frame components to separate the fundamental ($i_{Ld(\text{fund})}$ and $i_{Lq(\text{fund})}$) and harmonic ($i_{Ld(\text{har})}$ and $i_{Lq(\text{har})}$) components of the instantaneous load currents (i_{Ld} and i_{Lq}). As mentioned earlier, the main disadvantage of this algorithm is that it requires PLL to determine angular position of the source voltage so as to provide synchronization reference phases for the transformation process. After transforming the load currents into synchronous dq -frame, LPFs are applied to

separate the fundamental and harmonic components. Finally, the desired reference currents are generated by using the extracted harmonic components via inverse Park transformation.

B. Instantaneous Power (pq) Theory Algorithm

Instantaneous power (pq) theory is another well-known algorithm in the literature. This algorithm operates based on Clarke transformation, where the measured three-phase source voltages and load currents are simultaneously transformed into their respective two-phase $\alpha\beta$ representations. Next, the active and reactive powers that also compose of fundamental ($P_{(\text{fund})}$ and $Q_{(\text{fund})}$) and harmonic ($P_{(\text{har})}$ and $Q_{(\text{har})}$) components are calculated. Once calculated, LPFs are applied to separate the fundamental and harmonic components of active and reactive powers. Then, from the harmonic components of active and reactive powers, the harmonic components of load currents ($i_{\alpha(\text{har})}$ and $i_{\beta(\text{har})}$) are derived. Finally, the desired reference currents are generated by using the extracted harmonic components of load currents via inverse Clarke transformation. Since source voltages are involved directly with the calculation process, hence the generated reference current will be working in phase with the operating power system.

C. STF-Based Instantaneous Power (STF-pq Theory Algorithm)

As mentioned in Section I, STF is basically applied to deal with problems caused by nonideality of source voltages. In [20], [21], the STF is integrated with the existing pq theory algorithm to filter out voltage harmonics from the distorted source voltages before applying them in the calculation process of active and reactive powers. At the same time, the STF also operates to balance the filtered voltages. Additionally, another similar STF is applied to extract the harmonic components of load currents ($i_{\alpha(\text{har})}$ and $i_{\beta(\text{har})}$), which are then used together with the distortion-free filtered voltages in the pq theory calculation.

III. CIRCUIT CONFIGURATION AND CONTROL ALGORITHMS OF SAPF

Circuit configuration of the proposed three-phase three-level NPC inverter-based SAPF and its control algorithms are shown in Fig. 1. The SAPF is connected at point of common coupling (PCC) between three-phase source and nonlinear rectifier load. In operation, a typical SAPF injects an opposition current (also known as injection current) back into the polluted power system at PCC to cancel out harmonic currents and improve power factor, and at the same time drawing the necessary instantaneous dc-link charging current i_{dc} to regulate its switching losses. Based on Fig. 1(b), it is clear that effective operation of SAPF requires complete cooperation from its control algorithms that include reference current generation, dc-link capacitor voltage regulation, neutral-point voltage deviation, and current control algorithms.

Nevertheless, this paper focuses solely on reference current generation algorithm where a new control algorithm named as DFCE is proposed. For dc-link capacitor voltage regulation algorithm, PI technique [28] is applied. Next, neutral-point voltage deviation control algorithm with fuzzy-based dwell time allocation technique [29] is employed to maintain voltage balance of splitting dc-link capacitors. Basically, it delivers an appropriate incremental time interval ΔT with respect to the instantaneous voltages across each splitting dc-link capacitor (V_{dc1} and V_{dc2}), to maintain equal inflow and outflow of current at neutral-point Z. Finally, a 25-kHz space vector pulse width modulation (PWM) current control algorithm [30], [31] that operates based on the ICC scheme is adopted to govern switching operation of SAPF.

IV. DFCE ALGORITHM

The working principle of the proposed DFCE algorithm is shown in Fig. 2. Basically, the structure of DFCE composes of two STF-based fundamental component extraction parts that are executed simultaneously: the lower part (fundamental current extraction) generates the required reference current, and the upper part (fundamental voltage extraction) serves as synchronization algorithm to coordinate the phase of the generated reference current with respect to the phase of the operating power system.

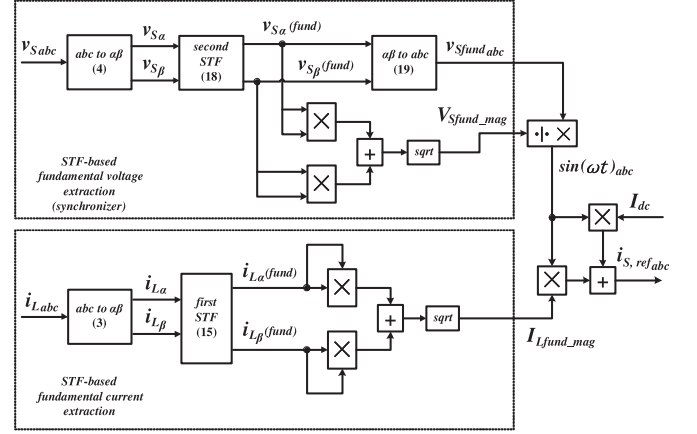


Fig. 2. Reference current generation algorithm based on DFCE.

The fundamental component extraction processes are performed in $\alpha\beta$ -frame where the measured three-phase load currents and source voltages are first transformed into their respective two-phase $\alpha\beta$ representation by using Clarke-transform matrix as follows:

$$\mathbf{T}_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} \cos \theta_1(t) & \cos \theta_2(t) & \cos \theta_3(t) \\ \sin \theta_1(t) & \sin \theta_2(t) & \sin \theta_3(t) \end{bmatrix} \quad (1)$$

where

$$\theta_{ph}(t) = \theta(t) + \frac{2\pi}{3}(ph - 1), \quad ph = 1, 2, 3 \quad (2)$$

and $\theta(t)$ is an angular arbitrary function and is considered as $\theta(t) = 0$.

Let the measured three-phase load currents and source voltages expressed in matrix form be $i_{Labc} = [i_a \ i_b \ i_c]^T$ and $v_{Sabc} = [v_a \ v_b \ v_c]^T$ respectively. Hence, their corresponding $\alpha\beta$ representations can be expressed as

$$\begin{bmatrix} i_\alpha & i_\beta \end{bmatrix}^T = \mathbf{T}_{\alpha\beta} i_{Labc} \quad (3)$$

$$\begin{bmatrix} v_\alpha & v_\beta \end{bmatrix}^T = \mathbf{T}_{\alpha\beta} v_{Sabc}. \quad (4)$$

Under the influences of nonlinear loads, load currents in $\alpha\beta$ -frame actually can be decomposed into fundamental (fund) and harmonic (har) components as follows:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \begin{bmatrix} i_{L\alpha(\text{fund})} + i_{L\alpha(\text{har})} \\ i_{L\beta(\text{fund})} + i_{L\beta(\text{har})} \end{bmatrix} \quad (5)$$

where $i_{L\alpha(\text{fund})}$ and $i_{L\beta(\text{fund})}$ represent the fundamental components of load currents in $\alpha\beta$ -frame, and meanwhile $i_{L\alpha(\text{har})}$ and $i_{L\beta(\text{har})}$ represent the distorted components of load currents in $\alpha\beta$ -frame.

For generating reference current, both fundamental load current $i_{L\alpha(\text{fund})}$ and $i_{L\beta(\text{fund})}$ components are required and they are extracted using STF. Basically, the transfer function of STF can be derived from integration process of the SRF as follow [32]–[34]:

$$V_{xy}(t) = e^{j\omega t} \int e^{-j\omega t} U_{xy}(t) dt \quad (6)$$

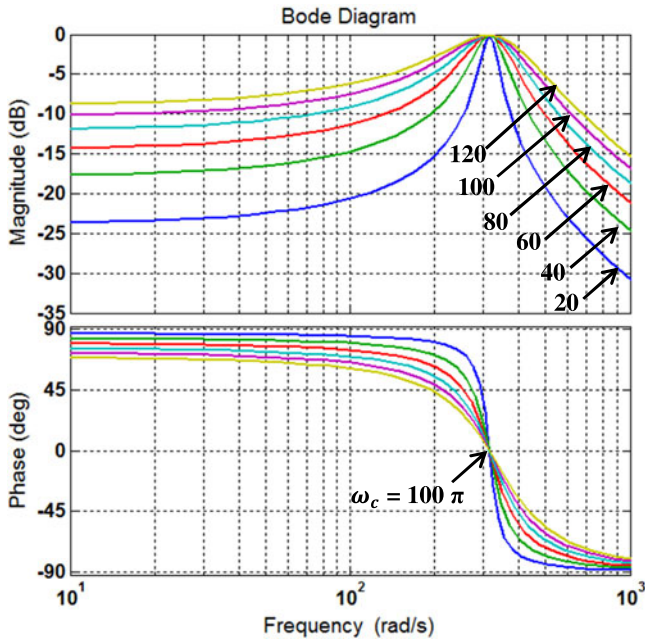


Fig. 3. Bode diagram of STF for different values of parameter K ($\omega_c = 100 \pi$ rad/s).

where $U_{xy}(t)$ and $V_{xy}(t)$ represent the instantaneous signal before and after integration process, and ω is the angular frequency of the signal.

Next, by performing Laplace transformation on the input $U_{xy}(t)$ and output $V_{xy}(t)$ signals, transfer function as follow can be obtained. It is important to note that $U_{xy}(t)$ and $V_{xy}(t)$ can be either current or voltage signals

$$H(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = \frac{s + j\omega}{s^2 + \omega^2}. \quad (7)$$

For the purpose of reference current generation in SAPF applications, an additional constant K is added in $H(s)$ [35]–[37] to restrict its magnitude at unity for $\omega = \omega_c$. Concurrently, the phase delay will be equal to zero at that particular angular cutting frequency ω_c . After adding the constant K , (7) can be rewritten as

$$H(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = K \frac{(s + K) + j\omega_c}{(s + K)^2 + \omega_c^2}. \quad (8)$$

The filtering performance of STF is strictly dependent on the value of parameter K . Fig. 3 shows frequency response of the STF tuned at $\omega_c = 100 \pi$ rad/s, for values of parameter K ranging from 20 to 120. It can be observed that the magnitude of STF is limited at $|H(s)| = 0$ dB and there is no phase displacement introduced by STF at ω_c . In other words, STF is able to perform without any phase delay and amplitude changing [21], [34], [36]. Moreover, it is also clear that selectivity of STF is better with smaller value of K . Furthermore, by taking inverse Laplace transform of (8), the time constant of STF is found to be equal to $1/K$ [21], [34]. Therefore, the dynamic response of STF improves (shorter response time) with larger value of K . Since, parameter K affects both selectivity and dynamic response of STF, hence it must carefully be selected for

achieving a good compromise between the selectivity and dynamic response, so as to ensure optimum performance of STF.

Transfer function $H(s)$ in (8) can be further expanded as

$$\begin{aligned} H(s) &= \frac{V_x(s) + jV_y(s)}{U_x(s) + jU_y(s)} \\ &= K \frac{(s + K) + j\omega_c}{(s + K)^2 + \omega_c^2} \end{aligned} \quad (9)$$

$$\begin{aligned} V_x(s) + jV_y(s) &= K \left(\frac{(s + K)}{(s + K)^2 + \omega_c^2} \right. \\ &\quad \left. + \frac{j\omega_c}{(s + K)^2 + \omega_c^2} \right) (U_x(s) + jU_y(s)). \end{aligned} \quad (10)$$

Next, by equating the real and imaginary parts, the following expression can be obtained:

$$V_x(s) = \frac{K(s + K)}{(s + K)^2 + \omega_c^2} U_x(s) - \frac{K\omega_c}{(s + K)^2 + \omega_c^2} U_y(s) \quad (11)$$

$$V_y(s) = \frac{K(s + K)}{(s + K)^2 + \omega_c^2} U_y(s) + \frac{K\omega_c}{(s + K)^2 + \omega_c^2} U_x(s). \quad (12)$$

Finally, by solving (11) and (12) simultaneously, they can further be simplified as

$$V_x(s) = \frac{K}{s} (U_x(s) - V_x(s)) - \frac{\omega_c}{s} V_y(s) \quad (13)$$

$$V_y(s) = \frac{K}{s} (U_y(s) - V_y(s)) + \frac{\omega_c}{s} V_x(s). \quad (14)$$

Here, for extracting fundamental load current $i_{L\alpha(\text{fund})}$ and $i_{L\beta(\text{fund})}$, the output signals $V_x(s)$ and $V_y(s)$ are replaced with $i_{L\alpha(\text{fund})}(s)$ and $i_{L\beta(\text{fund})}(s)$, respectively, and meanwhile the input signals $U_x(s)$ and $U_y(s)$ are replaced with $i_{L\alpha}(s)$ and $i_{L\beta}(s)$, respectively. As a result, transfer function of STF (for fundamental load current extraction) can be expressed and simplified as follows:

$$\begin{aligned} \begin{bmatrix} i_{L\alpha(\text{fund})}(s) \\ i_{L\beta(\text{fund})}(s) \end{bmatrix} &= \frac{K_1}{s} \begin{bmatrix} i_{L\alpha}(s) - i_{L\alpha(\text{fund})}(s) \\ i_{L\beta}(s) - i_{L\beta(\text{fund})}(s) \end{bmatrix} \\ &\quad + \frac{2\pi f_c}{s} \begin{bmatrix} -i_{L\beta(\text{fund})}(s) \\ i_{L\alpha(\text{fund})}(s) \end{bmatrix} \end{aligned} \quad (15)$$

where K_1 is a constant gain parameter and f_c is the cutting frequency. For the sole purpose of fundamental load current components extraction, STF is revealed to perform effectively for K_1 set between the ranges of 20–100, and f_c fixed at 50 Hz [20], [21]. Note that parameter K is relabeled as K_1 to indicate that it is applied for fundamental load current components extraction purposes.

With the extracted $i_{L\alpha(\text{fund})}$ and $i_{L\beta(\text{fund})}$, magnitude $I_{L\text{fund_mag}}$ of the desired sinusoidal reference current $i_{S, \text{ref}abc}$ is computed according to the following approach:

$$I_{L\text{fund_mag}} = \sqrt{i_{L\alpha(\text{fund})}^2 + i_{L\beta(\text{fund})}^2}. \quad (16)$$

TABLE I
COMPARISON AND EVALUATION OF REFERENCE CURRENT GENERATION ALGORITHMS

Features	Reference current generation algorithms			
	SRF [7], [13]	pq theory [14], [16]	STF-pq [20], [21]	The proposed DFCE
Characteristic of the generated reference current	Nonsinusoidal (suit DCC scheme)	Nonsinusoidal (suit DCC scheme)	Nonsinusoidal (suit DCC scheme)	Sinusoidal (suit ICC scheme)
Number of numerical filters required	2 LPFs	1 LPF or 2 HPFs	No	No
Additional elements/calculations required	PLL for synchronization purpose	Voltage preprocessing, active and reactive power computation	STF, voltage preprocessing, active and reactive power computation	STF, voltage preprocessing
Effectiveness under ideal source voltage	Yes	Yes	Yes	Yes
Effectiveness under non-ideal source voltage	No	No	Yes	Yes
Applied for selective harmonic mitigation	No	No	No	No
Advantages	Easily implementable, and most appropriate for harmonic mitigation under ideal source voltage condition	Easily implementable, does not require PLL, and effective performance under ideal source voltage condition	Does not require LPF, HPF, PLL, and effective performance under both ideal and nonideal source voltage conditions	Does not require LPF, HPF, PLL and power calculations (simplest structure), better mitigation performance due to implementation with ICC scheme, and effective performance under both ideal and non-ideal source voltage conditions.
Disadvantages	Require additional PLL element, suffer from time delay due to dependency on numerical filters, and not effective under nonideal source voltage conditions	Computational burden is higher than SRF due to additional voltage and power calculations, suffer from time delay due to dependency on numerical filters, and not effective under nonideal source voltage conditions	Computational burden is higher than pq theory due to additional STF elements, and require careful tuning of STF's gain parameter for effective operation.	Careful tuning of STF's gain parameter is required for effective operation.

On the other hand, under nonideal source voltage conditions, the measured source voltages that have been transformed into $\alpha\beta$ -frame can also be decomposed into fundamental and harmonic components. Hence, from (4), the source voltages in $\alpha\beta$ -frame can be rewritten as

$$\begin{bmatrix} v_{S\alpha} \\ v_{S\beta} \end{bmatrix} = \begin{bmatrix} v_{S\alpha(\text{fund})} + v_{S\alpha(\text{har})} \\ v_{S\beta(\text{fund})} + v_{S\beta(\text{har})} \end{bmatrix} \quad (17)$$

where $v_{S\alpha(\text{fund})}$ and $v_{S\beta(\text{fund})}$ denote the fundamental components of source voltage in $\alpha\beta$ -frame, and meanwhile $v_{S\alpha(\text{har})}$ and $v_{S\beta(\text{har})}$ refer to the distorted components of source voltage in $\alpha\beta$ -frame. The distorted components are the components existed due to nonideality of source voltages and must be removed to obtain the desired synchronization phases.

For generating the synchronization phases, another STF is adopted to extract the desired fundamental source voltage $v_{S\alpha(\text{fund})}$ and $v_{S\beta(\text{fund})}$ components. In this case, from (13) and (14), by replacing the output signals $V_x(s)$ and $V_y(s)$ with $v_{S\alpha(\text{fund})}(s)$ and $v_{S\beta(\text{fund})}(s)$, respectively, and the input signals $U_x(s)$ and $U_y(s)$ with $v_{S\alpha}(s)$ and $v_{S\beta}(s)$, respectively, transfer function of the second STF (for fundamental source voltage extraction) can be expressed and simplified as follows:

$$\begin{bmatrix} v_{S\alpha(\text{fund})}(s) \\ v_{S\beta(\text{fund})}(s) \end{bmatrix} = \frac{K_2}{s} \begin{bmatrix} v_{S\alpha}(s) - v_{S\alpha(\text{fund})}(s) \\ v_{S\beta}(s) - v_{S\beta(\text{fund})}(s) \end{bmatrix} + \frac{2\pi f_c}{s} \begin{bmatrix} -v_{S\beta(\text{fund})}(s) \\ v_{S\alpha(\text{fund})}(s) \end{bmatrix}. \quad (18)$$

Similarly, for effective performance of STF in extracting fundamental component of source voltages, K_2 should also be set between the range of 20–100 and f_c fixed at 50 Hz [20], [21]. Note that parameter K in this case, is relabeled as K_2 to indicate that it is applied for fundamental source voltage components extraction purposes. Nevertheless, for optimum filtering performance of the adopted STFs, a small study is conducted to determine the best K_1 and K_2 values with reference to the reported gain ranges.

With the extracted $v_{S\alpha(\text{fund})}$ and $v_{S\beta(\text{fund})}$, inverse Clarke transformation as expressed in (19) is executed to transform the extracted fundamental component of source voltages in $\alpha\beta$ -frame back into its three-phase representation $v_{S\text{fund } abc}$

$$\begin{bmatrix} v_{S\text{fund } a} \\ v_{S\text{fund } b} \\ v_{S\text{fund } c} \end{bmatrix} = \mathbf{T}_{\alpha\beta}^T \begin{bmatrix} v_{S\alpha(\text{fund})} \\ v_{S\beta(\text{fund})} \end{bmatrix}. \quad (19)$$

At the same time, $v_{S\alpha(\text{fund})}$ and $v_{S\beta(\text{fund})}$ are used to calculate the required amplitude $V_{S\text{fund } \text{mag}}$ of $v_{S\text{fund } abc}$ according to the following approach:

$$V_{S\text{fund } \text{mag}} = \sqrt{v_{S\alpha(\text{fund})}^2 + v_{S\beta(\text{fund})}^2}. \quad (20)$$

With the availability of $v_{S\text{fund } abc}$ and $V_{S\text{fund } \text{mag}}$, the desired synchronization phases $\sin(\omega t)_{abc}$ can be obtained according to

TABLE II
PARAMETERS SPECIFICATIONS OF THE PROPOSED SAPF

Parameter	Value	Unit
Fundamental source voltage (rms)	400 (line to line)	V
Fundamental frequency	50	Hz
DC-link capacitor	3300 (each)	μ F
Reference overall dc-link voltage	880	V
Limiting inductor	5	mH
Switching frequency	25	kHz

the following approach:

$$\begin{aligned} \sin(\omega t)_{abc} &= \left[\sin(\omega t) \quad \sin\left(\omega t - \frac{2\pi}{3}\right) \quad \sin\left(\omega t + \frac{2\pi}{3}\right) \right]^T \\ &= \frac{v_{Sfund\ abc}}{V_{Sfund_mag}}. \end{aligned} \quad (21)$$

Since the synchronization phases are obtained by processing directly the source voltages, hence the phases obtained in this manner will be equivalent to the actual phases of the operating power system. In other words, it can track the angular position of the operating power system. Finally, by using the generated synchronization phases $\sin(\omega t)_{abc}$, and together with I_{Lfund_mag} [obtained from (16)] as well as magnitude I_{dc} of instantaneous dc-link charging current i_{dc} (delivered by dc-link capacitor voltage regulation algorithm), the desired sinusoidal reference current $i_{S,ref\ abc}$ is generated according to the following approach:

$$i_{S,ref\ abc} = [I_{Lfund_mag} + I_{dc}] \sin(\omega t)_{abc}. \quad (22)$$

In this manner, the desired reference current can accurately be generated under any scenario of source voltages (both ideal and nonideal) and, thus, granting the proposed DFCE algorithm and also the connected SAPF, the ability to work effectively under nonideal source voltage conditions. Moreover, owing to the sinusoidal characteristic of the generated reference current $i_{S,ref\ abc}$, the designated SAPF is controlled under ICC scheme that enhances its mitigation performance.

For better clarification on the benefits of the proposed DFCE algorithm, the features of the proposed DFCE algorithm and the three existing time-domain-based reference current generation algorithms are compared and contrasted in an organized manner, as summarized in Table I.

V. SIMULATION RESULTS

Simulation model of the proposed SAPF and its control algorithms are developed and evaluated in MATLAB–Simulink. Table II summarizes the details of the proposed SAPF's parameters. To evaluate performance of the newly proposed DFCE algorithm, comprehensive simulation studies are performed by considering four cases of source voltages: in case 1, balanced-sinusoidal source voltage, in case 2, harmonic-distorted source voltage, in case 3, unbalanced-sinusoidal source voltage, and in case 4, unbalanced-distorted source voltage. The specifications of the applied source voltages are given as follows.

Case 1: Balanced-sinusoidal source voltage (THDa = THDb = THDc = 0.00%)

$$\begin{aligned} v_{S_a} &= 326 \sin(\omega t) \\ v_{S_b} &= 326 \sin(\omega t - 120^\circ) \\ v_{S_c} &= 326 \sin(\omega t + 120^\circ). \end{aligned} \quad (23)$$

Case 2: Harmonic-distorted source voltage (THDa = THDb = THDc = 32.17%)

$$\begin{aligned} v_{S_a} &= 326 \sin(\omega t) + 80 \sin(3\omega t) + 60 \sin(5\omega t) \\ &\quad + 30 \sin(7\omega t) + 10 \sin(9\omega t) \\ v_{S_b} &= 326 \sin(\omega t - 120^\circ) + 80 \sin(3(\omega t - 120^\circ)) \\ &\quad + 60 \sin(5(\omega t - 120^\circ)) \\ &\quad + 30 \sin(7(\omega t - 120^\circ)) + 10 \sin(9(\omega t - 120^\circ)) \\ v_{S_c} &= 326 \sin(\omega t + 120^\circ) + 80 \sin(3(\omega t + 120^\circ)) \\ &\quad + 60 \sin(5(\omega t + 120^\circ)) \\ &\quad + 30 \sin(7(\omega t + 120^\circ)) + 10 \sin(9(\omega t + 120^\circ)). \end{aligned} \quad (24)$$

Case 3: Unbalanced-sinusoidal source voltage (THDa = THDb = THDc = 0.00%)

$$\begin{aligned} v_{S_a} &= 326 \sin(\omega t) \\ v_{S_b} &= 286 \sin(\omega t - 120^\circ) \\ v_{S_c} &= 366 \sin(\omega t + 120^\circ). \end{aligned} \quad (25)$$

Case 4: Unbalanced-distorted source voltage (THDa = 14.71%, THDb = 17.48%, and THDc = 17.92%)

$$\begin{aligned} v_{S_a} &= 326 \sin(\omega t) + 30 \sin(3\omega t - 120^\circ) \\ &\quad + 20 \sin(5\omega t + 120^\circ) + 30 \sin(7\omega t) \\ &\quad + 10 \sin(9\omega t - 120^\circ) \\ v_{S_b} &= 286 \sin(\omega t - 120^\circ) + 40 \sin(3\omega t) \\ &\quad + 20 \sin(5\omega t + 120^\circ) + 20 \sin(7\omega t - 120^\circ) \\ &\quad + 10 \sin(9\omega t + 120^\circ) \\ v_{S_c} &= 366 \sin(\omega t + 120^\circ) + 50 \sin(3\omega t) + 40 \sin(5\omega t) \\ &\quad + 10 \sin(7\omega t - 120^\circ) \\ &\quad + 10 \sin(9\omega t + 120^\circ). \end{aligned} \quad (26)$$

An inductive nonlinear load is constructed using a three-phase uncontrolled bridge rectifier feeding a series connected 50 Ω resistor and 50-mH inductor. Comparative analysis is also conducted to investigate improvements achieved by the proposed DFCE algorithm in comparison to the existing SRF, pq theory, and STF-pq algorithms. The main performance parameter used to evaluate effectiveness of the proposed DFCE algorithm is the THD value of mitigated source current that must be maintained within the 5% limit set by IEEE Standard 519-2014.

Initially, a small study on selecting the best gain values (K_1 and K_2) for the applied STF is conducted. The study is con-

TABLE III
OBSERVATION TIME TO OBTAIN STABLE INJECTION CURRENT AND THD VALUE OF MITIGATED SOURCE CURRENT OBTAINED FOR SPECIFIED GAIN

K_1 and K_2	Inductive load	
	Time (s)	THDa (%)
20	0.20	2.20
30	0.14	2.90
40	0.12	2.27
50	0.10	1.73
60	0.08	1.87
70	0.06	2.37
80	0.05	1.74
90	0.04	1.75
100	0.04	2.76
110	0.03	2.22
120	0.03	2.24

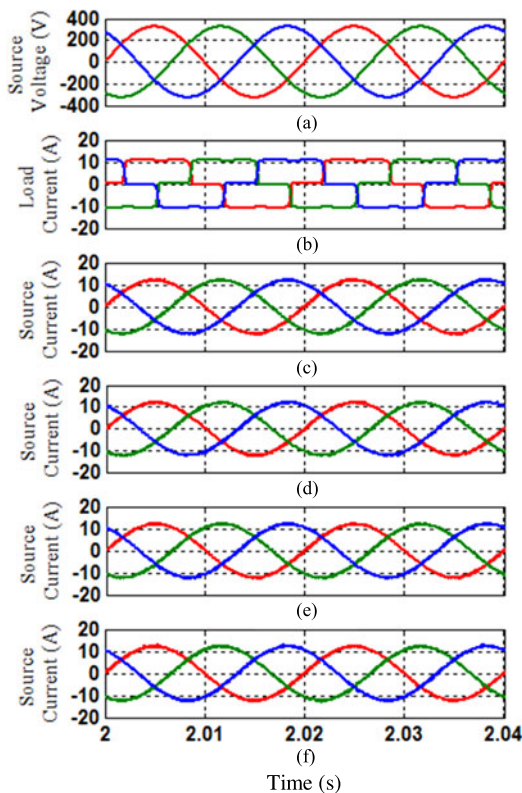


Fig. 4. Steady-state simulation waveforms (case 1) of SAPF, which include three-phase (a) source voltages v_S , (b) load currents i_L , (c) source currents i_S resulted from SRF algorithm, (d) source currents i_S resulted from pq theory algorithm, (e) source currents i_S resulted from STF-pq algorithm, and (f) source currents i_S resulted from DFCE algorithm.

ducted considering only case 1 balanced sinusoidal source voltages. Table III summarizes the observations regarding the time taken for DFCE algorithm to successfully form a stable injection current i_{inj} , and the THD measurements recorded for the mitigated source current i_S when K_1 and K_2 values are varied from 20 to 120. The findings are revealed to satisfy the theoretical characteristic of STF (as discussed in Section IV), where larger K_1 and K_2 values lead to shorter response time of STF. From Table III, the best K_1 and K_2 values are found at 90 where the time taken (response time) by the algorithm is only two

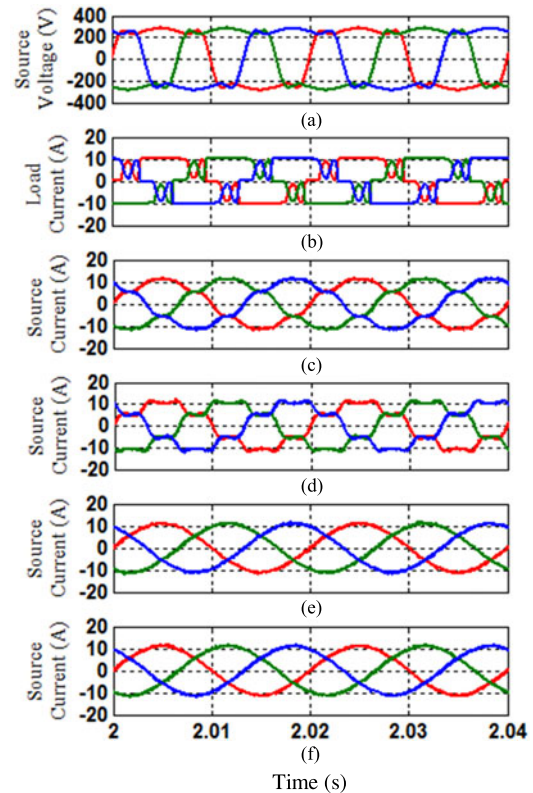


Fig. 5. Steady-state simulation waveforms (case 2) of SAPF, which include three-phase (a) source voltages v_S , (b) load currents i_L , (c) source currents i_S resulted from SRF algorithm, (d) source currents i_S resulted from pq theory algorithm, (e) source currents i_S resulted from STF-pq algorithm, and (f) source currents i_S resulted from DFCE algorithm.

cycles and the measured THD in within the allowable limits. Although a larger gain value can provide a quicker formation of stable injection currents i_{inj} , the THD of the mitigated source currents i_S is revealed to be higher. This is due to the fact that a larger gain value degrades the selectivity of STF [20], [21], [34]. Hence, the selected gain value should be as small as possible after considering the best time taken and THD values achieved.

Steady-state simulation waveforms of SAPF that includes three-phase source voltages v_S , load currents i_L , and source currents i_S mitigated by SAPF utilizing different reference current generation algorithms, obtained for cases 1, 2, 3, and 4 are shown in Figs. 4, 5, 6, and 7, respectively. Meanwhile, the corresponding THD values of source current i_S recorded before and after mitigation by the SAPF, for each source voltage condition are tabulated in Table IV.

From the findings, under balanced-sinusoidal (case 1) source voltage condition (refer Fig. 4), it is clear that the source currents i_S are well mitigated by SAPF utilizing each reference current generation algorithm. From Table IV, it can be observed that the THD values of source currents i_S are reduced from 27.34% to around 2%, and thus, complying with the allowable 5% limit. However, SAPF with the proposed DFCE algorithm performs outstandingly by achieving the lowest THD values as compared to the other algorithms.

Next, under harmonic-distorted (case 2) source voltage condition (refer Fig. 5), it can be observed that the performance of

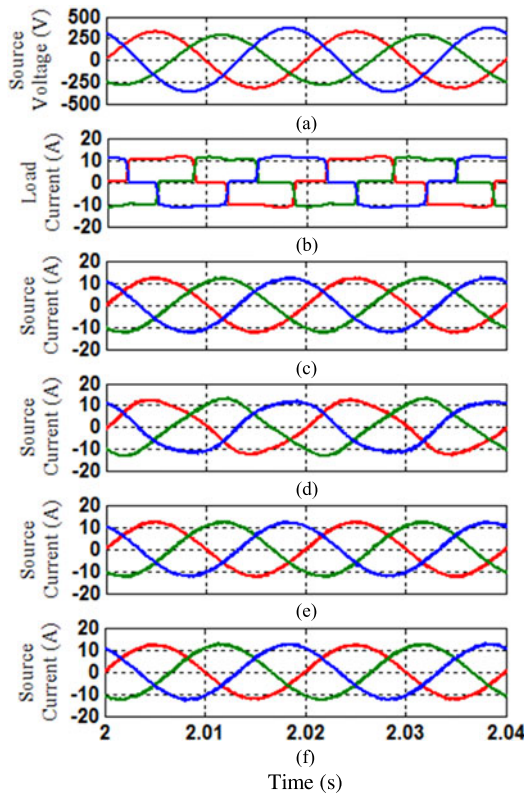


Fig. 6. Steady-state simulation waveforms (case 3) of SAPF, which include three-phase (a) source voltages v_S , (b) load currents i_L , (c) source currents i_S resulted from SRF algorithm, (d) source currents i_S resulted from pq theory algorithm, (e) source currents i_S resulted from STF-pq algorithm, and (f) source currents i_S resulted from DFCE algorithm.

both SRF and pq theory algorithms are not acceptable. As shown in Table IV, the THD values of source currents i_S are reduced from 33.54% to around 10% with the SRF algorithm [refer Fig. 5(c)] and around 20% with the pq theory algorithm [refer Fig. 5(d)]. However, by utilizing the STF technique, both STF-pq and the proposed DFCE algorithms are observed to perform effectively under harmonic-distorted source voltage condition. The THD values recorded are around 2.9% with STF-pq [refer Fig. 5(e)] and 2.4% with DFCE [refer Fig. 5(f)] algorithms.

Furthermore, under unbalanced-sinusoidal (case 3) source voltage condition (refer Fig. 6), it can be observed that all the reference current generation algorithms perform well except pq theory algorithm. Specifically, as shown in Table IV, the THD values of source currents i_S obtained by the pq theory algorithm [refer Fig. 6(d)] is around 8%, where it fails to comply with the IEEE standard 519-2014. Meanwhile, SRF [refer Fig. 6(c)] and STF-pq [refer Fig. 6(e)] algorithms manage to reduce the THD values to around 3%. Most importantly, the proposed DFCE algorithm [refer Fig. 6(f)] provides the best mitigation performance by achieving the lowest THD values of around 2%.

Finally, under unbalanced-distorted (case 4) source voltage condition (refer Fig. 7), it can be observed that the performance of both SRF and pq theory algorithms are once again not acceptable. Based on Table IV and by focusing on phase a source current i_{S_a} , the THD value recorded is 8.11% with the SRF algorithm [refer Fig. 7(c)] and 14.66% with the pq theory algorithm

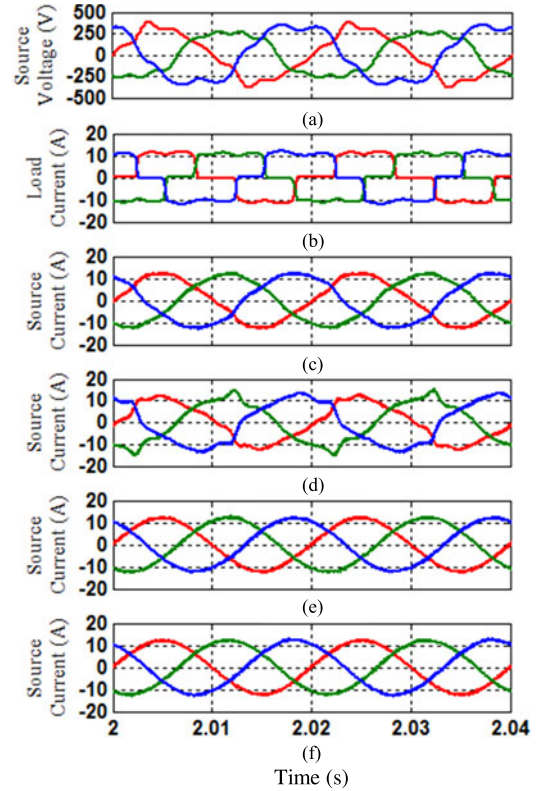


Fig. 7. Steady-state simulation waveforms (case 4) of SAPF, which include three-phase (a) source voltages v_S , (b) load currents i_L , (c) source currents i_S resulted from SRF algorithm, (d) source currents i_S resulted from pq theory algorithm, (e) source currents i_S resulted from STF-pq algorithm, and (f) source currents i_S resulted from DFCE algorithm.

[refer Fig. 7(d)]. However, the integration of STF technique has once again granted both STF-pq and the proposed DFCE algorithms, the ability to work effectively under unbalanced-distorted source voltage condition. The THD value recorded for phase a source current i_{S_a} is 2.96% with the STF-pq [refer Fig. 7(e)] and 2.40% with the DFCE [refer Fig. 7(f)] algorithms.

Additionally, graphical presentation on the THD values of source current i_S mitigated by SAPF using different reference current generation algorithms, for phases a , b , and c is shown, respectively, in Figs. 8(a)–(c), to provide a clearer observation on the performance of each reference current generation algorithm.

As an overall, the existing SRF and pq theory algorithms are observed to work effectively under ideal (balanced and sinusoidal) source voltage conditions but their performance are poor when the source voltage is nonideal (unbalanced and/or distorted). In other words, the nonideal source conditions have significantly degraded the performance of SAPF while using the existing SRF and pq theory algorithms. Nevertheless, this problem actually has been addressed in the literature with the development of STF-pq algorithm [20]–[22]. Besides, the simulation findings obtained in this study also supported the effectiveness of the existing STF-pq algorithm under both ideal and nonideal source voltage conditions. However, the important finding of this study is that mitigation performance of SAPF while using the proposed DFCE algorithm is revealed to be better than the existing STF-pq algorithm. Moreover, for all four cases of source

TABLE IV
THDS OF SOURCE CURRENT OBTAINED UNDER SPECIFIED CASES OF SOURCE VOLTAGE CONDITIONS FOR EACH REFERENCE CURRENT GENERATION ALGORITHM (SIMULATION RESULTS)

Source voltage conditions	Current THDs of the phases, (%)											
	SRF [13]			pq theory [14]			STF-pq [21]			DFCE		
	<i>a</i>	<i>b</i>	<i>c</i>	<i>a</i>	<i>b</i>	<i>c</i>	<i>a</i>	<i>b</i>	<i>c</i>	<i>a</i>	<i>b</i>	<i>c</i>
Before Connecting SAPF												
Case 1	27.34	27.34	27.34	27.34	27.34	27.34	27.34	27.34	27.34	27.34	27.34	27.34
Case 2	33.54	33.54	33.54	33.54	33.54	33.54	33.54	33.54	33.54	33.54	33.54	33.54
Case 3	27.84	30.47	24.27	27.84	30.47	24.27	27.84	30.47	24.27	27.84	30.47	24.27
Case 4	33.53	25.56	27.78	33.53	25.56	27.78	33.53	25.56	27.78	33.53	25.56	27.78
After Connecting SAPF												
Case 1	2.12	2.09	2.05	2.32	2.21	2.23	2.03	1.95	2.00	1.75	1.73	1.70
Case 2	10.69	10.74	10.80	20.77	20.66	20.74	2.89	2.90	2.94	2.41	2.43	2.44
Case 3	3.13	3.27	3.23	8.02	7.93	8.01	2.75	2.75	2.81	2.02	1.85	2.04
Case 4	8.11	5.29	7.19	14.66	12.72	14.86	2.96	2.29	2.76	2.40	2.00	2.15

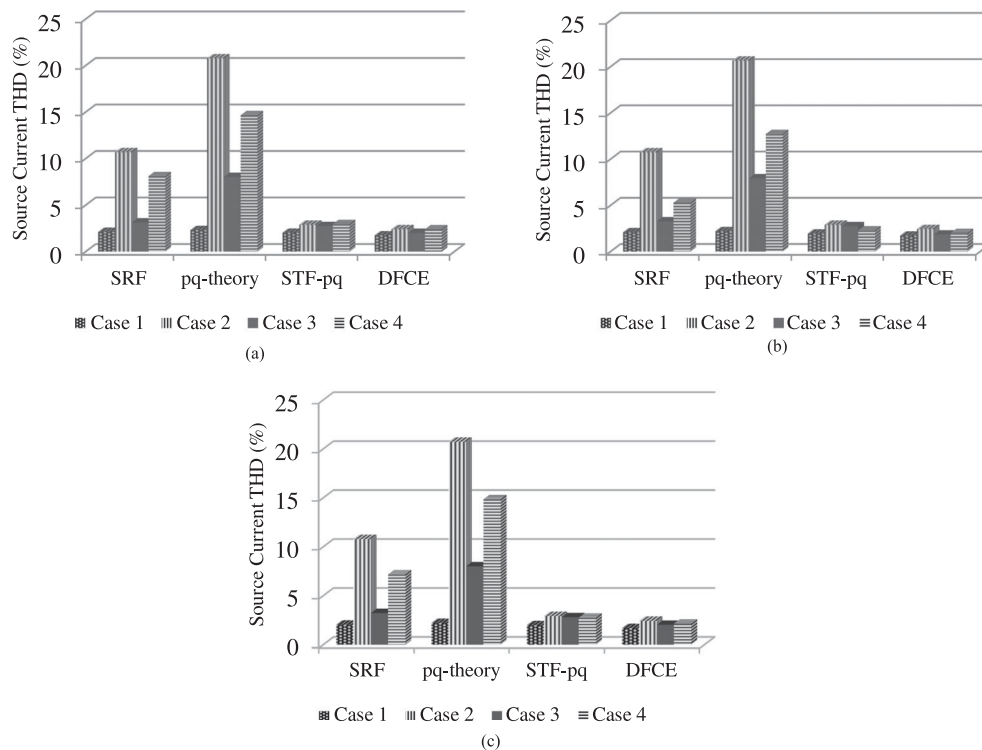


Fig. 8. Performance comparison of reference current generation algorithm for different cases of source voltage conditions: (a) phase *a*, (b) phase *b*, and (c) phase *c*.

voltage conditions, the source currents i_S mitigated by SAPF while using the proposed DFCE algorithm are observed to work in phase with their respective source voltages v_S , which leads to almost unity power factor. The benefit offered by the proposed DFCE algorithm is that the improved mitigation performance of SAPF can be achieved via a simpler control structure: without involving any additional low-pass filtering processes in isolating the harmonic and fundamental components of load currents, and PLL element in generating synchronization phases.

VI. EXPERIMENTAL RESULTS

A laboratory prototype is built to validate practically performance of the proposed DFCE algorithm. For experimental

testing, two distinct source voltage conditions are considered: in case A, balanced-sinusoidal source voltage and in case B, unbalanced-sinusoidal source voltage. Both source voltages are supplied from a three-phase programmable ac source (Chroma 6590). For case A, the supplied voltage is set at 50 Hz, 100 Vrms (line to line). Meanwhile, for case B, 50-Hz voltage supply with magnitude $v_{Sa} = 53$ Vrms, $v_{Sb} = 36$ Vrms, and $v_{Sc} = 45$ Vrms is applied. Next, the desired reference overall dc-link voltage is set at 220 V. A TMS320F28335 DSP board is configured and programmed to perform all control algorithms of SAPF and to generate the desired gate pulses for the NPC inverter.

The steady-state experimental waveforms of SAPF utilizing the proposed DFCE algorithm that includes three-phase source

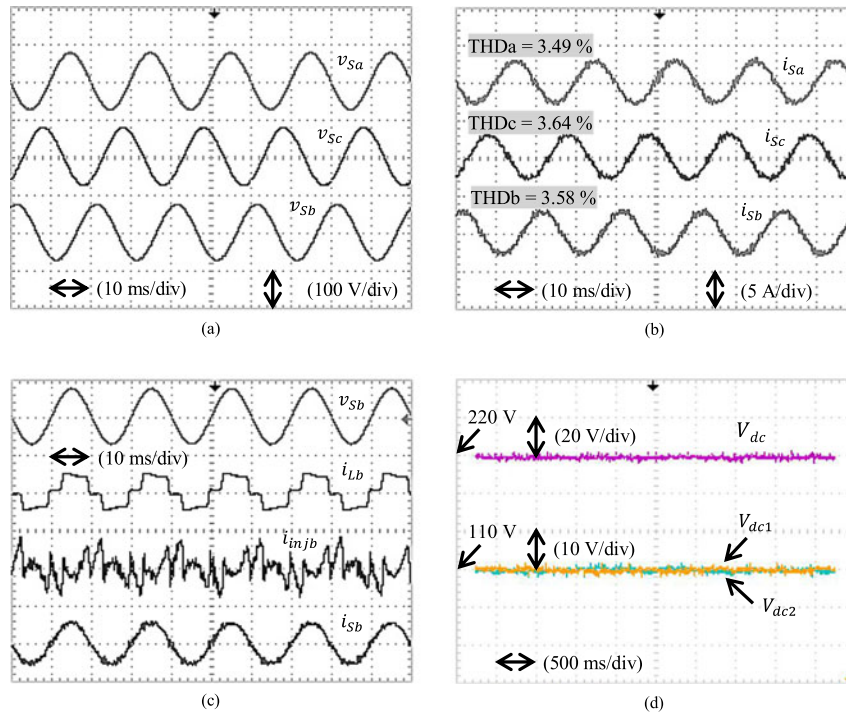


Fig. 9. Steady-state experimental waveforms (case A) of SAPF utilizing the proposed DFCE algorithm, which include (a) three-phase source voltages v_S , (b) three-phase source currents i_S , (c) phase b source voltage v_{Sb} (100 V/div), load current i_{Lb} (5 A/div), injection current i_{injb} (2 A/div), and source current i_{Sb} (5 A/div), and (d) dc-link voltages.

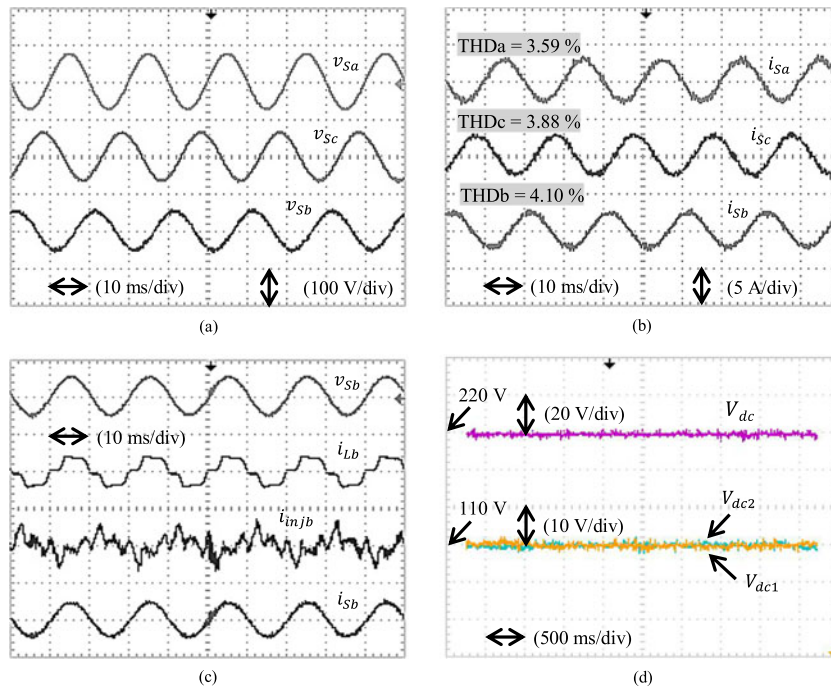


Fig. 10. Steady-state experimental waveforms (case B) of SAPF utilizing the proposed DFCE algorithm, which include (a) three-phase source voltages v_S , (b) three-phase source currents i_S , (c) phase b source voltage v_{Sb} (100 V/div), load current i_{Lb} (5 A/div), injection current i_{injb} (2 A/div), and source current i_{Sb} (5 A/div), and (d) dc-link voltages.

voltages v_S , three-phase source currents i_S , phase b voltage and currents, and dc-link voltages, obtained for cases A and B are shown in Figs. 9 and 10, respectively. Based on Fig. 9(b), it is clear that under balanced sinusoidal source voltage condition, SAPF utilizing the proposed DFCE algorithm shows effective mitigation of harmonics generated by the inductive

load, where THD values recorded for each phase of mitigated source current i_S are $\text{THDa} = 3.49\%$, $\text{THDb} = 3.58\%$, and $\text{THDc} = 3.64\%$, respectively.

Similarly, as shown in Fig. 10(b), SAPF utilizing the proposed DFCE algorithm is also revealed to work effectively under unbalanced sinusoidal source voltage condition, where THD

TABLE V
THDS OF MITIGATED SOURCE CURRENT OBTAINED UNDER SPECIFIED CASES
OF SOURCE VOLTAGE CONDITIONS (EXPERIMENTAL RESULTS)

Source voltage conditions	Current THDs of the phases, (%)					
	STF-pq [21]			DFCE		
	<i>a</i>	<i>b</i>	<i>c</i>	<i>a</i>	<i>b</i>	<i>c</i>
Case A	3.88	3.91	3.95	3.49	3.58	3.64
Case B	3.92	4.33	4.12	3.59	4.10	3.88

values recorded for each phase of mitigated source current i_S are $\text{THD}_a = 3.59\%$, $\text{THD}_b = 4.10\%$, and $\text{THD}_c = 3.88\%$, respectively. All THD values recorded are below 5% which comply with the IEEE Standard 519-2014. Moreover, from Figs. 9(c) and 10(c), the mitigated source currents i_S obtained for cases A and B, seems to work in phase with their respective source voltages v_S and, thus, achieving almost unity power factor.

In experimental work, performance achieved by SAPF while using the proposed DFCE algorithm is compared with the performance demonstrated by SAPF utilizing the existing STF-pq algorithm. Table V summarizes the comparative findings. Based on Table V, it is clear that the proposed DFCE algorithm performs with a lower THD value of source current as compared to the existing STF-pq algorithm and, thus, confirming superiority of the proposed DFCE algorithm. Concurrently, it also reveals superiority of ICC-based control over DCC-based control in terms of mitigation performance (lower THD value), which is achieved via minimization of switching ripples problems.

Furthermore, it can be observed from Figs. 9(d) and 10(d) that for both cases of source voltage conditions, all dc-link voltages (V_{dc} , V_{dc1} , and V_{dc2}) of the SAPF are properly regulated and maintained at their respective desired values. Besides, voltages across both splitting dc-link capacitors (V_{dc1} and V_{dc2}) of the SAPF are observed to have equally maintained at half of its overall dc-link voltage V_{dc} . Therefore, it can be confirmed that the design concept and operation of SAPF utilizing the proposed DFCE algorithm in harmonics mitigation are correct and valid under both ideal and nonideal source voltage conditions.

VII. CONCLUSION

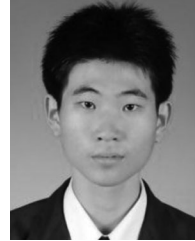
In this paper, the design concept and effectiveness of a newly proposed control algorithm that generates accurate sinusoidal reference current signal, for effective harmonics mitigation and reactive power compensation of SAPF under the case of ideal and nonideal grid voltage conditions have been discussed. An alternative time domain-based control algorithm, which operates under ICC scheme and is named as DFCE, is proposed where two STF-based fundamental component extraction algorithms are integrated together to manage distortion, unbalance and non-ideality of voltages and currents. In the proposed algorithm, the STF-based fundamental current extraction algorithm is used to extract balanced-sinusoidal load current signals. Concurrently, the STF-based fundamental voltage extraction algorithm pro-

cesses the distorted and unbalanced voltages to track the exact angular positions of the operating power system. The proposed algorithm provides the benefit of improved performance without the need for additional LPF in isolating the harmonic and fundamental components of load currents, and PLL element in tracking the angular positions. Simulation work reveals that utilization of the proposed DFCE algorithm has significantly improved mitigation performance of SAPF by achieving minimum THD values. Moreover, the proposed algorithm is proven to work effectively under different scenarios of grid voltage conditions (both ideal and nonideal). The minimum THD values recorded for mitigated source currents clearly show advantages of the proposed DFCE algorithm over the existing SRF, pq theory, and STF-pq algorithms especially when operating under nonideal grid voltage conditions. Furthermore, the experimental findings have confirmed effectiveness of the proposed DFCE algorithm under both ideal and nonideal grid voltage conditions as conducted in simulation work.

REFERENCES

- [1] Y. Hoon, M. A. M. Radzi, M. K. Hassan, and N. F. Mailah, "DC-link capacitor voltage regulation for three-phase three-level inverter-based shunt active power filter with inverted error deviation control," *Energies*, vol. 9, no. 7, pp. 533–557, Jul. 2016.
- [2] H. Akagi, "Active harmonic filters," *Proc. IEEE*, vol. 93, no. 12, pp. 2128–2141, Dec. 2005.
- [3] T. C. Green and J. H. Marks, "Control techniques for active power filters," *IEE Proc.—Elect. Power Appl.*, vol. 152, no. 2, pp. 369–381, Mar. 2005.
- [4] P. Xiao, G. K. Venayagamoorthy, and K. A. Corzine, "Seven-level shunt active power filter for high-power drive systems," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 6–13, Jan. 2009.
- [5] O. Vodyakho and C. C. Mi, "Three-level inverter-based shunt active power filter in three-phase three-wire and four-wire systems," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1350–1363, May 2009.
- [6] A. M. Massoud, S. J. Finney, A. J. Cruden, and B. W. Williams, "Three-phase, three-wire, five-level cascaded shunt active filter for power conditioning, using two different space vector modulation techniques," *IEEE Trans. Ind. Electron.*, vol. 22, no. 4, pp. 2349–2361, Oct. 2007.
- [7] Y. Hoon, M. A. M. Radzi, M. K. Hassan, N. F. Mailah, and N. I. A. Wahab, "A simplified synchronous reference frame for indirect current controlled three-level inverter-based shunt active power filters," *J. Power Electron.*, vol. 16, no. 5, pp. 1964–1980, Sep. 2016.
- [8] A. Bhattacharya and C. Chakraborty, "A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 421–428, Feb. 2011.
- [9] L. Asiminoaei, F. Blaabjerg, and S. Hansen, "Detection is key-harmonic detection methods for active power filter applications," *IEEE Ind. Appl. Mag.*, vol. 13, no. 4, pp. 22–33, Jul./Aug. 2007.
- [10] A. Bhattacharya, C. Chakraborty, and S. Bhattacharya, "Shunt compensation reviewing traditional methods of reference current generation," *IEEE Ind. Electron. Mag.*, vol. 3, no. 3, pp. 38–49, Sep. 2009.
- [11] M. Monfared, S. Golestan, and J. M. Guerrero, "A new synchronous reference frame-based method for single-phase shunt active power filters," *J. Power Electron.*, vol. 13, no. 4, pp. 692–700, Jul. 2013.
- [12] N. Jain and A. Gupta, "Comparison between two compensation current control methods of shunt active power filter," *Int. J. Eng. Res. Gen. Sci.*, vol. 2, no. 5, pp. 603–615, Aug./Sep. 2014.
- [13] S. S. Wamane, J. R. Baviskar, and S. R. Wagh, "A comparative study on compensating current generation algorithms for shunt active filter under non-linear load conditions," *Int. J. Sci. Res. Publ.*, vol. 3, no. 6, pp. 1–6, Jun. 2013.
- [14] N. Eskandarian, Y. A. Beromi, and S. Farhangi, "Improvement of dynamic behavior of shunt active power filter using fuzzy instantaneous power theory," *J. Power Electron.*, vol. 14, no. 6, pp. 1303–1313, Nov. 2014.
- [15] M. Popescu, A. Bitoleanu, and V. Suru, "A DSP-based implementation of the p-q theory in active power filtering under nonideal voltage conditions," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 880–889, May 2013.

- [16] Y. Hoon, M. A. M. Radzi, M. K. Hassan, and N. F. Mailah, "Enhanced instantaneous power theory with average algorithm for indirect current controlled three-level inverter-based shunt active power filter under dynamic state conditions," *Math. Probl. Eng.*, vol. 2016, Mar. 2016, Art. no. 9682512.
- [17] M. A. M. Radzi and N. A. Rahim, "Neural network and bandless hysteresis approach to control switched capacitor active power filter for reduction of harmonics," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1477–1484, May 2009.
- [18] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, "Decoupled double synchronous reference frame PLL for power converters control," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 584–592, Mar. 2007.
- [19] L. B. G. Campanhol, S. A. O. Silva, and A. Goedel, "Application of shunt active power filter for harmonic reduction and reactive power compensation in three-phase four-wire systems," *IET Power Electron.*, vol. 7, no. 11, pp. 2825–2836, Nov. 2014.
- [20] K. Djazia, F. Krim, A. Chaoui, and M. Sarra, "Active power filtering using the ZDPC method under unbalanced and distorted grid voltage conditions," *Energies*, vol. 8, pp. 1584–1605, Feb. 2015.
- [21] M. Abdulsalam, P. Poure, S. Karimi, and S. Saadate, "New digital reference current generation for shunt active power filter under distorted voltage conditions," *Elect. Power Syst. Res.*, vol. 79, no. 5, pp. 759–765, Dec. 2009.
- [22] S. Biricik, S. Redif, Ö. C. Özerdem, S. K. Khadem, and M. Basu, "Real-time control of shunt active power filter under distorted grid voltage and unbalanced load condition using self-tuning filter," *IET Power Electron.*, vol. 7, no. 7, pp. 1895–1905, Jul. 2014.
- [23] J. Fei, T. Li, F. Wang, and W. Juan, "A novel sliding mode control technique for indirect current controlled active power filter," *Math. Probl. Eng.*, vol. 2012, Jan. 2012, Art. no. 549782.
- [24] M. Adel, S. Zaid, and O. Mahgoub, "Improved active power filter performance based on an indirect current control technique," *J. Power Electron.*, vol. 11, no. 6, pp. 931–937, Nov. 2011.
- [25] B. N. Singh, A. Chandra, and K. Al-Haddad, "Performance comparison of two current control techniques applied to an active filter," in *Proc. Int. Conf. Harmonics Qual. Power*, Athens, Greece, Oct. 1998, pp. 133–138.
- [26] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 960–971, Oct. 1999.
- [27] S. Rahmani, K. Al-Haddad, and H. Y. Kanan, "Experimental design and simulation of a modified PWM with an indirect current control technique applied to a single-phase shunt active power filter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Dubrovnik, Croatia, Jun. 2005, pp. 519–524.
- [28] S. K. Jain, P. Agrawal, and H. O. Gupta, "Fuzzy logic controlled shunt active power filter for power quality improvement," *IEE Proc.—Elect. Power Appl.*, vol. 149, no. 5, pp. 317–328, Sep. 2002.
- [29] Y. Hoon, M. A. M. Radzi, M. K. Hassan, and N. F. Mailah, "Neutral-point voltage deviation control for three-level inverter-based shunt active power filter with fuzzy-based dwell time allocation," *IET Power Electron.*, vol. 10, no. 4, pp. 429–441, Apr. 2017.
- [30] H. Zhang, S. J. Finney, A. Massoud, and B. W. Williams, "An SVM algorithm to balance the capacitor voltages of the three-level NPC active power filter," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2694–2702, Nov. 2008.
- [31] U.-M. Choi, J.-S. Lee, and K.-B. Lee, "New modulation strategy to balance the neutral-point voltage for three-level neutral-clamped inverter systems," *IEEE Trans. Energy Convers.*, vol. 29, no. 1, pp. 91–100, Mar. 2014.
- [32] S. Ahmed, G. Madjid, M. Youcef, and T. Hamza, "Real time control of an active power filter under distorted voltage condition," *Int. J. Power Electron. Drive Syst.*, vol. 2, no. 4, pp. 424–433, Oct. 2012.
- [33] S. Biricik, O. C. Ozerdem, S. Redif, and M. I. O. Kmail, "Performance improvement of active power filter under distorted and unbalanced grid voltage conditions," *Elektronika ir Elektrotechnika*, vol. 19, no. 1, pp. 35–39, Dec. 2013.
- [34] S. Karimi, P. Poure, and S. Saadate, "High performances reference current generation for shunt active filter under distorted and unbalanced conditions," in *Proc. IEEE Power Electron. Spec. Conf.*, Rhodes, Greece, Jun. 2008, pp. 195–201.
- [35] A. Ghamri, M. T. Benchouia, and A. Golea, "Sliding-mode control based three-phase shunt active power filter: Simulation and experimentation," *Elect. Power Compon. Syst.*, vol. 40, no. 4, pp. 383–398, Jan. 2012.
- [36] S. Biricik, O. C. Ozerdem, S. Redif, and M. O. I. Kmail, "Novel hybrid active power filter structure to compensate harmonic currents and reactive power," in *Proc. IEEE Mediterranean Electrotech. Conf.*, Yasmine Hammamet, Tunisia, Mar. 2012, pp. 597–601.
- [37] M. Abdulsalam, P. Poure, and S. Saadate, "Hardware implementation of a three-phase active filter system with harmonic isolation based on self-tuning-filter," in *Proc. IEEE Power Electron. Spec. Conf.*, Rhodes, Greece, Jun. 2008, pp. 2875–2881.



Yap Hoon was born in Sitiawan, Perak, Malaysia, in 1990. He received the B.Eng. degree in electrical and electronic engineering and the Ph.D. degree in electrical power engineering from Universiti Putra Malaysia (UPM), Selangor, Malaysia, in 2013 and 2017, respectively.

He is currently associated with Centre for Advanced Power and Energy Research, UPM. His research interests include power electronics, power quality, and multilevel inverter.



Mohd Amran Mohd Radzi (M'01–SM'17) was born in Kuala Lumpur, Malaysia, in 1978. He received the B.Eng. (Hons.) and M.Sc. degrees in electrical power engineering from the Universiti Putra Malaysia (UPM), Selangor, Malaysia, in 2000 and 2002, respectively, and the Ph.D. degree in power electronics from the University of Malaya, Kuala Lumpur, Malaysia, in 2010.

He is currently an Associate Professor and the Head of the Department of Electrical and Electronic Engineering, UPM. He is also associated with the

Centre for Advanced Power and Energy Research, UPM. His research and teaching interests include power electronics, power quality, and renewable energy.

Dr. Radzi is a Member of the Institution of Engineering and Technology, U.K., and a Chartered Engineer.



Mohd Khair Hassan was born in Melaka, Malaysia. He received the B.Eng. (Hons.) degree in electrical and electronic engineering from the University of Portsmouth, Portsmouth, U.K., in 1998, the M.Eng. degree in electrical engineering from the Universiti Teknologi Malaysia, Johor, Malaysia, in 2001, and the Ph.D. degree in automotive engineering from the Universiti Putra Malaysia (UPM), Selangor, Malaysia, in 2011.

He is currently an Associate Professor in the Department of Electrical and Electronic Engineering, UPM. His area of interest includes control system, automotive control, electric vehicle, and AI applications. His current focuses are on x-by-wire technology and optimal strategy for energy consumption in electric vehicle.

Dr. Hassan is a Professional Engineer registered under Board of Engineers Malaysia, a Corporate Member of the Institution of Engineers Malaysia, and a Member of the Society of Automotive Engineers.



Nashiren Farzilah Mailah (M'01) was born in Johor, Malaysia. She received the B.Eng. (Hons.) degree in electrical and electronic engineering from the University of Huddersfield, Huddersfield, U.K., in 1999, the M.Eng. degree in electrical engineering from the Universiti Teknologi Malaysia, Johor, Malaysia, in 2001, and the Ph.D. degree in electrical power engineering from the Universiti Putra Malaysia (UPM), Selangor, Malaysia, in 2010.

She is currently a Senior Lecturer in the Department of Electrical and Electronic Engineering, UPM.

Her research interests include power electronics converter and its applications in machine drive and power systems.