Nonisolated Harmonics-Boosted Resonant DC/DC Converter With High-Step-Up Gain

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***Abstract*—High-step-up dc/dc converters are widely required in grid-connected applications with renewable energy sources. An extremely high-ratio step-up nonisolated dc/dc converter, in the form of a harmonics-boosted resonant converter, is proposed in this paper. This proposed converter consists of a high-frequency dc/ac inverter stage that is followed by a passive ac/dc rectifier stage connected in cascade. Conventionally, such a dc/ac inverter is designed to output a pure sinusoidal ac voltage with an amplitude several times the amplitude of the input voltage. However, for the proposed converter, the harmonics-boosted inverter stage is designed to contain selected voltage harmonics that significantly boost the amplitude of its output voltage. This greatly increases the overall gain of the converter. The adopted ac/dc stage is a diode-capacitor rectifier, which is of high efficiency and easily extendable to increase the voltage gain. Importantly, the proposed converter involves only one active switch. With only one active switch, the driver's loss is minimized and the converter's control is simplified. Zero-voltage switching is applied to reduce the switching loss, which also allows the converter to operate efficiently at high frequency, and thus can be designed for high power density. The optimal design of the two converter stages and their combined voltage gain is investigated and reported. Besides, a design guideline of the proposed converter is provided. A prototype of a 57-time harmonics-boosted resonant converter with 3.3 V input voltage, 500 kHz switching frequency, and 21 W output power, is built. The experimental result shows that the achieved converter's efficiency is as high as 88.6%.**

***Index Terms*—Extra-high-voltage gain, harmonics, resonant converter, voltage multiplier.**

I. Introduction

ELECTRICITY produced by renewable power generators like the thermoelectric generator, fuel cell, and photovoltaic panel, and reverse electrodialysis stack is of dc power form and exists at a relatively low voltage level (a few hundred millivolt to a few tens of volts) [1]–[3]. For these low-voltage renewable energy sources to become viable parts of dc microgrids (operate at 120 to 380 V) [4] or ac grids (110 or 220 V), power converters with a high or extremely high voltage gain are required for interfacing the sources and the grids [5]. The high-voltage-gain converter is also required for some unique types of load applications, e.g., electrostatic precipitator [6] and electrical vehicle battery [7]. Based on the types of components and configurations utilized, the possible solutions for achieving this kind of conversion can be classified into four categories: transformer-based converters, coupled-inductor-based converters, inductor-based converters (converters that contain inductor), and switched-capacitor (SC) converters.

For a transformer-based or coupled-inductor-based converter, a high-voltage gain is easily achievable through the use of large transformer's or coupled-inductor's turns ratio [8], [9]. However, the requirement for a transformer or coupled-inductor with large turns ratio necessitates the use of a large magnetic core, which is not only physically large, but heavy and relatively costly. Inclusion of such a magnetic component severely increases the converter's size and weight [10]. To reduce the transformers' or coupled-inductors' turns ratio, voltage multiplier, or voltage-lift circuits connected to the windings of the transformers or coupled-inductors have been proposed [11]–[13]. These circuits utilize capacitors as voltage sources that are connected in series with the windings to obtain extra voltage gain for the conversion. However, the incorporation of such circuits greatly complicates converters' operation. Moreover, transformer-based or coupled-inductor-based converters typically suffer from high voltage stress and severe electromagnetic interference (EMI) issues that are introduced by the leakage inductance of the transformers and coupled inductors. These issues confine the converters to needing high-voltage-rated switches that are inherently of a higher on-resistance, and the need for voltage-clamp circuit [14], active-clamp circuit [15], or snubber circuit [16].

SC converters, which consist of only switches and capacitors, can easily be configured to achieve a high conversion ratio. Since the magnetic component is absent from the SC converters, issues related to magnetics, e.g., large size and heavy weight of the magnetic core, EMI issues caused by leakage inductance, etc., are not of concern. This enables the SC converter to achieve high power density, light weight, and even integrated-circuit integration [3], [17], [18]. However, an increasing conversion ratio of the SC converter is typically accompanied by an increasing number of switches and capacitors. This increases the converter's cost and indirectly lowers the converter's reliability. Besides, the pulsating capacitor charging current (inherent nature of SC converters of which the current is dependent on the intrinsic circuit resistance) of the SC converter hinders its ap-

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plications to exclude those that require low input current ripple [8], [19]. Moreover, high current spikes and voltage spikes on the switches and the relatively poor line and load regulation also limit its applications [20], [21].

For inductor-based voltage step-up converters, a most common topology is the boost converter. However, the voltage gain of the boost converter is limited (normally, the gain is less than 5) as the efficiency achievable at very high voltage gain is low [3], [22]. To achieve a higher voltage gain, a two-stage converter comprising two boost converters that are connected in cascade, has been proposed [23]. However, this would require a set of synchronized controllers to control the respective active switches of the two converter stages, such that the beat-frequency phenomenon can be avoided. This causes complexity in the control [23]. Moreover, instability can easily arise in varied operating condition, e.g., changing input voltage and load conditions [24]. A hybrid converter involving the use of an SC voltage multiplier in a boost converter is proposed in [25] and [26]. The voltage conversion ratio of this hybrid converter is the product of the two ratios of the two stages, i.e., the boost stage and the SC multiplier stage. Since the voltage conversion ratio of the boost converter is also limited, the high-voltage gain of the hybrid converter is mainly achieved by the SC voltage multiplier stage. However, a high-voltage-gain SC multiplier requires a large number of capacitors and diodes. Besides, snubber circuits are required for its high frequency operation to avoid severe turn-off voltage surge [25].

Recently, two-stage converters comprising a high-frequency dc/ac resonant inverter that is cascaded with a high-frequency ac/dc rectifier have been proposed [27], [28] to achieve a high-voltage-gain step-up voltage conversion. The resonant nature of the converter allows soft-switching operation, which mitigates the switching loss of the converter. The soft-switching operation allows the converter to be designed for high frequency to increase the converter's power density. In the topology proposed in [28], a high conversion ratio is achieved via the connection of the multiple outputs of the rectifier stage in series. However, this topology is limited to applications where the grounds of the input and the output of the converter are isolated. For the converter proposed in [27], the voltage gain is mainly achieved by the inverter stage. The rectifier stage achieves little voltage gain. However, this is conversely true for the converter proposed in [28], of which the voltage gain is mainly achieved by the rectifier stage instead of the inverter stage. Both these approaches have their pros and cons. A high-voltage gain of the inverter stage will lead to a large power loss on inductors and a high-voltage gain of the rectifier stage will lead to a large number of capacitors and diodes. Thus, a balance between the voltage gains of the two stages should be considered in the perspective of maximizing efficiency, circuit complexity and cost. Besides, the output voltages of these converters are highly correlated to the peak output voltage of the inverter stage (the input of the rectifier stage). Thus, increasing this peak voltage can effectively increase the output voltage of the converter.

In this paper, such an approach is investigated along with the proposal of a type of two-stage converter comprising a high-frequency dc/ac harmonics-boosted inverter stage that is followed by a passive ac/dc rectifier stage. Unlike the existing inverter stages which output a pure sinusoidal voltage, the proposed inverter stage utilizes certain harmonic components to further increase the peak output voltage, such that a higher voltage gain of the converter can be achieved. This is the essence of the harmonics-boosted inverter stage utilized in this converter. With consideration to the extendability, ease of implementation (no need for tuning and control), and voltage boost capability [29], the Cockcroft–Walton multiplier [30] is adopted as the rectifier stage. In addition to achieving an extremely high-step-up gain, the proposed converter has the following characteristics: 1) only one active switch is required and 2) zero-voltage switching of the active switch is achieved. This paper is an extension of our previous conference publication [31]. The new contribution of this full paper includes:

1) The investigation on harmonic components' utilization to increase the voltage gain;
2) proposal of design procedure for the proposed converter;
3) loss analysis of the proposed converter; and
4) experimental results of a new prototype with a much higher voltage gain than that described in [31].

In this paper, the optimal voltage gain's combination of the two stages of the converter in achieving the highest possible efficiency is investigated.

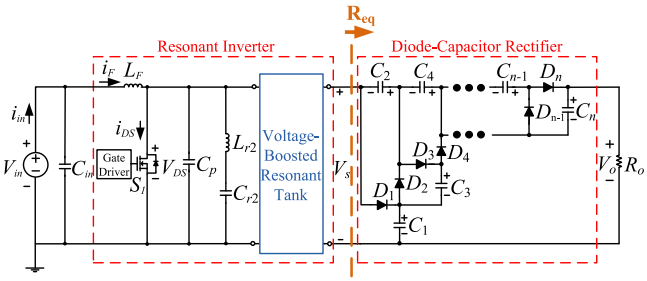


Fig. 1. Schematic diagram of the proposed harmonics-boosted resonant dc/dc converter.

II. Harmonics-Boosted Resonant DC/DC Converter

A. Structure of the Proposed Harmonics-Boosted Resonant Converter

The proposed converter (as shown in Fig. 1) consists of a resonant-inverter stage and a diode-capacitor-rectifier stage. The converter's voltage gain is the product of the voltage gains of the two stages. The topology of the diode-rectifier stage adopted is Cockcroft–Walton multiplier (as shown in Fig. 1). This topology is simple to implement and its voltage gain can be easily increased by increasing the number of laddered networks of capacitors and diodes. The resonant-inverter stage comprises one active switch S_1, standard resonant networks L_F, C_p, L_{r2}, C_{r2}, and a voltage-boosted resonant tank. The voltage $V_{\rm DS}$ on the active switch S_1 mainly comprises of dc component, fundamental component and selected higher harmonic components. The magnitude of these components are affected by the values of L_F, C_p, L_{r2}, C_{r2}, and also the elements of the voltage-boosted resonant tank. The voltage boosting capability of the resonant inverter

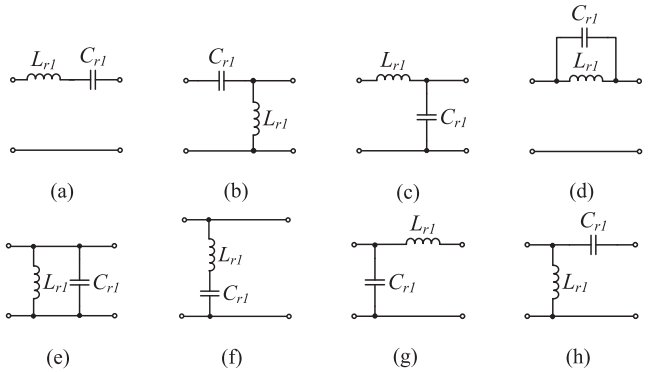


Fig. 2. Eight two-element tanks: (a) tank I, (b) tank II, (c) tank III, (d) tank IV, (e) tank V, (f) tank VI, (g) tank VII, and (h) tank VIII. The left side of each tank is the input side and the right side is the output side.

stage is mainly achieved by the voltage-boosted resonant tank. To simplify the design process of the voltage-boosted resonant tank, only two-element tanks, which consists of inductor L_{r1} and capacitor C_{r1}, are considered. The resonant frequency f_{r1} of the voltage-boosted resonant tank is equal to the switching frequency f_s. This tank will boost the fundamental component of $V_{\rm DS}$ and transmit the higher harmonics into V_s to further improve the peak voltage of V_s.

With different connections of L_{r1} and C_{r1}, there are eight possible two-element tanks as shown in Fig. 2 [32]. The voltage gain curves of these eight tanks are shown in Fig. 3. According to the requirements of the voltage-boosted resonant tank, tank II is adopted as it achieves the voltage boosting function and possesses the ability to transmit the required high frequency harmonics. While tank III provides a similar resonance gain at the fundamental frequency as tank II, however, due to its low-pass nature, it does not permit the transmission of the higher harmonics. Therefore, it does not perform harmonics-boosted function as required in the proposed converter. The schematic diagram of the proposed converter which adopts tank II as the voltage-boosted resonant tank, is shown in Fig. 4.

B. Operation of the Proposed Harmonics-Boosted Resonant Converter

1) Harmonics-Boosted Resonant Inverter Stage: Switch S_1 is driven by a constant-frequency pulse at 50% duty cycle. Its drain-to-source voltage $V_{\rm DS}$ is also the input voltage of the voltage-boosted resonant tank $L_{r1}C_{r1}$. Thus, the output voltage V_s of the inverter stage is tightly linked to $V_{\rm DS}$. With consideration of the low voltage stress of S_1, $V_{\rm DS}$ is designed to mainly contain the fundamental component and the third-harmonic component. Second-harmonic component is removed from $V_{\rm DS}$. With consideration to further increasing the peak voltage of V_s, the fourth-harmonic component is increased in $V_{\rm DS}$. Thus, $V_{\rm DS}$ is designed to compose of the dc, the fundamental, the third-harmonic, and the fourth-harmonic components.

The waveform of $V_{\rm DS}$ is determined by the network comprising L_F, C_p, L_{r2}, C_{r2}, L_{r1}, and C_{r1}. To remove the second-harmonic component, L_{r2} and C_{r2} are designed to resonate at the second harmonic of the switching frequency. Thus,

$$L_{r2}C_{r2} = \frac{1}{(2\cdot\omega_s)^2}, \tag{1}$$

where $\omega_s = 2\pi f_s$ and f_s is the switching frequency.

To achieve ZVS and the desired $V_{\rm DS}$, the two impedances Z_m [as shown in Fig. 5(a)] and $Z_{\rm ds}$ [as shown in Fig. 5(b)] must be designed ($R_{\rm eq}$ is the equivalent resistance of the rectifier stage) to satisfy following three conditions.

Condition (a): The magnitude of Z_m to have two peaks (P_1 and P_2), one of which (P_1) is located at a frequency near the fundamental frequency and the other (P_2) at a frequency between the third-and fourth-harmonic frequencies;

Condition (b): The magnitude of Z_m to have a minimum value located at the second-harmonic frequency, $\min(|Z_m(j\omega)|) = |Z_m(j(2\omega_s))|$; and

Condition (c): The phase angle of $Z_{\rm DS}$ at the fundamental frequency is above zero degree, $\angle Z_{\rm DS}(j\omega_s) > 0^\circ$.

Satisfaction of conditions (a)–(c) will result in $V_{\rm DS}$ mainly composing of the dc component, the fundamental, the third, and the fourth-harmonic components, as illustrated in Fig. 6.

The simplified equivalent circuit of the inverter stage can be represented as shown in Fig. 7. $V_{\rm DS}$ is converted to V_s by the voltage-boosted resonant tank L_{r1} and C_{r1}. The dc voltage component is removed as all dc components in the voltage-boosted resonant tank will be blocked by capacitor C_{r1}. Therefore, the input voltage of the equivalent circuit only contains the fundamental component ($V_{\rm DS_1}$), the third- and fourth-harmonic components ($V_{\rm DS_3}$ and $V_{\rm DS_4}$). The rectifier stage is represented by an equivalent resistance $R_{\rm eq}$. L_{r1} and C_{r1} are designed to resonate at the fundamental frequency f_s by using the equation

$$L_{r1}C_{r1} = \frac{1}{{\omega_s}^2}. \tag{2}$$

The transfer function of the voltage-boosted resonant tank is

$$G(s) = \frac{(\frac{s}{\omega_s})^2}{1 + \frac{L_{r1}}{R_{\rm eq}}s + (\frac{s}{\omega_s})^2}, \tag{3}$$

where $s = j\omega$ and $j^2 = -1$. According to (3), the voltage gain of the fundamental component ($V_{\rm DS_1}$) is $\frac{R_{\rm eq}}{L_{r1}}$. Therefore, by properly selecting the value of L_{r1}, the fundamental voltage component can be greatly boosted. The voltage gain of the third- and fourth-harmonic voltages are approximately equal to 1. Therefore, the voltage V_s is mainly composed of a high level fundamental component and low levels of the third- and fourth-harmonic components, as shown in Fig. 8. Compared to the waveform with only the fundamental component, the peak value, especially the one on the positive axis, can be increased by utilizing the third-and fourth-harmonic components.

2) n-Level Diode-Capacitor Rectifier Stage: An n-level diode-capacitor rectifier consists of n diodes and n capacitors. The maximum absolute values of the positive cycle and the negative cycle of V_s are $V_{\rm smax+}$ and $V_{\rm smax-}$, respectively. When V_s reaches $V_{\rm smax+}$, diodes $D_1, D_3, \ldots, D_n$ conduct. In the meantime, capacitors $C_2, C_4, \ldots, C_{n-1}$ are discharged and capacitors $C_1, C_3, \ldots, C_n$ are charged, as depicted in Fig. 9(a).

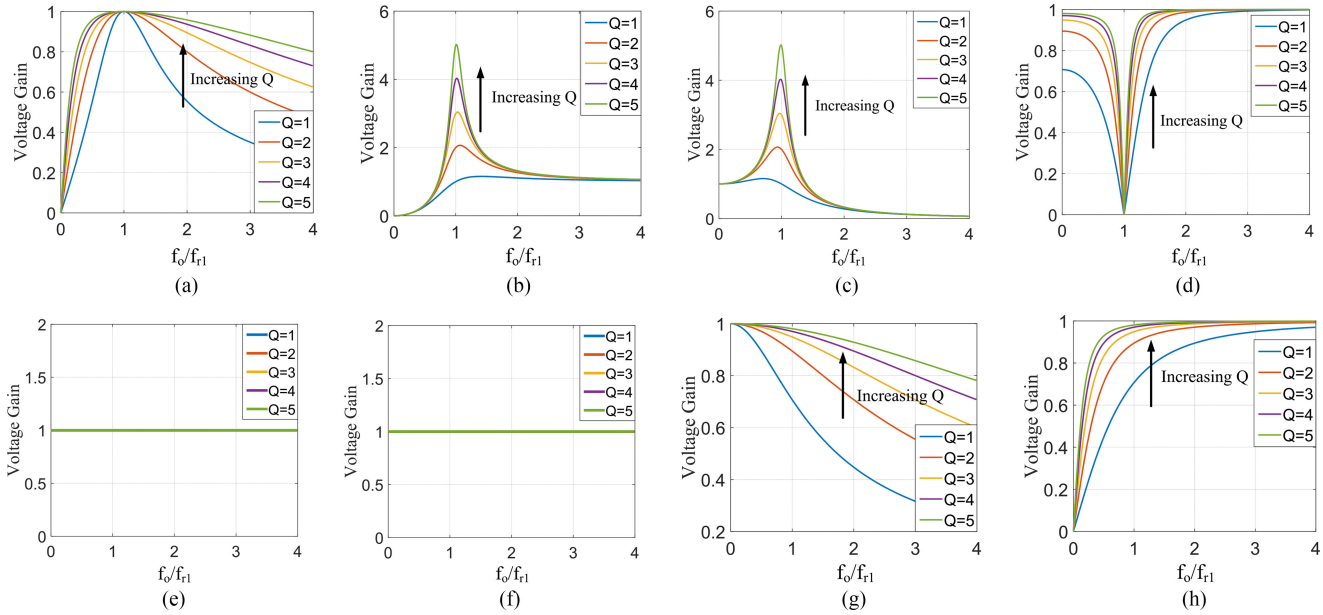


Fig. 3. Voltage gain of (a) tank I, (b) tank II, (c) tank III, (d) tank IV, (e) tank V, (f) tank VI, (g) tank VII, and (h) tank VIII versus the frequency ratio. $Q = \frac{R_{\text{eq}}}{\omega_{r1} L_{r1}}$, where $\omega_{r1} = 2\pi f_{r1}$, f_{r1} is the resonant frequency of L_{r1} and C_{r1}, and R_{eq} is the equivalent resistance of the rectifier stage.

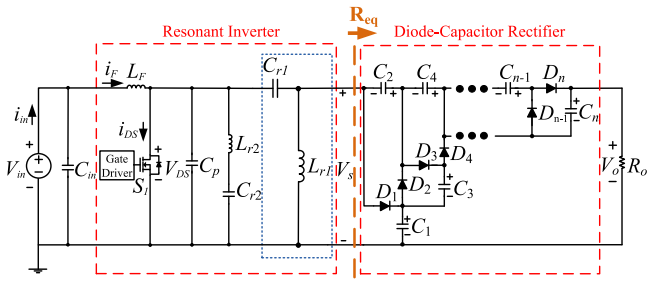


Fig. 4. Schematic diagram of the proposed harmonics-boosted resonant dc/dc converter. Tank II is adopted for the voltage-boosted resonant tank.

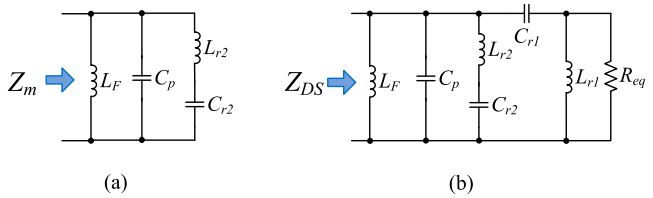


Fig. 5. Two impedances seen from the drain-source port of switch: (a) Z_m consists of L_F, C_{r2}, L_{r2}, and C_p, and (b) Z_{DS} consists of Z_m, C_{r1}, L_{r1}, and R_{eq}.

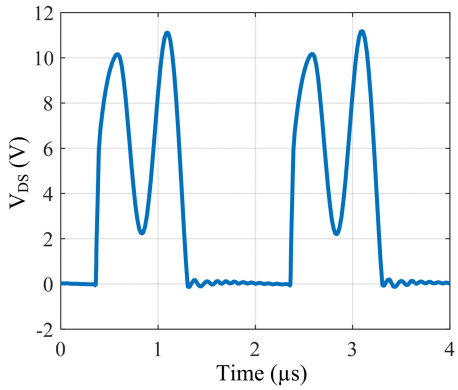


Fig. 6. Simulated V_{DS}. It mainly comprises dc, fundamental, third-harmonic and fourth-harmonic components.

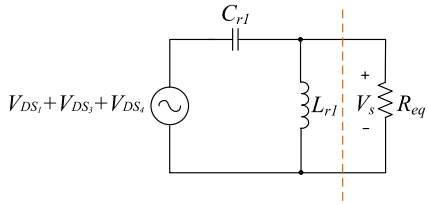


Fig. 7. Simplified equivalent circuit of the resonant inverter stage (V_{DS_1}, V_{DS_3}, and V_{DS_4} are the fundamental, the third harmonic-component, and the fourth-harmonic components of V_{DS} on S_1, respectively).

The set of equations describing this operation is

$$\begin{cases} V_{\text{smax}+} = V_{C_1} + V_{\text{dr}} \\ V_{\text{smax}+} + V_{C_2} = V_{C_1} + V_{C_3} + V_{\text{dr}} \\ \cdots \\ V_{\text{smax}+} + V_{C_2} + \cdots + V_{C_{n-1}} = V_{C_1} + V_{C_3} + \cdots + V_{C_n} + V_{\text{dr}} \\ V_{\text{smax}+} + V_{C_2} + \cdots + V_{C_{n-1}} - V_{\text{dr}} = V_o \end{cases}, \tag{4}$$

where V_{dr} is the forward voltage on the diodes. When V_s reaches $-V_{\text{smax}-}$, diodes $D_2, D_4, \ldots, D_{n-1}$ conduct. In the meantime, capacitors $C_2, C_4, \ldots, C_{n-1}$ are charged and capacitors $C_1, C_3, \ldots, C_n$ are discharged, as depicted in Fig. 9(b).

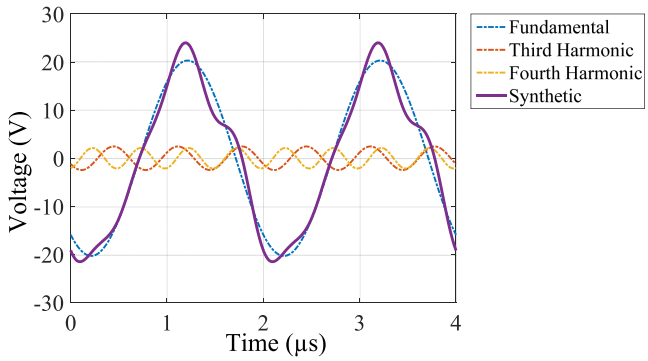


Fig. 8. Synthetic waveform comprising the fundamental, the third- and fourth-harmonic components, as compared to the waveform with only the fundamental component.

The set of equations describing this operation is

$$\begin{cases} V_{\text{smax}-} + V_{C_1} = V_{C_2} + V_{\text{dr}} \\ V_{\text{smax}-} + V_{C_1} + V_{C_3} = V_{C_2} + V_{C_4} + V_{\text{dr}} \\ \cdots \\ V_{\text{smax}-} + V_{C_1} + V_{C_3} + \cdots + V_{C_n} = V_{C_2} + V_{C_4} \\ \quad + \cdots + V_{C_{n-1}} + V_{\text{dr}} \\ V_{C_1} + V_{C_3} + \cdots + V_{C_n} = V_o \end{cases}. \tag{5}$$

Combining (4) and (5), we have

$$\begin{cases} V_{C_1} = V_{\text{smax}+} - V_{\text{dr}} \\ V_{C_k} = V_{\text{smax}+} + V_{\text{smax}-} - 2V_{\text{dr}} \\ V_o = \frac{n+1}{2} V_{\text{smax}+} + \frac{n-1}{2} V_{\text{smax}-} - nV_{\text{dr}} \end{cases}, \tag{6}$$

where $k = 2, 3, \cdots, n$. If $V_{\text{smax}+}$ is increased by $\Delta V_{\text{smax}+}$, the output voltage V_o can be increased by $\frac{n+1}{2}\Delta V_{\text{smax}+}$. If $V_{\text{smax}-}$ is increased by $\Delta V_{\text{smax}-}$, V_o can be increased by $\frac{n-1}{2}\Delta V_{\text{smax}-}$. Thus, an increase on the peak value of V_s will have a significant effect on the output voltage V_o, especially when the rectifier stage has a high level, i.e., n is large.

III. Design Considerations

A. Design of the Harmonics-Boosted Resonant Inverter Stage

1) Parameter Design of the Voltage-Boosted Resonant Tank $L_{r1}C_{r1}$: The value of L_{r1} and C_{r1} can be determined preliminarily through the following steps.

1) Determine the output load resistance using $R_o = P_o/V_o^2$, where V_o is the targeted output voltage and P_o is the desired output power.

2) Determine the value of L_{r1} and C_{r1}. As the fundamental voltage takes up a large part of V_s, the preliminary selection of L_{r1} and C_{r1} only considers the fundamental component of V_s. Then, the waveform of V_s is a sinusoidal waveform and $V_{\text{smax}+} = V_{\text{smax}-} = V_{\text{smax}}$. The voltage gain on the SC rectifier is M_{SC}. By neglecting the voltage drop on the diodes, $M_{\text{sc}} = n$ [according to the (6)]. Assume that there is no power loss of SC rectifier stage, then $\frac{V_o^2}{R_o} = (\frac{V_o}{\sqrt{2}M_{\text{SC}}})^2 \cdot \frac{1}{R_{\text{eq}}}$. Thus

$$R_{\text{eq}} = \frac{R_o}{2M_{\text{SC}}^2}. \tag{7}$$

Therefore, the peak value of V_s can be simplified to

$$V_{\text{smax}} = \frac{R_{\text{eq}}}{\omega_s L_{r1}} \cdot V_{\text{DS}_1}. \tag{8}$$

If conditions (a) to (c) in Section II-B1 are met, the relationship between V_{DS} and the input voltage V_{in} is $\frac{V_{\text{DS}_1}}{V_{\text{in}}} = \frac{4}{\pi}$, which is similar to the relationship in the case of V_{DS} with a quasi-trapezoid waveform. Therefore, the voltage gain of the resonant inverter stage can be simplified as

$$\frac{V_{\text{smax}}}{V_{\text{in}}} = \frac{4}{\pi} \cdot \frac{R_{\text{eq}}}{\omega_s L_{r1}}. \tag{9}$$

Thus, by combining (7) and (8), we have

$$\begin{cases} L_{r1} = \frac{2R_o V_{\text{in}}}{\pi V_o M_{\text{sc}} \omega_s} \\ C_{r1} = \frac{1}{{\omega_s}^2 L_{r1}} \end{cases}. \tag{10}$$

2) Parameter Design of L_F, C_P, L_{r2} and C_{r2}: The equation describing impedance Z_m shown in Fig. 5(a), is

$$Z_m(s) = \frac{sL_F(\frac{s^2}{4{\omega_s}^2} + 1)}{\frac{s^4 L_F C_p}{4{\omega_s}^2} + s^2(\frac{1}{4{\omega_s}^2} + L_F C_p + C_{r2} L_F) + 1}. \tag{11}$$

Z_m is designed following conditions (a) and (b).

A larger value of inductor L_F or capacitor C_p shifts locations of P_1 and P_2 to lower frequencies. The change of the value of L_F has a more significant effect on P_1 than P_2. A larger value of capacitor C_p will effectively reduce the magnitude of P_2, which leads to lower amplitude of the harmonic components (the third- and fourth-harmonic components) on V_{DS}. Increasing the value of inductor L_{r2} (simultaneously decreasing the value of capacitor C_{r2} to let the $L_{r2}C_{r2}$ tank resonate at the second harmonic) will shift P_1 to a higher frequency and P_2 to a lower frequency.

The equation describing impedance Z_{DS} is (12), as shown bottom of the next page, where $a = s^2 L_{r1} C_{r1} R_{\text{eq}} + sL_{r1} + R_{\text{eq}}$. To achieve ZVS, the phase angle of Z_{DS} at the switching frequency is set above zero, thereby complying condition (c).

The phase angle of Z_{DS} at the fundamental frequency can be increased by reducing L_F. However, a small value of L_F will lead to a high ac current flowing through the inductor. This leads to a high ac loss on L_F, which sacrifices the converter's efficiency. Alternatively, the phase angle of Z_{DS} can be increased by decreasing f_{r1} to be slightly lower than f_s, i.e., increase the value of C_{r1}. The slight shift of the resonant frequency from the switching frequency will have negligible effect on the voltage gain of the resonant tank $L_{r1}C_{r1}$.

The procedure of designing the harmonics-boosted resonant inverter is summarized as follows:

1) Based on the level n of the rectifier stage, the required output voltage and power rating of the converter, the preliminary value of L_{r1} and C_{r1} is first determined according to (10).
2) Next, the values of L_F, C_{r2}, L_{r2}, and C_p can be determined using (11) and (12), and conditions (a) to (c).
3) Simulation is performed to check the voltage gain of the converter and the ZVS condition on switch S_1. If the voltage gain of converter is lower than the required value,

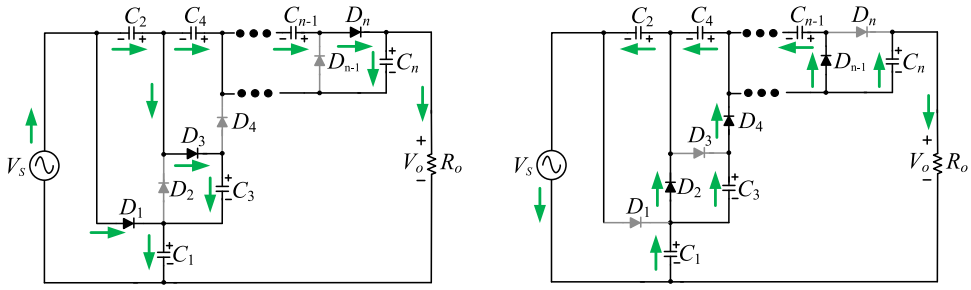


Fig. 9. Two operating states of the diode-capacitor rectifier. (a) When V_s reaches $V_{\text{smax}+}$ and (b) when V_s reaches $V_{\text{smax}-}$.

decrease L_{r1}. Conversely, if it is too high, increase L_{r1}. If ZVS does not occur, reduce the value of L_m or increase the value of C_{r1}.

B. Optimal Design of the Converter's Voltage Gain

The voltage gain of the proposed converter is the product of the voltage gains of the respective stages. By neglecting the voltage drop on the diodes, the voltage gain of the rectifier stage is

$$M_{\text{sc}} = n. \tag{13}$$

Thus, the voltage gain of the rectifier stage can be adjusted by changing the number of ladder network of the capacitors and diodes. By combining (7) and (8), the voltage gain of the inverter stage can be derived as

$$M_{\text{inv}} = \frac{2R_o}{\pi\omega_s L_{r1} {M_{\text{sc}}}^2}. \tag{14}$$

Thus, the voltage gain of the inverter stage can be adjusted through the design of the $L_{r1}C_{r1}$ tank. By combining (13) and (14), the voltage gain of the overall converter is derived as

$$M = \frac{2R_o}{\pi\omega_s L_{r1} n}. \tag{15}$$

There are different possible combinations of the voltage gains of the two stages to achieve the same overall voltage gain. However, there exists an optimal combination that achieves the highest power efficiency. Circuit simulation can be conducted to achieve this.

IV. Results and Discussion

This section describes the design of a 500 kHz, 57 times voltage gain converter that delivers 21 W of output power from a 3.3 V voltage source with open-loop control. The part number of S_1 is BSC010NE2LSI (voltage rating 25 V). The part number of diodes employed is NTSJ30U80CTG (80 V Schottky diode).

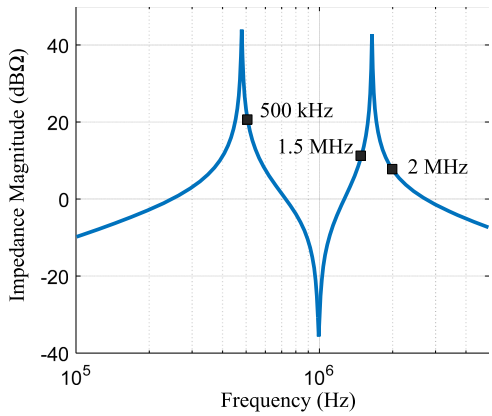


Fig. 10. Magnitude of impedance Z_m versus frequency with $L_F = 0.49$ μH, $C_p = 80$ nF, $L_{r2} = 0.23$ μH, and $C_{r2} = 109$ nF.

To find the optimal voltage gain combination for a 57 times voltage gain, the rectifier stage is set at 5-level to 15-level, of which circuit simulation will be performed. Under these settings, the inverter is designed for different combinations to attain a 57 times voltage gain.

The design process of the converter with 9-level diode-capacitor rectifier stage is detailed as an illustration.

1) According to (10), $L_{r1} = 0.66$ μH, and $C_{r1} = 153.5$ nF.
2) L_F, C_p, L_{r2}, and C_{r2} are chosen as 0.49 μH, 80 nF, 0.23 μH, and 109 nF. The Bode plots of impedance Z_m is shown in Fig. 10. The magnitude of Z_m peaks at the frequency near fundamental switching frequency and the frequency between third-and fourth-harmonic frequencies.
3) With these preliminary parameters, the simulation result shows that the voltage gain of the overall converter is 54 times. It is lower than the targeted voltage gain of 57 times.
4) The value of inductor L_{r1} is reduced to 0.62 μH and the C_{r1} is designed to resonate with L_{r1} at the switching frequency. The achieved voltage gain is now 57 times. However, the phase angle of Z_{DS} is lower than zero and ZVS cannot be achieved, as shown in Fig. 11.

$$Z_{\text{DS}}(s) = \frac{sL_F\left(1+\frac{s^2}{4{\omega_s}^2}\right)a}{\left(1+\frac{s^2}{4{\omega_s}^2}\right)\left(a+s^2L_FC_pa+s^2L_FC_{r1}(sL_{r1}+R_{\text{eq}})\right)+s^2L_FC_{r2}a}, \tag{12}$$

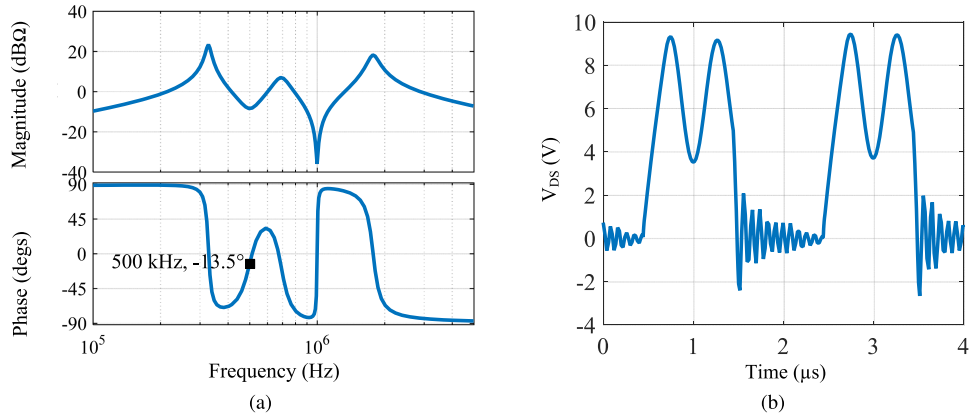


Fig. 11. (a) Bode plots of impedance Z_{DS} and (b) the simulated waveform of V_{DS} with $L_F = 0.49\,\mu H$, $C_p = 80$ nF, $L_{r2} = 0.23\,\mu$H, $C_{r2} = 109$ nF, $L_{r1} = 0.62\ \mu$H, and $C_{r1} = 162.4$ nF.

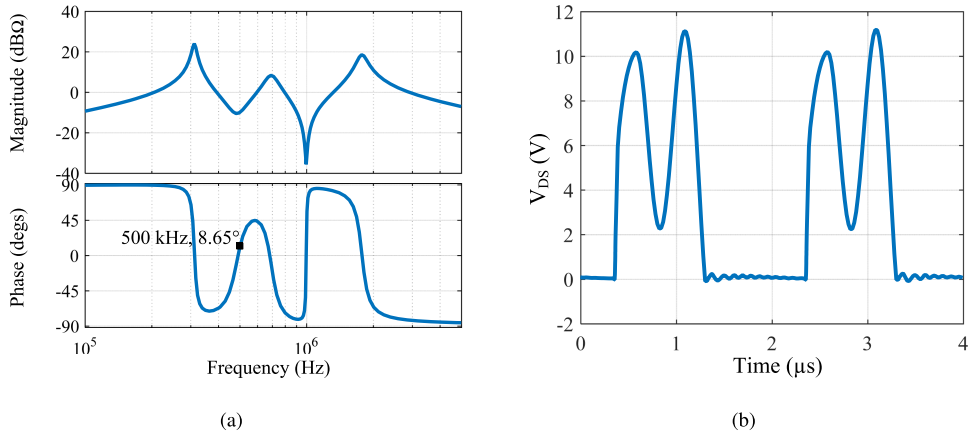


Fig. 12. (a) Bode plots of impedance Z_{DS} and (b) the simulated waveform of V_{DS} with $L_F = 0.49\,\mu$H, $C_p = 80$ nF, $L_{r2} = 0.23\,\mu$H, $C_{r2} = 109$ nF, $L_{r1} = 0.56\ \mu$H, and $C_{r1} = 195$ nF.

TABLE I
SIMULATION PARAMETERS OF THE CONVERTERS WITH DIFFERENT LEVEL RECTIFIER STAGES AT 3.3 V INPUT VOLTAGE, 57 TIMES VOLTAGE GAIN, 21 W OUTPUT POWER AND 500 KHZ SWITCHING FREQUENCY

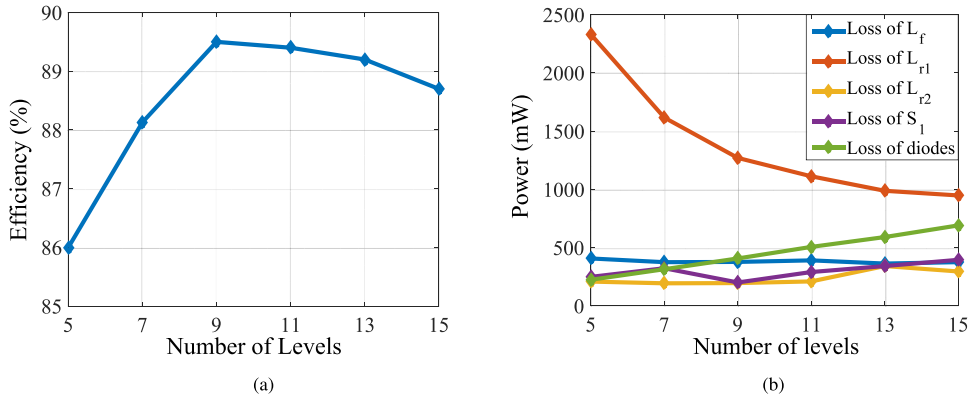
Level of Rectifier Stage	L_F (μH)	Cp (nF)	L_{r2} (μH)	C_{r2} (nF)	L_{r1} (μF)	C_{r1} (nF)
5	0.48	80	0.23	109	0.99	106
7	0.47	80	0.23	109	0.72	147
9	0.49	80	0.23	109	0.56	195
11	0.49	80	0.23	109	0.44	251
13	0.47	80	0.23	109	0.37	314
15	0.47	80	0.23	109	0.31	388

5) To achieve ZVS and 57 times voltage gain, L_{r1} is decreased to 0.56 μH and C_{r1} is set as 195 nF. The Bode plots of Z_{ds} is shown in Fig. 12(a). The phase of Z_{ds} at 500 kHz component is 8.65°. ZVS on S_1 is achieved as shown in Fig. 12(b).

By using the same procedure, 57-times resonant converters with 5-level to 15-level rectifier stages can be designed. The parameters are shown in Table I.

Fig. 13(a) shows the simulated efficiency of the converter for different levels of the rectifier stage. It is shown that the highest efficiency achievable by the converter is that with the nine-level diode-capacitor rectifier. The power loss breakdown of the converter for different levels of rectifier stage is shown in Fig. 13(b). The main loss of the inverter stage is from the loss on L_{r1}. It is decreased with an increasing rectifier's level. When the level is higher than 13, this loss does not change much. The loss on L_F , L_{r2}, and S_1 are quite stable from 5-level to 15-level. The loss on the diodes increases fairly linearly with an increasing level of the rectifier stage.

A prototype of the converter with nine-level diode-capacitor rectifier stage, as shown in Fig. 14, has been constructed. The parameters of the prototype are shown in Table II. Fig. 15 shows the waveforms of the input current and output voltage of the converter, the current of inductor L_F, the driver's signal and their ripples. The output voltage is 188 V, i.e., a voltage gain of 57 times is achieved. The ripple of the output voltage is 3.2 V, which is 1.7% of the output voltage. The input current ripple is 0.17 A which is 2.3% of the input current. The current of L_F is above zero at all time. This shows that there is no returning current flowing back into the power source. Fig. 16(a) shows



(a) (b)

Fig. 13. (a) Simulated efficiency and (b) the loss breakdown of the harmonics-boosted resonant converter with varying levels of the diode-capacitor rectifier stage at 3.3 V input voltage, 57 times overall voltage gain and 21 W output power.

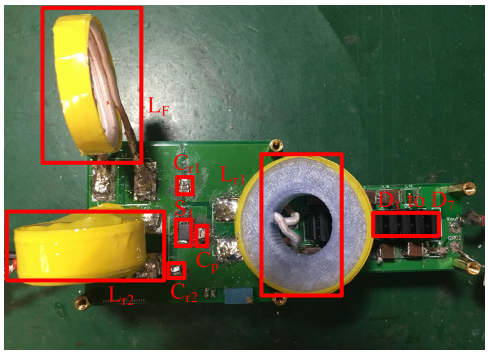


Fig. 14. Prototype of the harmonics-boosted resonant converter with nine-level diode-capacitor rectifier stage.

TABLE II
EXPERIMENTAL PARAMETERS OF THE HARMONICS-BOOSTED CONVERTER WITH 9-LEVEL DIODE-CAPACITOR RECTIFIER STAGE AT 3.3 V INPUT VOLTAGE, 57 TIMES VOLTAGE GAIN, 21 W OUTPUT POWER AND 500 KHZ SWITCHING FREQUENCY CONVERTER

Part	Value	Part Number
C_{in}	70 μF	7 Parallel C3216X5R1H106K160AB
L_F	0.49 μH	Air Core Inductor
L_r1	0.56 μH	Air Core Inductor
L_r2	0.23 μH	Air Core Inductor
C_p	80 nF	10 Parallel C1206C103J2GACAUTO
C_{r1}	195 nF	1 C3216COG2A104J160AC + 1 C2012C0G2A333J125AC + 1 C1206H4731GACTU + 1 C2012C0G1H153J085AA
C_{r2}	109 nF	1 C3216COG2A104J160AC + 1 GRM2195C1H752JA01D
S_1		BSC010NE2LSI
D_1 to D_9		NTSJ30U80CTG
C_1 to C_9		3 Parallel C5750X7S2A106M230KB

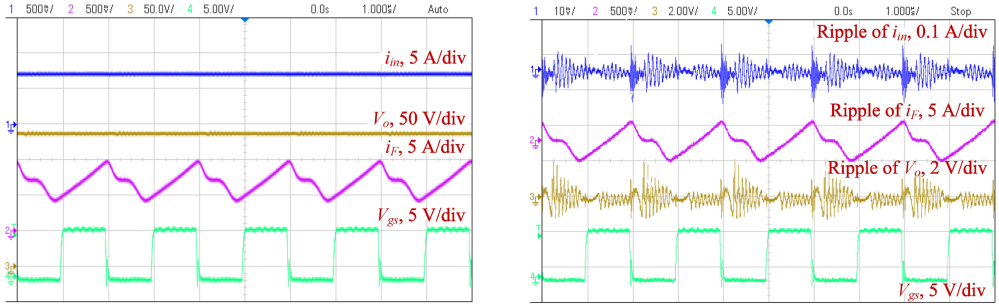
the waveforms of the drain-to-source voltage $V_{\rm DS}$, the output voltage V_s of inverter stage and the voltage across capacitors C_1 and C_3. Fig. 16(b) shows the waveforms of the ripple voltage across capacitors C_1 and C_3. The positive and negative peak voltages ($V_{\rm smax+}$ and $V_{\rm smax+}$) of V_s are around 27 and 20.4 V, respectively. The voltage across C_1 (V_{C_1}) is around 24 V, which is slightly lower than $V_{\rm smax+}$. The voltage across C_3 (V_{C_3}) is around 42 V, which is slightly lower than $V_{\rm smax+} + V_{\rm smax-}$. The ripple of V_{C1} is around 0.8 V, which is 3.3% of V_{C1}. The ripple of V_{C3} is around 1.15 V, which is 2.7% of V_{C3}. Fig. 17 shows the waveforms of the voltage across S_1 ($V_{\rm DS}$) and the driver signal V_{gs}. The enlarged figure shows that S_1 is operating with ZVS.

An fast Fourier transform (FFT) analysis of the inverter stage's output voltage (V_s) is conducted and the result is shown in Fig. 18(a). It shows that V_s is mainly composed of fundamental (magnitude 19.2 V), the third-harmonic (magnitude 3.4 V) and the fourth-harmonic (magnitude 2.5 V) voltage components. The waveforms of fundamental, third-harmonic, and fourth-harmonic voltage components of V_s, the synthetic voltage (sum of fundamental, third-harmonic, and fourth-harmonic voltage components) and V_s are depicted in Fig. 18(b). The difference between the synthetic voltage and V_s is small. Compared with the voltage containing only the fundamental voltage component, the peak value of the synthetic voltage, especially the positive one, has been increased by the third-and fourth-harmonic voltage components. Theoretically, with only the fundamental component, the amplitude of the inverter stage's output voltage will be 19.2 V, and the achievable V_o is 172.8 V even if power loss on the rectifier stage is neglected. Then, the voltage gain will be 52.4 times, which is lower than 57 times. The measured efficiency of the converter is 88.6%, which is slightly lower than the simulated efficiency of 89.5% given in Fig. 13(a). The slight difference is due to parameters' tolerance effect between practical components and components used in simulation. If the driver's loss of 0.21 W is included, the measured efficiency is 87.85%.

The performance of the proposed converter is compared with that of others works and is shown in Table III. It is shown that the proposed converter can achieve a high efficiency even with a low input voltage and at a very high voltage gain.

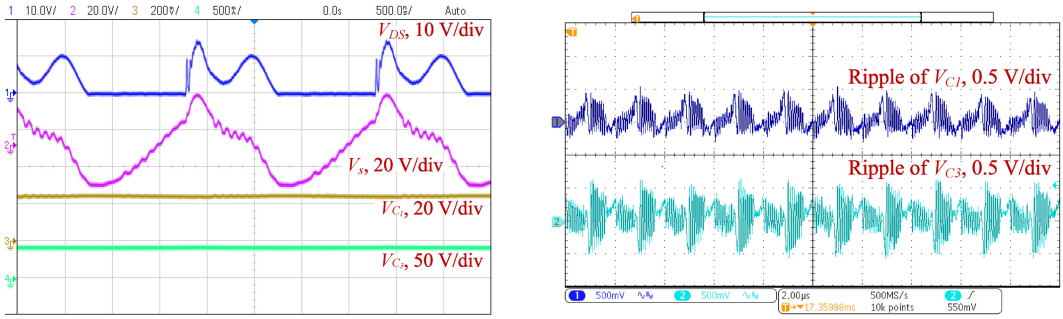
V. BRIEF DISCUSSION ON THE POTENTIAL CONTROL STRATEGIES

The potential control strategies for the proposed converter include the ON–OFFcontrol strategy [33], [34] and frequency



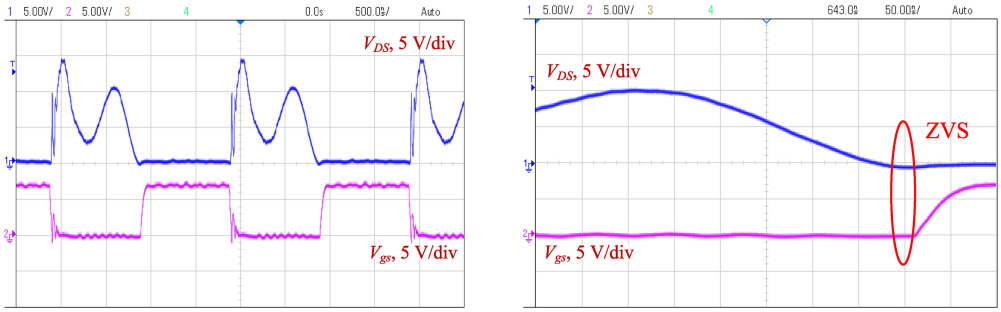
(a) (b)

Fig. 15. Waveforms of (a) input current, inductor L_F current, output voltage and driver's signal and (b) their ripples.



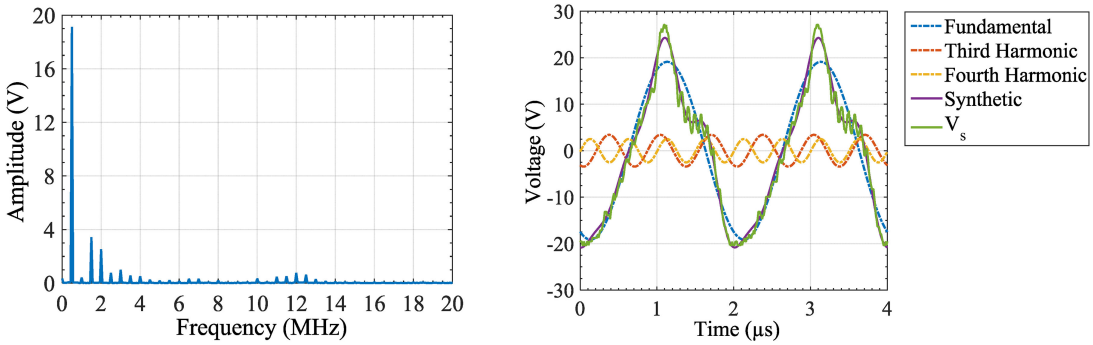
(a) (b)

Fig. 16. Waveforms of (a) $V_{\rm DS}$, V_s, V_{C_1}, and V_{C_3} and ripple of (b) V_{C_1} and V_{C_3}.



(a) (b)

Fig. 17. (a) $V_{\rm DS}$ and V_{gs}, and (b) enlarged $V_{\rm DS}$ and V_{gs}.



(a) (b)

Fig. 18. (a) FFT analysis of inverter stage's output voltage V_s and waveforms of (b) the fundamental, the third-harmonic, and the fourth-harmonic voltage components of V_s, synthetic voltage (the sum of fundamental, third- and fourth-harmonics voltage components) and V_s.

TABLE III
COMPARISONS FOR DIFFERENT HIGH-VOLTAGE-GAIN CONVERTERS

The converter in	Input Voltage (V)	Output Power (W)	Voltage Gain (times)	Switching Frequency (MHz)	Efficiency (%)
[12]	4.2	14	42.9	0.1	∼83
[25]	11	25	36.4	0.2	∼91.5
[28]	40	100	50	27.12	84
Proposed	3.3	21	57	0.5	88.6

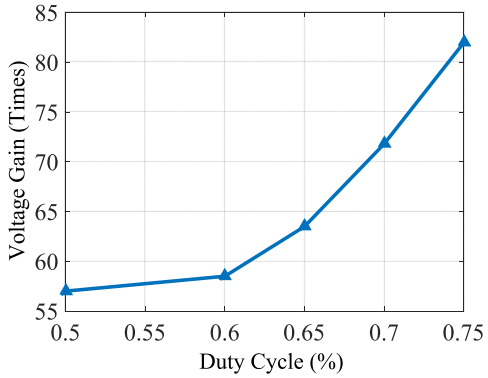


Fig. 19. Simulated voltage gain of the proposed converter versus duty cycle.

control strategy [35] that are commonly applied to resonant converters.

With the ON–OFF control strategy, output voltage regulation of the converter will be achieved by enabling and disabling the operation of the converter according to two prefixed set points. When the output voltage of the converter falls below a prefixed lower set point, the converter is enabled to operate at a fixed frequency and duty cycle in ZVS operation. When the output voltage rises above a prefixed upper set point, the converter is fully disabled until the next instance when the output voltage falls below the lower set point. Then, the converter is once again enabled to operate to increase the output voltage. Such a turning ON and OFF process of the converter is repeated to achieve the regulation of the output voltage. While this could be an effective means of providing voltage regulation, the use of this approach requires the output capacitor of the converter to be larger than otherwise required to achieve the same output voltage holding time of the converter.

On the other hand, it is also possible to utilize the frequency control strategy to adjust the switching frequency to achieve voltage regulation. However, similar to typical resonant converters, such a control strategy is good only for a narrow operating range of the input voltage and load, as ZVS may be lost when the switching frequency is deviated far from the nominal frequency. Moreover, the design of such a controller will require an appropriate mathematical model of the converter to be derived, which is not straightforward.

Alternatively, it may be possible to apply duty cycle control to the proposed converter to achieve voltage regulation. Our preliminary open-loop simulation result of the voltage gain versus the duty cycle of the switch of the converter, as shown in Fig. 19, has validated our hypothesis. It is shown that the voltage gain is increased from 57 times to 85.8 times with the increase of duty cycle from 0.5 to 0.75.

Nevertheless, as the implementation of such a controller is nontrivial and requires further investigation, it will be not reported in this research paper.

VI. CONCLUSION

In this paper, a nonisolated high step-up dc/dc converter that combines a harmonics-boosted resonant inverter stage and a passive diode-capacitor-rectifier stage is presented. Differing from conventional inverter stages that output a pure sinusoidal voltage waveform, in the proposed converter, the output of its inverter is a voltage waveform comprising the fundamental, the third- and fourth-harmonic components. The utilization of these harmonics increase the peak voltage of the inverter stage, which lead to a higher voltage gain of the overall converter. To facilitate the design of this converter, a set of conditions and guidelines are proposed. By complying these conditions, ZVS on the active switch is also achieved. A method of finding the optimal gain combination of the two stages of the converter to achieve the highest possible efficiency has also been proposed. Simulation results show that for a 57-time conversion ratio, 21 W output power and 3.3 V input voltage, the highest efficiency achievable by the proposed converter is one with a 9-level rectifier stage. The experimental results show that the converter achieves a voltage gain of 57 times, operates with ZVS, and that the achievable efficiency is as high as 88.6%. As compared to a similar converter operating without the harmonics boosting function, the output voltage of the inverter stage will be a pure sinusoidal waveform with an amplitude of 19.2 V, and that the output of the rectifier stage will only be 172.8 V dc even if power loss on the rectifier stage is neglected. This gives a gain of only 52.4 times, which is lower than that achievable by the proposed converter. Therefore, the usefulness of utilizing harmonic components in increasing the peak of the output voltage of the inverter stage to increase the voltage gain of the converter is validated. The main limitation of the proposed converter is that the voltage gain is sensitive to the load condition. Thus, the controller design for a wide load range is nontrivial.

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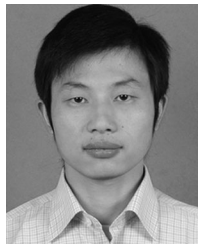
Mrs. Huang received the Best Paper Award at the 8th Annual IEEE Energy Conversion Congress & Expo (IEEE ECCE 2016).



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