Modified High-Efficiency *LLC* Converters With Two Split Resonant Branches for Wide Input-Voltage Range Applications

Wenjin Sun, *Student Member, IEEE*, Yan Xing, *Member, IEEE*, Hongfei Wu, *Member, IEEE*, and Jie Ding

***Abstract*—This paper proposes a novel modified *LLC* converter with two split resonant branches for wide input-range applications. It can operate in low-gain (LG) mode or medium-gain (MG) mode. The voltage gain of MG mode is 1.5 times that of LG mode, while they have same range of voltage gain $M_{\text{tank\_range}}$, i.e., the ratio of maximum voltage gain to minimum one. Therefore, the input voltage can be regulated in a wide range by operating the converter in different modes. To achieve the transition between modes, the required $M_{\text{tank\_range}}$ of the proposed converter is as low as 1.5, resulting in lower magnetizing current and higher efficiency within the entire operation range. Smooth transition can be achieved by adjusting the duty cycles of switches gradually. The proposed *LLC* converter with primary dual-bridge is analyzed in detail as an example. To verify the theoretical analysis and performance of proposed solution, a 1-kW 400-V output prototype with input voltage ranging from 80 to 200 V is built, tested, and compared with two existing full-bridge *LLC* converters. Analysis and experimental results indicate that smaller volume of transformers, reduced rectifying diodes, and higher overall efficiency are achieved with the proposed converter.**

***Index Terms*—DC–DC converter, *LLC* converter, two transformer, wide voltage range.**

I. Introduction

AMONG various clean energy sources, fuel cell is one of the most efficient energy sources that are promising in the near future to alleviate the environmental problems of global warming, air pollution, acid precipitation, and so on [1]–[3]. It has been an attractive power supply source for applications such as distributed generation power systems and electrical vehicles because of its cleanness, low noise, high efficiency, and high-power density [2]–[4]. However, due to the high output impedance and slow dynamic response, the fuel cell shows a wide variation in output voltage under different load conditions, which is too wide to source the inverter directly [5]–[8]. Then a dc–dc converter, capable of handling the wide input-voltage range, is needed. For safety and electromagnetic compatibility reasons, galvanic isolation is often required. Thus, high-frequency transformers are also involved in the dc–dc converter [7], [8].

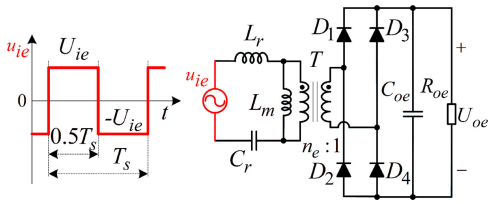

Fig. 1. Equivalent circuit of the *LLC* converters during the theoretic analysis of voltage gain.

As a common isolated dc–dc converter, the phase-shift full-bridge (PSFB) converter has been widely used for medium to large power applications [9]–[12]. However, it is faced with the loss of lagging switches' ZVS turn-ON at light load and the reverse recovery problem of secondary rectifiers. In [9] and [10], a hybrid bridge structure on the primary side has been provided to improve the ZVS condition of lagging switches. Furthermore, the problem can also be eased by an auxiliary half-bridge (HB) *LLC* converter in [11] and [12]. As the waveforms of secondary current are different, the main PSFB converter and the auxiliary HB *LLC* are first rectified and then in series or in parallel, leading to a lot of rectifying diodes. To solve the problem of reverse recovery, the scheme of clamping circuits on secondary-side can be adopted [11], [12]. However, all these methods will make the PSFB converter more complex.

Compared with the PSFB, the *LLC* converter has a simpler structure of rectifier circuit, and ZVS of all switches can be achieved within the entire operation range. These advantages make it a good candidate for wide input-range applications [13]–[18]. With the turn-ratio n of transformer, the voltage gain M of the conventional full-bridge (FB) *LLC* converter can be calculated as nU_o/U_{in}. And the range of M can be defined as M_{range}. However, there are different switching networks and rectifier circuits for *LLC* converters [19]–[23]. When analyzing their voltage gain ideally, all of them can be simplified into the same equivalent circuit in Fig. 1. The voltage gain M_{tank} of *LLC* resonant tank can be defined as $M_{\text{tank}} = n_e U_{oe}/U_{ie}$, where n_e, U_{ie}, and U_{oe} are the equivalent turn-ratio of transformer, input voltage, and output voltage, respectively. As dependent on load and limited by the ZVS achievement of switches,

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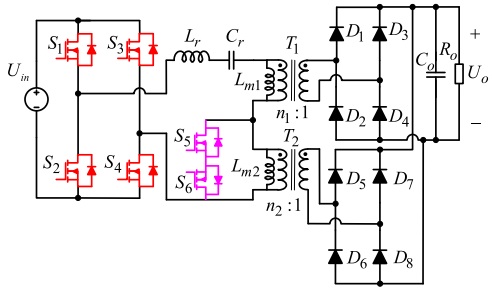

Fig. 2. Topology of the improved FB *LLC* converter with two transformers in [23].

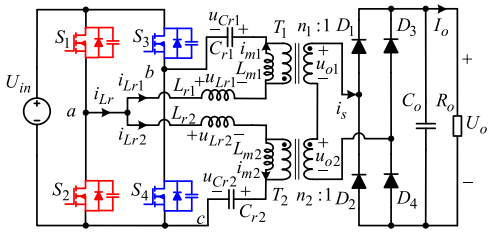

Fig. 3. Topology of the proposed SB *LLC* converter with dual-bridge and split inductors (DSBS *LLC*).

the range of M_{tank} within the whole load range is scaled by $M_{\text{tank\_range}} = M_{\text{tank\_max}}/M_{\text{tank\_min}}$. For the conventional FB *LLC* with center-tapped rectifier, $n_e = n$, $U_{ie} = U_{\text{in}}$, and $U_{oe} = U_o$. Then the ratio *A* of *M* to M_{tank} and the ratio *B* of M_{range} to $M_{\text{tank\_range}}$ are both 1. However, with the topology-morphing control in [22], the FB *LLC* can also be operated in HB mode, and then the ratio *A* can also be 0.5 due to $U_{ie} = 0.5\,U_{\text{in}}$. With two operation modes, the ratio *B* of FB *LLC* in [22] is 2.

When applied to wide input-range applications, the overall efficiency of traditional *LLC* converters will be deteriorated, owing to the small magnetizing inductance and increased circulating current. In order to overcome this issue, a lot of methods have been proposed [19]–[23]. An asymmetrical duty cycle control method is presented in [19] and [20] to achieve the regulation of input-voltage range by four times, i.e., $M_{\text{range}} = 4$. However, during the transition between two modes, the duty cycle of primary switches cannot be gradually changed. Another method is the topology-morphing proposed in [21] and [22]. As the up-switch of one bridge-leg is permanently OFF and the down-switch of the same leg is permanently ON, the FB *LLC* converter is morphed to a HB *LLC*. While they have the same range $M_{\text{tank\_range}}$ of *LLC* resonant tank, the voltage gain of HB *LLC* is half of FB *LLC*. And $M_{\text{tank\_range}}$ should be larger than 2 to achieve soft transition between modes. However, most design results demonstrate that the *LLC* converter has higher overall efficiency with $M_{\text{tank\_range}}$ below 1.6 [14]–[16]. To narrow the required range $M_{\text{tank\_range}}$, two transformers are employed in Fig. 2 [23]. With the help of auxiliary transformer, the converter can reduce primary current by adaptively changing the equivalent turn-ratio and magnetizing inductance. However, only the main transformer delivers power throughout. Owing to

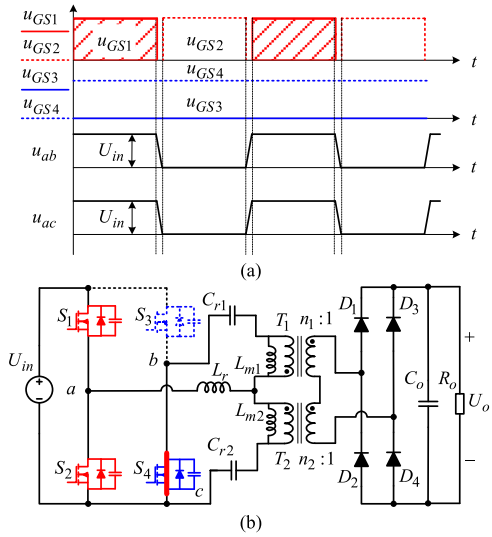

Fig. 4. Operation of the DSBS *LLC* converter in the LG mode: (a) Driver signals, and (b) equivalent circuit.

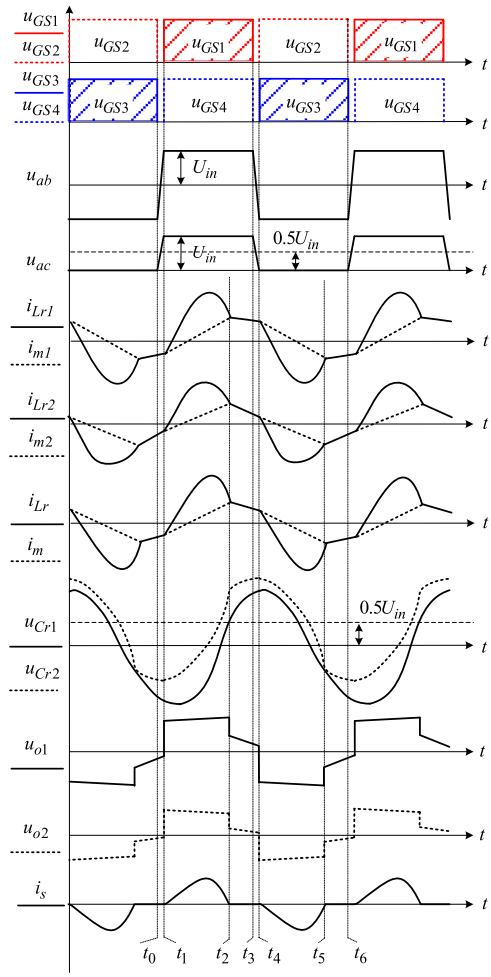

Fig. 5. Key operation waveforms of the proposed DSBS *LLC* converter in the MG mode with $f_s < f_r$.

low utilization, the total volume of transformers is larger. What is worse, it needs more secondary rectifiers. And the state of bidirectional switch $S_5\&S_6$ during the mode transition cannot be gradually changed.

Inspired by [9]–[12] and [21]–[23], the concept of splitting the *LLC* resonant tank into two branches has been proposed in this paper to narrow the required range $M_{\text{tank\_range}}$, thus improving the efficiency. The derived *LLC* converter can operate in low-gain (LG) mode or medium-gain (MG) mode, and the voltage gain of MG mode is 1.5 times that of LG mode. Then the proposed *LLC* converter can be used for wide input-voltage range applications. Different from these methods in [19]–[22], its required range $M_{\text{tank\_range}}$ to achieve the mode-transition is as low as 1.5. Both of two transformers transfer power within the entire operation range, resulting in high utilization ratio and smaller volumes of power transformers. In addition, reduced rectifying diodes, smooth transition between modes, and high overall efficiency can also be achieved by the proposed converter.

II. Proposed DSBS *LLC* Converter and Its Operational Principle

The proposed *LLC* converter with dual-bridge and two split resonant branches (DSBS *LLC*) is illustrated in Fig. 3. In order to narrow the required range $M_{\text{tank\_range}}$ of *LLC* resonant tank, a FB *LLC* converter and a HB *LLC* converter are in parallel on the primary and in series on the secondary. They have the same resonant parameters, i.e., $L_{r1} = L_{r2} = 2L_r$, $L_{m1} = L_{m2} = 2L_m$, $C_{r1} = C_{r2} = 0.5\,C_r$, and $n_1 = n_2 = 2n_e$. The switching-leg composed of S_1 and S_2 is shared by the FB and HB *LLC*, therefore, only four switches are used on primary side. The secondary windings of T_1 and T_2 are in series and connected to a FB rectifier. Therefore, the current flowing through the two secondary windings are always the same, while the voltage stress of rectifying diodes is clamped to the output voltage U_o.

By changing the modulation strategies, the proposed converter has two operation modes.

1) Low-gain mode: As shown in Fig. 4(a), the converter operates in the LG mode when S_3 is kept in OFF state while S_4 in ON state. The switches S_1 and S_2 are driven complementarily with 50% duty cycle. Then the voltage u_{ab} between middle points "*a*" and "*b*" of the two switching-legs is 50% rectangular wave with peak of $\pm U_{\text{in}}$. And so is the u_{ac}. In this case, the proposed converter in Fig. 4(b) operates as a HB *LLC*. Due to the simplicity, the detailed analysis of LG mode is not provided here.
2) Medium-gain mode: The converter operates in the MG mode when all the switches S_1-S_4 on primary side are high-frequency switched. The duty cycle of all these switches is 50%, and the switches in the same switching-leg are driven complementary, while the bridge-leg $S_3\&S_4$ is in 180° phase-shift relative to $S_1\&S_2$. The key operation waveforms of the proposed converter in the MG mode are shown in Fig. 5. The voltage u_{ac} is the 50% rectangular wave with peak of $+U_{\text{in}}$ and dc bias $0.5\,U_{\text{in}}$, while u_{ab} is still the one with peak of $\pm U_{\text{in}}$. When the converter operates at resonant frequency $f_s = f_r$, the output u_{o1} and u_{o2} of transformers are $\pm U_{\text{in}}/n_1$ and $\pm 0.5\,U_{\text{in}}/n_2$, respectively. The normalized voltage gain $n_e U_o/U_{\text{in}}$ is $(1+0.5)/2 = 0.75$.

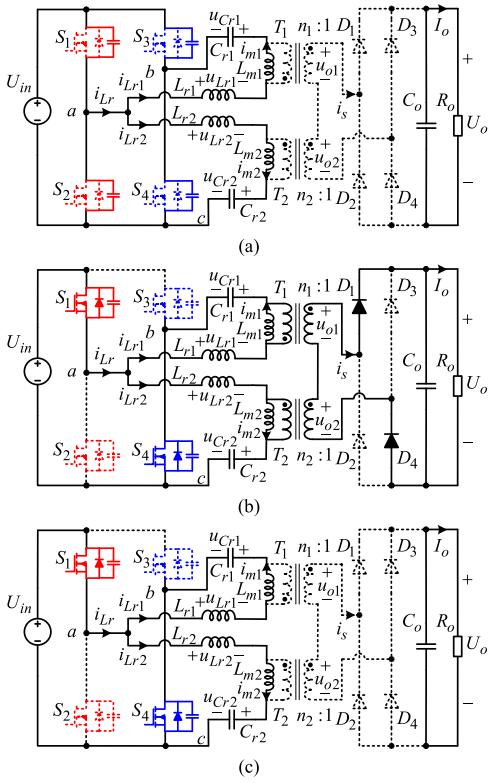

Fig. 6. Operation states of the DSBS *LLC* converter in the MG mode: (a) State 1 $[t_0,\ t_1]$, (b) state 2 $[t_1,\ t_2]$, and (c) state 3 $[t_2,\ t_3]$.

In Fig. 5, the resonant current i_{Lr} is the sum of two branches' currents i_{Lr1} and i_{Lr2}, and its corresponding magnetizing current is $i_m = i_{m1} + i_{m2}$. There are total six switching states during the whole cycle. Fig. 6 shows the equivalent circuits for each switching state during a half-cycle.

State 1 $[t_0,\ t_1]$ [see Fig. 6(a)]: Before t_0, switches S_2 and S_3 are turned ON. The resonant currents i_{Lr} and i_{Lr1} are negative. At t_0, all of switches are turned OFF. The current i_{Lr} charges the parasitic capacitor of S_2 and discharges the one of S_1. In a similar way, the current i_{Lr1} charges that of S_3 and discharges that of S_4. When the voltage u_a of the middle point "*a*" increases to the input voltage U_{in} and the voltage u_b decreases to 0, the negative current i_{Lr} and i_{Lr1} flow through the body diodes of S_1 and S_4, respectively, creating ZVS conditions for their turn on. This state ends at t_1.

State 2 $[t_1,\ t_2]$ [see Fig. 6(b)]: At t_1, switches S_1 and S_4 are turned ON with ZVS, and the secondary diodes D_1 and D_4 start to conduct. The voltage u_{ab} and u_{ac} is U_{in}, and the sum of output voltage u_{o1} and u_{o2} is U_o. Both of the voltages across two magnetizing inductance L_{m1} and L_{m2} are clamped by the reflected output voltage, resulting in their current i_{m1} and i_{m2} increasing. The inductor L_{r1} resonates with capacitor C_{r1}, while L_{r2} resonates with C_{r2}. The input source pumps the energy into the output load through two resonant branches. This

state continues until the currents i_{Lr}, i_{Lr1}, and i_{Lr2} meet their magnetizing currents i_m, i_{m1}, and i_{m2} at t_2.

State 3 [t_2, t_3] [see Fig. 6(c)]: As secondary current i_s decreases to zero naturally at t_2, the diodes D_1 and D_4 can achieve ZCS turn-off. During this state, the sum of u_{o1} and u_{o2} is between $-U_o$ and $+U_o$. And L_{m1} is free from the clamping of reflected output voltage and participates in the resonance along with L_{r1} and C_{r1}. So does L_{m2}. This state ends when the switches S_1 and S_4 are turned OFF at t_3. And a new state, symmetric to state 1, begins.

III. Characteristics of the DSBS *LLC* Converter

The discussion in Section II indicates that the proposed DSBS *LLC* converter has a unique architecture, which brought forth some special characteristics. For better understanding, these features are discussed in this section.

A. Voltage Gain of the DSBS LLC

In the LG mode, the proposed DSBS *LLC* operates as a conventional HB *LLC*. Then its voltage gain $M_{\rm LG}$ can be derived easily, and the ratio *A* is 0.5. The following is focused on the voltage gain $M_{\rm MG}$ in the MG mode.

According to the operation principles in the MG mode, it is obvious that u_{ab} has no dc bias, while u_{ac} has a dc bias $0.5\,U_{\rm in}$. Due to the volt-second balance of L_{r2} and L_{m2}, the dc bias $0.5\,U_{\rm in}$ of u_{ac} is undertaken by the resonant capacitor C_{r2} in Fig. 5. Hence, the state variables i_{Lr2}, i_{m2}, and $u'_{Cr2} = u_{Cr2} - 0.5\,U_{\rm in}$ can be calculated as a conventional HB *LLC* converter [24]. Ignoring the dead time t_0-t_1, the state variables of two resonant branches at t_0-t_2 can be expressed by

$$\begin{cases} \dot{u}_{Cr1} = i_{Lr1}/C_{r1} \\ \dot{i}_{Lr1} = -u_{Cr1}/L_{r1} + (U_{in} - n_1 u_{o1})/L_{r1} \\ \dot{i}_{m1} = n_1 u_{o1}/L_{m1} \end{cases} \tag{1}$$

$$\begin{cases} \dot{u}'_{Cr2} = i_{Lr2}/C_{r2} \\ \dot{i}_{Lr2} = -u'_{Cr2}/L_{r2} + (0.5\,U_{in} - n_2 u_{o2})/L_{r2} \\ \dot{i}_{m2} = n_2 u_{o2}/L_{m2}. \end{cases} \tag{2}$$

As the sum of (1) and (2), the current i_{Lr} and i_m at t_0-t_2 can be expressed as follows with $L_{r1} = L_{r2} = 2L_r$, $L_{m1} = L_{m2} = 2L_m$, $C_{r1} = C_{r2} = 0.5\,C_r$, and $n_1 = n_2 = 2n_e$:

$$\begin{cases} u_{Cr} = (u_{Cr1} + u'_{Cr2})/2 \\ \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = \dot{i}_{Lr1} + \dot{i}_{Lr2} = (-u_{Cr} + 0.75\,U_{in} - n_e U_o)/L_r \\ \dot{i}_m = \dot{i}_{m1} + \dot{i}_{m2} = n_e U_o/L_m. \end{cases} \tag{3}$$

Similarly, the current i_{Lr} and i_m at t_2-t_3 can be calculated by

$$\begin{cases} u_{Cr} = (u_{Cr1} + u'_{Cr2})/2 \\ \dot{u}_{Cr} = i_{Lr}/C_r \\ \dot{i}_{Lr} = \dot{i}_{Lr1} + \dot{i}_{Lr2} = (-u_{Cr} + 0.75\,U_{in} - n_e U_o)/(L_r + L_m) \\ i_m = i_{m1} + i_{m2} = i_{Lr1} + i_{Lr2}. \end{cases} \tag{4}$$

From (3) and (4), it can be found that the DSBS *LLC* in the MG mode has the same characteristics as a FB *LLC* converter, except for the existing source $0.75\,U_{\rm in}$ shown in Fig. 7. And then

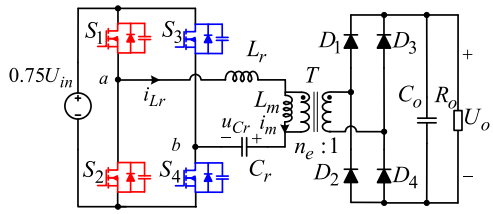

Fig. 7. Equivalent converter of the proposed DSBS *LLC* converter in the MG mode.

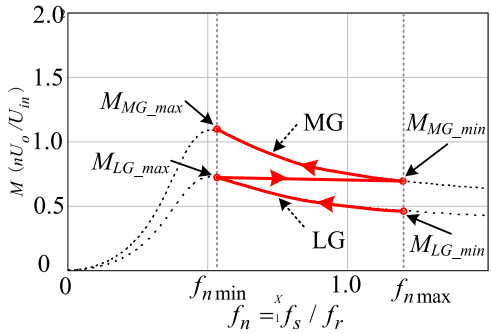

Fig. 8. DC gain curves of the proposed DSBS *LLC* converter under the same load condition.

the ratio *A* of MG mode is 0.75. Based on the FHA analysis, the voltage gain of DSBS *LLC* in the MG mode can be easily obtained as

$$M_{MG}(L_n, f_n, Q) = \frac{n_e U_o}{U_{in}} = \frac{0.75}{\sqrt{\left[1 + \frac{1}{L_n}\left(1 - \frac{1}{f_n^2}\right)\right]^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}}. \tag{5}$$

Where the magnetizing inductance ratio L_n, the normalized switching frequency f_n, and the normalized output power *Q* are defined as follows:

$$\begin{cases} L_n = L_m/L_r \\ f_r = 1/(2\pi\sqrt{L_r C_r}) \\ f_n = f_s/f_r \\ Q = \pi^2\sqrt{L_r/C_r}/(8n_e^2 R_o). \end{cases} \tag{6}$$

Although $M_{\rm LG}$ and $M_{\rm MG}$ have different ratio *A*, they have the same range, i.e., $M_{\rm tank\_range}$. Fig. 8 shows the voltage gains of the proposed DSBS *LLC* converter in two modes. As $M_{\rm MG}$ is 1.5 times of $M_{\rm LG}$, the maximum voltage gain $M_{\rm LG\_max}$ of LG should be larger than the minimum one $M_{\rm MG\_min}$ of MG to achieve the transition between two modes. Then it can be found from (7) that the range $M_{\rm tank\_range}$ of *LLC* resonant tank should be larger than 1.5 to achieve the transition. Operating in two modes, the DSBS *LLC* can achieve the regulation of wide input-voltage range, i.e., $M_{\rm range} = M_{\rm MG}/M_{\rm LG} * M_{\rm tank\_range} = 1.5 M_{\rm tank\_range}$ and the ratio $B = 1.5$. Since the higher overall efficiency of *LLC* converter can be achieved when $M_{\rm tank\_range}$ below 1.6, the optimal input-voltage range of the

DSBS *LLC* is around 2.4:

$$M_{\text{tank\_range}} = M_{\text{LG\_range}} = \frac{M_{\text{LG\_max}}}{M_{\text{LG\_min}}} \geq \frac{M_{\text{MG\_min}}}{M_{\text{LG\_min}}} = 1.5. \tag{7}$$

B. Power Distribution Between Two Transformers

Due to the same parameters of two resonant branches, it is obvious that the output power P_{T1} and P_{T2} of two transformers in the LG mode are equal to each other, i.e., $P_{T1} = P_{T2} = P_o/2$. And the power distribution in the MG mode is as follows.

From the waveforms of MG mode in Fig. 5, the average input power P_{in1} and P_{in2}, absorbed by two resonant branches from u_{ab} and u_{ac}, respectively, can be expressed as

$$P_{in1} = 2U_{in} f_s \int_{t0}^{t3} i_{Lr1} dt, P_{in2} = U_{in} f_s \int_{t0}^{t3} i_{Lr2} dt. \tag{8}$$

In addition, derived from the equivalent converter in Fig. 7, the total input power of DSBS *LLC* in the MG mode can be expressed as

$$P_{in} = 1.5\, U_{in} f_s \int_{t0}^{t3} i_{Lr} dt = 1.5\, U_{\mathbf{in}} f_s \int_{t0}^{t3} (i_{Lr1} + i_{Lr2}) dt. \tag{9}$$

Due to $P_{\text{in}} = P_{in1} + P_{in2}$, there are following constraints for currents i_{Lr1} and i_{Lr2}:

$$\int_{t0}^{t3} i_{Lr1} dt = \int_{t0}^{t3} i_{Lr2} dt. \tag{10}$$

Ignoring the power loss during power conversion, i.e., $P_{\text{in}} = P_o$, P_{in1} and P_{in2} in the MG mode can be calculated as (11). And the output power P_{T1} and P_{T2} of two transformers are just P_{in1} and P_{in2}, respectively. During the whole input range, the maximum of P_{T1} is $2P_o/3$ in the MG mode, whereas the maximum of P_{T2} is $P_o/2$ in the LG mode:

$$P_{\text{T1}} = P_{\mathbf{in1}} = 2P_o/3, P_{T2} = P_{\mathbf{in2}} = P_o/3. \tag{11}$$

The voltage gain M_{MG} is derived from the transient equations in the above section. Then (8) and (9) in a switching cycle are always true. As derived from them, the power distribution (11) of transformers in the MG mode will never change, no matter whether the load P_o or input voltage U_{in} changes. And it is also true for the LG mode.

During the transitions between LG and MG mode, a soft scheme is applied to make the mode transition smooth, which will be illustrated in Section IV-B. As is more difficult than the MG or LG mode, the power distribution of P_{T1} and P_{T2} during the mode transition is analyzed with the simulation in PSIM. As shown in Fig. 9, the transition from MG to LG is taken for example. T_Z is the sign that indicates the transition is whether happening ($T_Z = 1$) or not ($T_Z = 0$). If the input U_{in} is increased above the threshold voltage, the transition is triggered, and T_Z is set 1. When the transition is completed, T_Z is set 0 again. During the transition, the converter is still regulated to keep the output voltage U_o and current I_o constant. And the ratio P_{T1}/P_o is gradually reduced from 2/3 in the MG mode to 1/2 in the LG mode. Similarly, during the transition from LG to MG, the ratio P_{T1}/P_o is increased gradually in the reverse direction.

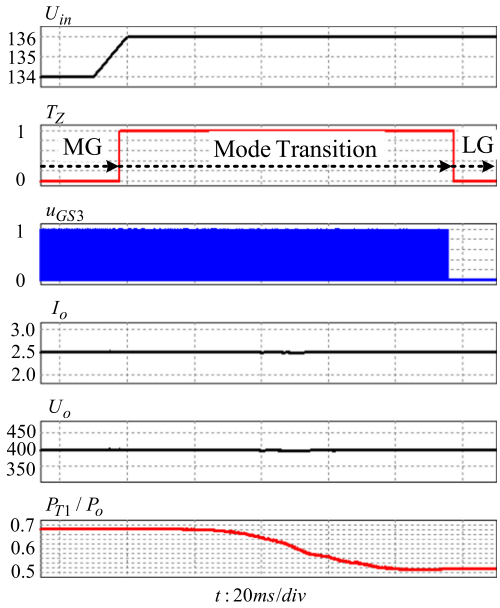

Fig. 9. Simulation waveforms of the power distribution during the transition from MG to LG.

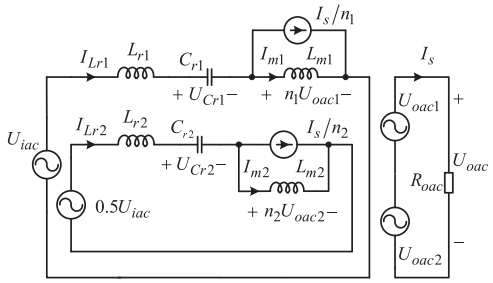

Fig. 10. FHA equivalent circuit of the proposed DSBS *LLC* converter in the MG mode.

C. Current Distribution Between Two Resonant Branches

Although the analysis methods mentioned in [25]–[28] feature high accuracy, the FHA analysis method is simpler and more straightforward to analyze the *LLC* converters [14]. As it can still meet the requirements of engineering, it is adopted here to analyze the characteristic of current distribution between two resonant branches of DSBS *LLC*.

Due to the same parameters of two resonant branches, it is obvious that the resonant currents i_{Lr1} and i_{Lr2} in the LG mode are equal to each other, i.e., $i_{Lr1} = i_{Lr2} = 0.5\, i_{Lr}$. The current distribution in the MG mode is as follows.

Fig. 10 shows the FHA equivalent circuit of DSBS *LLC* in the MG mode. And three constraint equations can be obtained as follows:

$$U_{iac} = I_{Lr1}[j\omega L_{r1} + 1/(j\omega C_{r1})] + j\omega L_{m1}(I_{Lr1} - I_s/n_1) \tag{12}$$

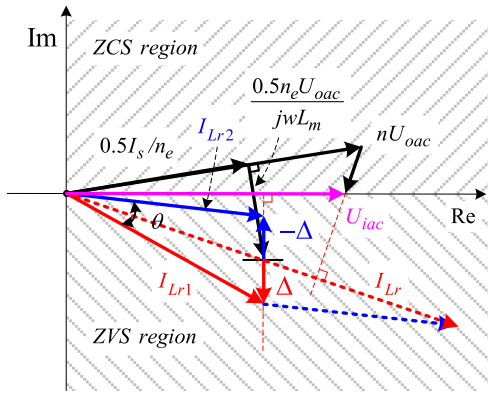

Fig. 11. Complex-plane analysis of the resonant currents I_{Lr}, I_{Lr1}, and I_{Lr2} in the MG mode.

$$0.5\,U_{iac}=I_{Lr2}[j\omega L_{r2}+1/(j\omega C_{r2})]+j\omega L_{m2}(I_{Lr2}-I_s/n_2) \tag{13}$$

$$\begin{aligned} &j\omega L_{m1}(I_{Lr1}-I_s/n_1)+j\omega L_{m2}(I_{Lr2}-I_s/n_2)\\ &\quad=n_1U_{oac1}+n_2U_{oac2}=2n_eU_{oac} \end{aligned} \tag{14}$$

where

$$U_{iac}=2\sqrt{2}U_{\mathrm{in}}/\pi, U_{oac}=2\sqrt{2}U_o/\pi, I_s=\pi I_o/(2\sqrt{2}). \tag{15}$$

By substituting $I_{Lr}=I_{Lr1}+I_{Lr2}$, $L_{r1}=L_{r2}=2L_r$, $L_{m1}=L_{m2}=2L_m$, $C_{r1}=C_{r2}=0.5\,C_r$, and (14) into (12)+(13), the relationship between the U_{iac} and U_{oac} can be derived as (16). And the resonant currents I_{Lr}, I_{Lr1}, and I_{Lr2} can be obtained as (17):

$$U_{iac}=\frac{4}{3}[I_{Lr}[1/(j\omega C_r)+j\omega L_r]+n_eU_{oac}] \tag{16}$$

$$\begin{cases} I_{Lr}=n_eU_{oac}/(j\omega L_m)+I_s/n_e\\ I_{Lr1}=0.5\,I_{Lr}+\Delta, I_{Lr2}=0.5\,I_{Lr}-\Delta \end{cases} \tag{17}$$

where

$$\begin{aligned} \Delta&=\frac{U_{iac}/8}{1/(j\omega C_r)+j\omega(L_m+L_r)}\\ &=\frac{-jU_{iac}/8}{[(L_n+1)f_n-1/f_n]\sqrt{L_r/C_r}}. \end{aligned} \tag{18}$$

Different from the equal currents of LG mode, two branches' current I_{Lr1} and I_{Lr2} are unequal in (17). They can be illustrated with the complex plane in Fig. 11 with U_{iac} at the real axis. When f_n approaches the minimum $f_{n\_\min}$, the primary current I_{Lr} in Fig. 11 is close to but not into the ZCS region [14]. Due to $f_{\mathrm{n}}>(L_n+1)^{-0.5}$, the Δ is pure negative imaginary. Compared with I_{Lr} and I_{Lr1} in the ZVS region, I_{Lr2} is much closer to the real axis, and even crosses over it into the ZCS region. Therefore, the waveform shape of i_{Lr2} in Fig. 5 is more like the one at ZVS/ZCS boundary [14], [25]. Fortunately, the ZVS achievement of switches is not influenced by i_{Lr2}: i_{Lr} flows through switches S_1 and S_2, whereas i_{Lr1} flows through

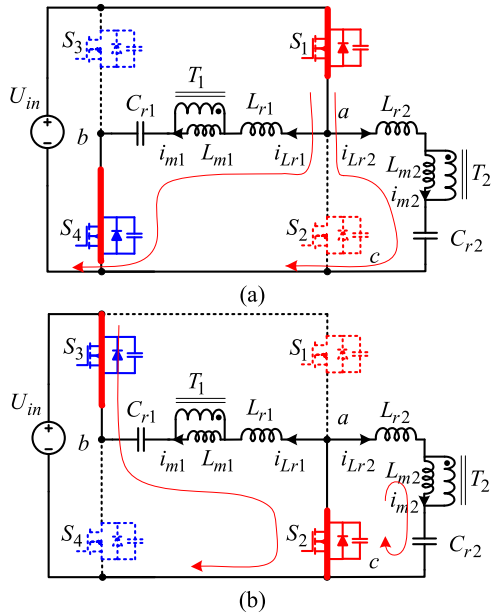

Fig. 12. States of the DSBS *LLC*'s primary circuits in the normal operation of MG mode: (a) Positive half-cycle, and (b) negative half-cycle.

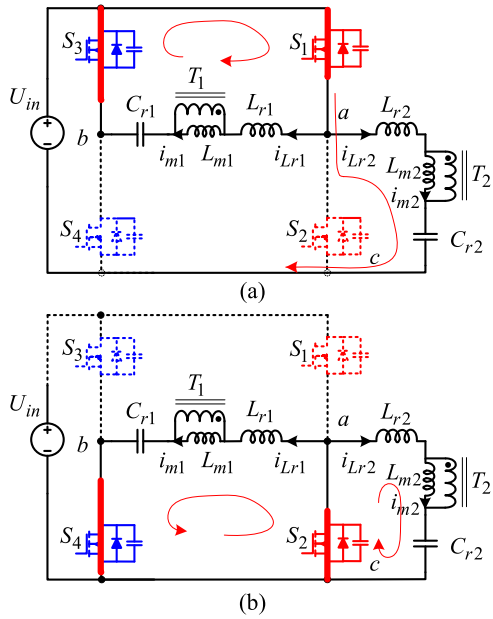

Fig. 13. Additional states of the DSBS *LLC*'s primary circuits during the switching instants of MG mode.

S_3 and S_4. Then the ZVS advantage of the conventional FB *LLC* converter is preserved in the proposed converter. That is another reason for the shared bridge-leg in the proposed converter.

D. Analysis of Circulating Current on the Primary Side

The proposed DSBS *LLC* in Fig. 3 is the combination of a FB *LLC* and a HB *LLC* with a shared primary bridge-leg. But there is not circulating currents on the primary side. As more complex than LG mode, the operation in the MG mode is analyzed in detail to illustrate the issue. And it can be analyzed on the primary and secondary side separately.

TABLE I
DESIGN SPECIFICATIONS

Items	Values
Input voltage ($U_{\rm in}$)	80 V–200 V
Output voltage (U_o)	400 V
Maximum output power (P_o)	1000 W
Resonant frequency f_r	140 kHz
Switching frequency range	80 kHz–160 kHz
Dead time T_d	160 ns

1) On the Primary Side: In the normal operation, the diagonal switches in the MG mode are conducting at the same time, and the two states of primary circuits are shown in Fig. 12. If there is a little delay between their drivers during the switching instants, the primary circuits may have two additional states in Fig. 13. From Figs. 12 and 13, it can be found that the currents of the branch *a-b* and *a-c* are independent of each other. In other words, there is no circuiting current on the primary side.

2) On the Secondary Side: As shown in Fig. 5, the output voltages u_{o1} and u_{o2} of transformers are always in the same direction when the secondary current i_s is nonzero at t_1–t_2 and t_4–t_5. Both of T_1 and T_2 transfer power to the output at the same time. Then there is no energy exchange between them. In other words, there is no circuiting current on the primary side.

IV. DESIGN CONSIDERATIONS AND COMPARISON

A. Design Considerations of DSBS LLC's Resonant Tank

A 1000-W prototype with design specifications in Table I is illustrated as an example of the parameter design procedure. In order to narrow the range of switching frequency, the proposed DSBS *LLC* is designed to operate in the ZVS region $f_s \le f_r$. As the voltage gain range $M_{\rm tank\_range}$ in (19) is same for two modes, the resonant parameters can be designed with the input-voltage range 120–200 V in the LG mode:

$$M_{\mathbf{tank\_range}} = \frac{U_{\mathbf{in\_max}}}{1.5\, U_{\mathbf{in\_min}}} = 1.67. \tag{19}$$

1) Design of Resonant Parameters: Among many design methods, the optimized design based on peak gain placement can provide better efficiency of *LLC* converters [29]. It is adopted here to design the equivalent resonant parameters n_e, L_r, C_r, and L_m of DSBS *LLC*.

In the LG mode, the DSBS *LLC* operates like a conventional HB *LLC*. The range of its input-voltage is 120–200 V. As shown in Table I, the range of switching frequency is 80–160 kHz, while the resonant frequency f_r is set 140 kHz. Then the parameters L_r, C_r, and L_m and the nominal input voltage $U_{\rm in\_norm}$ at $f_{\rm s} = f_{\rm r}$ can be designed with the method in [29]. After that, the equivalent turn-ratio n_e is obtained as (20). In practice, the turn-ratio n_1 and n_2 of two transformers are selected as $2n_e = 0.5$:

$$n_e = \frac{0.5\, U_{\mathbf{in\_norm}}}{U_o} = \frac{0.5 \cdot 200\ \mathbf{V}}{400\ \mathbf{V}} = 0.25. \tag{20}$$

2) ZVS Requirements: To simplify the analysis, the waveform of i_{Lr} at t_2-t_3 in Fig. 5 can be approximately as a platform [14]. Based on (3), the peak value of i_m at t_3 in Fig. 5 can be calculated as $I_{mp} = n_e U_o/(4L_m f_r)$ [14], which is same as that of LG mode. Due to the transformers' unequal power in (11), the peak value I_{mp1} and I_{mp2} of transformers' magnetizing current i_{m1} and i_{m2} can be calculated as $2I_{mp}/3$ and $I_{mp}/3$, respectively. In the LG mode, both of I_{mp1} and I_{mp2} are $I_{mp}/2$, and there are no switching actions for S_3 and S_4. With the same MOSFET for primary switches, the ZVS turn-on of S_3 and S_4 in the MG mode is more difficult to achieve than other conditions. Then the ZVS achievement of all switches can be assured, if (21) is satisfied. After checking (21), the other resonant tank parameters in Table II are designed with $L_{r1} = L_{r2} = 2L_r$, $L_{m1} = L_{m2} = 2L_m$, and $C_{r1} = C_{r2} = 0.5\, C_r$:

$$I_{mp1} \ge \frac{2\, U_{\mathbf{in}} C_{\mathbf{oss}}}{T_d} \tag{21}$$

where $C_{\rm oss}$ is the output capacitor of S_1-S_4.

3) Design of Resonant Inductors and Transformers: The area product *AP* denotes the size of the magnetic components and is usually used to design. The required *AP* of inductor $L_{\rm r1}$ and transformer T_1 can be calculated as (22), and so do L_{r2} and T_2. After selection of magnetic cores, the winding number N_{Lr1} of L_{r1} can be obtained from (23), and the same for N_{Lr2}. As earlier mentioned, the maximum of P_{T1} and P_{T2} are $2P_o/3$ and $P_o/2$, respectively. Then the secondary winding number N_{T1_sec} and N_{T2_sec} of T_1 and T_2 can be calculated as (24). After that, the other parameters of resonant inductors and transformers can be designed easily:

$$AP_{Lr1} = \frac{L_{r1} I_{Lr1} \Delta i_{Lr1}}{J K_u \Delta B},\ AP_{T1} = \frac{L_{m1}(I_{Lr1} + I_s/n_1)\Delta i_{Lm1}}{J K_u \Delta B} \tag{22}$$

$$N_{Lr1} = \frac{L_{r1} \Delta {\rm i}_{Lr1}}{A e_{Lr1} \Delta B} \tag{23}$$

$$N_{T1\,\mathbf{sec}} = \frac{2}{3} \cdot \frac{{\rm U}_o}{2 f_r A e_{T1} \Delta B},\ N_{T2\,\mathbf{sec}} = \frac{1}{2} \cdot \frac{{\rm U}_o}{2 f_r A e_{T2} \Delta B} \tag{24}$$

where I_{Lr1} and I_s are the primary and secondary rms currents at $f_{\rm s} = f_{\rm min}$. To achieve high accuracy, they can be obtained from simulation results. Δi_{Lr1} and Δi_{Lm1} are the peak–peak currents of L_{r1} and L_{m1}. ΔB, J, and K_u are the flux density, the current density, and the window utility factor. Ae_{Lr1}, Ae_{T1}, and Ae_{T2} are the core's cross section areas of L_{r1}, T_1, and T_2.

B. Control Strategy of DSBS LLC

In the normal operation, the pulse frequency modulation control is adopted to regulate the output of DSBS *LLC*. However, during the transitions between LG and MG mode, a soft scheme in [22] by gradually changing the duty cycle of switches S_3 and S_4 is applied to avoid large inrush current and make the transitions smooth. Based on this concept, Fig. 14 shows the sequence of drivers during the transition from MG to LG. And the drivers from LG to MG can be implemented in the reverse sequence.

Fig. 15 shows the control block diagram of the proposed DSBS *LLC* converter. The transition between modes is

TABLE II
PARAMETERS AND COMPONENTS OF THE CONVERTERS FOR COMPARISONS

Parameters or Components	Proposed DSBS *LLC*	Conventional FB *LLC*	Improved FB *LLC* in Fig. 2
Transformers' turn-ratio n_e, n_1, n_2	0.25, 0.5, 0.5	0.5, n/a, n/a	0.5, 0.35, 0.15
Inductance ratio L_n	3.7	2.7	$4.9(L_m/L_r)$, $3.4(L_{m1}/L_r)$
Resonant Inductance L_r, L_{r1}, L_{r2}	4.6 uH, 9.2 uH, 9.2 uH	10.5 uH, n/a, n/a	7.5 uH, n/a, n/a
Core of Resonant Inductor L_r, L_{r1}, L_{r2}	n/a, PC95PQ32/20 (Ap = 1.4 cm^4), PC95PQ32/20 (Ap = 1.4 cm^4)	PC95RM14 (Ap = 3.1 cm^4), n/a, n/a	PC95RM14 (Ap = 3.1 cm^4), n/a, n/a
Magnetizing Inductances L_m, L_{m1}, L_{m2}	17 uH, 34 uH, 34 uH	28 uH, n/a, n/a	36 uH, 25 uH, 11 uH
Peak magnetizing current I_{mp} at $f_s = f_r$	10.5 A	12.5 A	10 A
Core of transformers T, T_1, T_2	n/a, PC95PQ40/40(Ap = 6.6 cm^4), PC95PQ35/35 (Ap = 4.3 cm^4)	PC95PQ40/40 $*$ 2pcs (Ap = 13 cm^4), n/a, n/a	n/a, PC95EE42/15 $*$ 2pcs (Ap = 9.7 cm^4), PC95PQ35/35(Ap = 4.3 cm^4)
Resonant Capacitor value C_r, C_{r1}, C_{r2}	282 nF,141 nF, 141 nF	120 nF, n/a, n/a	168 nF, n/a, n/a
Peak-peak voltage $\Delta v_{\rm pp}$ of C_r	156 V	300 V	220 V
Primary switches	IRFP4332 $*$ 4pcs	IRFP4229 $*$ 4pcs	IRFP4229 $*$ 4pcs + IRF100s201 $*$ 2pcs
Secondary diodes	STTH806D $*$ 4pcs	STTH806D $*$ 4pcs	STTH806D $*$ 8pcs
Drivers for switches	IRS21864S $*$ 2pcs	IRS21864S $*$ 2pcs	IRS21864S $*$ 2pcs + VO3120 $*$ 1pcs

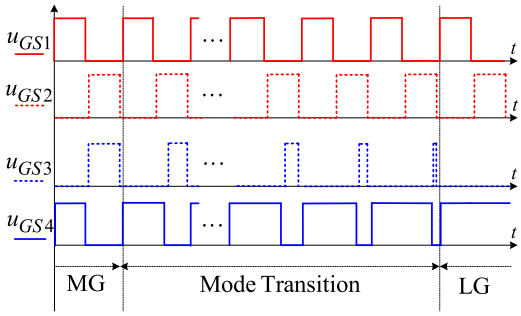

Fig. 14. Driver sequence of the proposed converter during the transition from MG to LG mode.

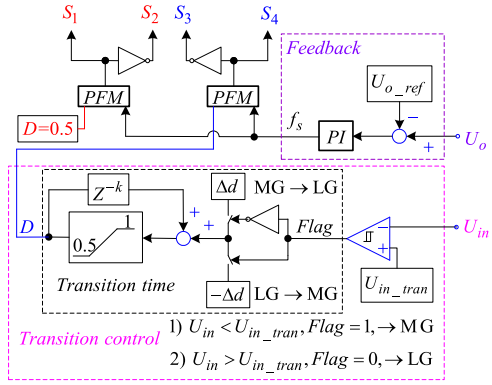

Fig. 15. Control block diagram of the proposed DSBS *LLC* converter.

triggered by the sensed voltage $U_{\rm in}$. To avoid the oscillation, a hysteresis comparator is used. For the design in this paper, the threshold voltage $U_{\rm in\_tran}$ from MG to LG is 135 V and 120 V in reverse. When $U_{\rm in} > U_{\rm in\_tran}$, the output *Flag* of the hysteresis comparator is 0, and the duty cycle D of S_4 is increased by Δd in every k switching cycles. When D reaches 1, the transition from MG to LG is completed. When $U_{\rm in} < U_{\rm in\_tran}$, the D of S_4 is reduced from 1 to 0.5 by Δd gradually with $Flag = 1$, and the transition is from LG to MG. During the transition procedure, the feedback controller is still working to regulate the output. Then the overshoot or undershoot of output voltage U_o can be small enough to meet the requirements. The control of the proposed converter can be easily and cost-effectively implemented with microcontrollers. The TMS320F28035 from TI is used in this paper.

C. Comparative Analysis

To help design tradeoff and topology selection in engineering applications, the proposed DSBS *LLC* converter is compared with the conventional FB *LLC* converter and the improved one in Fig. 2 [23]. When both of two transformers in Fig. 2 operate, the equivalent magnetizing inductance and turn-ratio of the improved FB *LLC* are $L_m = L_{m1} + L_{m2}$ and $n_{\rm e} = n_1 + n_2$. According to the specifications in Table I, the detailed parameters of three converters, designed with the method in [29], are provided in Table II.

Due to the smaller turn-ratio n_e, the capacitor value C_r of the proposed converter is larger than others'. However, its peak–peak voltage $\Delta v_{\rm pp}$ is much smaller. Then its volume will not increase obviously. As the equivalent turn-ratio n_e of three converters are different, it is better to compare their peak magnetizing current $I_{mp} = n_e U_o/(4 f_r L_m)$ at $f_s = f_r$ instead of L_m. Although its turn-ratio n_e is half of the others', the proposed DSBS *LLC* has lower I_{mp}. Second, the total AP and volume of its transformers are smallest. Third, compared with the improved FB *LLC* in Fig. 2, the proposed converter has reduced switches and diodes. It has less variation of drivers in stock.

With above discussions, the characteristics of three converters are compared in Table III. The comparison of overall efficiency is based on the experimental results in Section V. It is clear that each converter has its advantages and disadvantages. Overall, the proposed DSBS *LLC* converter is an excellent candidate for wide input-voltage applications with $2 \le M_{\rm range} \le 2.5$.

TABLE III
COMPARISON OF CHARACTERISTICS AMONG THREE CONVERTERS

Characteristic	Proposed DSBS *LLC*	Conventional FB *LLC* in [22]	Improved FB *LLC* in Fig. 2
Input-voltage range M_{range}	2–2.5	1–4	2–4
Transition between modes	Smooth	Smooth	Not smooth
Overall efficiency for $2 \le M_{\text{range}} \le 2.5$	High	Low	Medium
No. of devices	Less	Least	Many
Cost	Medium	Low	High

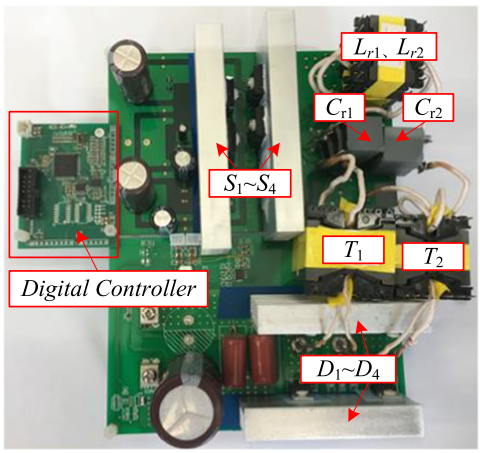

Fig. 16. Experimental prototype of the proposed DSBS *LLC* converter.

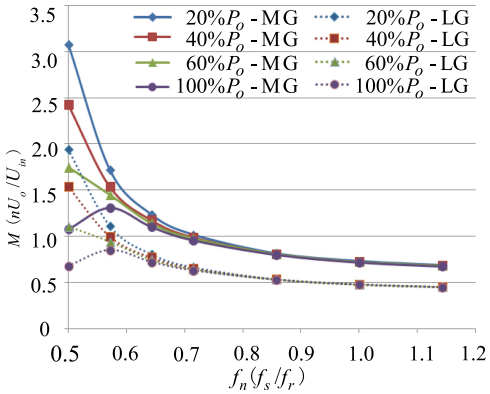

Fig. 17. Experimental voltage gain curves of the proposed DSBS *LLC* converter at different loads in the MG and LG mode.

V. EXPERIMENTAL VERIFICATION

A 1000-W prototype in Fig. 16 is built to verify the feasibility of the proposed DSBS *LLC* converter. And its parameters and components are listed in Table II. Besides, the two compared converters in Table II are also built. It should be noted that these prototypes are implemented with the same PCB, switches, power diodes, and core materials for fair comparisons.

A. Verification of the Voltage Gain

Fig. 17 shows the experimental voltage gains of the proposed DSBS *LLC*. Under the same load condition, the voltage gain of MG mode is just 1.5 times that of LG mode, which agrees well with the theoretical analysis.

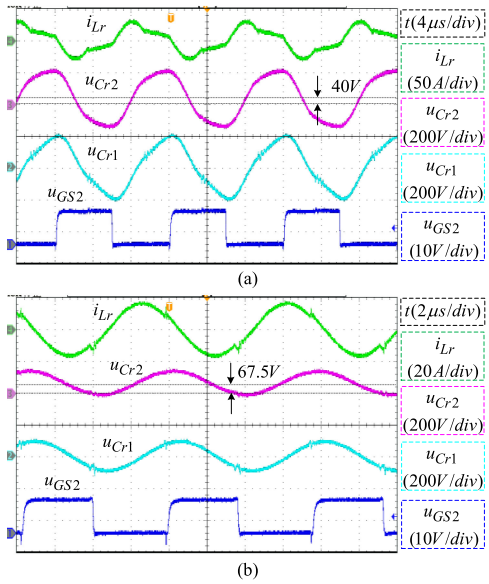

Fig. 18. Measured steady-state resonant voltage waveforms of the DSBS *LLC* in the MG mode: (a) At full load and 80-V input, and (b) at full load and 135-V input.

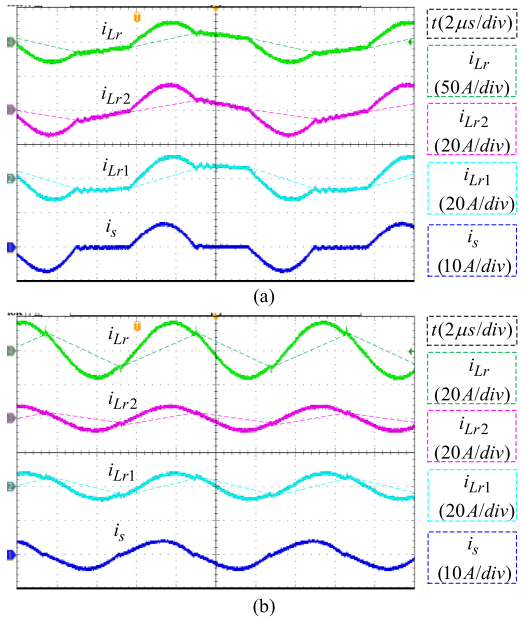

Fig. 19. Measured steady-state resonant current waveforms of the DSBS *LLC* in the MG mode: (a) At full load and 80-V input, and (b) at full load and 135-V input.

B. Verification of the Experimental Waveforms

Figs. 18–20 show the steady-state waveforms of the proposed DSBS *LLC* in the MG mode. In Fig. 18, u_{GS2} is the driving voltage waveform of switch S_2, and i_{Lr} is the total current waveform of two resonant branches, i.e., $i_{Lr} = i_{Lr1} + i_{Lr2}$. While the voltage u_{cr1} of C_{r1} is symmetric, the resonant voltage u_{cr2}

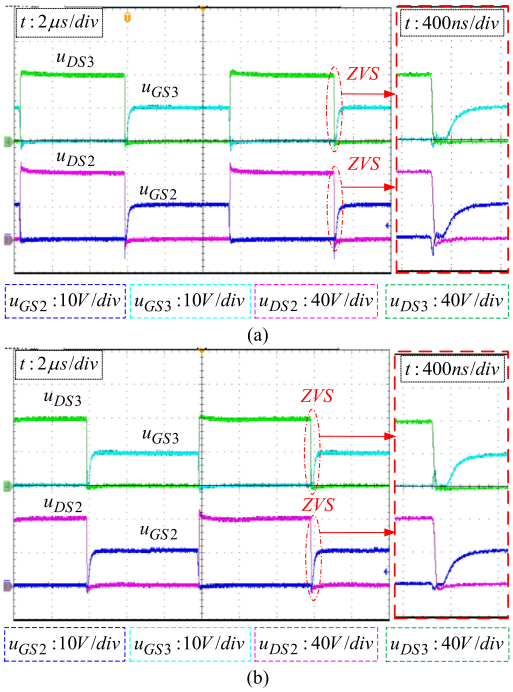

Fig. 20. ZVS waveforms of switches S_2 and S_3 of the DSBS *LLC* in the MG mode: (a) At 10% load and 80-V input, and (b) at full load and 80-V input.

of capacitor C_{r2} has a dc bias voltage $0.5U_{\text{in}}$ as the theoretical analysis.

Fig. 19 shows the waveforms of the primary resonant currents i_{Lr}, i_{Lr1}, and i_{Lr2}. The color dashed lines are just the magnetizing currents corresponding to them. And they deviate from their magnetizing current simultaneously with the secondary current i_s increasing from 0. When it occurs at minimum input voltage 80 V and full load in Fig. 19(a), the current i_{Lr2} is already positive, but i_{Lr} and i_{Lr1} are still negative for ZVS turn-on, which is in accordance with the above complex plane analysis.

Fig. 20 shows the driving voltage and drain–source voltage waveforms of switches S_2 and S_3 at 10% load and full load with 80 V input. The drain–source voltage decreases to zero before the driver comes, which means that ZVS of S_2 and S_3 can be achieved in the MG mode.

Fig. 21 shows the secondary voltage waveforms u_{o1} and u_{o2}, and output power P_{T1} and P_{T2} of DSBS *LLC*'s transformers in the MG mode. Due to the components' tolerance, the minimum ratio of P_{T2} to P_{o}, i.e., $P_{T2}/(P_{T1}+P_{T2})$, is 28.8% and close to the theoretical one 1/3, which has verified the above power distribution analysis.

In order to verify the dynamic performance, Fig. 22 shows the experimental waveforms of the DSBS *LLC* in response to the load step between 20% and 100%. And the transition waveforms between MG and LG modes are also provided in Fig. 23. In these figures, the undershoot and overshoot of output voltage U_o are tightly regulated under 20 V.

C. Efficiency Verification

Fig. 24 shows the efficiency comparisons of three converters at 20% load, 50% load, and full load. And the efficiency drops

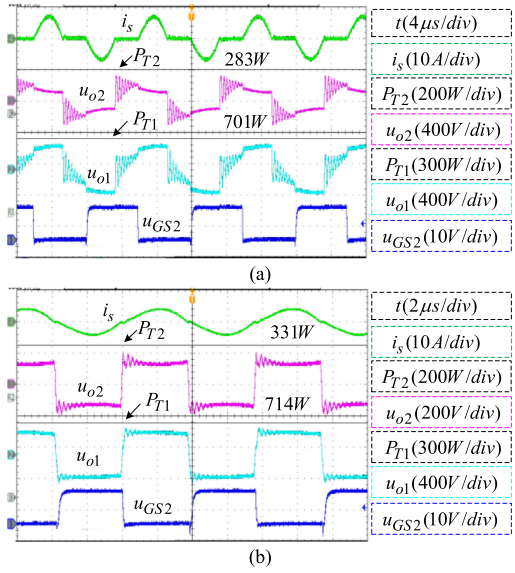

Fig. 21. Power distribution between two transformers of the DSBS *LLC* in the MG mode: (a) At full load and 80-V input, and (b) at full load and 135-V input.

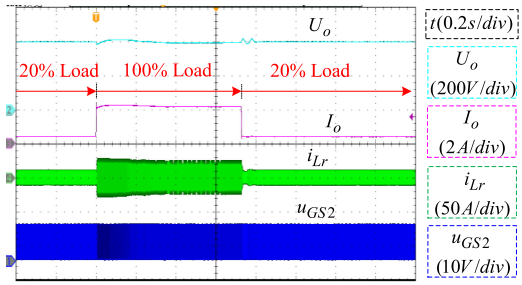

Fig. 22. Response waveforms of the DSBS *LLC* to the load step between 20% and 100% at $U_{\text{in}} = 80$ V in the MG mode.

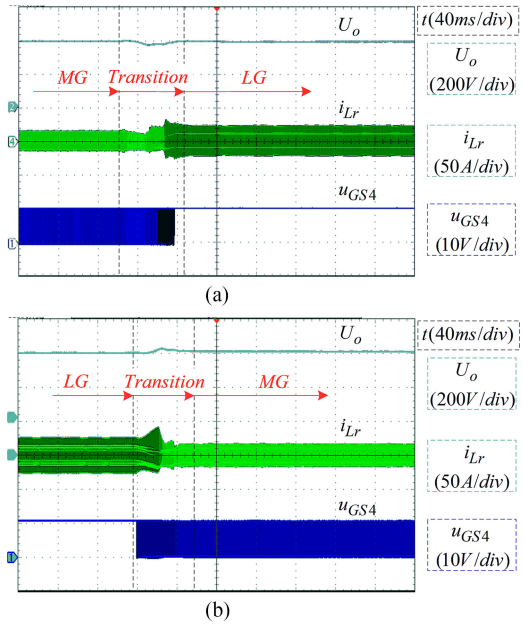

Fig. 23. Transitions waveforms of the DSBS *LLC* between MG and LG modes: (a) From MG to LG, and (b) from LG to MG.

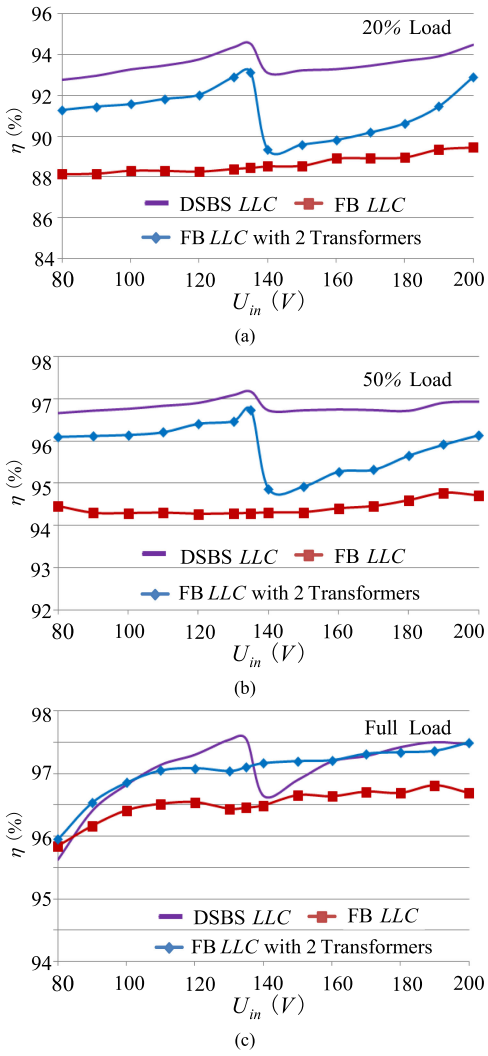

Fig. 24. Efficiency comparison of three converters in Table II: (a) At 20% load, (b) at 50% load, and (c) at full load.

of DSBS *LLC* and the improved FB *LLC* around 140 V input are caused by the transition between modes. Compared with the conventional FB *LLC*, the efficiency of the improved converter in Fig. 2 has been increased greatly. However, the proposed DSBS *LLC* has higher efficiency within the entire operation range. And a peak efficiency of 97.5% has been achieved.

Fig. 25 shows the comparison of calculated losses among three converters in Table II at full load with 80 and 200 V input, respectively. If the conduction loss of S_1 is designated by $P_{\rm con}$, the total conduction losses of S_1-S_4 of two compared FB *LLC* converters are $4P_{\rm con}$. However, due to about half of i_{Lr} flowing through the bridge-leg $S_3\&S_4$, the one of the proposed converter is around $2.5P_{\rm con}$. At 200-V input, all of three converters operate at resonant frequency f_r. Although the turn-ratio n_e is half of the others', the peak value I_{mp} of the proposed converter in Table II is still lower. As the geometric average of I_{mp} and the reflected output current $\pi I_{\rm o}/(2n_{\rm e})$, the rms of sinusoidal i_{Lr} of DSBS *LLC* is much less than two times i_{Lr} of two compared

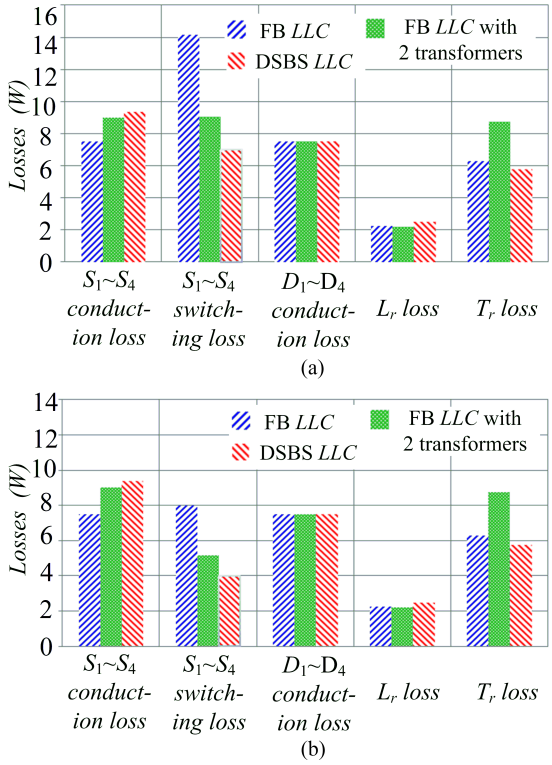

Fig. 25. Comparison of the calculated losses among three converters at full load: (a) 200-V input, and (b) 80-V input.

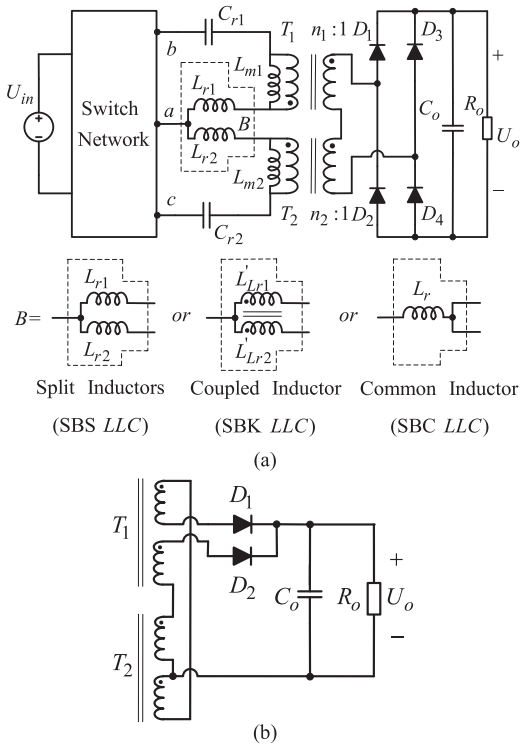

Fig. 26. Family of the proposed SB *LLC* converters: (a) Topology of SB *LLC* converters, and (b) the center-tapped rectifier.

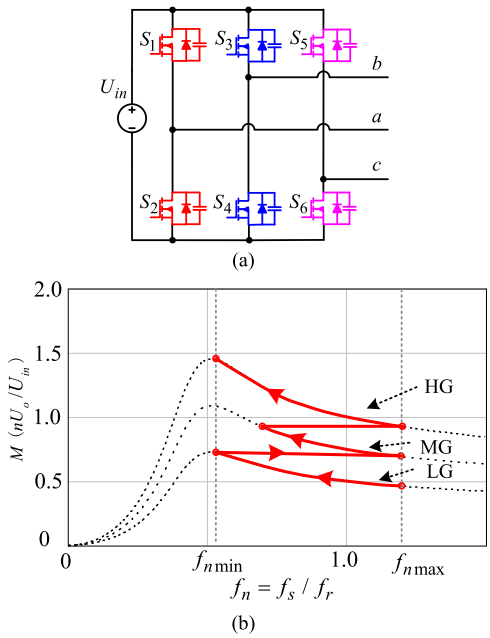

Fig. 27. SB *LLC* converter with triple-bridge (TSB *LLC*): (a) Triple-bridge switch network, and (b) DC gain curves under the same load condition.

converters. So the conduction losses of its switches S_1-S_4 are not much higher. It is also true for the comparison at 80 V input. In addition, the bidirectional switch $S_5\&S_6$ of the improved FB *LLC* with two transformers is consistently ON at 80 V input, producing more conduction losses.

Due to the ZVS turn-on and the small parasitic C_{oss}, the switching losses of MOSFETs are decided by their turn-off losses. At 200 V input, the DSBS *LLC* works into LG mode, and only S_1 and S_2 are switched. With lower peak value of magnetizing current I_{mp}, its switching losses have been cut down greatly. Despite S_1-S_4 switched at 80 V input, the turn-off current of S_3 and S_4 are about half of i_m, and thus the switching losses of DSBS *LLC* are still lower. Due to the smallest volume, the proposed converter has much lower losses of transformers than the others. Therefore, the DSBS *LLC* has higher efficiency than the conventional FB *LLC* at 200 V input and full load, as shown in Fig. 24(c). When the load decreases, the differences of primary conduction losses among three converters will decrease. However, as I_{mp} of three converters are nearly constant and the switching frequency f_s increases, the DSBS *LLC* will have much lower switching losses and core losses of transformers than others. Then the DSBS *LLC* has higher efficiency at 20% and 50% load in Fig. 24(a) and (b).

VI. Family of SB *LLC* Converters

Based on the proposed converter in Fig. 3, a family of the modified *LLC* converter with two split resonant branches (SB *LLC*) is presented in Fig. 26(a). To reduce the device number, the two split inductors of the converter (SBS *LLC*) can be integrated into a coupled inductor. With the coupling coefficient k, the self-inductor of the converter (SBK *LLC*) is $L'_{r1} = L'_{r2} = 2L_r/(1+k)$. When $k = 1$, the perfect coupled inductor can be further simplified into a common inductor L_r (SBC *LLC*). Besides the FB rectifier, the center-tapped rectifier in Fig. 26(b) can also be adopted for applications with low-voltage output. Using the aforesaid analysis method, the proposed SB *LLC* converters with dual bridge (DSB *LLC*) in the MG mode can be equivalent to the same converter in Fig. 7, no matter whether the resonant inductor is shared or split. Then they have the same voltage gain $n_e U_{\rm o}/U_{\rm in}$ and resonant current I_{Lr}.

Except for the double-bridge, the switch network of the SB *LLC* converters in Fig. 26(a) can also be a triple-bridge in Fig. 27(a), i.e., TSB *LLC*. Apart from the MG and LG modes, the proposed TSB *LLC* converters have one more mode, owing to two more switches. When the $S_3\&S_4$ and $S_5\&S_6$ have the same drivers in 180° phase-shift relative to the $S_1\&S_2$, the proposed converter operates as a FB *LLC*. Due to its highest gain, it is referred as high gain mode in Fig. 27(b). Operating in three modes, the TSB *LLC* converters can achieve the regulation of wider input-voltage range, i.e., $M_{\rm range} = 2M_{\rm tank\_range}$ and the ratio $B = 2$. Then its optimal input-voltage range is around 3.2.

VII. Conclusion

This paper has proposed a novel modified *LLC* converter with two split resonant branches for the wide input-voltage range application. It can operate in LG mode or MG mode. First, the voltage gain of MG mode is 1.5 times that of LG mode, which has been verified by the experimental results. Then the required range $M_{\rm tank\_range}$ to achieve the transition between modes is as low as 1.5, resulting in lower magnetizing current and higher efficiency within the entire operation range. Second, although the primary circuit has changed, the ZVS advantage of the conventional FB *LLC* converter has been preserved in the proposed converter. Furthermore, the number of the rectifying diodes has not increased. At last, as both of two transformers deliver power throughout, smaller core of transformers have been used.

A dual-bridge converter with split inductors (DSBS *LLC*), operating from 80 to 200 V, has been built to verify the analysis. Experimental results have shown that the proposed DSBS *LLC* converter has higher overall efficiency than the two compared FB *LLC* converters, and achieves the peak efficiency of 97.5%. All these advantages make the proposed converter more suitable for wide input-voltage range applications, such as the fuel-cell sourced power systems.

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